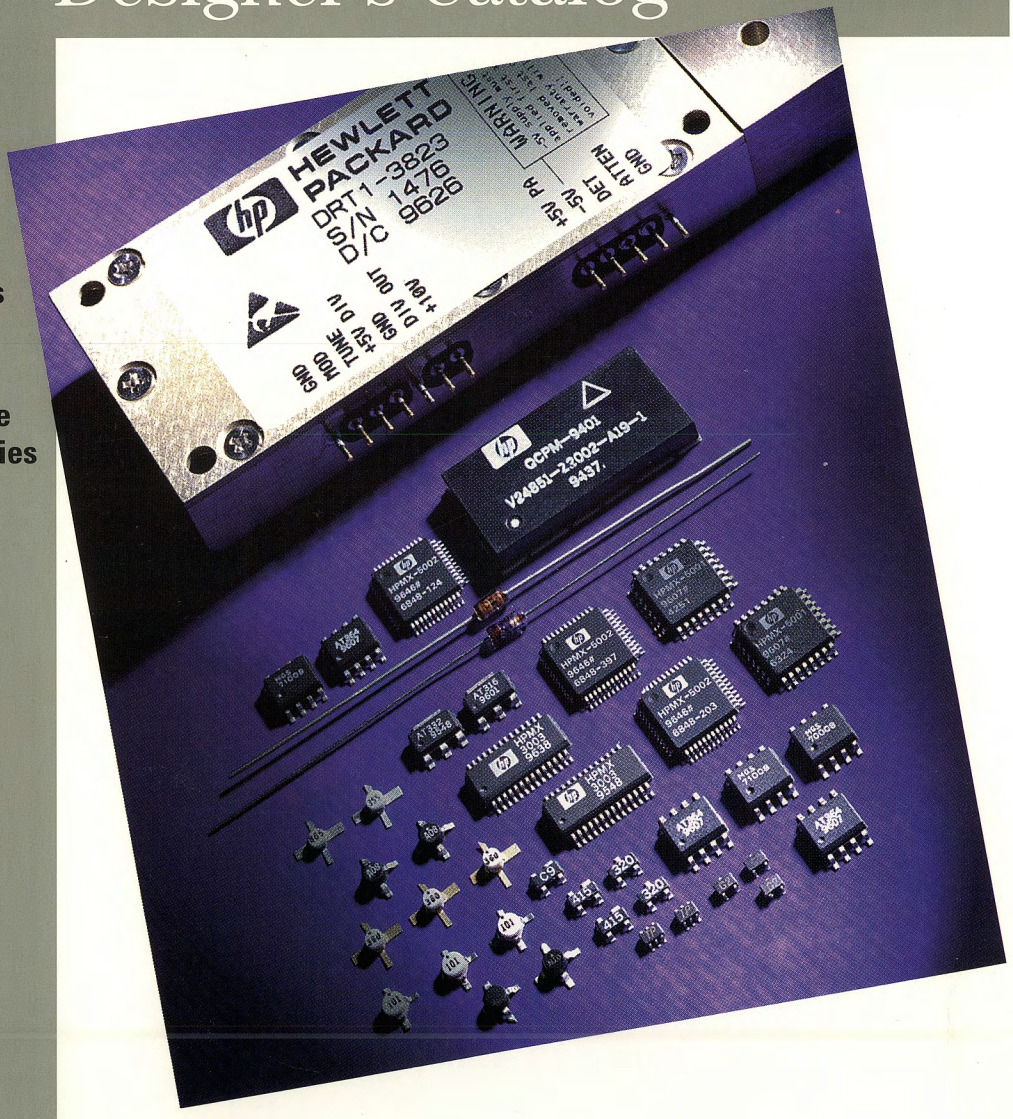
HEWLETT PACKARD

Communications Components Designer's Catalog

GaAs and Si RF and Microwave Semiconductors

Microwave and Millimeter-wave Hybrid Assemblies



HEWLETT® PACKARD

Hewlett-Packard: A Leader in Components

A Brief Sketch

Founded in 1961, and headquartered in San Jose, California, the Hewlett-Packard Company's Components Group is the world's largest independent supplier of communications components. Today the group has approximately 11,600 employees, and had fiscal 1996 revenues of $918 million (overall HP components revenues).

The Components Group includes four major divisions: Communication Semiconductor Solutions (CSSD), Wireless Infrastructure (WID), Optoelectronics (OED), and Integrated Circuit Business (ICBD), and serves five major markets: communications, computer/offfice, industrial, transportation and consumer.

Included in the Components Group's extensive line of more than 9,000 components are visible and infrared LED lamps; visible LED displays; light bars and arrays: Infrared Data Association (IrDA)-compliant infrared transceiver modules; fiber-optic transceivers, transmitters and receivers meeting most of today's industry standards; motion control devices; optocouplers and related optically-isolated control components; bar-code components; RF and microwave semiconductors; and communications amplifiers and assemblies. HP offers the world's brightest LEDs and is a technical leader for visible III-V products. HP is a leader in miniature packaging for RFICs and discrete semiconductors, and in the development of low cost packaging technologies for hybrid technologies.

The Components Group markets products through a sales force of 300 technically-educated sales professionals located in about 40 countries. HP components are also sold through a worldwide distributor network with more than 150 locations. Altogether, 95 percent of sales revenues are from customers external to HP.

The Components Group maintains five marketing centers worldwide in San Jose, California; Boeblingen, Germany; Tokyo, Japan; Pinewood, UK; and Hong Kong. Each is fully staffed with product application and support engineers and each is responsible for regional decision making. A design center in Tokyo is specifically chartered to develop products for the Japanese market.

Local decision-making is central of HP's transnational business strategy which focuses on customer satisfaction. In addition to providing the right product with superior quality and reliability, the Components Group strives to ensure worldwide product availability, accurate on-time delivery and up-to-date technical information for its customers.

Information about the products included in this catalog can be found on the World Wide Web at **http://www.hp.com/go/rf** Information about the Components Group and its complete line of products can be found on the World Wide Web at **http://www.hp.com/go/components**

About This Catalog

Hewlett-Packard manufactures innovative radio frequency (RF) semiconductors and assemblies for the communications marketplace. In addition to a broad line of general purpose devices, we also provide products specifically optimized for use in mobile communications handsets and base stations, as well as for TV distribution equipment. Combining HP's technology leadership with the appropriate choice of silicon or GaAs processes, our engineers create semiconductors and assemblies that achieve the highest value to the customer, packaged in the smallest size surface mount packages on the market. Our world-wide manufacturing facilities allow us to produce products with HP's proven quality, in high volumes, and at competitive prices.

About This Catalog

To help you choose and design with Hewlett-Packard RF and microwave semiconductors and modules, this catalog contains detailed product specifications. The catalog is divided into nine product sections:

1. PIN Diodes
2. Schottky Diodes
3. Silicon Bipolar Transistors
4. GaAs FETs
5. RFIC and MMIC Amplifiers
6. RFICs for Mixers, Modulators, Switches, Attenuators, Frequency Dividers, and Other Functions
7. Digital Radio Receiver and Transmitter Modules
8. Voltage Controlled Oscillators (VTOs)

How to Find the Right Information

- The Table of Contents helps you locate the product sections as well as the Data Sheet Index and selection guides for each product section.
- The Alphanumeric Index lists every component in this catalog and the page number on which the corresponding data sheet is located.
- Selection Guides allow you to quickly select products most suitable for your application.
- Application Information is either published in this catalog or abstracts list a variety of Application Notes detailing specific design examples.

How to Order

To order any component in this catalog, call your nearest HP authorized distributor or HP sales office.

A complete listing of HP authorized distributors is located on page 12-3. These distributors can offer off-the-shelf delivery for most HP components.

Service and Support

For technical assistance or for the location of your nearest HP sales office, distributor or representative, call (US and Canada only): 1-800-235-0312 or 408-654-8675.

Elsewhere in the world, call your local Hewlett-Packard sales office. Ask for a Components representative.

For Additional Information

Information on products in this catalog can be found on the World Wide Web at **www.hp.com/go/rf**

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at 1-800-450-9455, or from the Components Sales Response Center at 1-800-235-0312.

Elsewhere in the world, call your local HP sales office. Ask for a Components representative.

Information regarding these and other Hewlett-Packard Components Group products is available on the World Wide Web at **www.hp.com/go/components**

Literature is available regarding other HP Components Group products not listed in this catalog:

- *LED Lamps and Displays*
- *Infrared Products*
- *Optoisolators*
- *Motion Sensing and Control products*
- *Fiber-Optic and integrated circuit components*
- *Bar Code Components*

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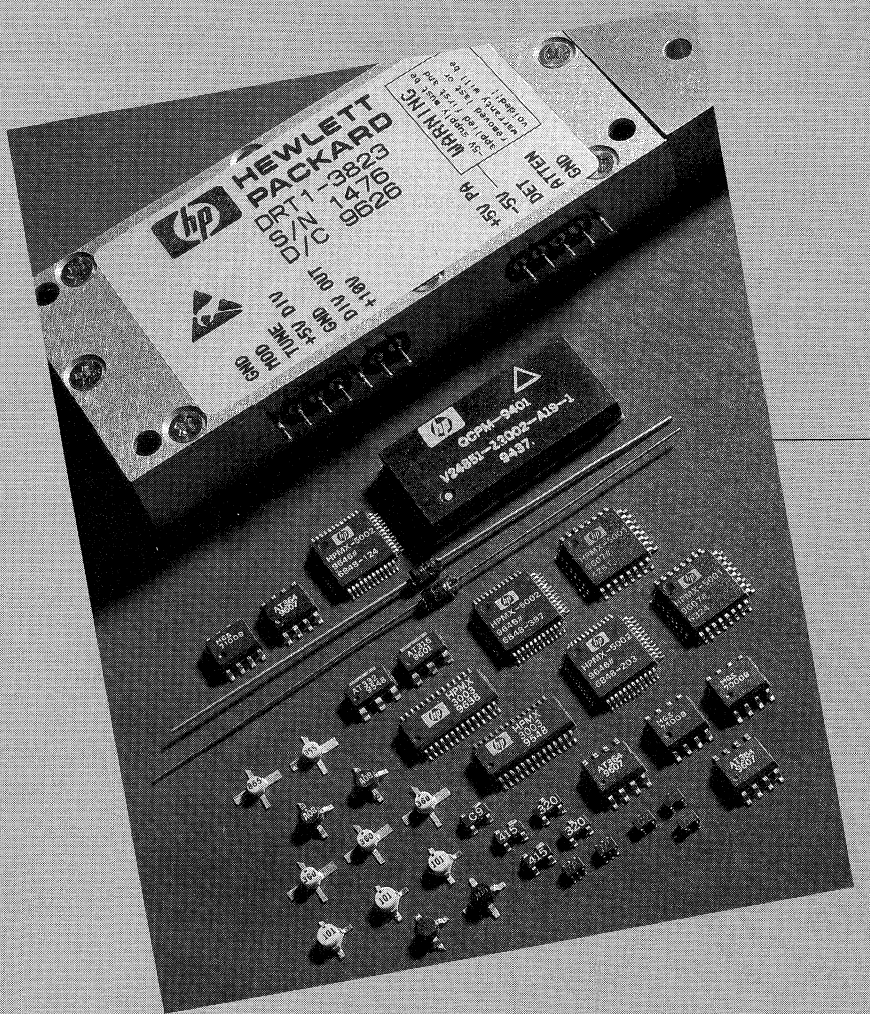
HEWLETT® PACKARD

Quality Assurance Concepts and Methodology



Quality Assurance Concepts and Methodology

Semiconductor Devices and Hybrid Assemblies

Reliability/Quality Philosophy

Recognizing the increasing importance of microwave component reliability for the consumer, industrial, and military markets, the Components Group of Hewlett-Packard has committed itself to achieve error free performance at all levels of manufacturing and to deliver the highest level of product quality and reliability performance. Three basic ingredients are integrated into the manufacture of reliable microwave components:

- The device must be designed with a technical understanding of the user's applications and quality requirements.
- The device must be manufactured with the optimum state-of-the-art technology for the application.
- Controls must be established in the manufacture of the device.

As a major manufacturer of microwave products, Hewlett-Packard produces a broad family of many devices. Since it is not practical, technically necessary, nor cost effective to qualify each of these products via life and environmental testing, the logical approach has been to differentiate assembly/package related failure mechanisms from failure modes associated with the wafer fabrication process. This "die process" and "package product" approach to reliability has been a consideration in the new military standards for microelectronic testing/reliability and is used at Hewlett-Packard with the following definitions:

- **Die Process Family** consists of devices which have appropriately similar wafer processing. This premise recognizes that component geometry and layout of a product will have little impact on reliability because established design rules apply to all products fabricated by the same process.

- **Package/Assembly Family** are those of like construction and are assembled with appropriately similar materials, manufacturing controls and operations.

Component reliability estimation can therefore be achieved with a high confidence level from environmental and life testing data derived from various product families. Accelerated stress testing techniques are employed to obtain definitive working knowledge of reliability performance, whereby the resulting information is used to predict long-term device reliability for the intended application.

In-process Control and Reliability Testing

The reliability performance of microwave components can be affected by numerous operations associated with device manufacturing, among these being:

- Wafer fabrication process/technology
- Device design and layout
- Packaging design
- The manufacturing processes
  - —Wafer fabrication
  - —Package materials
  - —Assembly materials and procedures
- In-process controls
- Final electrical test procedures
- Quality Assurance inspection procedures
- Post-assembly reliability screening

One of the most important aspects of insuring quality and reliability is through adequate in-process controls of these operations. Wafer fabrication controls provide the assembly operation with a high quality, reliable chip, while the process controls associated with the assembly operation assure the optimum in package integrity. Typical Quality Assurance process controls may be summarized according to the fabrication and assembly operations:

Quality Assurance Process Controls

Wafer Fabrication	Assembly
Particle count	Die Visual
Temperature/Humidity control	Die shear test
Capacitance vs. Voltage plots	Wire bond pull
Furnace tube cleaning	Incoming package evaluation
Deionized water checks	Pre-seal visual
Metal thickness monitor	Hermeticity
Metal SEM monitor	Electrical test
Inspection of starting material	Molding compound evaluation
Plating bath in-process monitor	

Life and Environmental Stress Tests

To ensure the highest product reliability commensurate with the intended use of the device, numerous life and environmental tests have been designed to assess device performance. The majority of these tests are designed to simulate more extreme operating conditions than would actually be encountered in most practical applications. This ensures the reliability performance of the device relative to its intended application. Typical device testing at Hewlett-Packard may include any of the following environmental and life tests, as appropriate.

Life Tests

High Temperature Reverse Bias (HTRB)
High Temperature Operating Life (HTOL)

Environmental Tests

Moisture Resistance
Hermeticity
Solderability
Mechanical Shock
Thermal Shock
Lead Fatigue
Temperature Cycling
Vibration
Autoclave
Constant Acceleration
Terminal Strength
Salt Atmosphere
Marking Permanency

Specific methods and conditions of these tests are in compliance with MIL-STD-202, MIL-STD-750, MIL-STD-883 or JEDEC JESD22 test specifications, depending upon the nature of the device being tested and its functional classification.

Reliability Assessment and Prediction

Numerous concepts and mathematical models have been proposed to assess the reliability performance of semiconductor components. Of these, essentially three fundamental parameters are widely used in the industry for reliability assessment and prediction of failure rate:

- The failure rate, λ
- The probability of survival, P_S
- The activation energy, E_a

The Failure Rate is related to the population of units failed under life testing and the duration of the test as:

$$\lambda = \frac{N_F}{N_0 t}$$

where
λ = assessed failure rate
N_F = quantity of failures occurring in a time interval t
N_0 = quantity of acceptable devices at zero hours
t = time interval or duration of test

Generally it is more meaningful to discuss failure rates in terms of the Mean Time To Failures or MTTF, which is the reciprocal of the failure rate and expressed as MTTF = $1/\lambda$. It is important to recognize that both λ and MTTF are statistical averages and apply only to the useful life of the product.

The **Probability of Survival** is the likelihood that a particular device will survive for a given period of operating time and may be expressed as:

$$P_S = e^{-\lambda t} = e^{-t/(MTTF)}$$

where
t = operating time of the device
λ = failure rate = 1/MTTF

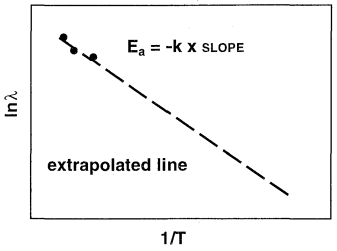
The third mathematical relationship of importance to reliability is expressed in a form of the Arrhenius Equation which relates the rate of a thermally accelerated process to temperature as:

$$\lambda = A \exp^{(-E_a/kT)}$$

or $$\ln\lambda = -E_a/kT + \ln A$$

where
E_a = Activation Energy
k = Boltzmann's Constant
(8.62×10^{-5} eV/°K)
T = Temperature in Kelvin (°K)
λ = Failure Rate at Temperature T
A = Constant

A plot of $\ln\lambda$ versus 1/T will yield a straight line as illustrated:



The activation energy E_a can therefore be determined by

$$E_a = -k * (slope)$$

For products which are extremely reliable, the failure rates are too low to be measured within a reasonable test duration. In that case, the failure rate can be determined by stressing parts at an elevated temperature and extrapolating along the straight line, on the plot illustrated above, to the temperature of interest. The temperature of interest can be the junction temperature, the ambient temperature, the case temperature, or whichever conditions the user is most concerned about. In practice, a simplified equation, with a known E_a can be used for the prediction of failure rates at different temperatures, or for the determination of an acceleration factor, by changing the stress temperature from T1 to T2 expressed as:

$$\ln\frac{\lambda_2}{\lambda_1} = -\frac{E_a}{k}\left(\frac{T1 - T2}{T1 * T2}\right)$$

Reliability Monitor Program

The reliability monitor program is administered and executed by the Quality Assurance Department. The intent of this program is:

- To provide a periodic evaluation of our product reliability on an on-going basis, exemplified by the matrix that follows.[1]
- To maintain a pulse on the fabrication and assembly processes.
- To identify, via long-term stress testing, the limitations of our products and thereby provide future direction for engineering design, development, and manufacturing improvements.

Fabrication and assembly variables were considered in the construction of the matrix to assure that these products would best represent all product families and their associated processes with meaningful volumes.

In addition to the following listed products, all new products must pass an extensive reliability test program prior to introduction. This ensures that the tradition of high quality is upheld in all new devices.

Note:
1. Periodic is defined as somewhere between 2 and 4 months, depending upon current production volumes. New products are added to the matrix as is appropriate, once volume production is established.

Reliability Monitor Process/Device Matrix

Product Type	Fabrication Process	Package Process	Package Type	Device Group	Typical Device
Diode	Schottky	Glass, Hermetic	15	5082-28XX	5082-2800
		Plastic	SOT-23/-143	HSMS-281X	HSMS-2810
				HSMS-282X	HSMS-2820
			SOT-323	HSMS-820X	HSMS-820B
	PIN	Glass, Hermetic	15	5082-30XX	5082-3039
		Plastic	SOT-23/-143	HSMP-380X	HSMP-3800
				HSMP-389X	HSMP-3890
			SOT-323	HSMP-389X	HSMP-389B
Si Bipolar Transistor; Integrated Circuit	SAT	Plastic	84, 85, 86	AT-4XX8X	AT-41485
			SOT-23/-143	AT-3XX11/33	AT-31033
			SOT-223	AT-33X25	AT-33225
			04, 05	MSA-XX0X	MSA-1105
			84, 85, 86	MSA-XX8X	MSA-0886
	ISOSAT, Single-Level Metal	Plastic	84, 85, 86	INA-XXX8X	INA-03184
	ISOSAT, Double-Level Metal	Plastic	SOT-143	INA-3XX11	INA-30311
			SOT-363	INA-5XX63	INA-51063
			SOIC-8	IAM-XXX08	IAM-81008
			SOIC-16	HPMX-200X	HPMX-2003
		Ceramic, Hermetic	SOIC-8	IAM-XXX28	IAM-82028
GaAs Transistor; Integrated Circuit	Lifted-Y Gate	Ceramic, Hermetic	70	ATF-1XX70	ATF-13170
		Ceramic, Non-Hermetic	35, 36	ATF-1XX3X	ATF-13036
		Plastic	84, 86	ATF-1XX8X	ATF-13284
	Plated-Y Gate	Plastic	84, 86	ATF-2XX8X	ATF-21186
	PHEMT	Ceramic, Non-Hermetic	76, 77	ATF-3XX7X	ATF-36077
		Plastic	SOT-363	MGA-8XX63	MGA-86563

Reliability Monitor Test Conditions

Test	Conditions
Operating Life	1000 hrs @ AC switch between maximum forward power and Vr = 80% Vbr for discrete diodes, typical DC bias at elevated temperature that enables maximum junction temperature for transistors, amplifiers and ICs
High Temperature Reverse Bias (for diodes only)	1000 hrs @ Vr = 80% Vbr (min) and max. rated temp.
Thermal Shock	200 cycles @ max/min storage temperature, liquid to liquid
Temperature Cycling	200 cycles @ max/min storage temperature, air to air
Mechanical Shock[1]	1500 g's 0.5 msec pulse @ Y1, Y2, X axis
Hermeticity[1]	Fine and Gross Leak
Autoclave[2]	96 hrs @ 121°C, 100% RH, 15 psig
Moisture Resistance[3]	1000 hrs @ 85°C ad 85% RH
Solderability	16 hrs steam aging, 245°C, 5 sec dwell
Marking Permanency	Resistance to solvent groups
Lead Integrity	Lead Pull
Infrared Reflow Simulation[4]	3 passes @ max temp 230 ± 10°C, preheat @ 125 ± 25°C for 130 secs max, temp above 183°C is 110–180 secs

Notes:
1. Required for hermetic packages only
2. Required for plastic packages only
3. Required for non-hermetic ceramic packages only; optional alternative to autoclave for plastic packages. Unbiased for GaAs devices.
4. Surface mount plastic packages only

Reliability Monitor Sample Sizes

Reliability Monitor Matrix[1] 267 units (for diodes), 215 units for transistors and ICs				
104 units for diodes, 52 units for transistors and ICs	104 units	22 units	22 units	15 units
Op Life (52 units) HTRB (52 units for diodes)	Environmental/ Mechanical Tests[2]	Lead Integrity	Solderability	Marking Permanency

Notes:
1. The frequency of test is every three months.
2. For:

Hermetic: (52 units) Hermeticity → Thermal Shock → Mechanical Shock → Hermeticity
(52 units) Hermeticity → Temperature Cycling → Hermeticity

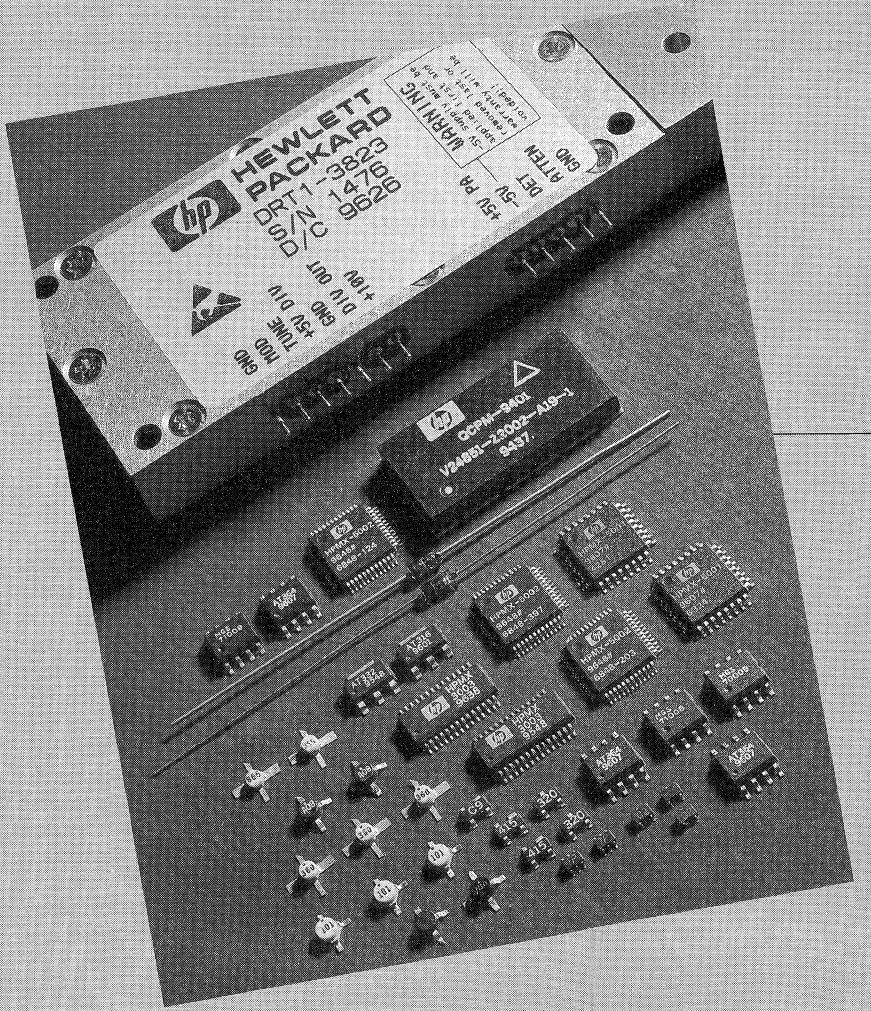
Plastic: (52 units) Preconditioning → Thermal Shock → Autoclave or Moisture Resistance
(52 units) Preconditioning → Temperature Cycling
Preconditioning Test consists of: Moisture Soak @ 85°C/85% RH @ 168 hrs → Ir Reflow 3 passes

Non-Hermetic: (52 units) Thermal Shock → Mechanical Shock → Moisture Resistance

Ceramic: (52 units) Temperature Cycling

HEWLETT PACKARD

PIN Diodes



PIN Diodes

Characteristics

The most important feature of the PIN diode is its basic property of being an almost pure resistor at RF frequencies, whose resistance value can be varied from approximately 10,000 Ω to less than 1 Ω by the control current flowing through it. Most diodes exhibit this characteristic to some degree, but the PIN diode is optimized in design to achieve a relatively wide resistance range, good linearity, low distortion, and low current drive. The characteristics of the PIN diode make it suitable for use in switches, attenuators, modulators, limiters, phase shifters, and other signal control circuits.

Device Characteristics

The principal parameters of a PIN diode which play major roles in determining the performance of a circuit include the following:

Capacitance

Diode capacitance limits switch and attenuator performance at high frequencies in the form of isolation rolloff and increased insertion loss. Optimum performance can be achieved by one of several alternatives available. Using a low capacitance diode would be one solution. Since the junction capacitance of a PIN diode is related to the geometry and electrical properties of the I-layer similar to the case of RF resistance, an R-C trade-off may be feasible. Special techniques can be employed to minimize capacitance (and other parasitic) effects, and in some cases even to take advantage of them. (Some of the techniques for improving high frequency performance are discussed in Application Note 922, "Applications of PIN Diodes" and Application Note 957-2, "Reducing the Insertion Loss of a Shunt PIN Diode".)

Dielectric Relaxation Frequency

When current is removed from a PIN diode, most of the charges return to the P and N layers. However, some charges remain in a portion of the I layer, the undepleted portion. At low frequencies this undepleted I layer resistance shorts out a portion of the I layer capacitance. A low frequency capacitance measurement would be relatively high because only a portion of the I layer, the depleted portion, would be measured. At higher frequencies the reactance of the undepleted I layer is smaller and the resistance of the undepleted charges is not small enough to cause this capacitance error; no reverse bias is needed to deplete the I layer. The frequency where the resistance of the undepleted charge equals the reactance of the undepleted layer is called the dielectric relaxation frequency (F_{DR}). Below this frequency, reverse voltage is needed to measure the minimum value of the diode's junction capacitance (C_J). Above the F_{DR}, the zero bias value of C_J is almost the same as the reverse bias C_J value.

For example, when the HSMP-3810 PIN diode is mounted in series in a 50 ohm line and measured at a fixed frequency, a plot of total capacitance (C_T) vs. reverse voltage (V_R) such as shown in Figure 1 would result. At the low frequency of 1 MHz and zero bias, the capacitance is relatively high, about 0.45 pF. As the frequency is increased, still at zero bias, to 30 MHz the capacitance drops significantly to a quarter dB. As frequency increases further, capacitance is flat at about 0.20 pF. Applying reverse bias at the higher frequencies does not significantly affect the total capacitance. Figure 2 shows similar results for the HSMP-3830 PIN diode. Note the HSMP-3810 is flat above 100 MHz and the

HSMP-3830 becomes relatively flat about 1 GHz.

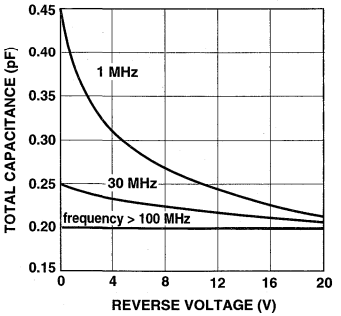


Figure 1. RF Capacitance vs. Reverse Bias at 25°C, HSMP-3810 Series.

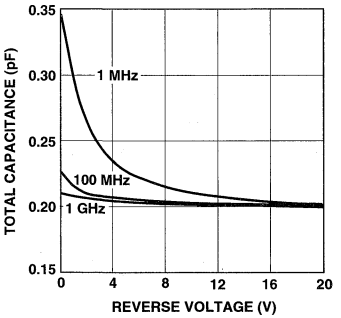


Figure 2. RF Capacitance vs. Reverse Bias at 25°C, HSMP-3830 Series.

RF Resistance

The PIN diode structure consists of an I (Intrinsic) layer of very high resistivity material sandwiched between regions of highly doped P (positively charged) material and N (negatively charged) material. With reverse or zero bias, the I-layer is depleted of charges and the PIN diode exhibits very high resistance. When forward bias is applied across the PIN diode, positive charge from the P region and negative charge from the N region are injected into the I-layer, therefore increasing its conductivity and lowering its resistance.

The high off resistance and low on resistance make the PIN diode attractive for switching applications.

At RF frequencies, the PIN diode with forward bias behaves essentially as a pure resistor. The resistance of the PIN diode is related to the bias current, the geometry of the I-layer and the properties of the carriers. For a given type of PIN diode with uniform characteristics, resistance is inversely proportional to the forward bias current. Whereas, only high off resistance and low on resistance are important in switching applications, the resistance characteristics in the entire dynamic range are of concern in attenuator applications. Linearity of resistance with bias makes the PIN diode useful for attenuator applications.

Power Handling

The calculation of power handling in a PIN diode is complicated and involves the nature of the RF signal (frequency, CW or pulsed, duty cycle), the resistance of the PIN diode (a function of bias) and the package, the ambient temperature, the number and arrangement of PIN diodes in the circuit, the amount of reverse bias on the unbiased diodes, and the thermal resistance of the diode and its package. For a switch, with two extreme states (on and off) there are two diode conditions to consider:

1 when the PIN diode is forward biased, it can be represented as a resistor. You control the resistance by the amount of forward bias.
2 when the PIN diode is reverse biased, the limitation is the sum of reverse (DC) bias plus the peak reverse RF voltage of the source.

For further details, read AN 922, "Applications of PIN Diodes."

Power Handling Capability

The RF power (CW or pulse) that can be handled safely by a diode switch is limited by two factors—the breakdown voltage of the diode, and thermal considerations, which involve the maximum junction temperature and the thermal resistance of the diode and packaging. Other factors affecting power handling capability are ambient temperatures, frequency, attenuation level (which is related to diode resistance), pulse width and duty cycle. (See Application Note 922, "Applications of PIN Diodes," for details.)

Thermal Resistance

Thermal resistance is normally designated by θ_{jc} "theta-j-c" or the thermal resistance from the junction to the case. It is specified in terms of °C per Watt (°C/W).

Using this number θ_{jc} and knowing the amount of power being dissipated as heat in the diode, one can calculate the temperature rise of the junction with respect to the case. Conversely, one can reverse the process and use temperature rise and power data to compute θ_{jc}. This calculation is based upon the measurements which we made when we produced our diode data sheet.

The numbers to use are:

1 T_{jmax}, the maximum junction operating temperature
2 P_{max}, the maximum DC power dissipation
3 C_t, the case temperature = 25°C

Items 1 and 2 are found in the Maximum Ratings table on the diode's data sheet. The computation is as follows:

$\theta_{jc} = (T_{jmax} - C_t) / P_{max}$

As an example, consider the HSMP-3860 PIN diode.
In this case,

$T_{jmax} = 150°C$

$P_{max} = 250\ mW = 0.25\ W$

and our calculation yields

$\theta_{jc} = (150 - 25) / 0.25 = 500°C/W$

Modeling

Proper modeling of PIN diodes requires careful analysis of carrier lifetime. Since the Spice engine does not model this important parameter, HP does not support Spice models for PIN diodes.

Touchstone, a linear modeling program, can be used to model linear performance of PIN diodes using the following diagram.

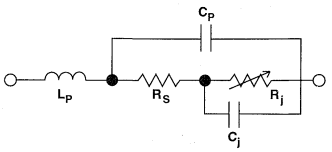


Figure 3.

Distortion

Distortion in a PIN diode is a function of I-layer thickness, not carrier lifetime. It turns out that diodes with thick I-layers also have long lifetimes, but the lifetime is an effect, not a cause.

Much valuable work on PIN diode amplitude distortion has been done by Dr. Robert Caverly of Southeastern Massachusetts University. References can be found in Application Note 1048, "A Low-Cost Surface Mount PIN Diode π Attenuator."

This application note presents an empirically optimized four diode π attenuator covering 300 KHz to 3 GHz using the HSMP-3814 diodes. Modeling the signals and the resulting distortion products is not practical as multiple diodes, in any configuration, will produce a rich spectrum of distortion products, all at different values of amplitude and phase angle. These signals, distortion products, and passive circuit elements (bias elements, etc.) will interact by reinforcing or canceling and make predicting the results impractical.

Carrier Lifetime

An important parameter of the PIN diode is the carrier lifetime, τ, which is useful for defining the low frequency limit, $f_o = 1/2\pi\tau$, for linear performance of the diode. For RF signal frequencies below f_o, the PIN diode rectifies the signal much like an ordinary PN junction diode, and considerable output distortion results. (See Application Note 957-3, "Rectification Effects in PIN Attenuators," for additional discussion on rectification causes and effects.) At frequencies above f_o, less rectification occurs with increasing frequency, allowing the PIN diode to appear more linear, approaching a pure resistor.

For applications requiring good linearity and low distortion the minimum signal frequency should be ten times f_o, i.e., $f_{min} = 10/2\pi\tau$, $= 1.6/\tau$. This restriction is not important in switching applications, where the diode is normally biased either completely OFF or ON. In those states, since most of the power is either reflected or transmitted, the effect of RF current on the total charge is small and distortion is not a problem.

Insertion Loss

The loss of signal attributed to the diode when the switch is on (transmission state) is insertion loss. For low insertion loss, low resistance is needed in a series switch (Figure 4). Low capacitance (particularly at high frequencies) is needed in a shunt switch (Figure 5).

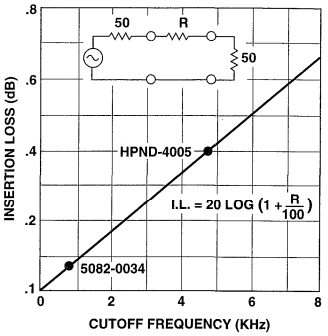


Figure 4. Typical Insertion Loss of Series Diode Switch.

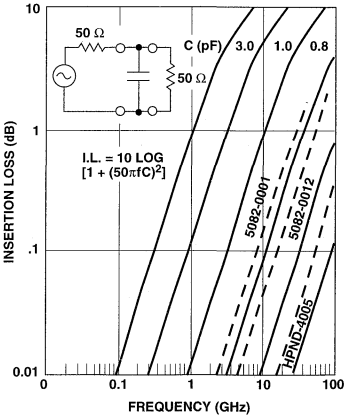


Figure 5. Typical Insertion Loss of Shunt Diode Switch.

Isolation

Isolation is the measure of RF leakage between the input and output when the switch is off. For high isolation (low transmission) low capacitance is required in a series switch especially at high

frequencies (Figure 6). Low resistance is required in a shunt switch (Figure 7).

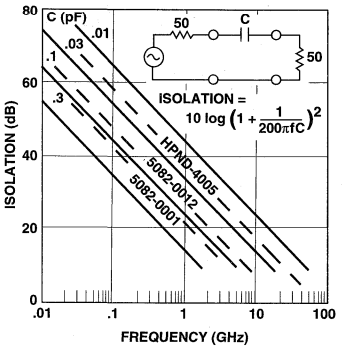


Figure 6. Typical Isolation of Series Diode Switch.

Reverse Recovery Time

Reverse recovery time is a measure of switching time, and is dependent on the forward and reverse bias applied. With forward bias current, charge is stored in the I-layer. When a reverse pulse is applied, reverse current will flow for a short period of time, known as delay time, t_d. When a sufficient number of carriers have been removed, the current begins to decrease. The time required for the reverse current to decrease from 90% to 10% is called the transition time, t_t. The sum, $t_d + t_t$, is the reverse recovery time, which is a measure of the time it takes to switch the diode from ON to OFF.

Reverse Breakdown Voltage

The reverse breakdown voltage defines the maximum signal level which may be applied to the diode. Operation at signal levels above the reverse breakdown voltage may result in degradation of diode characteristics or in permanent damage to the diode.

Cutoff Frequency (f_c)

At frequencies much below cutoff (f_c), a PIN diode tends to behave as a simple PN junction, while well above the cutoff frequency the diode exhibits the characteristics of a simple current controlled resistor.

The recombination lifetime in a PIN diode, usually designated as τ (tau), is the time required for the stored charge in the I region of a forward biased PIN diode to decay to 1/e of its initial (DC biased) value. Determined by diode design, lifetime is an important characteristic of these diodes in that it affects switching speed as well as distortion performance. τ can range from 10 nsec to 2 μsec. The Cutoff Frequency is calculated by

$$f_c = 1/(2\pi\tau)$$

A plot of lifetime (τ) versus f_c is provided in Figure 8.

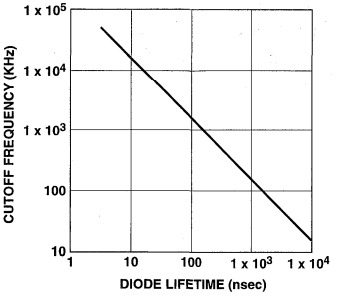


Figure 8. Diode Lifetime, nsec.

Switching Speed

In many applications, switching time is very important. Reverse recovery time is a measure of the switching time of a PIN diode, the time required to switch the diode from ON to OFF. The time needed to switch the diode from OFF to ON is shorter. (See Application Note 929, "Fast Switching PIN Diodes," for details.)

Applications of PIN Diodes

PIN diodes are used principally for the control of RF and microwave signals. Applications include switching, attenuating, modulating, limiting and phase shifting. Certain diode requirements are common to all these control functions, while others are more important in a particular type of usage.

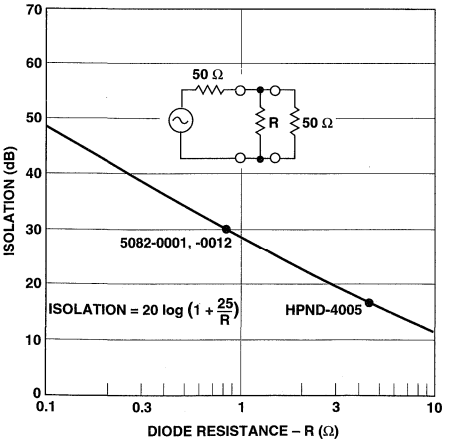


Figure 7. Typical Isolation of Shunt Diode Switch.

Switching Applications
The performance of a PIN diode circuit is directly related to the basic characteristics of the diode. As an illustrative example, the performance of a PIN diode switch can be simply approximated by treating the PIN diode essentially as a resistor in the forward biased state and a capacitor in the reverse biased state. Switch performance is normally evaluated by the Insertion Loss, Isolation, Switching Speed, and Power Handling Capability characteristics. These are summarized in the "Characteristics of PIN Diodes" section.

Attenuators
Whereas a switch is used only in its maximum ON or OFF state, an attenuator is operated throughout its dynamic range (or resistance range in the case of a diode attenuator). Although a single diode series or shunt switch can be used as an attenuator, it cannot offer in its entire dynamic range constant input and output impedance, which is required for optimum source and load matching in most attenuator applications. By using a multiple diode circuit such as π, T, or bridged-T attenuator, constant input and output impedance can be achieved throughout the attenuation range.

An additional requirement in most attenuator applications is low distortion. Distortion can be kept to a minimum, if the carrier lifetime of the PIN diode used is greater than the inverse of the signal frequency. HP recommends the minimum signal frequency be ten times the cutoff frequency, f_c, i.e., $f_c = 10/2\pi\tau$ or $1.6/\tau$, where τ is the carrier lifetime and f is the signal frequency.

See Distortion in the "Characteristics of PIN Diodes" section.

Limiters
Sensitive amplifiers, mixers, and detectors in microwave systems can be protected against damage by high level signals with the use of a PIN diode limiter shunting the transmission line.

A PIN diode limiter is essentially an attenuator that uses self bias rather than externally applied bias. As the RF input increases, the rectified current generated by the PIN diode (in some limiter circuits by an auxiliary Schottky diode) biases the diode to a low resistance state. Most of the input power is then attenuated, allowing very little to be transmitted. The sensitive equipment that follows is thus protected.

For a limiter circuit to be efficient, it is essential that the PIN diode has fast switching time. Without an auxiliary diode, a PIN diode with good rectification efficiency is needed to achieve low resistance. Another diode requirement is good heat transfer characteristics (low thermal resistance).

Phase Shifters
The high speed switching capabilities and low ON and high OFF resistance states of the PIN diode make it also very useful for many types of high speed, current controlled phase shifter applications. Another important requirement for these applications is the uniformity of diode characteristics such as capacitance and resistance, particularly in systems where a large number of elements are involved.

Application Recommendations

Applications	HSMP 380x	HSMP 381x	HSMP 382x	HSMP 383x	HSMP 386x	HSMP 388x	HSMP 389x	Glass Axial Lead	Beam Lead	Chip	Pkgd	General Interest
Attenuators	•	•		•	•				•	•		
Switching			•	•	•	•	•		•	•		
AGC Circuits	•	•			•					•		
Power Limiters			•									
Phase Shifting									•	•		
Modulating									•	•		
Application Notes Number/Subject												
A001 Notes on Choke Network Design												•
A004R ESD and ESD Control												•
A005 Transistor Chip Use										•		
A006 Packaged Semi Mounting											•	
922 Applications	•	•	•	•	•	•	•		•	•	•	•
929 Fast Switching			•	•	•	•	•					
957-2 Reducing Shunt Insertion Loss			•	•	•	•	•					
957-3 Rectification Effects											•	
979 Handling/Bonding of Beam Lead Devices									•			
985 Hi Iso in Series Apps with HPND 4005									•			
992 Beam Lead Attachment Methods									•			
993 Beam Lead Bonding to Soft Substrate									•			
1048 Low-Cost SMT Pi Attenuator	•	•		•	•							
1049 Low Distortion Switch			•	•	•		•					
1050 Low-Cost Power Limiters							•					
1054 Low-Cost Frequency Multipliers			•									
1067 SPDT T/R Switch for PCN Applications			•	•	•	•	•					
1072 HSMP 3890 Switching Applications							•					

Application Information

The following application information is either published in this catalog or available from your local Hewlett-Packard sales office, authorized distributor, or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

Application Notes

Abstracts

Applications of PIN Diodes

Application Note 922

Introduction

The most important property of the PIN diode is the fact that it can, under certain circumstances, behave as an almost pure resistance at RF frequencies, with a resistance value that can be varied over a range of approximately 1 Ω to 10 KΩ through the use of a DC or low frequency control current.

When the control current is varied continuously, the PIN diode is useful for leveling and amplitude modulating an RF signal. When the control current is switched "on" and "off" or in discrete steps, the device is useful for switching, pulse modulating, attenuating, and phase shifting of an RF signal.

In addition, the PIN's small size, weight, high switching speed, and minimized parasitic elements make it ideally suited for use in miniature, broadband RF signal control components.

This application note describes the important properties of the PIN diode and illustrates how it can be applied in a variety of RF control circuits. Related HP publications of special interest are:

1. AN 929, Fast Switching PIN Diodes.
2. AN 985, Achieve High Isolation in Series Applications with the Low Capacitance HPND-4005 Beam Lead PIN.
3. AN 957-1, Broadbanding the Shunt PIN Diode SPDT Switch.
4. AN 957-2, Reducing the Insertion Loss of a Shunt PIN Diode.
5. AN 957-3 Rectification Effects in PIN Attenuators.
6. AN 979, Handling and Bonding of Beam Lead Devices.

Characteristics of the PIN Diode

A PIN diode is a silicon semiconductor consisting of a layer of intrinsic (high resistivity) material of finite area and thickness which is contained between highly doped p and n type material. When the diode is forward biased, charge is injected into the intrinsic or "I" region. This charge consists of holes and electrons which have a finite lifetime before recombination. The density of charge in the intrinsic region and its geometry determines the conductance of the device, while the lifetime [denoted by τ (tau)] determines the approximate low frequency limit of useful application.

The conductance of the diode is proportional to the stored charge and the charge is in turn related to the diode current by

$$I_d = \frac{dQ_d}{dt} + \frac{Q_d}{\tau} \qquad (1)$$

where I_d = Diode current
Q_d = Charge stored in the diode
τ = Recombination lifetime
d = delta

If the diode is biased with only a constant current, the stored charge is constant and is equal to:

$$Q_d = I_d \tau \qquad (2)$$

If the bias consists of both a constant current and a low frequency RF or time varying signal, then the dc component of stored charge will be "modulated" by the presence of an ac component. The degree of modulation depends on the relative level of the two charge components and the frequency of the RF signal.

This dependence on frequency can be readily seen by solving the Laplace transform of Eq. (1) which yields

$$Q_d(\omega) = \frac{i_d\tau(j\omega)}{1 + j\omega\tau} \qquad (3)$$

where $(\omega) = 2\pi$ freq.

This is plotted in Figure 1(a) and illustrates that at signal frequencies below $f_c = 1/2\pi\tau$ the RF signal has about the same effect as the dc bias. Above f_c however, the modulation effect decreases by about 6 dB/octave.

The lifetime of PIN diodes is determined by design and is usually based on the desired switching speed. Typically, τ can be in the range of 0.005 µsec to over 3 µsec. For a value of 100 nsec, f_c is ≅ 1.6 MHz. Thus, the diode can be simply visualized as follows: At frequencies well below f_c, the PIN diode behaves as an ordinary PN junction diode. The RF signal incident on the diode will be rectified and considerable distortion of the signal will occur. In the vicinity of f_c, the diode begins to behave as a linear resistor with a small nonlinear component. The signal consequently suffers some degree of distortion. At frequencies well above f_c, the diode appears essentially as a pure linear resistance whose value can be controlled by a dc or a low frequency control signal.

a) Low and High Frequency Equivalent Circuits

Because of this behavior, the equivalent circuit of the PIN diode also depends on the frequency. At frequencies much less than f_c, the equivalent circuit is as shown in Figure 2(a) and is that of a normal PN junction diode.

In this circuit

L_P = Package Inductance
C_p = Package Capacitance
R_s = Series Resistance
R_j = Junction Resistance $\cong \frac{nkT}{qI_{dc}}$

For a typical n = 1.8 and at room temperature

$$R_j \cong \frac{48}{I_{dc(mA)}}$$

I_{dc} = Forward dc Bias Current
$C_{j(v)}$ = Junction Capacitance = a function of applied voltage

At frequencies just below and just above f_c, the equivalent circuit of a PIN diode depends upon the way in which the device was designed. It can reflect behavior which is strongly inductive or strongly capacitive. In addition, operation at moderate bias levels in this frequency range will result in the generation of large amounts of distortion.

At frequencies much higher than f_c, the equivalent circuit is as shown in Figure 2(b). Here the elements L_p, C_p and R_s are the same as in Figure 2(a). The element C_I, represents the I-layer capacitance which is constant and dependent only on the geometry of the I-layer. This capacitance can be measured by conventional bridge techniques and at a low (usually 1 MHz) frequency if the diode is reverse biased past the punch-through voltage to assure that the I-layer is fully depleted. Typical values of C_I for present HP PIN diodes are in the range of 0.02 to 2 pF, depending on the diode design. The element R_I represents the *effective* RF resistance of the I-layer. Although shown as variable, *this resistance is constant with respect to the RF signal*, providing the

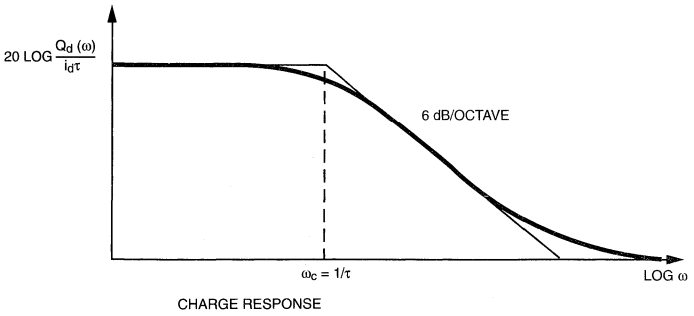


Figure 1. PIN Behavior as a function of Frequency.

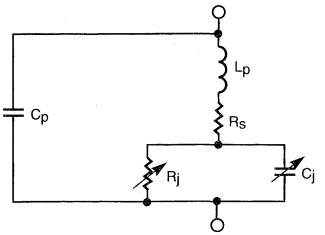


Figure 2(a). PIN Low Frequency Equivalent Circuit.

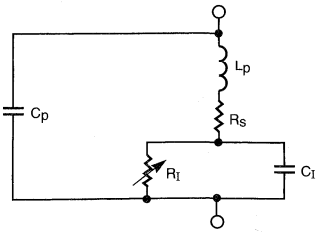


Figure 2(b). PIN High Frequency Equivalent Circuit.

frequency of the signal is much higher than f_c, It is, however, variable by the dc or very low frequency control current.

b) The RF Resistance Characteristic

Although the PIN diode is a two-terminal device, it behaves essentially as a two-port device. With respect to the DC or low frequency control signal, it appears as the circuit shown in Figure 2(a), and with respect to RF signals of frequency > $10f_c$, it appears as the circuit shown in Figure 2(b). The transfer characteristic of this unconventional two-port is governed by the resistance R_I, which can be written as

$$R_I = K/I_{dc}^{x}$$

where R_I is the effective high frequency resistance and I_{dc} is the dc bias current in mA. The dependence of R_I on I_{dc} is similar in form to the dependence of R_j on I_{dc} in the low frequency equivalent circuit; however, the constant K and the exponent x are different. The high frequency resistance function is plotted in Figure 3 for the HPND-4165 diode. Due to a variety of mechanisms that exist in the diode at RF frequencies, both K and x must be determined empirically. For a specific diode design, the exponent x is usually a constant. For the HPND-4165, x is typically 0.92. The constant K and therefore, R_I, however, are highly dependent on the fabrication and process control and its value can vary by as much as 3:1 from diode to diode. For switching or pulse modulating application, the variation of R_I between diodes at a given bias is not significant since the diode is usually switched between a very high and a very low value of resistance by the control current. For analog applications such as attenuating and modulating, and particularly where repeatability and tracking of the attenuation with bias current is desired, this variation of R_I from unit to unit can impose a design and performance limitation. The HPND-4165 is precisely controlled in manufacturing, and resistance values at specific bias points are specified and the slope of resistance vs. bias matched within narrow limits. The specification limits of these parameters are:

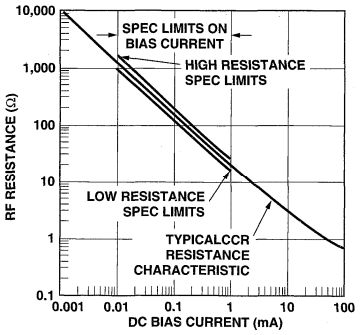


Figure 3. Typical RF Resistance versus Bias Current for HPND-4165.

HPND-4165 PIN Specifications

Parameter	HPND-4165	Test Conditions
High Resistance Limit R_H	1100-1660 Ohms	10 μA
Low Resistance Limit R_L	16-24 Ohms	1 mA
Max Diff. in Resistance vs. Bias Slope Δ x	0.04	10 μA and 1 mA

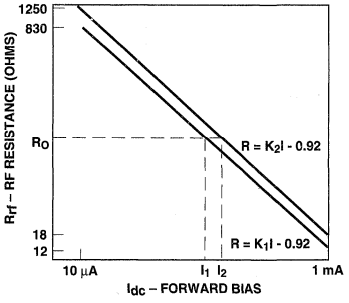


Figure 4. Matching of PIN Diodes by Offset Current.

Both of the resistance limits and the slope are determined by measurement at a test frequency of 100 MHz. An example of these resistance limits is shown graphically in Figure 4. The placement of resistance limits on both extreme values of resistance *and* independently on the slope, assures that the resistance vs. bias curves for individual diodes will be essentially parallel lines lying within the tunnel defined by the

high and low resistance limits. Extremely close tracking between diodes can therefore be achieved by offsetting the bias on one diode with respect to the other. The offset current ratio required to achieve this is given by

$$\frac{I_2}{I_1} \cong \left(\frac{K_2}{K_1}\right)^{\frac{1}{x}}$$

The K values of the individual diodes can be readily determined by measuring the RF resistance of the diodes at a 1 mA dc bias current.

c) Effects of Package Parasitics

Typical HP PIN diode packages are illustrated in Figure 5. With the exception of the Stripline (Style 60) package, all the other packages introduce additional reactive elements in the form of package inductance L_p and package capacitance C_p. These elements are shown in Figure 2 and typical values for some packages are given in Figure 5.

In some applications these parasitic elements can be either "tuned-out" by additional external reactances or actually utilized by forming a resonant circuit around the diode. The bandwidth of such structures is, however, limited. When these elements cannot be tuned out, performance over a broad bandwidth will generally suffer.

As an example, Figure 6 shows the attenuation versus bias characteristics of the same diode in three different packages. In all cases, the device is mounted in shunt across a 50 ohm system. The frequency of operation is 500 MHz and in no case were any package parasitics tuned out. The solid lines are contours of constant attenuation calculated from an assumed equivalent circuit consisting of a parallel resistance R_p and a reactance X_p in shunt across a 50 Ω system. The coordinates of the graph are the resistance R_p and reactance X_p elements. The attenuatlon performance of a particular diode can be easily determined by plotting its equivalent R_p and X_p components at any frequency of interest.

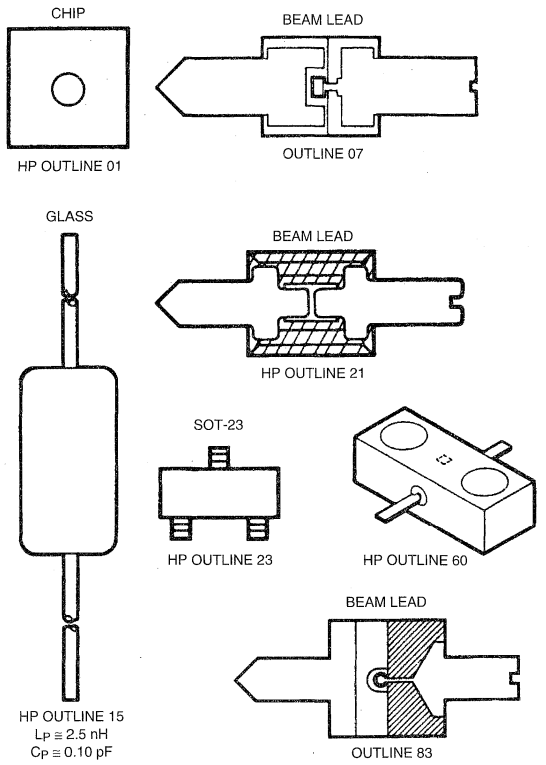


Figure 5. Package Outlines

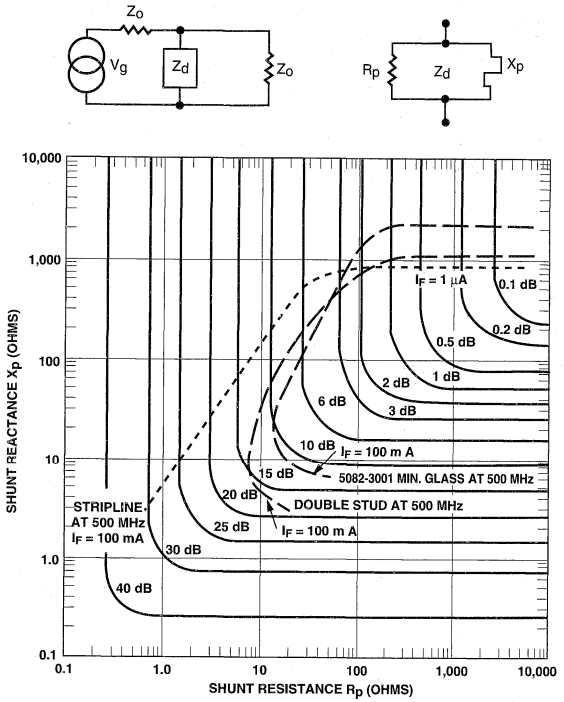


Figure 6. Attenuation Produced by a Shunt PIN Diode as Its Impedance Varies with Changes of Bias Current.

500 MHz is a relatively low frequency, nevertheless differences in the attenuation characteristics of different packaged diodes are evident. At frequencies much higher than 500 MHz, the glass and the double stud diodes will show lower attenuation.

The Stripline package does not exhibit this limitation because the internal reactance elements are proportioned to form a low-pass filter structure with a high (30 GHz) cut-off frequency.

Because of this design, the Stripline PIN diode does not require any external matching elements when used in a 50 ohm Stripline circuit and can be used in the design of extremely wide-band RF control circuits.

d) Distortion in PIN diodes

Two basic methods are used to fabricate PIN diodes. In the case of BULK diodes, a wafer of very pure (intrinsic) silicon is heavily doped on the top and bottom faces to form P and N regions. The result is a diode with a very thick, very pure I region. The epitaxial layer (or EPI) diode starts as a wafer of heavily doped silicon (the P or N layer), onto which a thin I layer is grown. After the epitaxial growth, diffusion is used to add a heavily doped (N or P) layer on the top of the epi, creating a diode with a very thin I layer populated by a relatively large number of imperfections.

These two different methods of design result in two classes of diode with distinctly different characteristics, as shown in the table below:

Parameter	EPI Diode	Bulk Diode
I-layer	Thin	Thick
Lifetime	Short	Long
Distortion	High	Low
Current	Low	High

While manufacturers seldom classify their PIN diodes as bulk or epi devices, one can generally identify them by their lifetime, τ. Lifetime is generally short (35 to 200 nsec.) for epi diodes and relatively long (400 to 3000 nsec.) for bulk diodes.

At frequencies above $10f_c$, the PIN diode acts as if it were a variable resistor. However, it is a non-linear device and, as such, it generates distortion. There are three kinds of distortion; harmonic, intermodulation and crossmodulation. While they are different from each other, they are related. All of them are strongly influenced by the lifetime of a PIN diode, as well as the RF power which is applied to the diode. Long lifetime bulk diodes produce such little distortion that the accurate measurement of it is often very difficult with the best of instruments. Short lifetime epi diodes produce high amounts of distortion; under some bias conditions, such a PIN diode behaves very much like a SRD (Step Recover Diode) comb generator.

PIN diode distortion drops suddenly as bias is set to zero (or reverse bias) or to very high levels of current. Distortion is worst at the intermediate levels of bias where the PIN diode's resistance is some moderate value. Thus, it can be seen that attenuator applications require the use of a long lifetime bulk diode to minimize distortion. In switch applications, where the bias is always at one extreme or the other, epi diodes generally perform satisfactorily and offer the advantage of low current consumption.

In reading the following paragraphs, it should be borne in mind that the bulk diode is always used for attenuator applications and sometimes as a switch, while the epi diode is used as a switching element only.

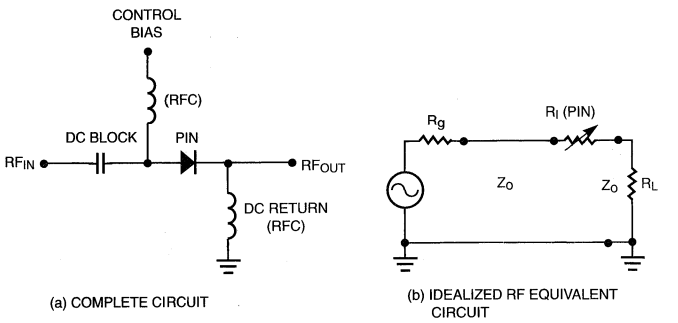


Figure 7. Series PIN RF Attenuator or Switch.

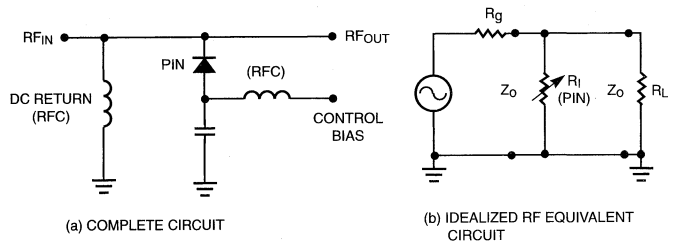


Figure 8. Shunt PIN RF Attenuator or Switch.

PIN Diode Applications

a) Design of Broadband Reflective SPST Switches and Attenuators

The previously described characteristics of the PIN diode make it ideally suited for use in attenuating or switching of RF signals. Two of the simplest circuits that can be used for this are shown in Figures 7 and 8.

The attenuation in the Series PIN circuit is decreased as the RF resistance of the PIN is reduced by increasing the forward current. The opposite occurs for the shunt configuration. If the control bias is switched rapidly between high and low (zero) values, then the circuit acts simply as a switch. When used as a switch, the residual attenuation that exists when the switch is "ON" is usually called Insertion Loss (I.L.). The attenuation provided when the switch is "OFF" is usually called Isolation (I.S.). If the diode is assumed to be a pure resistance at RF, then the attenuation for each circuit is given as:

$$\alpha_{(series)} = 20 \log \left(1 + \frac{R_I}{2Z_o}\right);$$

$$\alpha_{(shunt)} = 20 \log \left(1 + \frac{Z_o}{2R_I}\right);$$

where $Z_o = R_G = R_L$ Circuit, Generator and Load Resistance, respectively.
R_I = PIN diode RF resistance at the specified bias current.

As can be seen, the attenuation is not dependent on frequency and is a function of the ratio of the circuit resistance to the diode resistance. As the bias on the diode is varied, the load resistance as seen by the source also varies; consequently, attenuation is achieved primarily by reflection and partly by dissipation in the PIN diode. Circuits of this type are generally referred to as reflective switches or attenuators.

As was shown previously, a real diode contains several reactance elements due to the diode and the package. Consequently, when a real diode is used, the attenuation characteristic becomes frequency dependent. For an equivalent circuit shown in Figure 9, the attenuations for the two circuits are given by:

$$\alpha'_{(series)} = 10 \log \left[\frac{\left(\frac{R'_S}{Z_o} + 2\right)^2 + \left(\frac{X'_S}{Z_o}\right)^2}{4} \right]$$

$$\alpha'_{(shunt)} = 10 \log \left[\frac{\left(\frac{R'_S Z_o}{R'^2_S + X'^2_S} + 2\right)^2 + \left(\frac{X'_S Z_o}{R'^2_S + X'^2_S}\right)^2}{4} \right]$$

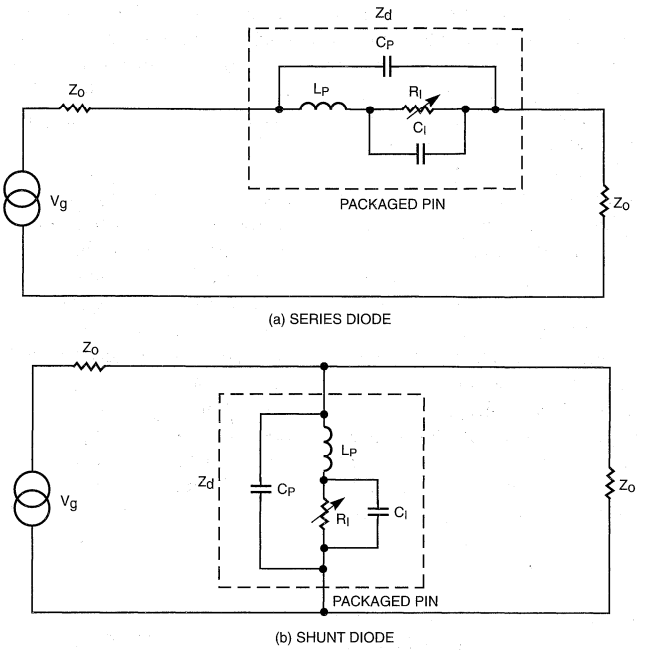


Figure 9. Packaged Diodes Used as Reflective Attenuators.

where R'_S and X'_S are the series equivalent resistance and reactance of the diode impedance, i.e., $Z_d = R'_S + jX'_S$.

These α functions are plotted as a function of frequency in Figures 10(a) and 10(b) which show what values of isolation and insertion loss might be typically obtained for single packaged diodes in either shunt or series reflective attenuators. These curves are based on typical values of diode and package parameters. The upper frequency performance can be improved slightly by tailoring the circuit geometry around the diode package. For example, the high package inductance (~ 3 nH) of the glass packaged diode can be reduced in the series circuit by moving the ground plane or planes of the transmission line closer to

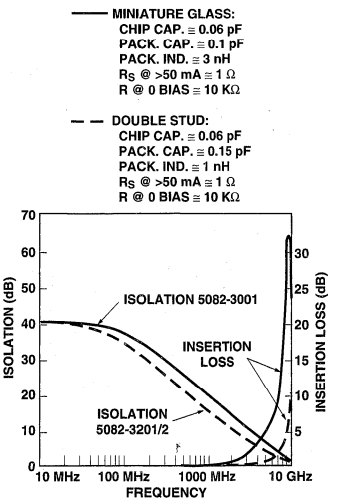


Figure 10(a). Attenuation of Series Diodes Used as a Switch in a 50 Ohm System.

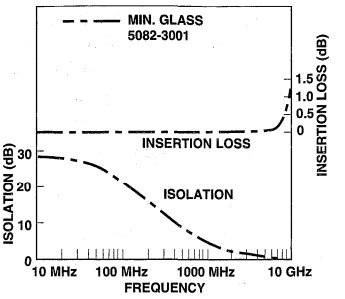


Figure 10(b). Attenuation of Shunt Diodes Used as a Switch in a 50 Ohm System.

the diode package, as shown in Figure 11. This technique reduces the package inductance by making it appear more like a transmission line. It also reduces the series coupling capacitance of the package by cutting the axial electric field across the diode. The former effect decreases the insertion loss and the latter increases the isolation at higher frequencies. The Stripline diode does not begin to exhibit these limitations until approximately 18 GHz because the internal reactances of the package and diode are part of a low pass filter structure. The mini-strip or microstrip package can be made part of a low pass filter by tailoring the lead inductance so the reactance equals the characteristic impedance of the line at the cutoff frequency. This is the frequency where the capacitive reactance of the diode is half the line impedance. The combination of the two leads and the diode forms a three element low pass filter. Other combinations of cutoff frequency and lead inductance may be obtained from tables of filter elements.

b) Design of Resonant SPST Switches

Another way that the performance of a packaged diode can be improved at high frequencies is to "tune-out" the parasitic elements by the addition of external reactances. Such circuits are generally referred to as resonant switches in which the PIN diode is used essentially as a switch which switches the circuit parameters from a parallel resonant condition to a series resonant condition. The high and low impedances produced by the parallel and series resonant circuits, respectively, constitute the "ON" and "OFF" states of the switch. Although the performance can be improved at the design frequency, the bandwidth of resonant switches is necessarily limited, usually to $\leq 10\%$.

Figure 12 shows two typical resonant switch circuits which are useful at frequencies below 1 GHz, or where the required external inductance L is much greater than the diode parasitic inductance L_p and the external capacitance C is much greater than the package capacitance C_p. Under these conditions, the diode parasitic elements have a negligible effect on performance. The equivalent circuits for the two states of this resonant switch are shown in Figure 12 (c) and (d). When the diode is forward biased, the elements L_1, and C_I are in parallel resonance and the circuit between A and B appears as a high impedance. When the diode is reverse biased, the elements L_2, and C_I are in series resonance and the circuit between A and B appears as a low impedance. In both cases, the impedances between A and B are finite due to the presence of diode resistance and finite element Q's. Both of these effects are represented as loss resistances R_{sp} and R_{ss}, respectively. The expected insertion loss, maximum attenuation, and bandwidth can be obtained from the formulas given in Table 1. For L_1 and L_2 being equal, the resonant frequency in both

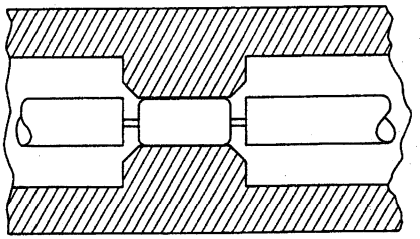


Figure 11. Optimizing a Glass Packaged Diode for Series Reflective Attenuating in a Coaxial Line.

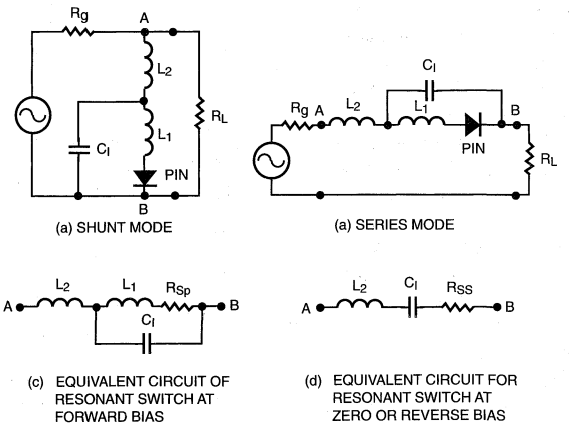


Figure 12. Resonant PIN Switch Circuits.

cases is approximately

$$f_o \cong \frac{1}{2\pi\sqrt{L_I C_I}}$$

the approximation being due primarily to the fact that diode parasitic elements affect the two resonant states differently. In the parallel resonance state, there will also be a secondary series resonance at approximately $f_2 = 1.4\ f_o$.

At frequencies higher than 1 GHz, the circuits shown in Figure 12 are difficult to design because the values of the external reactances begin to approach those of the diode parasitic reactances and considerable interaction between the various elements occurs. Although this mode is still possible, the synthesis will generally have to be empirical.

Resonant switches can also be built by utilizing the package parasitics and the diode chip capacitance C_I, if these are of the right value, or by tailoring these package parasitics; which is possible with the microstrip package. In this mode of operation, the equivalent circuit of Figure 13 applies. The mode of operation is similar to the one described previously and is evident in Figures 10(a) and 10(b) where it can be observed that as the frequency increases, the insertion and isolation curves approach each other and finally reverse roles as the equivalent circuits approach parallel and series resonance.

The element values are chosen such that L_p and C_I are in series resonance when the diode is reverse or zero biased, and the elements L_p and C_p are in parallel resonance when the diode is forward biased. For maximum isolation and minimum insertion loss, the two resonant frequencies must be equal which dictates that $C_I = C_p$. This, of course, requires a careful choice of the diode and the package for the frequency of interest. In many applications, however, a sufficiently high isolation to insertion loss ratio can be achieved by working on the slopes of two resonant responses of dissimilar frequencies. Consequently, C_I need only be approximately equal to C_p.

In a packaged diode, C_p can be varied over narrow limits by addition of external capacitance if $C_p < C_I$ which is generally true for large diodes, or by reducing the axial electric field around the diode in the manner described previously. The inductance can be controlled by external addition if L_p is less than required. The synthesis of the circuit is therefore very much controlled by the proper choice of the diode chip capacitance C_I, since this parameter cannot be controlled by the user.

The impedance appearing across A-B for the two resonant conditions is then

Series Resonance

$$R_{SR} \text{ where } R_{SR} = \frac{R_I}{1 + \frac{R_I^2}{X_{CI}^2}}$$

Parallel Resonance

$$R_S(1 + Q^2) \quad Q = \frac{X}{R_S}$$

and $R_S = R_I$ @ high forward bias

The isolation, insertion loss, and bandwidth may also be found from Table 1, simply by substituting R_{SR} for R_{SS} and R_S for R_{SP}. X is the reactance of either the resonating inductance or capacitance.

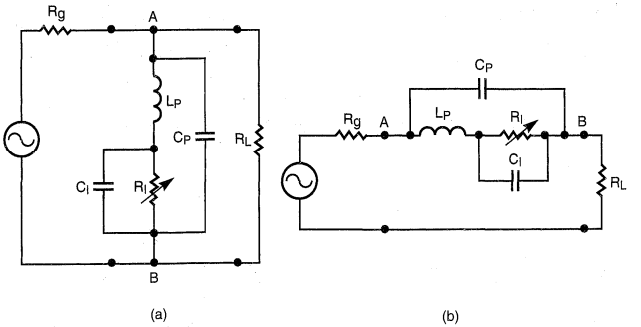


Figure 13. Resonant PIN Switches Realized with Use of Package Parasitics and Chip Capacitance.

Table 1.

	Attenuation (α)	Insertion Loss	Bandwidth
Series Mode Resonant Switch	Forward Bias $20 \log \left(\frac{R_{SP}^2 + X^2}{2Z_o R_{SP}} + 1 \right)$	Reverse Bias $20 \log \left(\frac{R_{SS}}{2Z_o} + 1 \right)$	Forward Bias $[4\pi Z_o C_1 X 10^{\alpha - 20}]^{-1}$
Shunt Mode Resonant Switch	Reverse Bias $20 \log \left(\frac{Z_o}{2R_{SS}} + 1 \right)$	Forward Bias $20 \log \left(\frac{Z_o R_{SP}}{2(R_{SP}^2 + X^2)} + 1 \right)$	Reverse Bias $\frac{Z_o}{4\pi L_2} X 10^{-\alpha/20}$

Applicable when $R_g = R_L = Z_o$

where:

$$R_{SP} = \left(\frac{Q_1}{1 + Q_1^2} \right) X$$

$$R_{SS} = \frac{X}{Q^2}$$

X = reactance of either the resonating inductance or capacitance

c) Design of Multiple Diode and Multi-throw Switches and Attenuators

When the maximum attenuation or isolation requirements are greater than what can be obtained by a single diode, multiple diode circuits using series, parallel or series-parallel arrangements can be used. Examples of such circuits are shown in Figure 14. A simple parallel or series connection of two diodes will only increase the attenuation by a maximum of 6 dB and will also increase the insertion loss.

However, if n diodes are spaced at quarter wavelength intervals, as shown in Figure 14(b), the overall attenuation can be increased by more than n times that of a single diode. The insertion loss, if it is due to parasitic elements, may also decrease because the 1/4 wavelength ($\lambda/4$) spacing produces cancellation of these reactances. Where $\lambda/4$ spacing is not practical, higher isolation can be achieved by using a series-shunt connection as shown in Figure 14(c). In this connection, isolations greater than the sum of that obtained with a single series and a single parallel diode may be obtained.

The discussion so far has been concerned with circuits that are essentially single-pole single-throw switches or two-port attenuators. A variety of multiple throw arrangements are also possible as shown in Figure 15. The design considerations for these circuits are similar to those outlined above except that interaction between diodes must be considered in the design. The SPDT circuit of Figure 15(a) operates as follows: When diode D_1 is forward biased and diode D_2 is zero or reverse biased, the RF power flows from Port 3 to Port 2 and Port 1 is isolated. When the two bias conditions are reversed, RF power flows to Port 1 and Port 2 is isolated. To minimize reactive loading of the open port by the closed port, the diodes are spaced $\lambda/4$ away from the feed point. The RFC provides a dc return for the bias currents and an open circuit for the RF signal. The capacitors C_1 and C_2 provide an RF ground for the diodes and an open circuit for the bias current. For increased isolation, additional diodes can be used which are spaced $\lambda/4$ away from the first set.

When $\lambda/4$ spacing is impractical or its bandwidth restriction is undesirable, a series configuration, as shown in Figure 15(b), can be used.

In this circuit, increased isolation can be provided by placing shunt diodes singly or in $\lambda/4$ spaced pairs at the output ports after the series diodes. This configuration is particularly useful for design of multiple-throw wideband switches. For multiple-throw configurations, additional series or series/parallel sections are added to the common feed point.

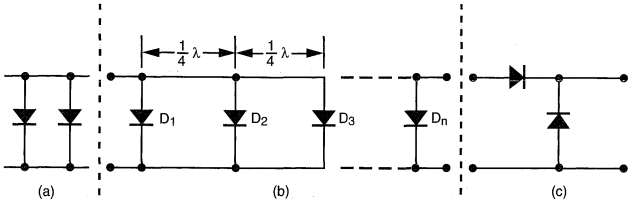


Figure 14. Reflective Mode Attenuators.

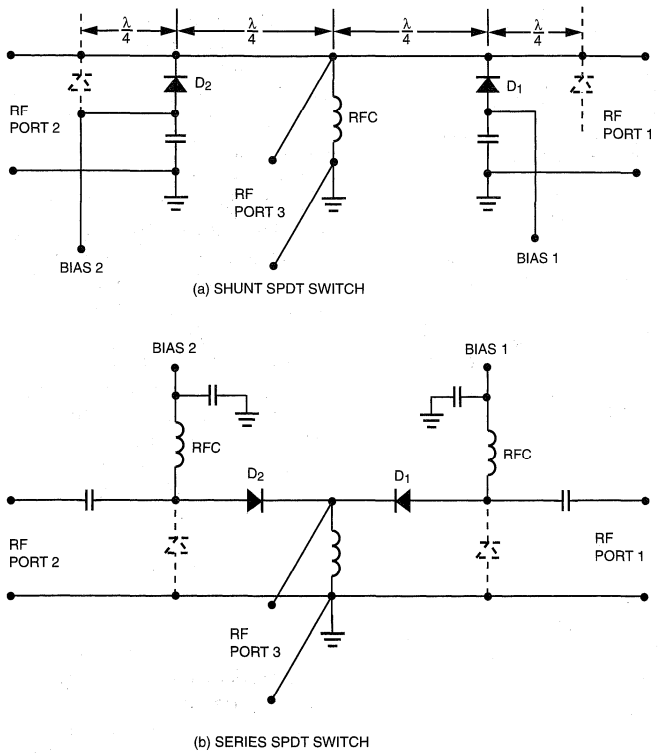


Figure 15. Multiple Throw PIN Switches.

d) Design of Constant Impedance Switches and Attenuators

For some RF systems, the high reflection coefficient at the RF ports of the reflective switches cannot be tolerated. For such applications, a variety of constant impedance switches and attenuators can be built using PIN diodes. Several such circuits are shown in Figure 16. The circuits of Figure 16(a), (b), and (c), operate by absorbing the undesired RF signal power in the PIN diodes. The circuits of 16(d), (e), and (f) operate by reflecting the power to a different RF port. In Circuits a and b, the control current variation through each diode is arranged in such a way that the impedance at both RF ports remain essentially constant at the design value, while the overall attenuation can be varied over a range of less than 1 dB to greater than 20 dB. In Circuit c, the input impedance is kept constant by using a distributed structure with a large number of diodes. The impedance variation of each diode is also shaped so that the diodes in the center of the structure vary more than those near the ports. The resulting tapered impedance structure results in an essentially constant impedance at the ports, while the overall attenuation can be varied up to a range of 40-80 dB, depending on the length of the structure. The π and T circuit structures are generally very compact and are particularly useful at low frequencies in the range of 10 MHz to 500 MHz. In addition to being constant impedance, they exhibit very little change of phase with attenuation and are very useful for providing gain control in RF transistor amplifiers in which bandpass and phase characteristics must be maintained over a large range of gain variation. Performance information on the π attenuator is contained in HP Application Note 1048.

Because of its distributed nature, the circuits of Figure 16(c) are generally too large to be useful at lower frequencies but are very useful above 1 GHz. This circuit is particularly attractive when very large attenuation ranges are required. Additional design information on this type of attenuator is contained in Ref. 1.

The attenuator circuits of Figure 16(d), (e), and (f) achieve constant impedance characteristics by virtue of the properties of the coupling elements which are placed between the RF ports and the PIN diodes. In the circuit of 16(d), the power incident on Port A of a 3 dB, 90° hybrid divides equally between Ports B and C, and Port D is isolated. The mismatch produced by the PIN diode resistance in parallel with the load resistance at Ports B and C reflects part of the power. The reflected powers at B and C combine and exit out of Port D. Port A, in this case, is isolated and therefore appears matched to the input signal. The maximum attenuation that can be achieved with this scheme depends on the directivity of the coupler and the quality of the terminations at Ports B and C when the diodes are unbiased. The VSWR at Port A will depend on the

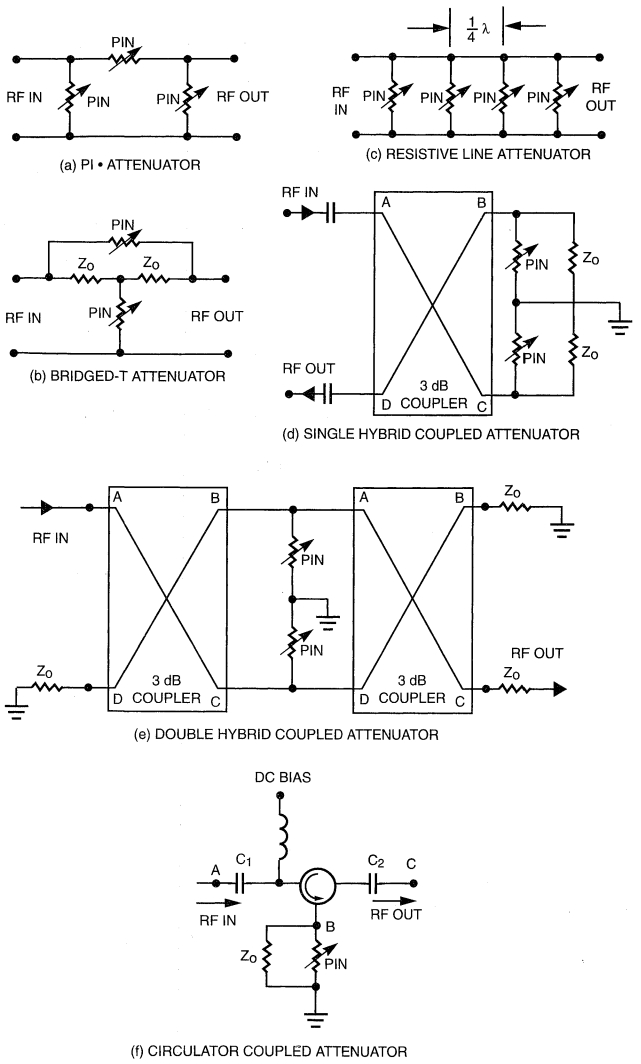


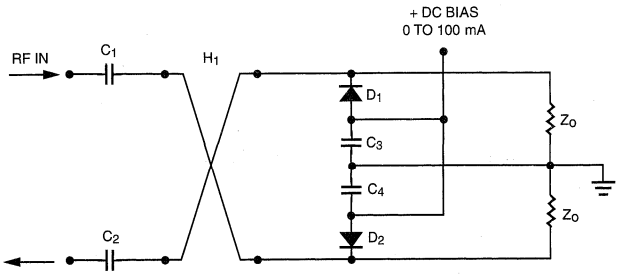
Figure 16. Constant Impedance PIN Diode Attenuators.

equality of the power split in the hybrid and the equality of the reflection coefflcients at Ports A and B. To assure the latter, the diodes must be reasonably well matched and must be spaced equally from Ports B and C. The insertion loss will depend on the losses and the equality of power split in the coupler and the minimum resistance of the PIN diodes when forward biased.

Circuits of this type can be easily and economically constructed in 50 ohm stripline form using the HP Stripline PINs. These diodes require no external matching structure and are very consistent in respect to the position of the effective internal reflection plane. The typical performance that was obtained with this type of circuit is illustrated in Figure 18 for the circuit of Figure 17. As can be seen, this kind of attenuator is useful over a wide frequency range. However, due to the hybrid directivity, there will be a considerable ripple in the high attenuation state. The ease with which the Stripline PIN diodes can be incorporated in such circuits is illustrated in Figure 19. Here broad-band biasing is achieved by applying the bias current to the diode at an "RF ground" point. After passing through the diode, the bias currents are returned to ground through the 50 ohm terminating loads.

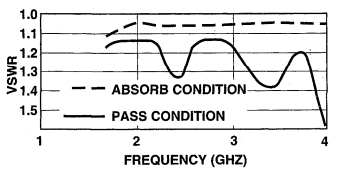
The ripple in the attenuation characteristics of the single hybrid coupled attenuator can be eliminated by using two identical hybrids as shown in Figure 16(e). This circuit eliminates the dependency of attenuation on hybrid directivity and its variation with frequency. The typical performance achieved with the double hybrid circuit using HP diodes is illustrated in Figure 21 for the circuit of Figure 20. The construction of this circuit is also in stripline but differs from the previous one by the biasing scheme. Instead of using ceramic RF bypass capacitors, the diodes make direct contact with the RF ground planes and bias is applied through inductors L_1 and L_2, which appear as a high impedance to the RF signal. As in the previous circuit, the spacing of the diodes from the hybrid ports must be equal and the diodes must be reasonably well matched.

The circuit of Figure 16(f) achieves constant impedance characteristics by virtue of the isolation properties of the circulator. The PIN diode shunts the matched B port impedance Z_o. When the PIN appears as a high resistance, all power is absorbed in Z_o at Port B. As the PIN impedance changes, Port B is progressively mismatched and power is reflected and passed by circulator action to Port C where it is absorbed in a matched load. The maximum attenuation attainable in this circuit depends on the matched port circulator isolation and the quality of the match of the circuit at Port B when the PIN diode is zero or reverse biased. The mechanical and electrical properties of the Stripline PIN diode make it ideally suited for direct integration into the usual stripline ferrite circulator structures.

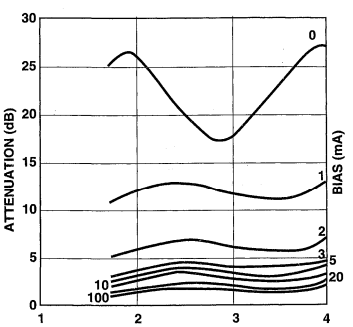


H_1 – 3 dB, 90° 1/8" STRIPLINE COUPLER (15 dB DIRECTIVITY OR BETTER 0.8 TO 4.3 GHz)
D_1, D_2 – HP STRIPLINE PIN DIODE
C_1, C_2 – DC BLOCKS
C_3, C_4 – 480 pF CERAMIC RF BYPASS CAPACITORS
Z_o – 50 OHM STRIPLINE LOADS

Figure 17. S-Band Single Hybrid Coupled PIN Attenuator.



(a) VSWR VERSUS FREQUENCY



(b) ATTENUATION VERSUS FREQUENCY

Figure 18. Performance of an S-Band Single Hybrid Coupled PIN Attenuator.

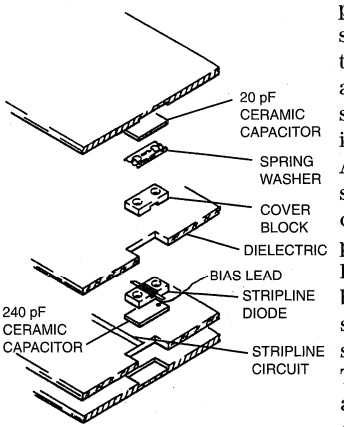


Figure 19. PIN Diode Biasing in Stripline Structures.

PIN Diode Phase Shifters

The high speed switching capabilities and the low "ON" and high "OFF" impedance states of the PIN diode make it also very useful for many types of high speed, current controlled phase shifter applications. Figure 22 shows a number of practical PIN diode phase-shifter circuits. All of these circuits are easily realized in economical stripline form and require no diode matching structures.

As an illustration, a two-bit, 90°-180°, phase-shifter circuit is shown in Figure 22(a). The circuit uses a conventional stripline 3 dB hybrid and HP stripline PIN diodes. The diode mounting and biasing was as shown in Figure 19. 90° and 180° of phase shift was obtained by biasing Ports 1 and 2, respectively. The insertion loss in any state should be approximately 1 dB and the VSWR < 1.1:1. For smaller phase increments, diodes can be spaced closer, however the effective electrical length of the package and the operating frequency will set the limit on the minimum phase increment in this kind of circuit. At higher frequencies and/or smaller phase increments, electrically shorter low parasitic diode packages, such as the HP beam lead, can be used or the circuit can be modified by cascading several stages of hybrid coupled phase shifters as shown in Figure 22(b). The hybrid coupled phase-shifters are generally economical to build and require a small number of diodes.

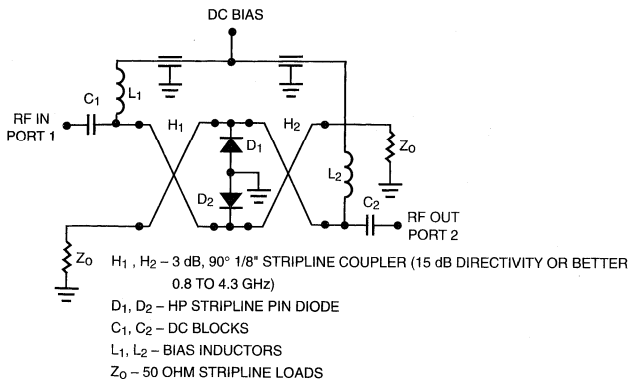


Figure 20. S-Band Double Hybrid Coupled PIN Attenuator.

Other phase-shifter circuits, as shown in 22(c) and (d), are usually more expensive (circulator cost) or require more diodes. The loaded line circuit which had been popular in early phase-shifter designs requires a very large number of diodes. The design of this kind of circuit is well covered in existing literature, particularly Ref. 2.

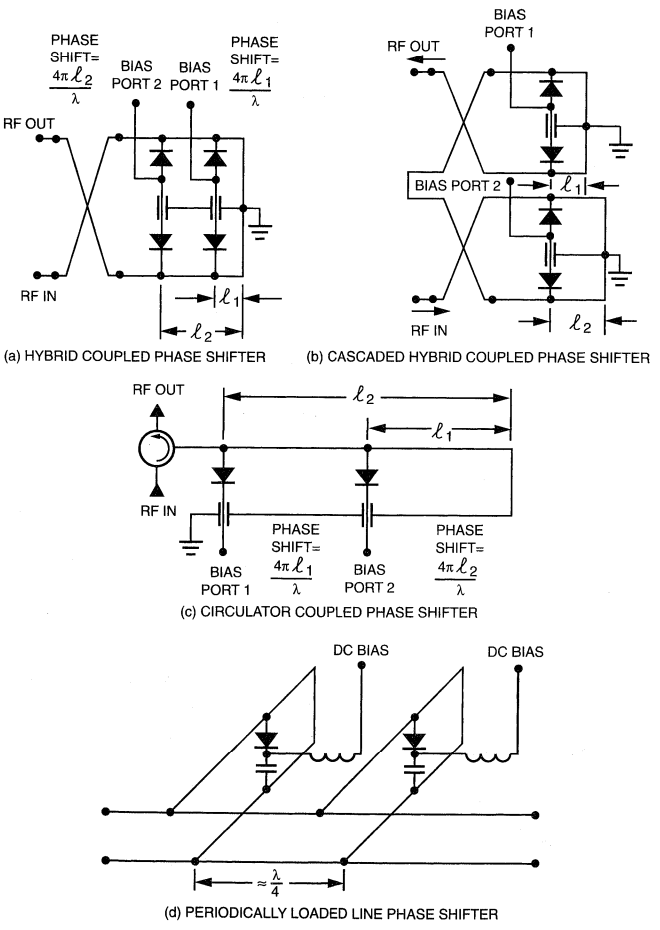


Figure 22. PIN Diode Phase Shifters.

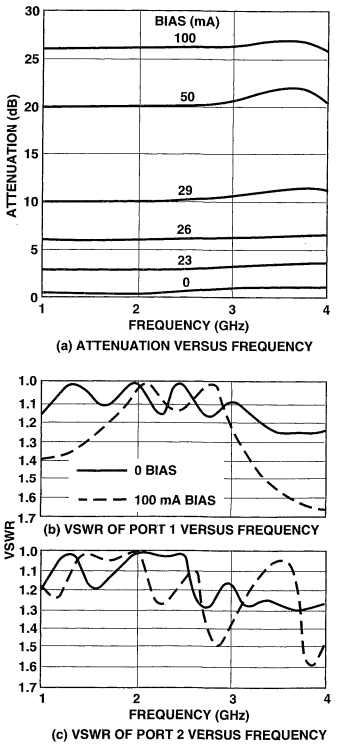


Figure 21. Performance of an S-Band Double Hybrid Constant Impedance PIN Attenuator.

PIN Diode Power Handling

The maximum signal RF power that a PIN diode can handle is limited by either the diode's breakdown voltage or its power dissipation capability. In most cases, power dissipation capability sets the lower limit on signal power handling.

Because PIN diodes are usually operated in a reflective mode, the amount of signal power that can be handled by a PIN in a circuit is usually very much larger than the actual power dissipated in the diode. The ratio of the power dissipated in the diode to the incident power depends on the impedance of the diode relative to the circuit impedance, the number of diodes, and their relative spacing. The following calculation sequence refers to Figures 23 and 24 which relate the CW Power Multiplier to either resistance or attenuation.

1. Read the power dissipation limit from the absolute maximum ratings given in the appropriate data sheet.
2. Determine the CW Power Multiplier from Figure 23 if diode resistance is known. Alternatively, use Figure 24 if circuit attenuation is known.
3. Multiply the power dissipation limit by the CW Power Multiplier determined in (2).

For example, for the series mode and a diode with a low and high resistance state of 1 and 10K ohms, respectively, approximately 2% (CW Power Multiplier = 50) of the input power will be absorbed by the diode in either the "ON" or the "OFF" state. If such a diode can dissipate 3 watts, it can therefore handle 150 watts of signal power. In the shunt mode, the low resistance state corresponds to the highest absorbed power, which in this case is 7.5% (CW Power Multiplier = 13.3) of the incident power. Hence, this same diode can handle 40 watts of signal power.

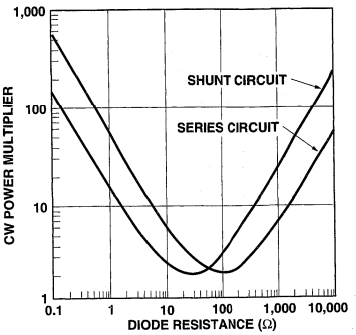


Figure 23. CW Power Multiplier vs. Diode Resistance.

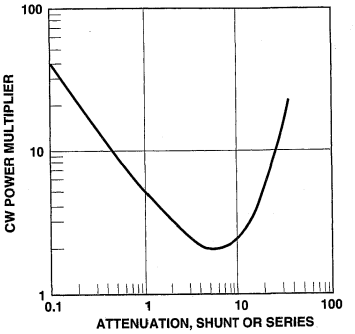


Figure 24. CW Power Multiplier vs. Series or Shunt Attenuation.

If two diodes are used in shunt to gain higher isolation, their spacing determines how much power is dissipated in each. The lead diode in a paralleled diode set will absorb either an equal or a greater amount of power than the second diode, depending upon the electrical spacing of the two diodes. Figure 25 shows what fraction of the input power will be dissipated in the lead diode as a function of total circuit attenuation and diode spacing for a shunt paralleled diode set in a 50 ohm system. Dotted curves indicate the constant resistance contours to which the diodes are biased.

A common switching application uses two shunt diodes in a double throw circuit, as shown in Figure 15. One shunt diode is used in each arm of the switch. The diodes are located a quarter wave from the junction of the two output arms and the input arm.

The power multiplier for either shunt diode in this circuit is much larger than the multiplier for a single shunt diode. For example. the multiplier for a 1 ohm diode is 53, compared to 13.5 for a single diode. For a 0.5 ohm diode, the multiplier is 103, compared to 26 for a single diode. The advantage is approximately a factor of four, so that a shunt diode in this double throw configuration can switch the same power as a series diode.

Since power handling can be many times greater than the power dissipated in the diode. the latter should be minimized and carefully controlled in high power applications. The maximum power that a PIN diode can dissipate is given by:

$$P_{max} = \frac{T_{j(max)} - T_A}{\theta_{jc} + \theta_{jA}}$$

where:

$T_{j(max)}$ = maximum operating diode junction temperature
T_A = Ambient temperature
θ_{jc} = Thermal resistance – junction to case
θ_{jA} = Thermal resistance – case to ambient

The junction-to-case thermal resistance is determined by diode and package design. The case-to ambient thermal resistance is

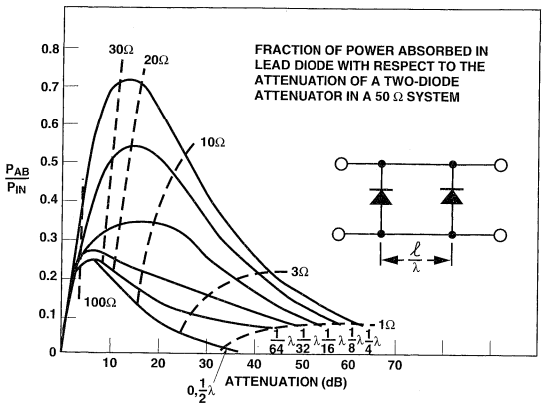


Figure 25. Fraction of Power Absorbed in Lead Diode with Respect to the Attenuation of a Two-Diode Attenuator in a 50 Ω System.

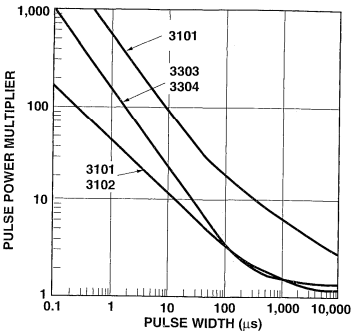


Figure 26. Pulse Power Multiplier vs. Pulse Width.

determined by how well the diode is mounted. For very low θ_{jc} diodes, good thermal mounting is particularly important. The HP Stripline package, with its large, flat, copper body and 2-bolt mounting capability, is particularly well suited for applications requiring a minimum overall thermal resistance.

If the PIN diode is used to control pulsed RF power, the peak power that can be handled increases as the pulse width decreases. This is because the effective thermal resistance decreases with pulse width. For a given pulse width, the maximum peak dissipated power can be determined from Figure 26. For example, at a pulse width of 10 μsec, the peak power handling capacity is increased by ten times.

In all cases, the voltage breakdown limit must be checked. For the series circuit this is expressed as:

$$P_A\,(max) = \frac{(V_{BR} - V_{BIAS})^2}{400}\,W$$

and for the shunt circuit:

$$P_A\,(max) = \frac{(V_{BR} - V_{BIAS})^2}{100}\,W$$

This limit is optimized by using zero reverse bias (V_{BIAS}). However, at low frequencies and/or high power, forward current may flow on the positive swing of the RF voltage, reducing the diode impedance. Reverse bias may be necessary in these cases. Reverse bias may also be needed to reduce switching time. See AN929, Fast Switching PIN Diodes, for details of this application.

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HEWLETT® PACKARD

Fast Switching PIN Diodes

Application Note 929

Switching Speed Definitions

The switching speed of a PIN diode may be defined and measured in a number of ways. Ideally, we would like to think of it as the time it takes the device to make the transition from the minimum insertion loss case to the maximum isolation case or vice versa. Because of the charge nonlinearities during switching of the device and the need for reasonable measurement techniques, we often settle for some definitions less than ideal.

A figure of switching capability commonly used by industry is the reverse recovery time (t_{rr}). Figure 1a shows the diode in the RF test circuit. Figure 1b shows the monitored current through the diode used to determine the reverse recovery time.

Note that under initial conditions, a forward bias (I_F) is forcing a charge equilibrium to exist in the intrinsic layer of the PIN diode. This equilibrium charge can be represented by $I_F\tau$ where τ is the minority carrier lifetime. To totally remove this charge, it is necessary to apply a reverse current through the device such that $I_F\tau = \int_{t_o}^{\infty} i_r dt$. In other words, the total area under the reverse

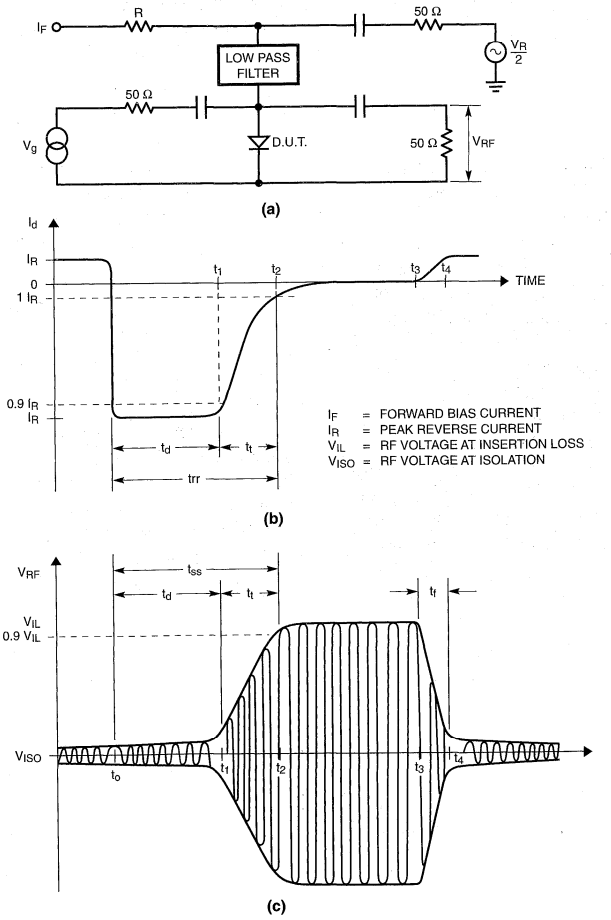


Figure 1. Switching Time Test Circuit with Drive Current Waveform and Switched RF Voltage

current vs. time curve just equals the charge stored under the forward bias conditions. This relation holds as long as $(t_2 - t_o) << \tau$, otherwise charge will be dissipated through recombination. It can be seen from Figure 1b that two prominent states may exist during reverse recovery. The first state from t_o to t_1 is essentially a plateau of constant reverse current and impedance. This is called the delay time and it may be varied easily by changes in the ratio of forward current I_F and peak reverse current I_R, i.e.,

$$t_d \propto \frac{I_F}{I_R}.$$

The second region is that known as the transition time and denotes the interval during which the impedance of the diode is changing very rapidly. This transition time depends primarily on diode design, i.e., doping profile and geometry, and only slightly on the forward bias current. It should be emphasized that **the minimum realizable time it takes to switch between the two impedance states is the transition time part of the reverse recovery waveform.** Figure 2 illustrates that devices manufactured by different processes may have identical reverse recovery times under similar drive conditions, but considerably different transition times. It may be seen that D_2 cannot be switched much faster than t_{rr}. To switch D_1 means reducing the delay time, a simple matter of decreasing forward current or increasing peak reverse current. The HP fast switching PIN diodes are designed to yield as short a transition time as possible, yet keep their identity as a PIN. Retaining PIN identity is a significant benefit to the customer requiring a switching or modulating device capable of low harmonic distortion.

The reverse recovery time is the sum of the delay time and the transition time, and is measured from the zero current crossing of the reverse current to the time at which the reverse current is 90% down from its maximum value.

The reverse recovery time has a close analogy to how fast the device will react to a drive pulse and switch an RF signal. Consider the compensated shunt PIN 5082-3141; during the delay time a constant reverse current is flowing and the RF impedance changes only slightly. This impedance would be that set up by the previously flowing forward bias, I_F. If the forward bias put the device in saturation, i.e., its lowest impedance state, then the delay time would indicate the time during which the switch remained in its maximum isolation state. During the transition period, the diode's impedance is changing from its lowest value to some relatively high value. At the end of t_t, the switch will be in a relatively low attenuation state, i.e., insertion loss condition. Figure 1c shows the switched RF voltage when the diode is driven by the same forward and reverse current characteristic as Figure 1b. Here we will define the switching speed as to which is the time from pulse initiation (t_o) to 90% of the RF voltage appearing across the load when the switch is in the insertion loss state. If we look at t_{ss} it appears approximately equal to t_{rr}; however, as defined, the time t_{ss} does not necessarily equal the reverse recovery time (t_{rr}) but rather depends on the device reaching a specific RF impedance. The total insertion loss of the device at time t_{ss} will be its steady state insertion loss at the frequency of interest plus 0.9 dB.

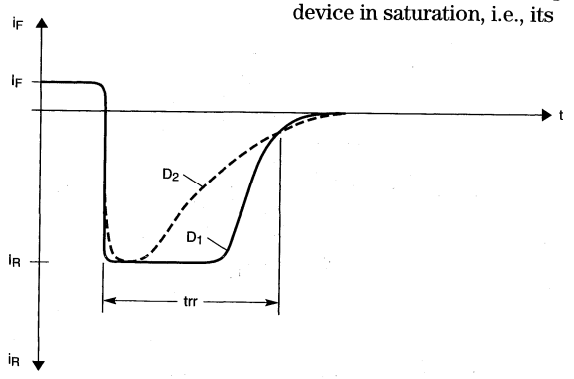


Figure 2. Reverse Recovery Time for Differently Processed Diodes

It should now be obvious that t_{rr} is in itself not descriptive of the minimum time an RF signal may be switched from maximum isolation to insertion loss or vice versa. The following section on drive requirements will consider the device under actual use conditions. The HP 5082-3141 will be used as an example for the following discussions. These devices are the fast switching PIN in the compensated stripline packages. For this reason, no matching structure is necessary to obtain maximum isolation or minimum insertion loss, and the switch configuration is that of a shunt-mounted diode.

Basic Drive Requirements

The HP Stripline series is designed to switch over very high

isolation to insertion loss ratios with an absolute minimum of required drive power. The following are considerations to be taken before settling on the drive network.

Isolation Required

To obtain the maximum isolation, the forward bias current should completely saturate the intrinsic region with charge producing the lowest possible impedance level. The region approaching saturation is extremely nonlinear in that large increases in forward current produce very small decreases in the residual impedance (see Figure 3) while still injecting considerable charge. To remove this charge requires considerable reverse bias current or a long delay time. For minimum switching times, the device should be biased only to the extent needed to obtain the required isolation. For example, at 2 GHz, an increase of forward bias from 10 mA to 20 mA produces an isolation increase of only 2 dB, yet means a switching time increase from 3 to 4 ns for a reverse pulse of 10 volts.

Switching Time Required

Figure 4 indicates typically what is required in forward bias and peak reverse voltage to initiate a particular switching speed, t_{ss}.

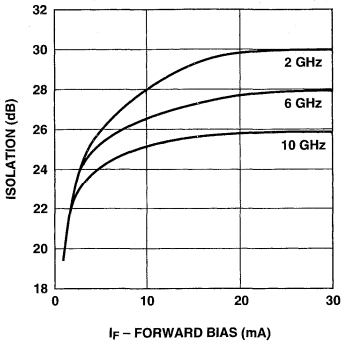


Figure 3. Typical Isolation vs. Forward Bias

The switching speeds illustrated are for a shunt diode switching from isolation to insertion loss, i.e., from storage to depletion of intrinsic layer charge. In the opposite case, switching to forward bias, the isolation follows the risetime of the driving pulse after an initial 2 nanosecond delay. It can be seen that driving of the diode from a forward biased state to reverse bias is the important consideration in determining the switching speed.

When driving the HP fast switching diode, the following parameters should be considered in the design of a driver to optimize the switching time:

- Reverse pulse voltage available
- Forward bias current available
- Driver impedance
- Pulse risetime
- Frequency of switched RF
- Allowable drive pulse leakage to the RF line

These parameters and their role in driver design will be discussed in the following section on switch configurations.

Switching Considerations

One of the most widely used and easiest switch configurations to drive is that utilizing the diode in shunt with the RF line. We will consider here the basic considerations necessary to optimize the use of the HP fast switching stripline packaged PIN. This fast switching PIN is also available in other package styles with basically similar drive requirements.

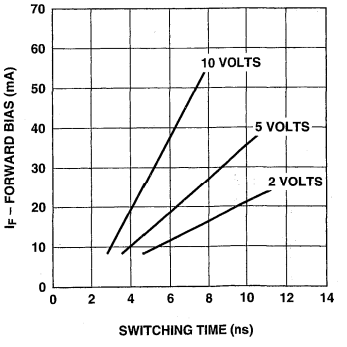


Figure 4. Switching Time vs. Forward Bias for Peak Reverse Voltage as a Parameter

Driving the Diode from Forward to Reverse Bias

As a shunt element in a 50-ohm RF system, the diode's impedance state appears as the effective load to the drive source. If the diode is initially forward biased and a reverse bias pulse is used to turn it off, then the peak reverse current flowing through the diode will simply be the open circuit pulse voltage divided by the drive impedance. By consulting Figure 3, the desired isolation may be transposed to the necessary forward bias current. From Figure 4, the forward bias current may be used to determine either the switching time when the peak reverse voltage is known or the peak reverse voltage necessary when a desired switching time is required. With the reverse voltage decided upon, the proper combination of driver impedance, voltage, and risetime may be set to yield the desired speed. For optimized switching, the reverse drive pulse risetime should be less than one-half the transition time, which for these devices is approximately 2 nanoseconds. Very short drive pulse risetimes should not be used if minimum filtering and low pulse leakage to the RF line is desired. Higher than necessary reverse pulse magnitudes will also increase the drive pulse leakage and result in the need for additional filtering.

Driving the Diode from Reverse to Forward Bias

When driving the diode into forward conduction, the desired isolation will set the forward bias current, and the risetime of the

switch will simply follow that of the driver after a 2 nanosecond delay. Here again, the allowable pulse leakage and degree of filtering will set a limit on the minimum risetime.

Practical Switching Circuits

Figures 5a, b, and c illustrate just a few of the realizable switching networks using a shunt-mounted PIN. Figures 5a and b are possibly the most commonly used and are relatively easy to produce in any transmission line system. The low pass filter cutoff frequency is determined by the minimum drive pulse risetime and should offer high isolation of the RF line from the driver. For a one-nanosecond drive pulse risetime, this cutoff frequency is approximately 400 MHz. The RF line filters may be either high pass for broadband switching or band pass for narrowband. In Figure 5b, the feedthrough capacitor, C_1, acts as a pulse source low pass and the RF ground.

The design of high pass filters will depend upon the degree of drive pulse leakage allowable. If the difference in frequency between the low pass cutoff and the RF signal is large, then often only capacitive coupling is necessary to reduce the leakage to acceptable levels. A problem with the basic design in Figure 5a is that for broadband operation, high isolation of the RF signal from the drive line is difficult to obtain and often compromises produce ringing of the pulsed RF. A cleaner method of entering the RF line from the driver is shown in Figure 5c. Here, a tapered polyiron load is used as a low pass filter while acting as an excellent broadband termination for the RF signal. The polyiron load will have a minimum effect on the pulse risetime if its length is set for a minimum signal frequency of operation approximately two octaves higher than the required drive pulse bandwidth. For example, at a signal frequency of 2 GHz, three inches $\frac{1}{2}\lambda$ of tapered polyiron will offer a good signal termination with less than 20 percent degradation of a one-nanosecond drive pulse. At much higher frequencies, the physical load length required reduces in proportion to the decrease in wavelength, with practically no degradation to the drive pulse risetime.

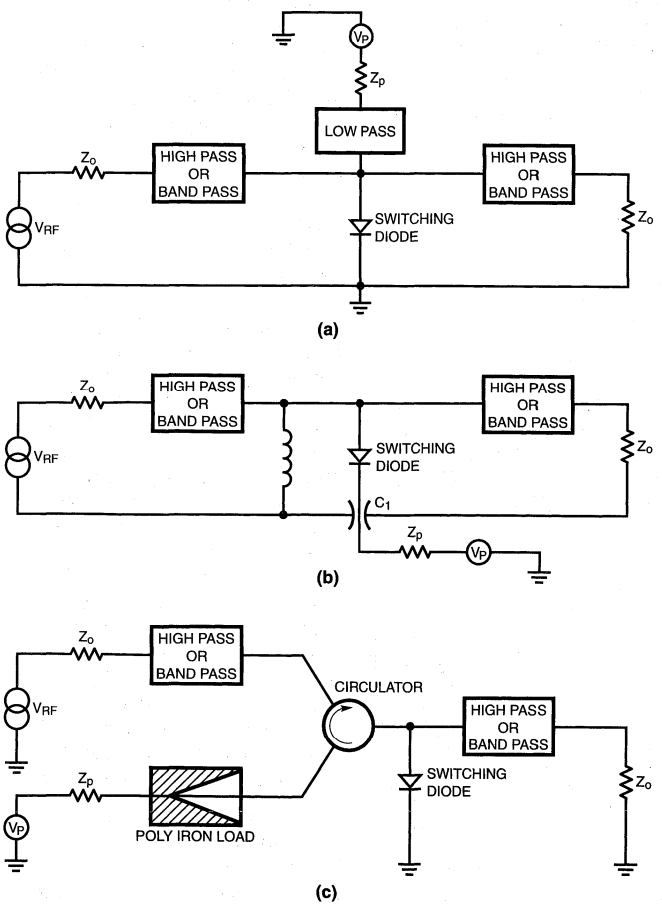


Figure 5

HEWLETT® PACKARD

A Low-Cost Surface Mount PIN Diode π Attenuator

Application Note 1048

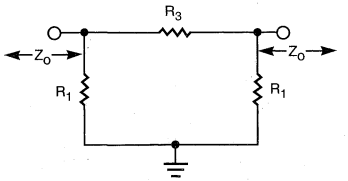
Introduction

Analog attenuators find wide application in RF and microwave networks. Realized as either GaAs MMICs or PIN diode networks, these circuits are used to set the power level of an RF signal from a voltage control. In commercial applications, such as cellular telephone, PCN (Personal Communication Networks), wireless LANs (Local Area Networks) and portable radios, cost is a significant consideration in the design of such attenuators. This paper describes a low cost wideband PIN diode π (Pi) attenuator which utilizes plastic packaged surface mounted devices.

Background

The basic π fixed attenuator is shown, along with its design equations, in Figure 1. Shunt resistors R_1 and the series resistor R_3 are set to achieve some desired value of attenuation A = 20 log(K) while simultaneously providing an input and output impedance which matches the characteristic impedance of the system.

When operated at frequencies well above its cutoff frequency f_c (see Appendix A), the PIN diode can be used as a current controlled variable resistor. Three diodes can be used to replace the fixed resistors of the π circuit to create a variable attenuator, and such circuits have been described in the literature. For example, a three diode π attenuator[1] is shown in Figure 2 which provides good performance over the frequency range of 10 MHz to over 500 MHz. However, the use of three diodes as the three variable resistors in a π attenuator leads to asymmetry in the network, which results in a rather complicated bias network.



$$R_1 = Z_o\left[\frac{K+1}{K-1}\right]$$

$$R_3 = \frac{Z_o}{2}\left[K - \frac{1}{K}\right]$$

WHERE K IS THE INPUT TO OUTPUT VOLTAGE RATIO AND Z_o IS THE IMPEDANCE OF THE SOURCE AND LOAD

Figure 1. Basic π Attenuator.

[1] "The PIN Diode," from the Hewlett-Packard RF and Microwave Applications Seminar, 1973.

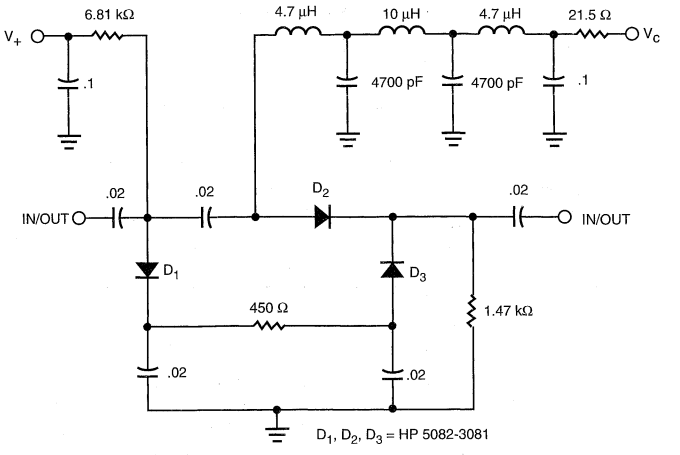


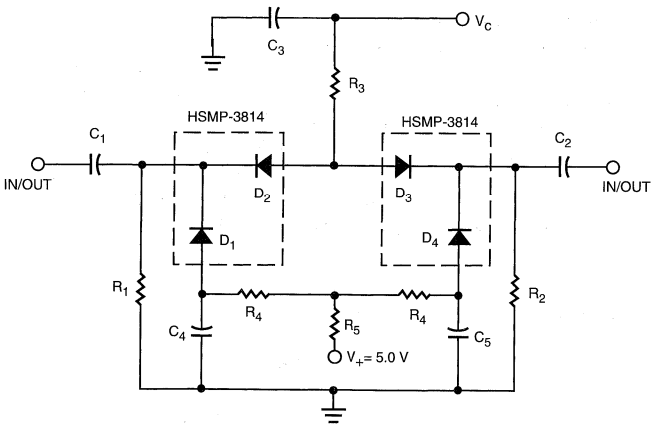
Figure 2. 3 Diode Attenuator.

Four Diode π Attenuator

If resistor R_3 is replaced by two diodes, as shown in Figure 3, several benefits result. First, since the maximum isolation of the network is set by the capacitive reactance of the series diode(s), the use of two diodes in place of one will increase the maximum attenuation or double the upper frequency limit for a given value of attenuation. Second, the twin diodes which occupy the position of the series resistor are physically set up 180° out of phase, resulting in the cancellation of even order distortion products[2]. Third, the resulting attenuator network is symmetrical and the bias network is substantially simplified. V_+ is a fixed voltage, and V_C is the variable voltage which controls the attenuation of the network. The only drawback to using two series diodes in place of one is the slight increase in insertion loss, amounting to less than 0.5 dB additional loss. R_1 and R_2 serve as bias returns for series diodes D_2 and D_3; they must be set high enough to minimize insertion loss; however, if they are set too high, an excessively large control voltage V_C will result. If the designer does not require very large bandwidth, some savings in insertion loss can be achieved by adding chokes between R_1 and R_2 and the RF line, using these inductors to decouple the resistors from the RF portion of the network. R_3 and R_4 are chosen to match the characteristics of the specific PIN diodes used; properly selected, they will provide for the correct split of bias current between series and shunt diodes required to maintain good impedance match over the entire dynamic range of attenuation. While analysis can be used to determine the values of R_1 through R_4, it is much quicker and easier to select them empirically.

The HP HSMP-3810 series of surface mount PIN diodes features good distortion performance, low cutoff frequency and low price. To save cost and space on the board, two HSMP-3814 common-cathode pairs were chosen over four individual HSMP-3810 diodes. Having chosen these diodes, and selecting $V_+ = 5V$ and $0 \le V_C \le 15V$, the values of R_1 through R_4 were empirically determined. Values for all components used in the tested circuit are shown in Figure 3.

The attenuator was laid out on a 2 inch square of 0.032" thick HT-2 PC board, as shown in Figure 5. This material, a high performance alternative to conventional FR4, is described in detail in Appendix B. Using chip resistors and capacitors, the entire attenuator occupies a 0.5 in^2 space as shown in Figure 5.



COMPONENT	VALUE	MFG./PART NUMBER
R_1,R_2	560 Ω	KYOCERA CR21-561JB1
R_3	330 Ω	KYOCERA CR21-331JB1
R_4	1640 Ω	KYOCERA CR21-162JB1
R_5	680 Ω	KYOCERA CR21-6B1JB1
C_1-C_5	47000 pF	KYOCERA 0805Z473M2P03
D_1-D_4	-	HEWLETT-PACKARD HSMP-3814

Figure 3. Wideband 4 Diode π Attenuator.

Test Results

In Figure 6, the measured attenuation vs. frequency is given for several values of control voltage. Good performance is obtained over the frequency range of 300 KHz to 3 GHz. Figure 7 contains the plot of return loss vs. frequency at the maximum and minimum values of V_C. For all other values, the return

[2]Raymond Waugh, "A Low Distortion PIN Diode Switch Using Surface Mount Devices," Proceedings of RF EXPO WEST, pp 455 - 461, Feb. 5 - 7, 1991.

loss was higher; the data for $V_C = 0$ represents the worst case. In Figure 8, a plot is given for attenuation vs. control voltage at a number of frequencies. Finally, the intermodulation distortion performance of the attenuator is plotted in Figure 9. The data are given as intercept points; for a detailed explanation of intercept points, see Appendix C.

Conclusion

As can be seen from these data, the four diode π attenuator provides very good match and very flat attenuation over an extremely wide band. Using surface mount devices, it has the additional benefit of being low cost. Realized as a thin-film or thick-film hybrid circuit with chip PIN diodes, it would fit within a TO-8 can.

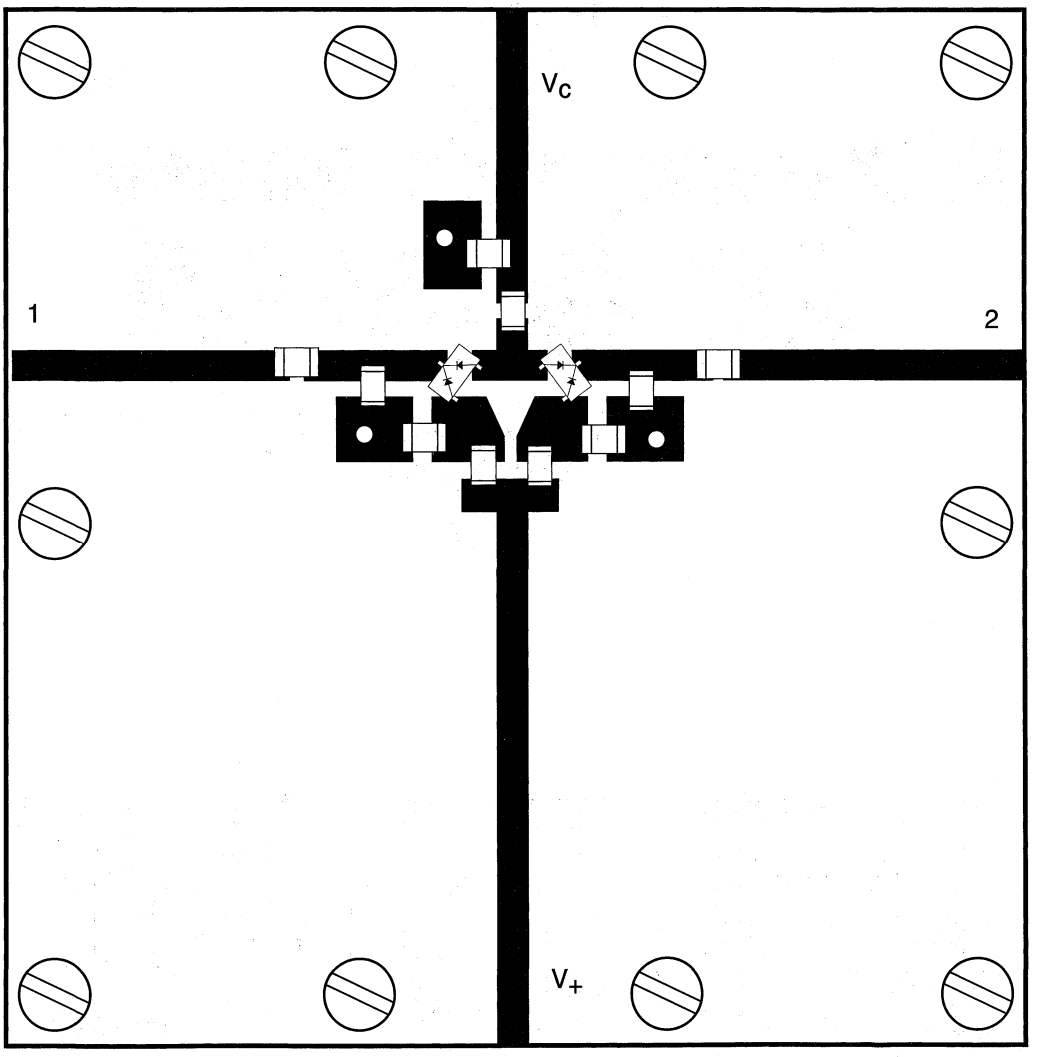


Figure 4. Circuit Board Layout.

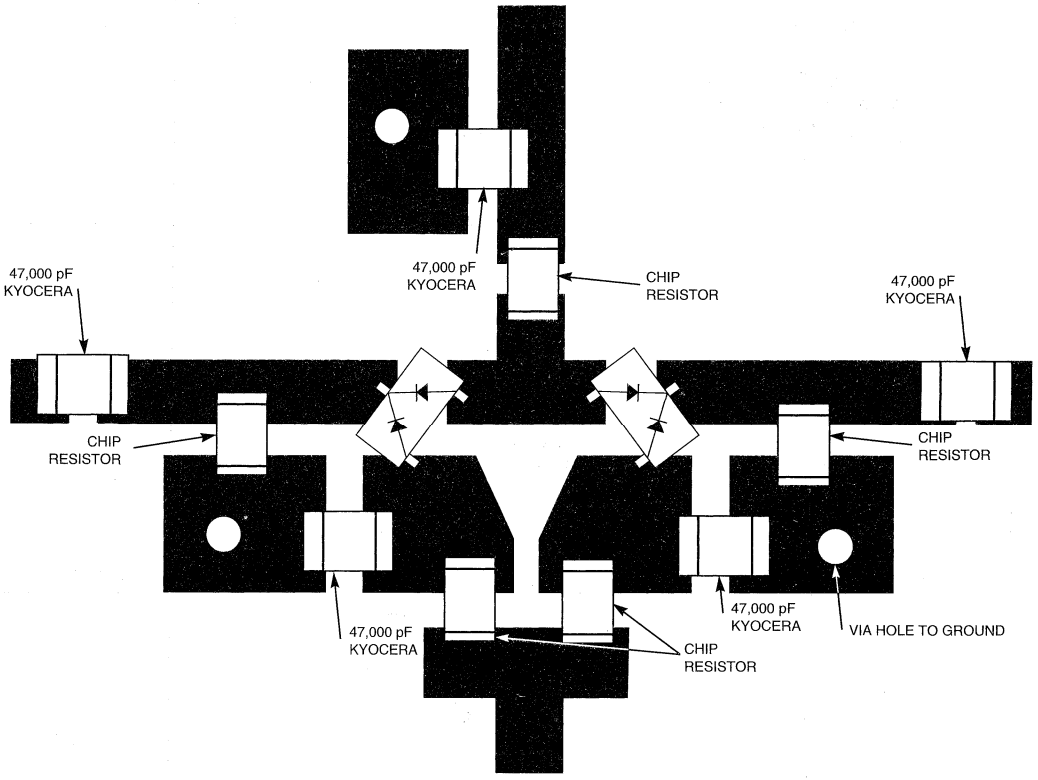


Figure 5. Detail of Circuit Layout.

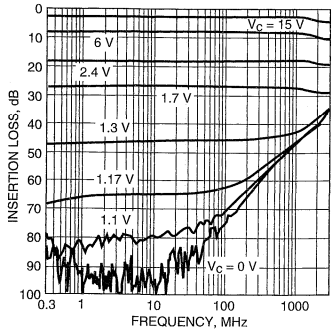


Figure 6. Attenuation vs. Frequency.

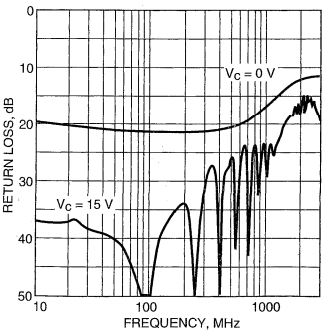


Figure 7. Return Loss vs. Frequency.

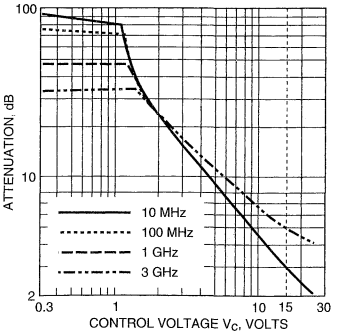


Figure 8. Attenuation vs. Control Voltage.

Appendix A - PIN Diode Cutoff Frequency

The PIN diode is generally considered to be a current controlled RF resistor. However, this model is accurate only at frequencies well above the diode's cutoff frequency, $f_C = 1 / 2\pi\tau$, where τ is the minority carrier lifetime of the device. At frequencies 10 times f_C, a PIN diode can accurately be modelled as a current controlled resistance in parallel with a small (and constant) junction capacitance (neglecting package parasitics). At frequencies under 0.1 f_C, the PIN diode behaves as an ordinary PN junction diode. For 0.1 $f_C \leq$ frequencies $\leq 10\ f_C$, the characteristics of the PIN diode become very complex; it will generally behave as a frequency-dependent resistance shunted by a very large frequency and current dependent inductance or capacitance. Additionally, distortion performance will usually be very poor when operating in this frequency range. For the HSMP-3810 series of diodes, $\tau \cong 1500$ nsec, resulting in a cutoff frequency of 100 kHz. This diode should therefore provide frequency-independent values of pure resistance at frequencies above 1 MHz. However, because this diode has been optimized for wideband attenuator applications, its characteristics remain generally well behaved down to frequencies below f_C, as can be seen from the 300 kHz measured data shown in Figure 6.

Appendix B - Board Material

Several printed circuit board materials are in common use for RF circuits such as this one. Two of the most popular are FR4 and fiberglass reinforced PTFE (Teflon®). The former provides good mechanical stability and durability at low cost. However, it suffers from high losses and a dielectric constant which is poorly controlled and strongly frequency-dependent. The latter exhibits very good RF properties, but is expensive, suffers from poor mechanical stability, and cannot survive certain SMT (Surface Mount Technology) processing steps. Hewlett-Packard's new HT-2 board material provides durability and high temperature performance which are actually superior to FR4 with a controlled dielectric constant ($\varepsilon r \cong 4.3$) and a loss tangent which is half that of FR4. These properties make it ideal for microstrip circuits operating beyond 6 GHz.

At the time of this printing, HT-2 is available through Dan Schutte of International Circuits, 1319 South Arkle Street, Visalia, CA.

Appendix C - The Intercept Point

Of the several types of distortion products, one of the most troublesome is intermodulation distortion. Unlike harmonic distortion, this is a multi-tone product resulting when two or more signals of equal (or unequal) amplitude mix in a non-linear device such as a PIN diode. The frequency of the resulting unwanted signal is related to those of the original input voltages. In certain industries, the number of input signals may exceed 10, and both test and analysis become very complex. To keep matters as simple as possible, many semiconductor manufacturers make two-tone measurements using two voltages which are equal in amplitude and closely spaced in frequency. Given two such input signals at frequencies f_1 and f_2, one can compute several significant intermodulation distortion products from the equation

$$Kf_1 \pm Mf_2$$

where K, M = 1, 2, 3, ...

The order of the distortion product is given by the sum
N = K + M.

Of the infinite number of distortion products described by this equation, one is of special significance. The third order products given in Figure 1 are important because they exist on either side of the original signals f_1 and f_2 and cannot be removed by filtering.

The behavior of all types of distortion products is shown on Figure 10. As can be seen, an increase of 1 dBm in the applied signal's power will result in a 2 dBm increase in the second order products and a 3 dBm increase in the third order products. Since the level of measured distortion is dependent upon the level of the input signal, it is convenient to specify distortion in

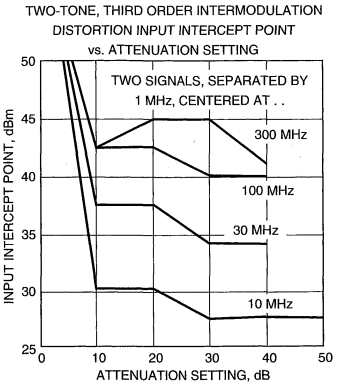


Figure 9. Measured Distortion Performance.

terms of a fictitious constant, the intercept point. This is the point at which the extrapolated fundamental signal and the extrapolated distortion product meet. In making distortion measurements, it is most convenient to measure the input power of the signal(s) applied to the DUT (Device Under Test) and the output power of the distortion products. For this reason, and because the input intercept point varies less with attenuation, the input intercept point is the one most often calculated and specified. Using it, we can neatly specify the performance for a given type of distortion using a single number.

The equation for input intercept point is

$$IP_{in} = \frac{N(P_{in} - \alpha) - P_{dist}}{N - 1} + \alpha \text{, in dBm}$$

where N = order of distortion product, and all power levels are specified in dBm.

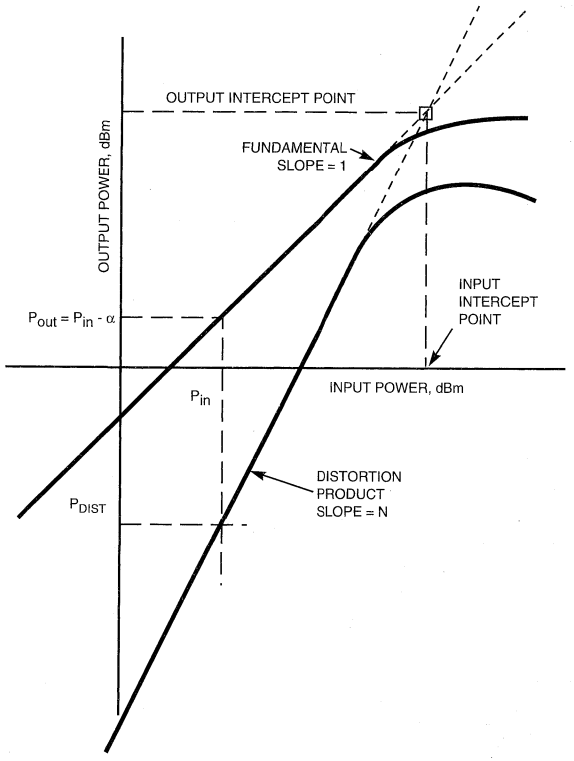


Figure 10. Behavior of Distortion Products.

HEWLETT® PACKARD

A Low Distortion PIN Diode Switch Using Surface Mount Devices

Application Note 1049

Abstract

One of the practical applications of the surface mounted PIN diode is in the design of low current, low cost RF switches. In the design of such circuits, the diode is generally treated as a current controlled ideal resistor which is switched between low resistance and high resistance states.

However, the PIN diode has some important second order non-linear characteristics which can give rise to the generation of harmonic and intermodulation distortion in switching circuits, particularly those which employ high RF power. A low distortion SPDT switch, using a new type of PIN diode designed specifically for low distortion performance, is described.

Introduction

All circuits which contain non-linear elements such as diodes and transistors produce certain kinds of distortion to various degrees. The three types of distortion which are most often of concern are as follows:

Harmonic Distortion:
This is a single-tone distortion product, resulting when a voltage at a single frequency f, applied to a non-linear device, creates spurious voltages at frequencies 2f, 3f, ..., Nf. Of most concern, because they are the closest to the desired signal, are the second and third harmonics. The order of the distortion product is given by the frequency multiplier; for example, the second harmonic is a second order product.

Intermodulation Distortion:
This is a multi-tone distortion product. It results when two or more signals, of equal or unequal amplitude, mix in a non-linear device to produce unwanted signals whose frequencies are related to those of the original input voltages. In certain industries, the number of input signals may exceed 10, and analysis becomes very complex. To keep matters as simple as possible, many semiconductor manufacturers make two-tone measurements using two voltages which are equal in amplitude and closely spaced in frequency. Given two such input signals at frequencies f_1 and f_2, one can compute several significant intermodulation distortion products from the equation

$$Mf_1 \pm Nf_2$$

where M, N = 1, 2, 3, ...

The order of the distortion product is given by the sum M + N.

Of the infinite number of distortion products described by this equation, one is of special significance. The third order products given in Table 1 are important because they exist on either side of the original signals f_1 and f_2 and cannot be removed by filtering.

HARMONIC DISTORTION:
GIVEN AN INPUT AT FREQUENCY f
SECOND HARMONIC AT 2f
THIRD HARMONIC AT 3f
INTERMODULATION DISTORTION:
GIVEN TWO EQUAL AMPLITUDE INPUTS AT FREQUENCIES f_1 AND f_2
THIRD ORDER AT $2f_1 - f_2$
THIRD ORDER AT $2f_2 - f_1$

Table 1. Important Distortion Products.

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Cross Modulation Distortion: This is another form of multi-tone distortion. The non-linear device causes modulation on one signal of frequency f_1 to be transferred to a second signal or carrier of frequency f_2. Cross modulation distortion will not be treated in this paper. However, it is worth noting that Lepoff[1] has shown that the intercept point for this distortion product is generally 2.5 dB below that for third order harmonics.

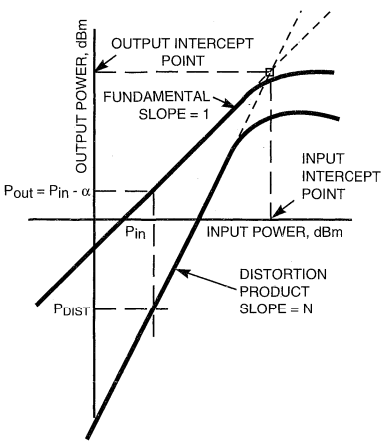
The behavior of all three types of distortion products is shown in Figure 1. As can be seen, an increase of 1 dBm in the applied signal's power will result in a 2 dBm increase in the second order products and a 3 dBm increase in the third order products. Since the level of measured distortion is dependent upon the level of the input signal, it is convenient to specify distortion in terms of a fictitious constant, the intercept point. In making distortion measurements, it is most convenient to measure the input power of the signal(s) applied to the DUT (Device Under Test) and the output power of the distortion products. For this reason, and because the input intercept point varies less with attenuation, the input intercept point is the one most often calculated and specified. However, in the case of the PIN diode switch, insertion loss (α) is typically less than 1 dB, so the input and output intercept points are essentially equal. For the balance of this paper, reference will therefore simply be made to the intercept point, and the simplified equations shown in the box in Figure 1 will be used.

The primary source of distortion in PIN diode switches is conductivity modulation of the charge within the I layer of the diode under forward bias and capacitance modulation of the diode under reverse bias. Distortion can be controlled by the proper choice of diode characteristics and by the design of the switch circuit itself.

PIN Diode Considerations

In their seminal treatment of distortion in PIN diodes, Caverly and Hiller[2,3,4] discuss the origins of distortion and the effects of various device parameters upon distortion performance. In summary, their work shows that:

- For a given forward biased diode and frequency, series PIN diodes produce more distortion than shunt diode switches and attenuators.
- For a given forward biased diode and circuit topology, distortion improves (decreases) as the frequency of the im-pressed signal(s) increases.
- In reverse biased PIN diodes, distortion gets worse with increase in frequency and improves with increase in diode I layer thickness.



α = ATTENUATION
IP_{in} = INPUT INTERCEPT POINT, dBm
IP_{out} = OUTPUT INTERCEPT POINT, dBm

DISTORTION PRODUCT	SLOPE = N
2nd HARMONIC	2
3rd HARMONIC	3
2nd ORDER IM	2
3rd ORDER IM	3

GENERAL EQUATIONS FOR INTERCEPT POINT

$$IP_{out} = \frac{NP_{out} - P_{dist}}{N - 1}$$

$$IP_{in} = \frac{N(P_{in} - \alpha) - P_{dist}}{N - 1} + \alpha$$

FOR THE CASE OF $\alpha \leq 1$ dB,

2nd ORDER $IP_{in} = 2P_{in} - P_{dist}$

3rd ORDER $IP_{in} = \frac{3P_{in} - P_{dist}}{2}$

Figure 1. Behavior of Distortion Products.

[1]Jack Lepoff, "A New PIN Diode For UHF-VHF Applications," Proceedings of the National Electronics Conference, Vol. XXVI, pp 434 - 439, Dec. 7 - 9, 1970.

[2]Robert Caverly and Gerald Hiller, "Distortion in PIN Diode Control Circuits," IEEE Trans. MTT, vol. MTT-35, No. 5, pp 492 - 500, May 1987.

[3]Robert Caverly, "A Nonlinear PIN Diode Model For Use in Multi-Diode Microwave and RF Communication Circuit Simulation," Proceedings of the International Symposium on Circuits and Systems, pp 2295 - 2299, August 1988.

[4]Robert Caverly and Gerald Hiller, "Distortion in Microwave and RF Switches by Reverse Biased PIN Diodes," IEEE MTT-S Digest, pp 1073 - 1076, May 1989.

- In forward biased PIN diode switches, the intercept point for distortion is proportional to the square of the diode's carrier lifetime divided by I layer thickness.
- The second order intermodulation distortion products will be 6 dB higher than that of the second harmonic.
- The third order intermodulation distortion products will be 9.5 dB higher than that of the third harmonic.

The equations which predict distortion intercept points are shown in Table 2.

To illustrate the use of these equations in the prediction of a given diode's distortion performance, four surface mount PIN diodes were analyzed and tested as listed in Table 3. They ranged in I layer thickness from 5.5 μ to 130 μ and nominal lifetime varied from 60 ns to 3 μs. The first two were designed for low cost, low current switching applications, the third is a general purpose diode of an older design and the fourth is a new product targeted specifically for low distortion switching applications. Since certain applications, such as battery powered portable radios, are limited in the amount of current which is available, each diode was tested at two or three current levels. The highest current for each nearly saturated the diode; at that current the I layer resistance was close to its minimum. At least one lower current was chosen such that the insertion loss of the diode, when operated as a series switch, would be well under 1 dB. It is worth noting that the lifetime of a PIN diode varies slightly over this range of currents.

The first diode, HSMP-3820, has twice the capacitance (0.6 pF) of the other three (0.3 pF); because it is not directly comparable in frequency performance, its evaluation will be saved for the next section.

The three 0.3 pF diodes were each mounted in series in a 50 Ω microstrip line, and biased with external bias tees. Insertion loss under forward bias and isolation under reverse bias was recorded. Using the equipment illustrated in Figure 2, harmonic distortion was measured at two forward currents and three frequencies for each. It is worth commenting that, at certain frequencies with some diodes, the distortion products were more than 100 dB below the input signal; good filters are essential to accurate measurements of this type. The data were converted to intercept points which are plotted in Figure 3.

The measured intercept points show good agreement with those predicted by the equations of Figure 3. Certainly, those performance indicators summarized at the beginning of this section are borne out in the data. Distortion performance improves with frequency, with diode lifetime, with I layer thickness and with forward

IM_2 = 2 - TONE 2nd ORDER INTERMODULATION DISTORTION INTERCEPT POINT

$= 34 + 20 \text{ LOG } \frac{fQ}{R_s} \text{ dB}$

IP_2 = 2nd HARMONIC INTERCEPT POINT

$= IM_2 + 6 \text{ dB}$

IM_3 = 2 - TONE 3rd ORDER INTERMODULATION DISTORTION INTERCEPT POINT

$= 24 + 15 \text{ LOG } \frac{fQ}{R_s} \text{ dB}$

$= \frac{3}{4} IP_2 - 1.5 \text{ dB}$

IP_3 = 3rd HARMONIC INTERCEPT POINT

$= IM_3 + 9.5 \text{ dB}$

WHERE

f = FREQUENCY, MHz

$= \frac{f_1 + f_2}{2}$ FOR TWO-TONE MEASUREMENTS

$Q = I\tau$

I = DIODE FORWARD CURRENT, mA

τ = DIODE LIFETIME AT A GIVEN CURRENT, μSEC

R_s = DIODE RESISTANCE AT A GIVEN CURRENT, Ω

Table 2. Equations For Intercept Points For a Single Diode, from Caverly and Hiller.

DIODE	W(μ)	I (mA)	R_S (Ω)	τ (ns)
HSMP-3820	5 1/2	5.0	0.55	60
		1.0	1.3	65
		0.2	5.0	75
HSMP-3890	6 1/2	10.0	1.5	170
		0.5	5.3	200
HSMP-3830	22 1/2	40.0	1.1	250
		4.0	4.4	300
HSMP-3880	130	40.0	1.2	3000
		7.5	3.5	3600

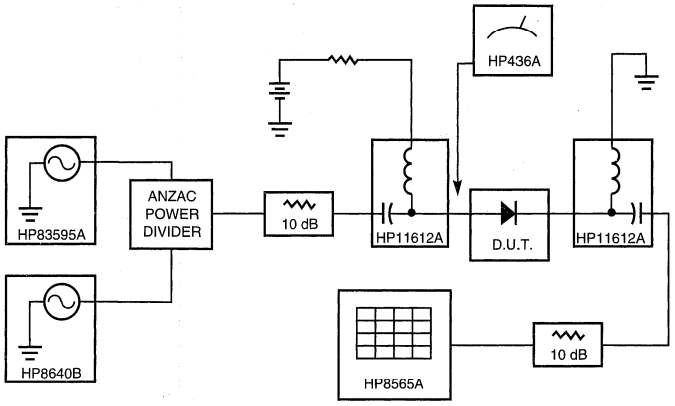
WHERE τ = LIFETIME, W = I-LAYER THICKNESS

Table 3. PIN Diode Evaluation.

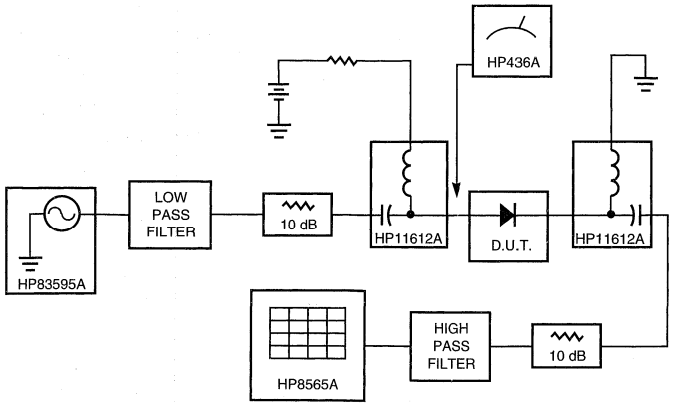
current. For example, the lifetimes of the tested samples of HSMP-3830 and HSMP-3890 were nearly the same. However, the I layer thickness of the former is more than 3 times that of the latter, resulting in substantially improved distortion performance. When the HSMP-3880 is used with 40 mA of bias at frequencies above 100 MHz, the second harmonic intercept point is above 1 GW (10^9 W), indicating very low distortion produced at normal operating power levels. In the section which follows, it will be seen that this intercept point can be easily increased by another 15 dBm.

In order to obtain the second harmonic data described above, distortion levels as low as -130 dBc had to be measured. The equations of Table 2 predict third harmonic and two-tone third order distortion products as low as -180 to -200 dBc at 300 MHz, levels beyond the capability of the equipment used. For this reason, third order products were measured only at 123 MHz, and are shown in Table 4. Even at this lower frequency, these products were difficult to measure at saturation currents. Nevertheless, good agreement is seen between predicted intercepts and those which could be measured.

When using the equations of Table 2 to predict the distortion performance of a forward biased diode, one must know its resistance and lifetime at the current one plans to use. Resistance information is generally found in PIN diode data sheets, and it can easily be verified by measuring the insertion loss of a forward biased series diode and computing the value of Rs which corresponds to that loss. The measurement of lifetime is somewhat more complicated, and lifetime varies from lot to lot of a given diode. However, typical lifetime data are available

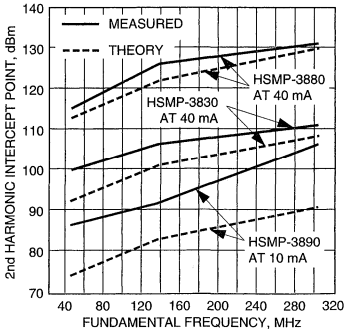


a) EQUIPMENT USED TO MEASURE INTERMODULATION DISTORTION



b) EQUIPMENT USED TO MEASURE HARMONIC DISTORTION

Figure 2. Measuring Equipment.



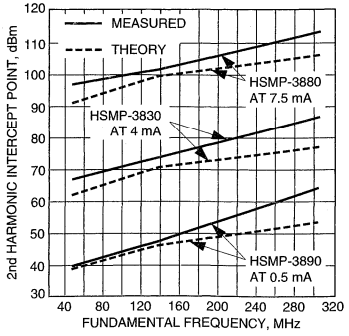


Figure 3. Distortion in Forward Biased PIN Diodes

from diode manufacturers, and quite good accuracy can be obtained if one uses 120% of that value at the reduced current which results in an R_S of 4 Ω.

In a SPDT switch designed as described in the section below, the diodes in the "ON" arm are forward biased, with distortion performance as described above. However, the diodes in the "OFF" arm are reverse biased. A thorough discussion of the distortion characteristics of reverse biased diodes is beyond the scope of this note. However, at these frequencies and with the diodes evaluated, distortion products under reverse bias were less significant than those produced in forward bias.

Circuit Considerations

In the practical application of SOT-23 packaged PIN diodes, the very large inductance of that package (≈2 nH) makes it difficult to obtain good levels of isolation from a shunt diode at frequencies much above 150 MHz. This inductance is much less troublesome in the case of the series diode switch, where diode and package capacitance are important in the maintenance of good isolation. For this reason, this paper will focus on the application of surface mounted PIN diodes as series switching elements.

In the previous section, PIN diode characteristics were treated without regard to circuit considerations. However, a review of Figure 4 will show how certain distortion products can be reduced by means of a circuit "trick."

Figure 4 provides a simplified equivalent circuit for a single series PIN diode as well as two different arrangements of two series diodes. The single diode can be represented by a resistor R_S in series with a voltage generator v(t). This voltage, resulting from the excitation of the diode by input current i(t), consists of an infinite series containing all of the unwanted distortion products. When two identical diodes, with the same value of R_S, are placed in series in the same orientation, the two coherent voltage generators combine their outputs in-phase, resulting in a lowering of the distortion intercept points (an increase in distortion). For N identical diodes in series, Caverly[3] gives the equations for second and third order intermodulation distortion intercept points as:

IP_2 = Second order IMD intercept point, dBm

$$= K_1 \frac{N^2 A}{(1 - \sqrt{A})^4}$$

IP_3 = Third order IMD intercept point, dBm

$$= K_2 \frac{N^2 A}{(1 - \sqrt{A})^3}$$

where N = number of identical diodes in series, and

$$A = \frac{2Z_O}{2Z_O + NR_S}, \text{ and}$$

K_1, K_2 = factors independent of the number of diodes.

For values of R_S less than 4 Ω, these equations predict that two in-phase series diodes will have a second order IMD intercept point ≈6 dB lower, and a third order IMD intercept point ≈3 dB lower, than that for a single diode of the same type and biased with the same current.

DIODE TYPE: HSMP-3890

IF mA	RES. OHMS	τ nsec	CALC 2nd	MSRD 2nd	CALC 3rd	MSRD 3rd	CALC IM3	MSRD IM3
10	1.00	170	83	86	66	>60	56	–
1	3.70	190	54	63	44	45	35	38
0.5	5.30	200	47	48	39	33	29	34

DIODE TYPE: HSMP-3830

IF mA	RES. OHMS	τ nsec	CALC 2nd	MSRD 2nd	CALC 3rd	MSRD 3rd	CALC IM3	MSRD IM3
40	1.10	250	101	107	79	>58	70	–
4	4.40	300	71	74	56	51	47	–

DIODE TYPE: HSMP-3880

IF mA	RES. OHMS	τ nsec	CALC 2nd	MSRD 2nd	CALC 3rd	MSRD 3rd	CALC IM3	MSRD IM3
40	1.20	3000	122	126	95	>65	85	–
7.5	3.50	3600	100	102	78	>65	69	–

2nd = SECOND HARMONIC DISTORTION
3rd = THIRD HARMONIC DISTORTION
IM3 = TWO-TONE THIRD ORDER INTERMODULATION DISTORTION

Table 4. One and Two Tone Distortion Intercept Points, Measured At 123 MHz.

However, when two PIN diodes are placed anti-series, the equivalent circuit (shown at the bottom of Figure 4) predicts that even order (2nd, 4th, etc.) distortion products will cancel out to the extent that the two diodes are matched in their characteristics.

To experimentally verify the theory outlined above, three circuits were built using the HSMP-3820 PIN diode. This device was chosen because its thin I layer and short lifetime result in relative high (and easily measured) levels of distortion. The first circuit consisted of a single series diode, as shown schematically at the top of Figure 4. The second consisted of two diodes in series, in-phase. The third consisted of two diodes in anti-series configuration, with a wideband choke (Coilcraft 1008CS-561 560 nH surface mount inductor) providing bias to the center. All three circuits used wideband external bias tees at input and output. Measured data are compared to predicted for second harmonics, third harmonics and two-tone third order intermodulation distortion at three different currents. In general, there is good correspondence between forecast and observed intercepts, except for second harmonics in the anti-series pair. In this specific case, illustrated by the plot at the bottom of Figure 5, the improvement over the in-phase pair is typically 20 dBm, with a 15 dBm increase in intercept point when compared to the single diode.

Thus, it can be seen that the use of an anti-series pair of PIN diodes as a switching element can lead to very low levels of even-order distortion products, even when a high distortion diode is chosen for the task.

In the case of all four types of diodes, it was found that the theory of Caverly and Hiller for forward biased series diode switches was reasonably accurate in the prediction of intercept points.

SPDT Switch

The concept of anti-series PIN diodes as a switching element was incorporated into a wideband SPDT switch, as shown schematically in Figure 6. All components are of the surface mount type. Hewlett-Packard HSMP-3880 PIN diodes were chosen because of their extremely low distortion. Each PIN diode has a capacitance (at negative bias) of less than 0.3 pF, resulting in a total capacitance in each arm under 0.15 pF. This sets the upper limit on the useful frequency range of the switch at something well over 1 GHz. 560 nH Coilcraft chokes were chosen because their self resonance frequency is well over 1 GHz, yet they have sufficient inductance to permit the switch to be used at frequencies as low as 50 MHz. The large capacitance of the Kyocera capacitors provides good bypassing over this entire frequency range.

The switch was realized on 0.032" thick FR-4 microstrip as shown in

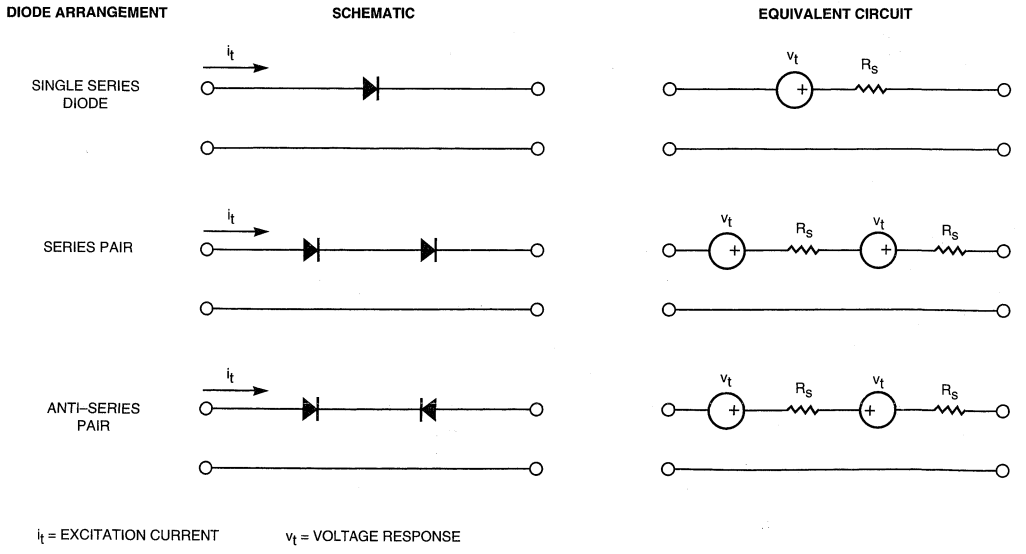


Figure 4.

ONE AND TWO TONE DISTORTION INTERCEPT POINTS, MEASURED AT 123 MHz

SINGLE HSMP-3820 DIODE

IF mA	RES. OHMS	TAU nsec	CALC 2nd	MSRD 2nd	CALC 3rd	MSRD 3rd	CALC IM3	MSRD IM3
5	0.55	60	77	87	61	61	51	–
1	1.30	65	56	59	45	41	36	34
0.2	5.00	75	31	23	27	22	18	23

SERIES PAIR, HSMP-3820 DIODE

IF mA	RES. OHMS	TAU nsec	CALC 2nd	MSRD 2nd	CALC 3rd	MSRD 3rd	CALC IM3	MSRD IM3
5	0.55	60	71	81	58	60	48	–
1	1.30	65	50	55	42	40	33	34
0.2	5.00	75	25	24	24	22	15	24

ANTI-SERIES PAIR, HSMP-3820 DIODE

IF mA	RES. OHMS	TAU nsec	CALC 2nd	MSRD 2nd	CALC 3rd	MSRD 3rd	CALC IM3	MSRD IM3
10	0.55	60	–	103	58	60	48	–
2	1.30	65	–	77	42	41	33	32
0.4	5.00	75	–	41	24	19	15	24

2nd = SECOND HARMONIC DISTORTION
3rd = THIRD HARMONIC DISTORTION
IM3 = TWO-TONE THIRD ORDER INTERMODULATION DISTORTION

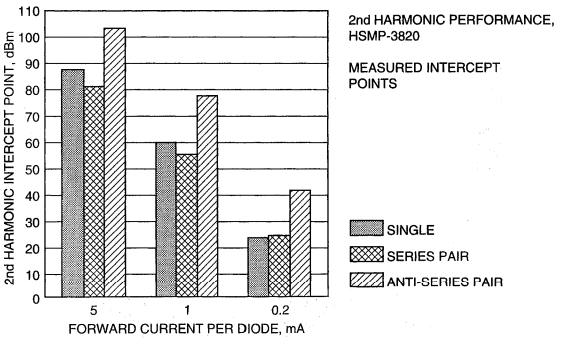
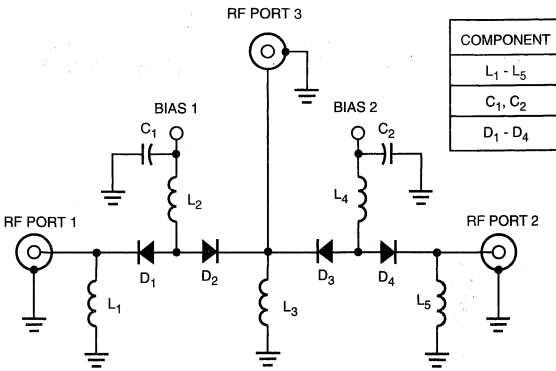


Figure 5.



COMPONENT	VALUE	MFG/PART NUMBER
L_1 - L_5	560 nH	COILCRAFT 1008CS-561
C_1, C_2	47,000 pF	KYOCERA 0805Z473M2P03
D_1 - D_4	–	HEWLETT-PACKARD HSMP-3880

Figure 6.

Figure 7. Note that, in order to provide reasonable distance between components for ease of assembly, the diodes are spaced about 0.27" apart. This separation, amounting to 15° at 1000 MHz, provides an additional 7 dB of isolation at that frequency. Three via holes provide ground on the upper surface of the board.

Swept frequency measurements of the switch are shown in Figures 8 and 9. Insertion loss in the "ON" arm is under 1 dB from 50 to 1000 MHz with 80 mA of bias applied to the two diodes. Using 15 mA of bias results in an increase in insertion loss to 1.3 dB. Return loss over the band was 10 dB minimum, with a typical value of 20 dB or more. Over this same frequency range, "OFF" arm isolation was 32 dB minimum, 40 dB typical. It is worth noting that these diodes are fully depleted at zero Volts reverse bias; the use of negative bias on the "OFF" arm diodes did not increase isolation. The "hole" in the isolation at 160 MHz is the result of the "OFF"

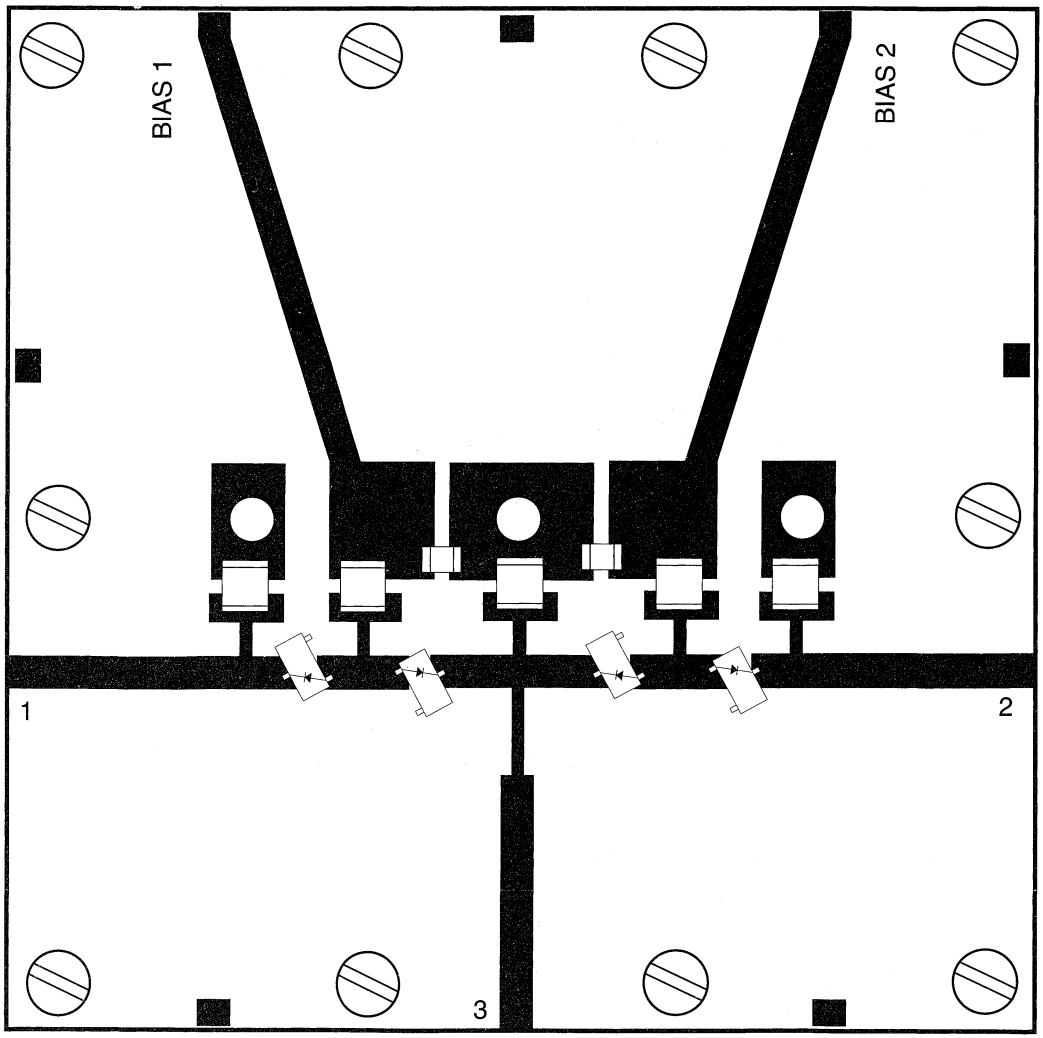


Figure 7.

arm becoming a filter structure consisting of shunt 560 nH inductors and series 0.3 pF capacitors.

Measurements were made of the second harmonic performance of the switch. A +18 dBm signal at 123 MHz was applied at the common junction (port 3) and observations were made of second harmonic power at both the isolated ("OFF") and connected ("ON") outputs. Measurements were made using both 15 and 80 mA bias on the "ON" diodes and from zero to -20V on the "OFF" diodes. Results of the worst case (15 mA forward bias) are shown in Figure 10. From this plot, it can be seen that second harmonic distortion is worst at the "ON" arm, and is improved by the addition of negative bias to the "OFF" diodes. This would indicate that some of the distortion measured in the "ON" arm is being produced in the diodes of the "OFF" arm.

Converting these data, and data taken at 80 mA forward bias, to intercept points results in the plot shown in Figure 11. Here it is seen that the use of anti-series low distortion diodes with a large amount (40 mA each) of forward bias can result in second harmonic intercept points as high as 117 dBm (500 MW).

Conclusion

A simple structure, an anti-series pair of PIN diodes, has been shown to substantially reduce even order harmonic distortion products. A wideband (50 - 1000 MHz) low distortion SPDT switch, using inexpensive surface mount devices, has been described. Finally, it has been shown that the theory of Caverly and Hiller can be used to predict distortion performance in forward biased PIN diodes with reasonable accuracy.

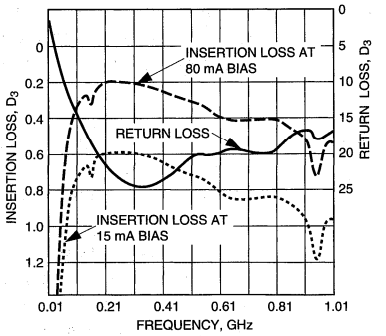


Figure 8. Insertion Loss and Return Loss vs. Frequency

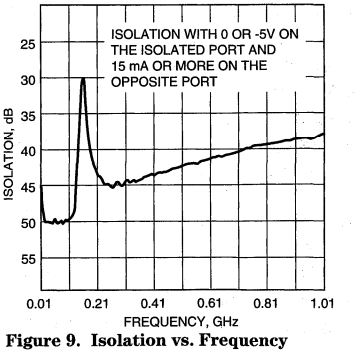


Figure 9. Isolation vs. Frequency

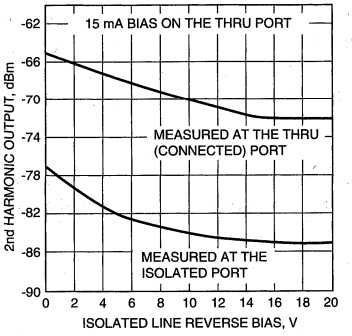


Figure 10. 2nd Harmonics at 123 MHz Input

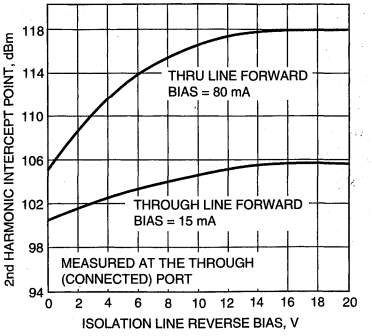


Figure 11. Harmonic Distortion at 123 MHz Input

HEWLETT® PACKARD

An SPDT PIN Diode T/R Switch for PCN Applications

Application Note 1067

Introduction

The PCN (**P**ersonal **C**ommunications **N**etwork) market has shown dramatic growth in the past several years, and promises to expand even more rapidly before the end of the decade. Hand held terminals providing voice and data transmission in cells smaller than those used for cellular telephone are either in the design phase or undergoing trials in Europe, Japan and the U.S. Various frequency bands are being used, but most of the activity is taking place in the range of 1.7 to 2.0 GHz. This paper describes a 1750 MHz SPDT T/R (**T**ransmit/**R**eceive) antenna switch suitable for such a hand-held terminal. The design concepts contained in this paper can be applied to other frequency bands as well.

Design Requirements

An SPDT T/R antenna switch carries with it a unique set of design requirements when it is being designed for a battery operated application. In addition to the usual specifications for good match and low loss, the following requirements apply:

- Very low or zero current consumption while in the standby or receive mode.
- Moderate current consumption while in the transmit mode.
- High isolation in the receiver arm to protect the front end from damage when the transmitter is operating.
- Sufficient isolation in the transmit arm to isolate the receiver from variations in the transmitter's output impedance.
- Small size.
- Low cost.
- Surface mountable.

From a reading of these requirements, it is clear that this type of SPDT switch is not necessarily symmetrical. For example, 10 dB of isolation in the transmit arm is sufficient to prevent any variation in the output impedance of the transmitter (when in standby mode) from affecting the performance of the receiver. However, to protect the receiver (P_{in} < +10 dBm) from being damaged by a 1 Ω transmitter, more than 20 dB of isolation will be required in the receiver arm. Putting numbers to these design requirements results in the specification shown in Table 1.

This set of specifications, then, formed the design goal for the SPDT T/R switch described below.

Design Approach

In order to conserve bias current in the standby or receive mode, a switch of the type shown in Figure 1 can be used. When zero (or a small positive) voltage is applied to the bias port, both PIN diodes are in the high resistance (reverse biased) state. This isolates the transmitter (Tx) from the antenna,

Table 1. Specifications for SPDT T/R Switch

Requirement	Transmit Arm	Receive Arm
Insertion Loss, dB	<1	<1
Isolation, dB	>10	>25
Return Loss, dB	>15	>15
Bias current, mA	minimum	zero

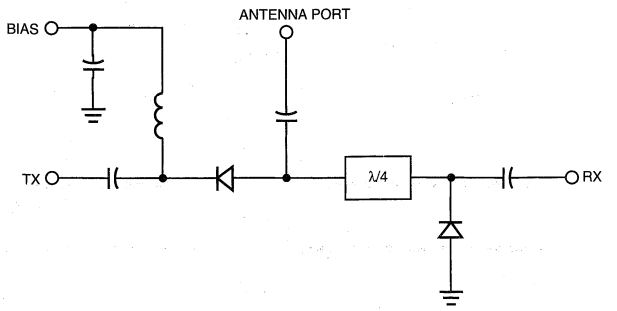


Figure 1. Low Current T/R Switch.

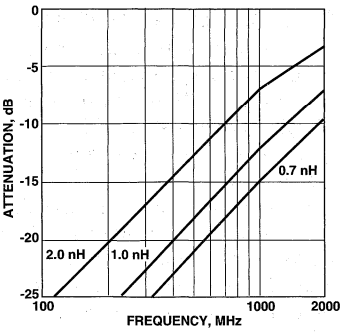


Figure 2. Attenuation vs. Frequency, Inductor Shunting a 50 Ω line.

and connects the receiver (Rx) to it. The application of a negative voltage to the bias port causes current to flow through both diodes. This puts the diodes into their low resistance (forward bias) state, connecting the transmitter to the antenna and isolating the receiver. Such a design approach, using a λ/4 section to transform the short circuit formed by the shunt diode to an open circuit at the common junction, will operate only over a limited bandwidth. However, good performance will be obtained over a 20% to 30% bandwidth, more than sufficient for most applications.

Note that having the diodes in series in the bias circuit conserves current, compared to operating them in parallel.

Diode Limitations

PIN diode switches, operating in the frequency ranges of HF through millimeter waves, have been produced for years. However, in an application such as this one, cost considerations require that plastic packaged surface mount diodes be used in some type of planar transmission line. The SOT-23 package has become a virtual industry standard, and is the type which is described in this note. Unfortunately, the SOT-23 package leads and bondwire add approximately 2.0 nH of parasitic inductance to the diode. As can be seen in Figure 2, even an ideal diode (R = 0 Ω) with this much inductance will produce less than 5 dB of isolation when mounted in shunt in a 50 Ω system.

The HSMP-4890 PIN diode overcomes the problem of excessive parasitic inductance in the SOT-23 by using two leads for the anode contact, as shown in Figure 3. This diode is a special low inductance variation of the standard HSMP-3890 series. Measured inductance for this product is ≅ 1.0 nH, half the usual value. Reference to Figure 2 will show that this results in an improvement in isolation compared to a conventional diode. However, isolation in the PCN band is still less than 10 dB, and other methods must be sought to bring the receiver arm isolation up to the required value.

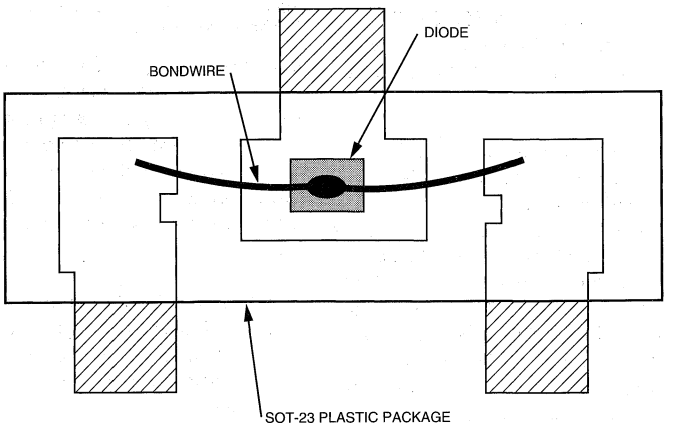


Figure 3. HSMP-4890 Low Inductance Diode.

Circuit Design Approach

Two circuit design "tricks" can be used to extract sufficient isolation from the shunt HSMP-4890 diode. The first is to substitute CPW (**Co**Planar **W**aveguide) transmission line for the familiar microstrip. Described in Appendix A, this planar transmission medium offers the advantage of having ground on the same (top) surface of the board as the conductor. When the HSMP-4890 is mounted such that it straddles the CPW, as shown in Figure 4, the availability of ground potential within 0.006" of both sides of the center conductor reduces the parasitic inductance of the HSMP-4890 to ≅ 0.7 nH. From Figure 2 it can be seen that an ideal shunt diode with this value of inductance produces more than 10 dB of isolation in the PCN band. Thus, CPW was chosen over microstrip for the design of this switch.

In order to insure that a SOT-23 package can straddle a CPW, the sum of the linewidth plus both gap widths must be less than 0.055 inch. A design curve[1] for such a CPW on **HT-2** PCB material is given in Figure 5. See Appendix B for a discussion of **HT-2** PCB material, which was chosen over the more familiar FR-4 in order to minimize losses.

The second circuit approach which can be used to realize sufficient isolation in the receiver arm is to use two shunt diodes separated by 90° of electrical length. If a single shunt diode will produce 11 dB of isolation at 1.75 GHz, then two in cascade with 90° between them will exhibit (2 x 11) + 6 = 28 dB. At frequencies which are lower than those discussed here, a lumped element phase delay circuit such as

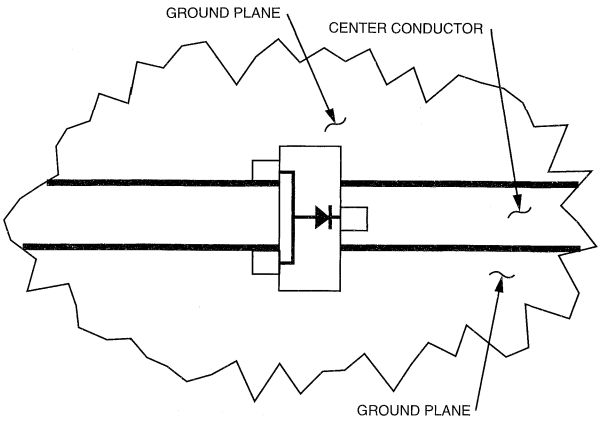


Figure 4. HSMP-4890 Diode Mounted in Shunt Across a CPW.

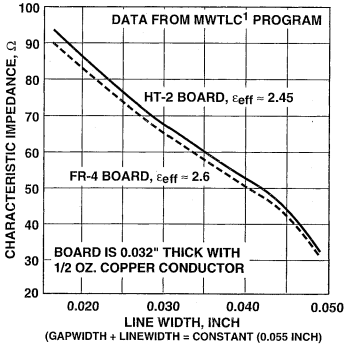


Figure 5. Impedance vs. Linewidth, CoPlanar Waveguide.

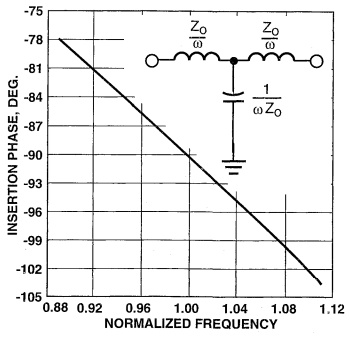


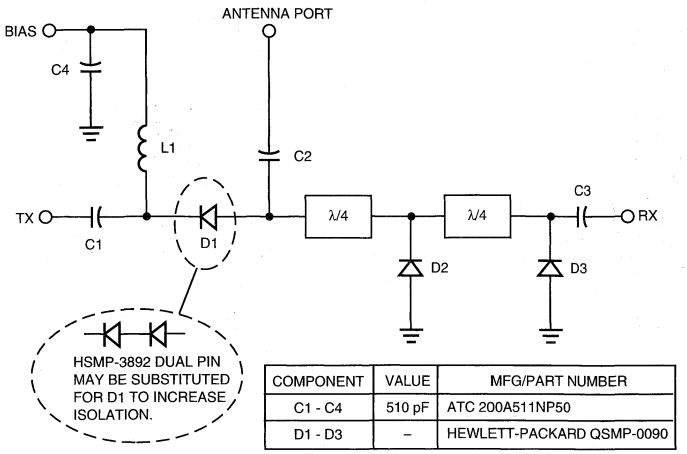
Figure 6. 90° Phase Delay Circuit.

that shown in Figure 6 would offer low losses and compact size. However, as frequencies approach 2 GHz, the losses in inductors (and, to a lesser extent, capacitors) become excessive and λ/4 transmission lines become more attractive.

Using this combination of diode and circuit design elements, the switch shown schematically in Figure 7 was designed, laid out and fabricated.

Circuit Layout and Component Selection

At frequencies above 1 GHz, care must be taken to avoid unnecessary losses in any circuit. Before the final layout of the switch was undertaken, therefore, the initial design was modelled and analyzed using MMICAD®[2]. In particular, it was found that the distance from series diode D1 to the switch common junction had a significant effect upon the reverse bias insertion loss in the receive arm. This distance was, therefore, kept to an absolute minimum. An air



COMPONENT	VALUE	MFG/PART NUMBER
C1 - C4	510 pF	ATC 200A511NP50
D1 - D3	–	HEWLETT-PACKARD QSMP-0090

Figure 7. Schematic of the prototype Switch.

core solenoid was selected for L1, in that it provided 50 nH of inductance with high Q and low cost. Since this is a surface mount design, chip capacitors were selected for bypassing and bias blocking. However, it was found that many chip capacitors which show good performance at VHF frequencies can exhibit losses of 0.2 to 0.3 dB each when they are used for bypass and blocking devices in the PCN band. Several different types were characterized before those shown in Figure 7 were chosen. In order to save board space, the λ/4 50 Ω line between D2 and D3 was folded upon itself.

The physical layout of the switch is shown in Figure 8. Finished width and length were 1.6" x 1.8".

CPW brings with it a number of layout requirements which are unique. It is essential that the grounds on both sides of the conductor are maintained at the same potential. The two anode leads of D2 and D3 serve the purpose of providing a bridge between ground planes in the switch's only long transmission line. The common junction deserved some special attention because it is a TEE junction. Three via holes were used to connect the three ground surfaces to a triangular interconnecting patch on the otherwise blank underside of the board, as can be seen in Figure 8. Alternatively, the ground plane could have been interconnected on the top surface and the conductors interconnected on the underside, as shown in the lower inset. This need to maintain symmetry in a CPW circuit is illustrated by the use of a pair of capacitors to realize the bypass C4. If only one is used, touching the bias conductor at the input will induce ripples in the passband response of the switch.

Finally, any circuit realized in CPW must, at some point, interface with conventional microstrip. A straightforward transition between the two lines is shown in Figure 9, where twin via holes are used to connect the two overlapping groundplanes.

Measured Performance

The switch shown in Figure 8 was fabricated and fitted with E.F. Johnson 142-0701-801 SMA connectors. These end launchers have ground fingers in the same plane as the connector's center conductor, making them ideal for use with CPW.

Before final measurements were made, a HSMP-3892 PIN diode pair (two diodes, connected in series in a single SOT-23 package) was substituted for series diode D1 shown in Figure 8. This was done to increase the transmitter arm isolation by halving the effective reverse bias capacitance of D1. The layout of the circuit board allows physical interchangeability between the HSMP-3892 and the HSMP-4890 products.

Data obtained from the prototype switch are given in the swept frequency measurements of Figures 10 through 13. As can be seen from all four data plots, return loss at 1750 MHz is greater than 15 dB at all ports for both bias conditions (+5 V and -20 mA). Receiver arm isolation is 28 dB at the design frequency, and the transmit arm isolation is 15 dB. Insertion loss for the same two arms is 0.8 dB and 0.7 dB respectively.

The measured value of transmitter arm isolation was well above the 10 dB originally specified. Use of the HSMP-4890 (or standard product HSMP-3890) for the HSMP-3892 dual diode in the D1 series diode position would result in a reduction in isolation to ≅ 12 dB, a value which would be satisfactory for many applications. This might be considered by those manufacturers for whom it is important to

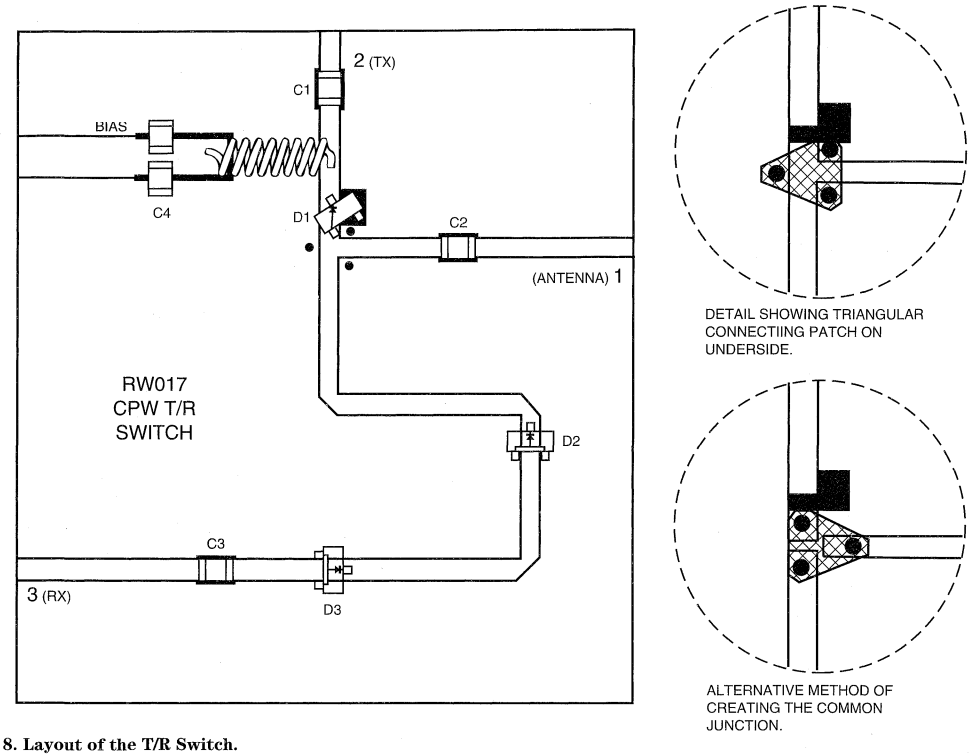


Figure 8. Layout of the T/R Switch.

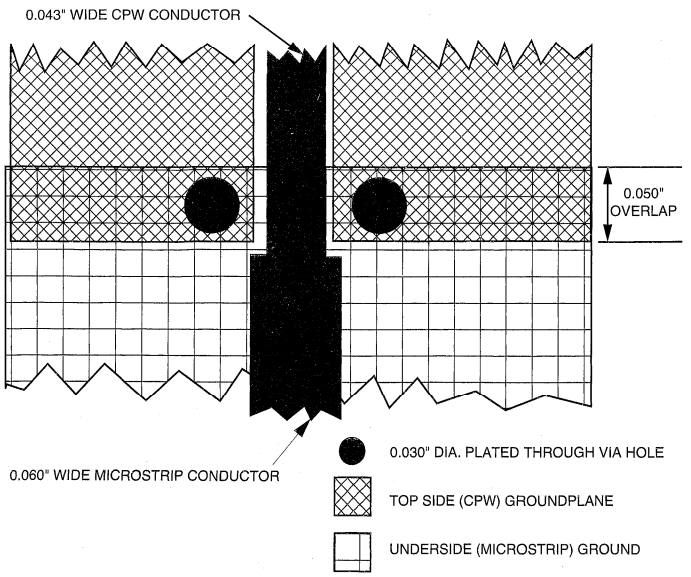


Figure 9. Microstrip to CPW Transition on 0.032" HT-2.

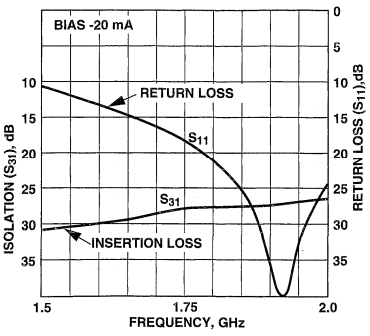


Figure 10. Receiver Arm Isolation.

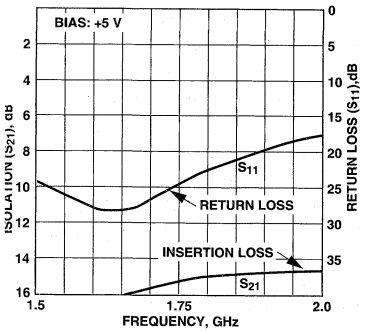


Figure 11. Transmitter Arm Isolation.

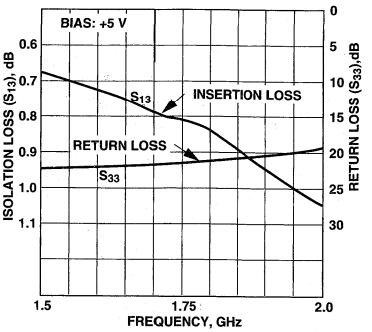


Figure 12. Receiver Arm Insertion Loss.

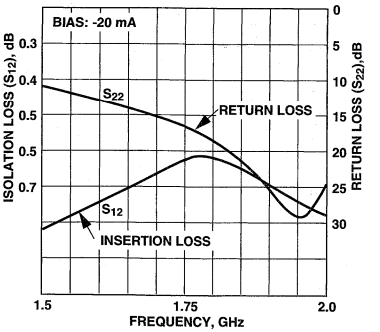


Figure 13. Transmitter Arm Insertion Loss.

minimize the number of different diode part numbers kept in stock.

Conclusion

An inexpensive, low power consumption SPDT switch for PCN hand-held applications has been described, along with design concepts based upon CoPlanar Waveguide and a new, low inductance PIN diode. The design approach contained in this paper is easily scaled to other frequency ranges.

Appendix A: CoPlanar Waveguide

What Is Coplanar Waveguide?

CoPlanar Waveguide (CPW)[3,4,5,6,7,8] is a RF-microwave transmission line having all conducting elements on the same side of a suspended substrate. A CPW transmission line consists of a center strip conductor with semi-infinite groundplanes running in parallel on both sides, separated from the center conductor by a width of exposed dielectric material. See Figure 14. Analytical expressions for the characteristic impedance (Z_o) and effective dielectric constant can be obtained if the two slots are modelled as magnetic walls. If we assume the metallization thickness to be zero, the overall line capacitance per unit length can be computed as the sum of two capacitances; the

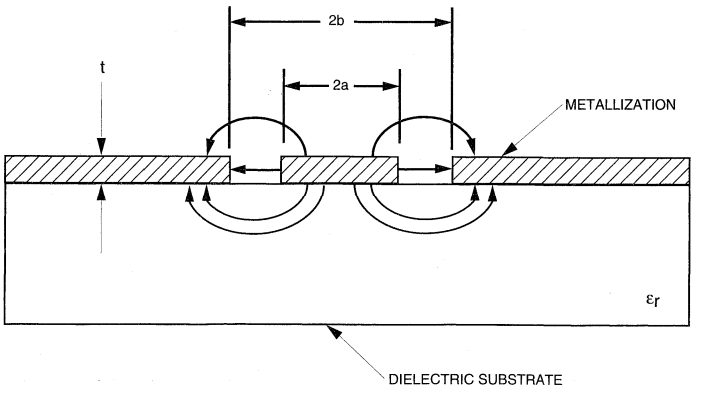


Figure 14. Cross-Section of CoPlanar Waveguide.

upper half with ε_o and the lower half with ε_r. The phase velocity (v_p) is

$$v_p = \frac{c}{\sqrt{\varepsilon_{eff}}}$$

where c = the speed of light in a vacuum

and

$$\varepsilon_{eff} \cong \frac{\varepsilon_r + 1}{2}$$

The characteristic impedance of a transmission line is

$$z_o = \frac{1}{Cv_p}$$

where C = line capacitance

Thus, within reasonable limits, the characteristic impedance is unaffected by substrate thickness, and is solely dependent upon the ratio a/b. The effective dielectric constant ε_{eff} is also relatively independent of Z_o, unlike the case with microstrip.

Why Use CPW?

CPW offers several advantages over the more commonly used microstrip layouts. The most significant of these are shunt connections that are easy to make as series connections, elimination of costly via holes or wraparounds, low radiation loss and insensitivity to substrate thickness. On the down side, CPW does have higher ohmic losses due to the concentration of its currents near the metal edges, though this does not pose much of a problem at lower microwave and RF frequencies. The surface mounting of devices on CPW imposes thermal constraints since it is a suspended substrate. This problem can be minimized by the improved thermal characteristics of some new materials (such as aluminum nitride) or the use of conductor backed CPW.

What Are Reasonable Limits?

As mentioned above, Z_o is relatively independent of substrate thickness, within reasonable limits. This assumption holds true provided that D > 2b (see Figure 15). In order to treat the ground planes as semi-infinite, and therefore be able to neglect them, S1 > 3b. Reducing the width of the ground planes leads to increases in Z_o. Another desirable simplification is that upper and lower metal covers have no effect upon Z_o. This will be the case if H1 > 4b and H2 > 3b. When these limits are exceeded, the effect of the upper and lower lids will be to lower Z_o. Line to line coupling is obviously dependent upon the width of the ground plane between them. A safe rule of thumb to follow is to maintain S2 > 5b to avoid unwanted coupling between parallel conductors.

Some Practical Tips On Designing With CPW

Since most circuits are likely to consist of more than a single transmission line, there are some basic guidelines to follow when laying out CPW circuits. Since the ground plane is on the same

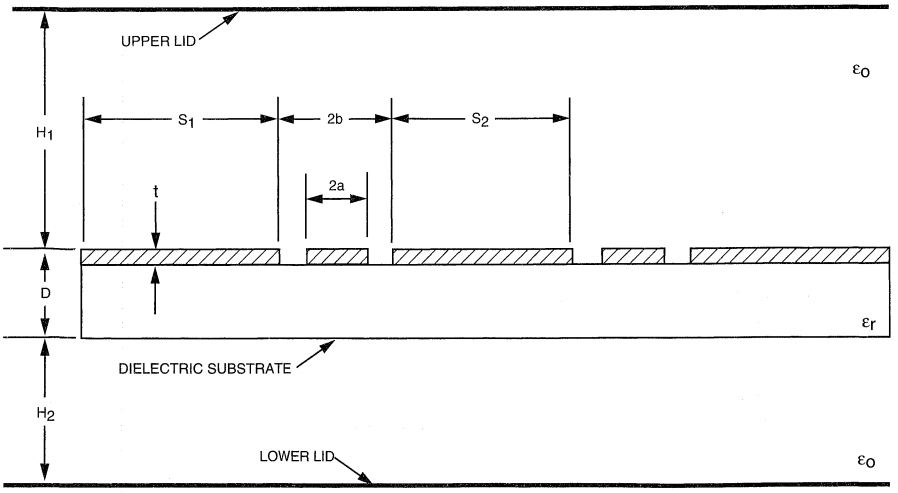


Figure 15. CoPlanar Waveguide with Top and Bottom Covers.

surface as the transmission lines it is very important to keep all of the ground planes at the same potential. This can be done through the use and proper spacing of conductive bridges (see Figure 16). Any time there is an intersection of conductors, or open or short circuit stubs, care must be taken to ensure that the ground planes remain at the same potential on both sides of the center conductor. This is accomplished through the use of conductive bridges, as shown in Figure 17. The same problem arises for bends in transmission lines. The best solution is to break the line at the bend, allowing metallization on the substrate to connect the ground planes, and use a conductive bridge to join the transmission lines. See Figure 18 for an illustration. Alternatively, one can use a ground plane conductive bridge in a manner similar to that illustrated in Figure 17 to force ground potentials to be equal at both ends of the bend.

It should be kept in mind that, for CPW formed on plastic laminate boards such as FR4, conductive bridges are most easily formed using plated through holes to connect to a small etched line on the underside of the board.

The effect of TEEs, intersections, and abrupt changes in linewidth (Z_o) is to add discontinuities to the CPW line which must be taken into account in the design of high frequency circuits. For example, in an open circuit shunt stub such as that shown in Figure 17, the short section of transmission line immediately on either side of the stub has a transverse field normal to G2 but not to G1. This can be modelled as a short section of high impedance line of $Z_o \cong 110\ \Omega$. If the open circuit stub is symmetrical with respect to the center

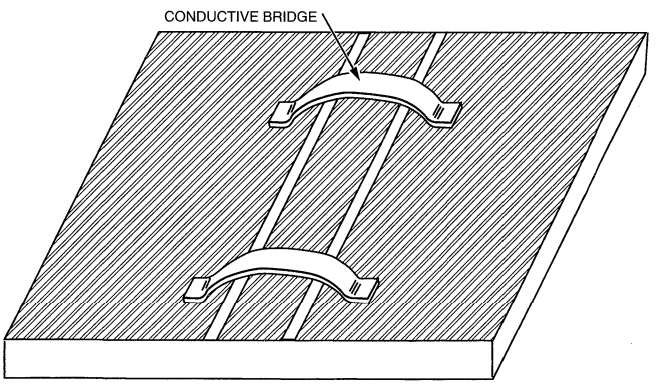


Figure 16. CPW with Conductive Bridge.

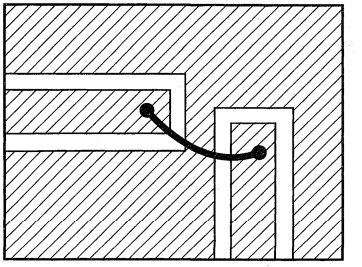


Figure 18. Ground Continuity is Maintained.

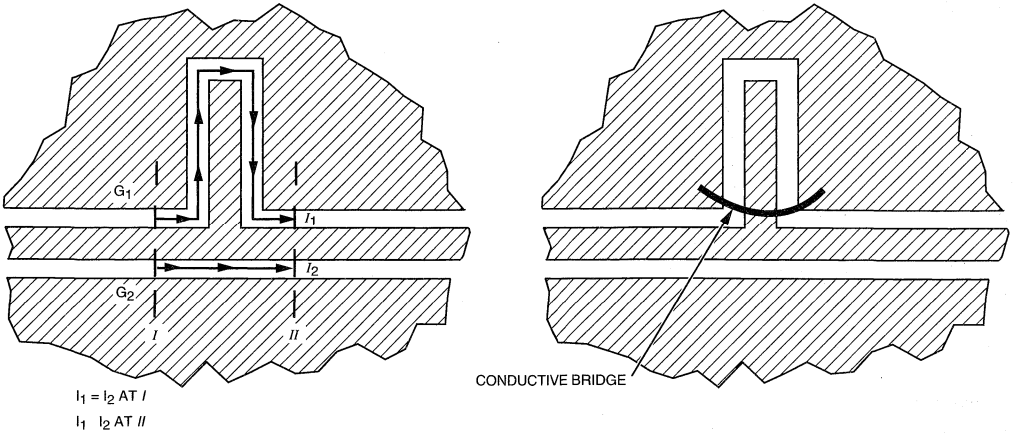


Figure 17. Control of Ground Currents in CPW.

conductor, extending into G2 as well as G1, the impedance would be slightly higher. Renewed interest in CPW has led to more studies of CPW discontinuities and models for them.[9]

Appendix B: HT-2 PCB Material

Several printed circuit board materials are in common use for RF circuits such as this one. Two of the most popular are FR4 and fiberglass reinforced PTFE (Teflon®). The former provides good mechanical stability and durability at low cost. However, it suffers from high losses and a dielectric constant which is poorly controlled and strongly frequency-dependent. The latter exhibits very good RF properties, but is expensive, suffers from poor mechanical stability, and cannot survive certain SMT (**S**urface **M**ount **T**echnology) processing steps. Hewlett-Packard's new **HT-2** board material provides durability and high temperature performance which are actually superior to FR4 with a controlled dielectric constant ($\varepsilon_r \cong 4.3$) and a loss tangent which is one third less than that of FR4. These properties make it ideal for microstrip circuits operating at frequencies up to or above 6 GHz.

To compare the performance of this material with FR-4 in a CPW, two experimental 50 Ω lines, 3.6 inches in length, were fabricated and tested. Cross section dimensions were identical in both cases, with board thickness = 0.032", linewidth = 0.043" and gapwidth = 0.006". Insertion loss and return loss were measured from 10 MHz to 8 GHz, using the same E.F. Johnson connectors described in the body of this paper. When the losses due to connector mismatch were subtracted, the resulting curve of resistive loss vs. frequency was linear in both cases. Using a value of $\varepsilon_{eff} = 2.70$ for the FR-4 and 2.57 for the **HT-2**, the loss vs. frequency curve was found to correspond to constant values of loss per wavelength. For the **HT-2** line, that constant was 0.5 dB/λ, much less than the 0.8 dB/λ of the FR-4 line. It is interesting to note that similar measurements on microstrip lines with h = 0.032" have resulted in identical values of loss/wavelength, even though the higher value of ε_{eff} on microstrip results in wavelengths which are shorter than those in CPW.

At the time of this printing HT-2 is available through Dan Schutte of International Circuits, 1319 S. Arkle St., Visalia, CA.

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HEWLETT® PACKARD

Applications for the HSMP-3890 Surface Mount Switching PIN Diode

Application Note 1072

Introduction

The PIN diode is generally considered to behave like a current controlled RF variable resistor[1]. In the microwave frequency range, this simplification is generally quite accurate. However, in the RF frequency range (below 2 GHz), matters are much more complicated, and the incorrect choice of diode can produce disastrous results in terms of circuit performance.

The discussion which follows assumes that the reader has had some exposure to RF signal control using PIN diodes. If not, you may refer to Appendix A, "Back To Basics," at the end of this note.

PIN Diodes

In RF and microwave networks, mechanical switches and attenuators are bulky, often unreliable, and difficult to manufacture. Switch ICs, while convenient to use and low in cost in small quantities, suffer from poor distortion performance and are not as cost-effective as PIN diode switches and attenuators in very large quantities. For over 30 years, designers have looked to the PIN diode for high performance/low cost solutions to their switching and level control needs.

In the RF and microwave ranges, the switch serves the simple purpose which is implied by its name; it operates between one of two modes, ON or OFF. In the ON state, the switch is designed to have the least possible loss. In the OFF state, the switch must exhibit a very high loss (isolation) to the input signal, typically from 20 to 60 dB. The attenuator, however, serves a more complex function. It provides for the "soft" or controlled variation in the power level of a RF or microwave signal. At the same time as it attenuates the input signal to some predetermined value, it must also present a matched input impedance (low VSWR) to the source. Every microwave network which uses PIN diodes (phase shifter, modulator, etc.) is a variation on one of these two basic circuits.

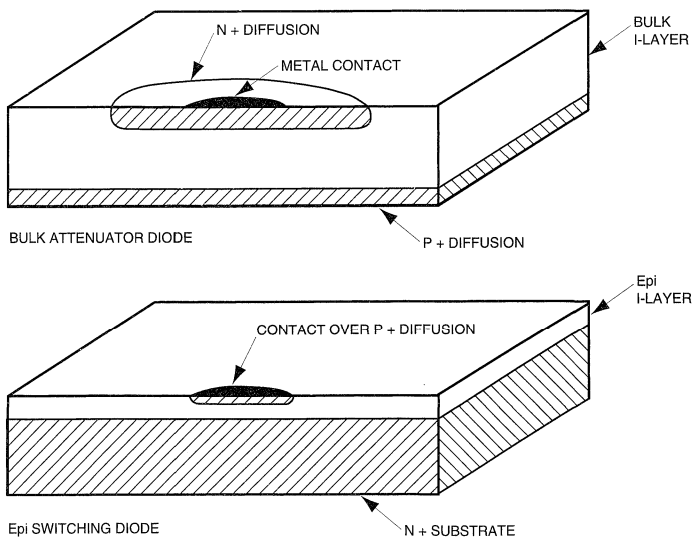


Figure 1.

1. Hewlett-Packard Application Note 922, *Application of PIN Diodes.*

One can see that the switch and the attenuator are quite different in their function, and will therefore often require different characteristics in their PIN diodes. These properties are easily controlled through the way in which a PIN diode is fabricated. See Figure 1.

Diode Construction

At Hewlett-Packard, two basic methods of diode fabrication are used. In the case of bulk diodes, a wafer of very pure (intrinsic) silicon is heavily doped on the top and bottom faces to form P and N regions. The result is a diode with a very thick, very pure I region. The epitaxial layer (or EPI) diode starts as a wafer of heavily doped silicon (the P or N layer), onto which a thin I layer is grown. After the epitaxial growth, diffusion is used to add a heavily doped (N or P) layer on the top of the epi, creating a diode with a very thin I layer populated by a relatively large number of imperfections.

These two different methods of design result in two classes of diode with distinctly different characteristics, as shown in Table 1.

As we shall see in the following paragraphs, the bulk diode is almost always used for attenuator applications and sometimes as a switch, while the epi diode (such as the HSMP-3890) is generally used as a switching element.

Diode Lifetime and Its Implications

The resistance of a PIN diode is controlled by the conductivity (or resistivity) of the I layer. This conductivity is controlled by the density of the cloud of carriers (charges) in the I layer (which is, in turn, controlled by the DC bias). Minority carrier lifetime, indicated by the Greek symbol τ, is a measure of the time it takes for the charge stored in the I layer to decay, when forward bias is replaced with reverse bias, to some predetermined value. This lifetime can be short (35 to 200 nsec. for epi diodes) or it can be relatively long (400 to 3000 nsec. for bulk diodes). Lifetime has a strong influence over a number of PIN diode parameters, among which are distortion and basic diode behavior.

To study the effect of lifetime on diode behavior, we first define a cutoff frequency $f_c = 1/\tau$. For short lifetime diodes, this cutoff frequency can be as high as 30 MHz while for our longer lifetime diodes $f_c > 400$ KHz. At frequencies which are ten times f_c (or more), a PIN diode does indeed act like a current controlled variable resistor. At frequencies which are one tenth (or less) of f_c, a PIN diode acts like an ordinary PN junction diode. Finally, at $0.1\ f_c \le f \le 10\ f_c$, the behavior of the diode is very complex. Suffice it to mention that in this frequency range, the diode can exhibit very strong capacitive or inductive reactance — it will not behave at all like a resistor. However, at zero bias or under heavy forward bias, all PIN diodes demonstrate very high or very low impedance (respectively) no matter what their lifetime is.

Diode Resistance vs. Forward Bias

If we look at the typical curves for resistance vs. forward current for bulk and epi diodes (see Figure 2), we see that they are very different:

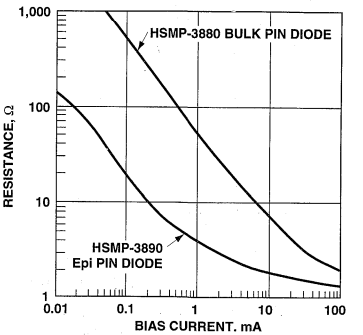


Figure 2. Resistance vs. Bias Current, Hewlett-Packard PIN Diodes

Of course, these curves apply only at frequencies > 10 f_c. One can see that the curve of resistance vs. bias current for the bulk diode is much higher than that for the epi (switching) diode. Thus, for a given current and junction capacitance, the epi diode will always have a lower resistance than the bulk diode. The thin epi diode, with its physically small I region, can easily be saturated (taken to the point of minimum resistance) with very little current compared to the much larger bulk diode. While an epi diode is well saturated at currents around 10 mA, the bulk diode may require upwards of 100 mA or more. Moreover, epi diodes can achieve

Table 1. Bulk and EPI Diode Characteristics

Characteristic	EPI Diode	Bulk Diode
Lifetime	Short	Long
Distortion	High	Low
Current required	Low	High
I Region Thickness	Very thin	Thick

reasonable values of resistance at currents of 1 mA or less, making them ideal for battery operated applications.

Having compared the two basic types of PIN diode, we will now focus on the HSMP-3890 epi diode, the subject of this note.

Given a thin epitaxial I region, the diode designer can trade off the device's series resistance R_S and junction capacitance C_j by varying the diameter of the contact and I region. Hewlett-Packard produces two epi switching PIN diodes, the HSMP-3820 and the HSMP-3890. The former features very low R_S, making it suitable for high-Q applications such as band switching an oscillator's resonant circuit. However, its relatively high total capacitance (typically 0.75 pF) limits its performance in high frequency (UHF) switching applications. The HSMP-3890, however, was designed with the 930 MHz cellular and RFID, the 1.8 GHz PCS and 2.45 GHz RFID markets in mind. Combining the low resistance shown in Figure 2 with a typical total capacitance of 0.27 pF, it forms the basis for high performance, low cost switching networks.

Single Diode Switches

In order to predict the performance of the HSMP-3890 as a switch, it is useful to construct a model which can then be used in one of the several linear analysis programs presently on the market. Such a model is given in Figure 3, where Rj > 3/I and I is the current in mA. This equation, of course, applies only for f > 10 f_c, or approximately 100 MHz.

It should be noted that nonlinear analysis programs such as SPICE

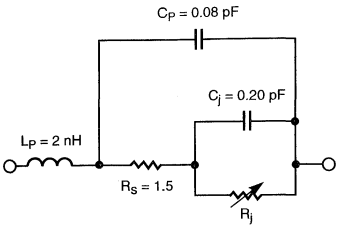


Figure 3. Model of Single Diode Switch.

lack a key parameter, carrier lifetime, in their diode model. Thus, they cannot be used to predict the performance of a circuit containing a PIN diode unless the diode is modelled as a resistor.

The HSMP-3890 can be used as a single switching element, either as a series or a shunt switch, as shown in Figure 4. We can simplify the model given in Figure 3 to achieve the equivalent circuits of the diode in the isolation mode (reverse bias for the series diode, forward bias for the shunt diode). These two equivalent circuits can then be analyzed to predict the isolation which either configuration will produce.

The circuits from Figure 4 were analyzed on AppCAD[2] with the results shown in Figure 5. It can be seen that the series diode switch provides higher isolation at any given frequency, which is a result of the high parasitic inductance of the SOT-23 package. Nevertheless, both configurations provide useful amounts of isolation at frequencies under 1 GHz.

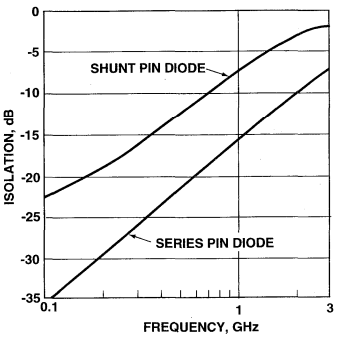


Figure 5. Isolation of a Single HSMP-3890 PIN Diode in a 50 Ω System.

2. AppCAD, an MS-DOS program available from your HP sales office.

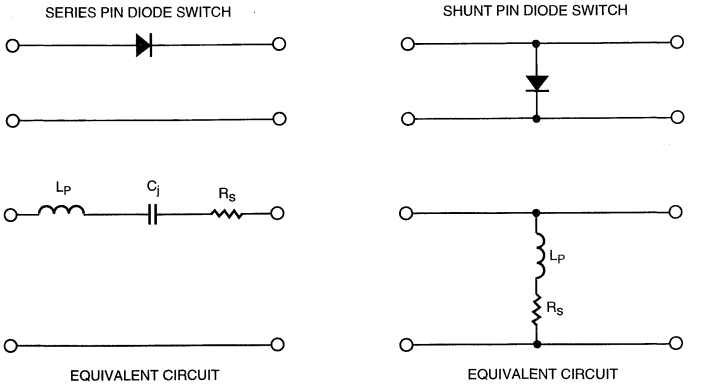


Figure 4. Series and Shunt PIN Diode Switches.

Multiple Diode Switches

For higher levels of isolation, there are a number of circuit design techniques which can be used.[1,3] The most useful of these is to cascade series and shunt diode switches, as shown in Figure 6, keeping the spacing between them small with respect to a wavelength. The resulting isolation, calculated using AppCAD, is dramatically higher than that produced by a single diode. This arrangement can be implemented with two HSMP-3890 diodes, or with the HSMP-3892 pair (also in the SOT-23 package).

If the series/shunt combination of Figure 6 is cascaded (using four diodes), the resulting isolation will be twice that of a single pair (40 dB instead of 20 dB, etc.).

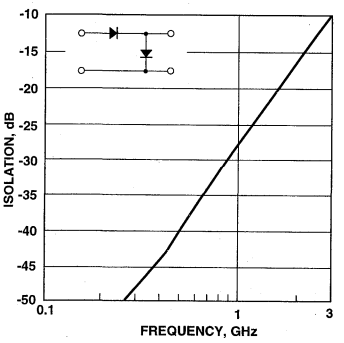


Figure 6. Isolation of a Series/Shunt pair of HSMP-3890 PIN Diodes in a 50 Ω System.

For the designer who wishes to use the shunt switch but needs more isolation, the low inductance HSMP-4890 can be used, as shown in Figure 7 (along with its equivalent circuit).

Other switch design approaches are given in the data sheet for the HSMP-389X series of switching PIN diodes.

Of course, the typical application of switching PIN diodes is multi-throw switches, rather than the SPST described above. While the single HSMP-3890 can be used with good results in multi-throw switches, the multi-diode products can offer savings in space, as illustrated in Figures 8 and 9.

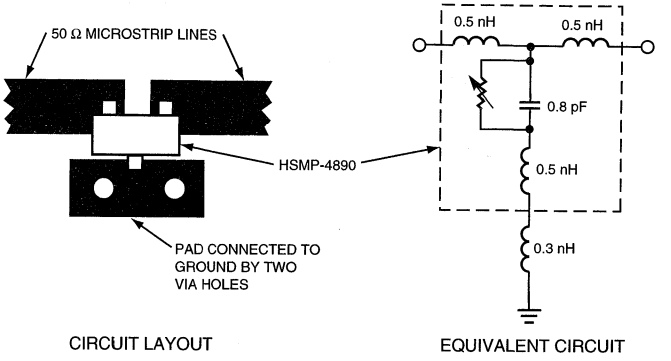


Figure 7.

3. R.W. Waugh and M.M. Waugh, "SPDT Switch Serves PCN Applications," *Microwaves & RF*, January, 1994.

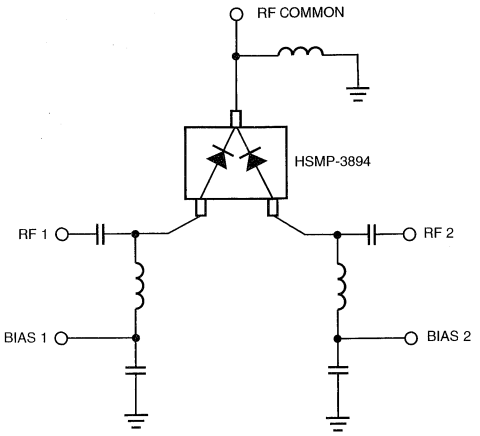


Figure 8. Simple SPDT Switch.

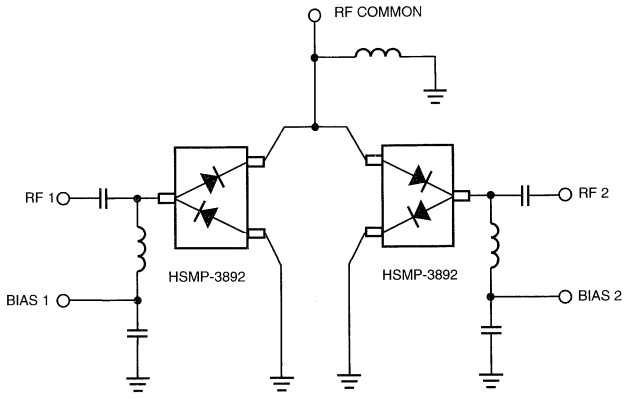


Figure 9. High Isolation SPDT Switch.

Conclusion

The HSMP-3890 PIN diode has been described and shown to be an excellent choice for a high performance/low cost RF switch. For further information, contact your local HP sales office.

Appendix A: Back to Basics

The most important property of the PIN diode is the fact that it appears as an almost pure resistance at RF (radio frequencies), whose resistance can be varied over a range of approximately 1 to 10,000 Ω through the use of a DC (direct current) control current. When the control current is varied continuously, the PIN diode is useful for leveling and amplitude modulating an RF signal (operating as a so-called attenuator). When the control current is switched "on" and "off " or in discrete steps, the device is useful for switching (and other switch type functions, such as phase shifting, pulse modulating, etc.). The PIN diode's small size and weight, as well as its high switching speed and freedom from parasitic elements, make it ideally suited for use in miniature, broadband signal control components.

A PIN diode is a silicon semiconductor consisting of a layer of intrinsic (high resistivity) material of finite area and thickness which is contained between highly doped P and N type materials. When the diode is forward biased with DC current, charge is injected into this intrinsic or "I" region. This charge consists of holes and electrons which have a finite lifetime before they recombine. The density of charge in the intrinsic region, and its geometry, determine the conductance of the device. The lifetime (denoted by the Greek symbol τ or "tau") determines the approximate low frequency limit of useful application, as well as other important parameters of the diode.

Applications

The application notes represented by these abstracts are available from your local Hewlett-Packard sales office or nearest Hewlett-Packard authorized distributor or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

Applications Data

Device data are made available on computer discs to evaluate device performance and facilitate CAD.

DesignPak
The DesignPak is a comprehensive data library of S-parameter and noise parameter data for the following products:

- Discrete Schottky diodes
- Discrete GaAs FET devices
- GaAs MMIC products
- Discrete Bipolar transistors
- Silicon MMIC gain blocks
- Silicon MMIC products

All S-parameters are in a standard *.S2P ASCII file format for use on most linear circuit simulators.

Publication No. 5963-2301E

Primer 3
Thermal Properties

Publication No. 300124

Primer 3A
Thermal Resistance

Publication No. 300126

General Application Notes

AN A001
Notes on Choke Network Design
Stability; Bipolar Transistor and GaAs FET choke networks

Publication No. 5091-8824E

AN A004R
Electrostatic Discharge Damage and Control
Identifying and preventing ESD damage

Publication No. 5091-8803E

AN A006
Mounting Considerations for Packaged Microwave Semiconductors
Mechanical, thermal, and soldering information

Publication No. 5091-8696E

AN 979
The Handling and Bonding of Beam Lead Devices Made Easy
Beam Lead devices are particularly attractive for hybrid circuits because of their low parasitics and small size. The availability of equipment and techniques specifically designed for their small size has facilitated the handling and bonding of these devices. This application note describes some of this equipment and techniques, and outlines suggestions for the proper handling and bonding of Beam Lead devices

Publication No. 5953-4435

AN 992
Beam Lead Attachment Methods
This application bulletin gives a general description of various methods of attaching beam lead components to both hard and soft substrates. A table summarized the most common attachment methods with advantages, disadvantages, and equipment costs.

Publication No. 5091-9074E

AN 993
Beam Lead Diodes Bonding to Soft Substrate
The hard gold surface on standard PC boards with soft substrate material makes it almost impossible to successfully bond beam lead diodes onto the boards with normally recommended thermocompression bonding. Described in this application note is a new method of resistive spot welding or modified gap welding,

which uses a single electrode to weld the beam lead while the conductor is contacted separately. This method allows tight pressure to be used on the weld probe, resulting in an effective bond without damaging the beam lead device.

Publication No. 5954-2227

AN 957-1
Broadbanding the Shunt PIN Diode SPDT Switch
Covers an impedance matching technique which improves the bandwidth of shunt PIN diodes switches.

Publication No. 5964-3902E

AN 957-2
Reducing the Insertion Loss of a Shunt PIN Diode
Examines a simple filter design which includes the shunt PIN diode capacitance into a low pass filter, thereby extending the upper frequency limit.

Publication No. 5952-0491

PIN Diode Selection Guides

Hewlett-Packard PIN diodes are available in chip form and several types of packages, which make each more suitable for a particular application.

For switching, attenuating, and other general purpose applications particularly in the VHF/UHF range, the low cost glass package (Outline 15) and the surface mount, SOT-23 package are suitable.

The stripline package (Outline 60) contains built-in low pass matching circuits which can be used in broadband designs up to 10 GHz. Because of good heat sinking, it can handle high power in switching, attenuating and limiting applications.

The beam lead devices with low parasitics are designed for use in stripline or microstrip circuits using welding or thermocompression bonding techniques.

Surface Mount/SOT-23 Package PIN Diodes[1]

Application	Part Number	C_T (pF) max/typ	R_s (Ω) max	Page No.
Attenuator				
lowest distortion	HSMP-381x[3]	0.35/0.27	3.0	2-63
lowest distortion/low inductance	HSMP-481x	0.40/0.35	3.0	2-71
specialty	HSMP-383x	0.3/0.2	1.5	2-71
low distortion	HSMP-380x	0.37/0.32	2.0	2-71
Switching				
best 900 MHz	HSMP-389x[2,3]	0.3/0.2	2.5	2-71
>2 GHz shunt	HSMP-489x	0.38/0.33	2.5	2-71
low Rs	HSMP-382x	0.8/0.6	0.6	2-71
low Rs/low inductance	HSMP-482x	1.00/0.75	0.6	2-71
high power	HSMP-3880	0.4/0.3	6.5	2-71
specialty	HSMP-383x	0.3/0.2	1.5	2-71
Power Limiter				
low Rs	HSMP-382x	0.8/0.6	0.6	2-71
low inductance/high frequency	HSMP-482x	1.00/0.75	0.6	2-71
General Purpose				
typical specs	HSMP-386x[3]	—/0.20	1.5	2-71

Notes:
1. See the specific data sheet for test conditions.
2. Also available in SOT-143 package.
3. Also available in SOT-323 package.

For reliability data see pages 2-105 through 2-112.

RF Non-Surface Mount PIN Diodes

Glass Axial Lead, Beam Lead, Chip, Stripline

Part Number	C_T Max. pF	R_S Max. at 100 mA (Ω)	V_{BR} Min. (V)	t_{rr} Typ. (ns)	Lifetime τ Typ. (ns)[1]	Package	Page No.
5082-3001	0.25	1	200	100	100	glass axial lead	2-101
5082-3039	0.25	1.25	150	100	100	glass axial lead	2-101
1N5719	0.3	1.25	150	100	100	glass axial lead	2-101
5082-3077	0.3	1.5	200	100	100	glass axial lead	2-101
5082-3188	1	0.6[2]	35	12	70[3]	glass axial lead	2-101
5082-3080	0.4	2.5	100		1300	glass axial lead	2-101
1N5767	0.4	2.5	100		1000	glass axial lead	2-101
5082-3379	0.4		50		1300	glass axial lead	2-101
5082-3081	0.4	3.5	100		2500	glass axial lead	2-101
HPND-0001	0.2	2	100	500	1800	chip	2-93
HPND-0002	0.2	3.5	100	300	1500	chip	2-93

Notes:
1. Lifetime measured at I_F = 50 mA, I_R = 250 mA
2. R_S Max. at 10 mA
3. I_F = 10 mA, I_R = 6 mA

For reliability data see pages 2-105 through 2-112.

Microwave PIN Diodes

Silicon PIN Diodes

Part Number	C_T Typ. pF	R_S Typ. (Ω)	V_{BR} Min. (V)	t_{rr} Typ. (ns)	Lifetime τ Typ., (ns)	Package	Page No.
5082-0001[2]	0.10	0.8	70	5	35[2]	chip	2-95
HPND-4018[2]	0.22	4.3	60	2	26[2]	beam lead	2-86
HPND-4005[2]	0.02	4.7	120		400[3]	beam lead	2-83
5082-0012[2]	0.10	1.0	150	100	400	chip	2-95
HPND-4028[2]	0.04	2.6	60	2.6	37[3]	beam lead	2-86
HPND-4038[2]	0.06	1.7	60	2.4	45[3]	beam lead	2-86
5082-3042[2]	0.40	1.0	70	5 (max)	35	15	2-101
5082-3043	0.40	1.5	50	10 (max)	35	15	2-101

Silicon Stripline PIN Diodes

Part Number	Isolation Min., (dB)	Insertion Loss Max., (dB)	SWR Max.	Lifetime τ Typ., (ns)	Package	Page No.
5082-3140	20	0.5	1.5	400	60[1]	2-97
5082-3141	20	1.0	1.5	35	60	2-97

Notes:
1. Denotes anode heat sink; all other parts are cathode heat sink
2. R_S Max. at 5 mA
3. I_F = 10 mA, I_R = 6 mA

For reliability data see pages 2-105 through 2-112.

HEWLETT® PACKARD

Surface Mount PIN Diodes in SOT-323 (SC-70)

Technical Data

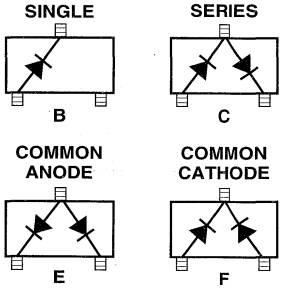
HSMP-381A Series
HSMP-386A Series
HSMP-389A Series

Features

- **Diodes Optimized for:**
  Low Current Switching
  Low Distortion Attenuating
  Ultra-Low Distortion Switching
  Microwave Frequency Operation
- **Surface Mount SOT-323 (SC-70)Package**
  Single and Pair Versions
  Tape and Reel Options Available
- **Low Failure in Time (FIT) Rate***

* For more information see the Surface Mount PIN Reliability Data Sheet.

Package Lead Code Identification (Top View)



Description/Applications

The HSMP-381A series is specifically designed for low distortion attenuator applications. The HSMP-386A series is a general purpose PIN diode designed for low current attenuators and low cost switches. The HSMP-389A series is optimized for switching applications where low resistance at low current, and low capacitance are required.

Absolute Maximum Ratings[1], T_C = + 25°C

Symbol	Parameter	Unit	Absolute Maximum
I_f	Forward Current (1 µs Pulse)	Amp	1
P_{iv}	Peak Inverse Voltage	V	Same as V_{BR}
T_J	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	300

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = 25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications, T_C = +25°C, each diode

PIN Attenuator Diodes

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Total Resistance R_T (Ω)	Maximum Total Capacitance C_T (pF)	Minimum High Resistance R_H (Ω)	Maximum Low Resistance R_L (Ω)
381B 381C 381E 381F	E0 E2 E3 E4	B C E F	Single Series Common Anode Common Cathode	100	3.0	0.35	1500	10
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10\ \mu A$	I_F = 100 mA f = 100 MHz	V_R = 50 V f = 1 MHz	I_R = 0.01 mA f = 100 MHz	I_F = 20 mA f = 100 MHz

PIN General Purpose Diodes

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Typical Total Resistance R_T (Ω)		Typical Total Capacitance C_T (pF)
386B 386C 386E 386F	L0 L2 L3 L4	B C E F	Single Series Common Anode Common Cathode	50	3.0	1.5*	0.20
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10\ \mu A$	I_F = 10 mA f = 100 MHz I_F = 100 mA*		V_R = 50 V f = 1 MHz

PIN Switching Diodes

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Total Resistance R_T (Ω)	Maximum Total Capacitance C_T (pF)
389B 389C 389E 389F	G0 G2 G3 G4	B C E F	Single Series Common Anode Common Cathode	100	2.5	0.30
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10\ \mu A$	I_F = 5 mA f = 100 MHz	V_R = 5 V f = 1 MHz

Typical Parameters at T_C = +25°C

Part Number HSMP-	Total Resistance R_T (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance (pF)
381A Series 386A Series 389A Series	75 22 3.8	1500 500 200*	300 80 —	0.27 0.20 —
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 50 mA T_R = 250 mA I_F = 10 mA* I_R = 6 mA*	V_R = 10 V I_F = 20 mA 90% Recovery	50 V

Note:

1. Package marking code is laser marked.

Typical Performance, T_C = 25°C

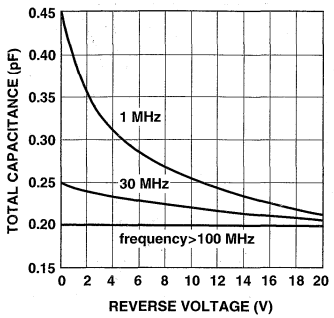


Figure 1. RF Capacitance vs. Reverse Bias, HSMP-381A Series.

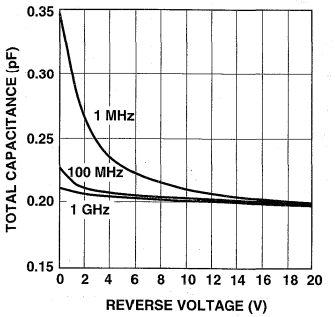


Figure 2. RF Capacitance vs. Reverse Bias, HSMP-386A Series.

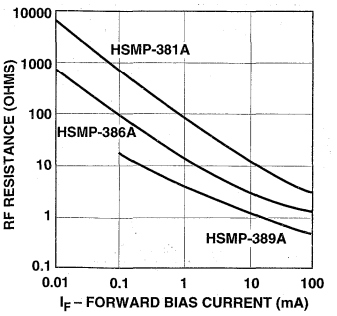


Figure 3. Total RF Resistance at 25° C vs. Forward Bias Current.

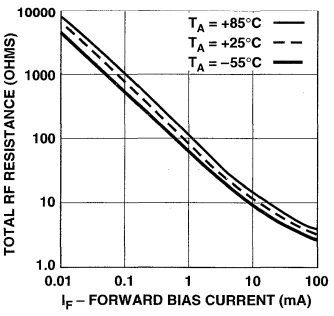


Figure 4. RF Resistance vs. Forward Bias Current for HSMP-381A Series.

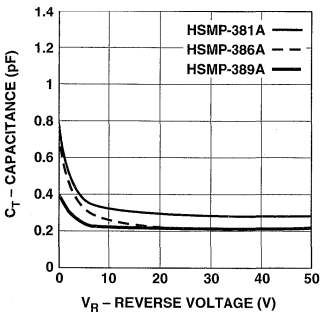


Figure 5. Capacitance vs. Reverse Voltage at 1 MHz.

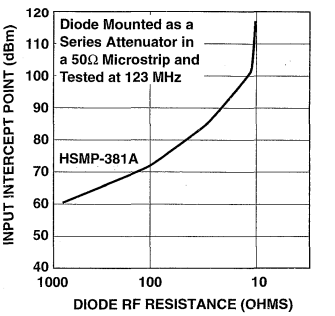


Figure 6. 2nd Harmonic Input Intercept Point vs. Diode RF Resistance for Attenuator Diodes.

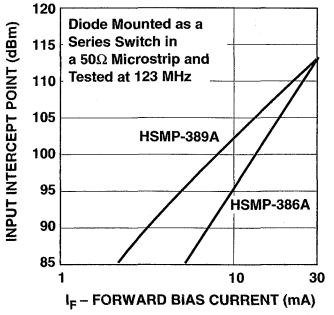


Figure 7. 2nd Harmonic Input Intercept Point vs. Forward Bias Current for Switch Diodes.

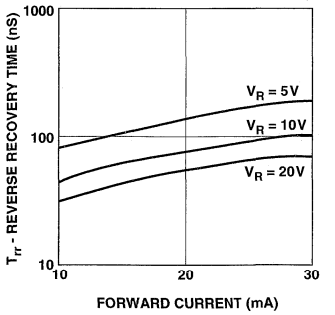


Figure 8. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages. HSMP-386A Series.

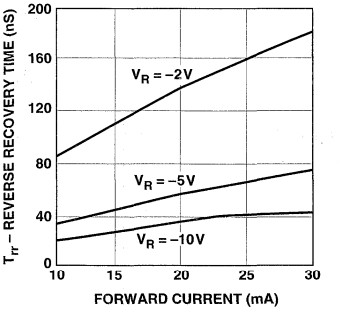


Figure 9. Typical Reverse Recovery Time vs. Reverse Voltage. HSMP-389A Series.

Typical Performance, T_C = 25°C

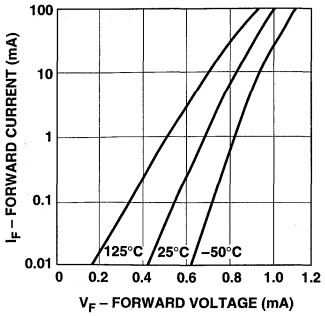


Figure 10. Forward Current vs. Forward Voltage. HSMP-381A Series.

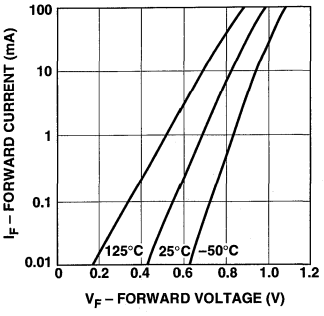


Figure 11. Forward Current vs. Forward Voltage. HSMP-386A Series.

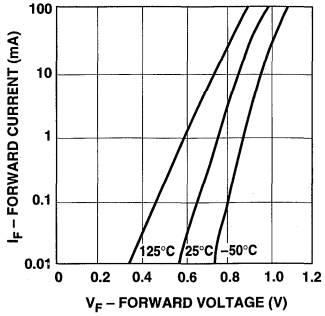


Figure 12. Forward Current vs. Forward Voltage. HSMP-389A Series.

Typical Applications for Multiple Diode Products

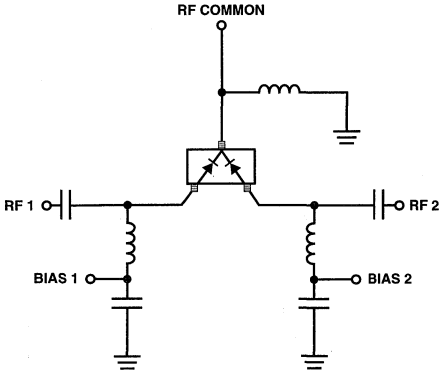


Figure 13. Simple SPDT Switch, Using Only Positive Bias Current.

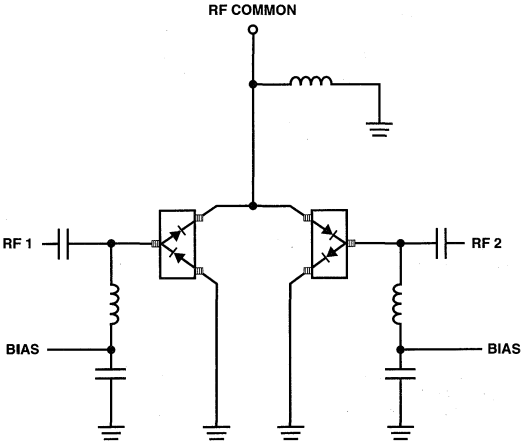


Figure 14. High Isolation SPDT Switch.

Typical Applications for Multiple Diode Products (continued)

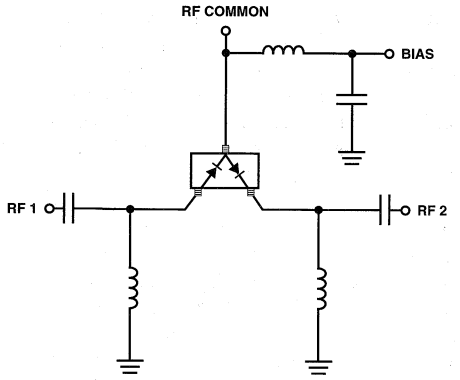


Figure 15. SPDT Switch Using Both Positive and Negative Bias Current.

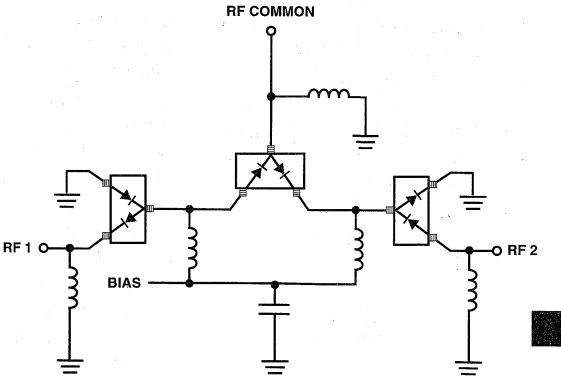


Figure 16. Very High Isolation SPDT Switch.

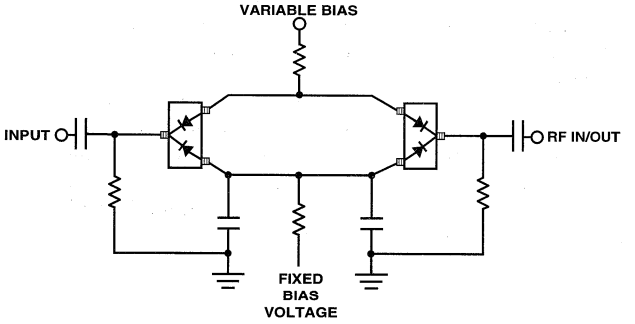


Figure 17. Four Diode π Attenuator.

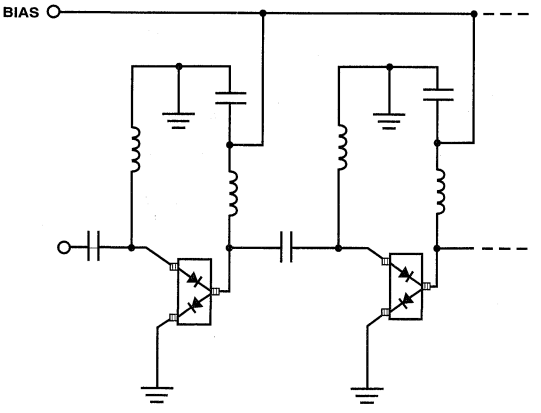


Figure 18. High Isolation SPST Switch (Repeat Cells as Required).

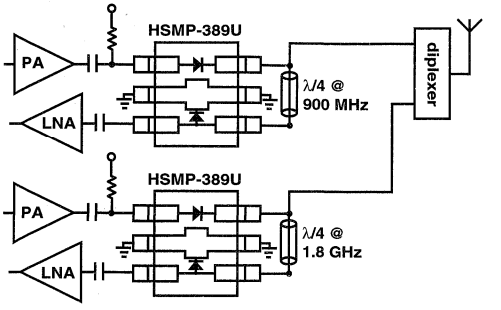


Figure 19. Dualmode 900/1800 MHz Tx/Rx Switch.

Assembly Information

SOT-323 PCB Footprint

A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 20 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair performance.

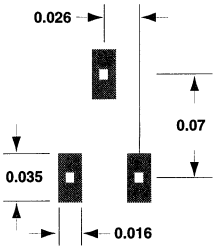


Figure 20. PCB Pad Layout (dimensions in inches).

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-323 package, will reach solder reflow temperatures faster than those with a greater mass.

HP's SOT-323 diodes have been qualified to the time-temperature profile shown in Figure 21. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235 °C.

These parameters are typical for a surface mount assembly process for HP SOT-323 diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

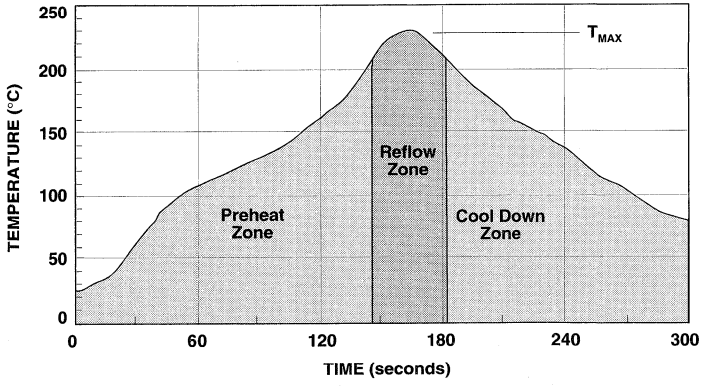
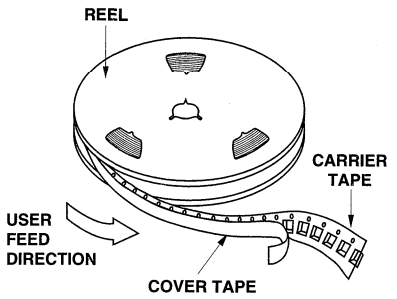
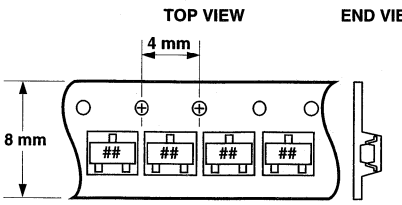


Figure 21. Surface Mount Assembly Profile.

Device Orientation

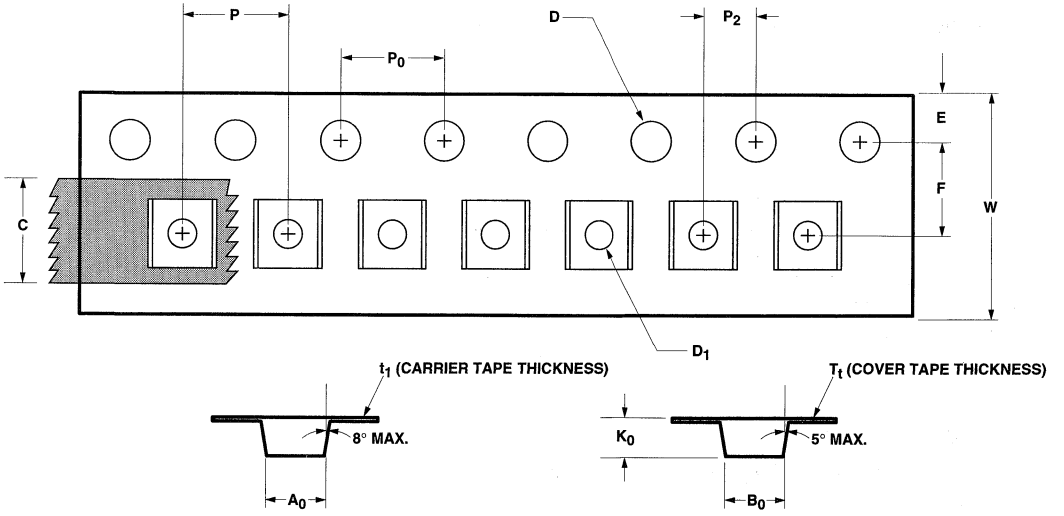




Note: "##" represents Package Marking Code.

Tape Dimensions

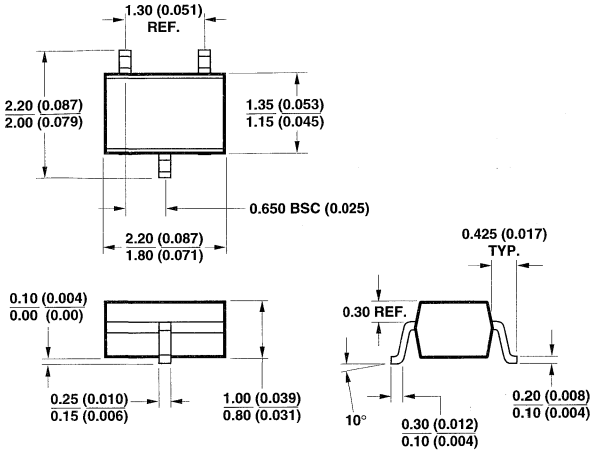
For Outline SOT-323 (SC-70 3 Lead)



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

Package Dimensions

Outline SOT-323 (SC-70)



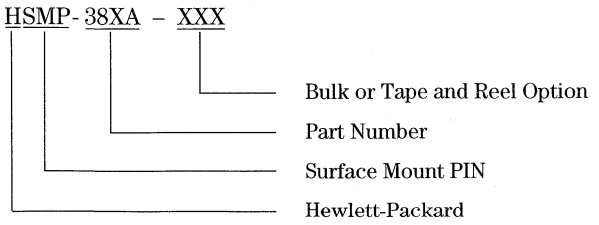
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Package Characteristics

Lead Material ..... Copper
Lead Finish ..... Tin-Lead 85/15%
Maximum Soldering Temperature ..... 260°C for 5 seconds
Minimum Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)

Ordering Information

Specify part number followed by option. For example:



Option – BLK = Bulk, 100 pcs. per antistatic bag
Option – TR1 = Tape and Reel, 3000 devices per 7" reel

Conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement." Standard Quantity is 3,000 Devices per Reel.

HEWLETT® PACKARD

Surface Mount PIN Diodes

Technical Data

HSMP-38XX and HSMP-48XX Series

Features

- **Diodes Optimized for:**
  Low Current Switching
  Low Distortion Attenuating
  Ultra-Low Distortion Switching
  Microwave Frequency Operation
- **Surface Mount SOT-23 and SOT-143 Packages**
  Single and Dual Versions
  Tape and Reel Options Available
- **Low Failure in Time (FIT) Rate[1]**

Note:
1. For more information see the Surface Mount PIN Reliability Data Sheet.

Description/Applications

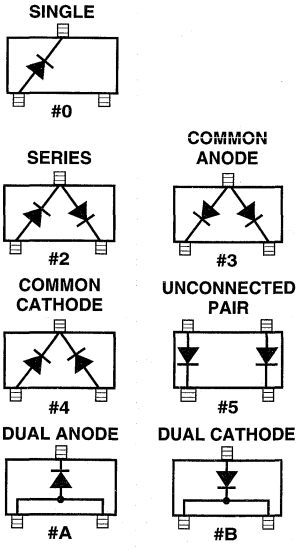
The HSMP-380X and HSMP-381X series are specifically designed for low distortion attenuator applications. The HSMP-382X series is optimized for switching applications where ultra-low resistance is required. The HSMP-3880 switching diode is an ultra low distortion device optimized for higher power applications from 50 MHz to 1.5 GHz. The HSMP-389X series is optimized for switching applications where low resistance at low current and low capacitance are required. The HSMP-48XX series are special products featuring ultra low parasitic inductance in the SOT-23 package, specifically designed for use at frequencies which are much higher than the upper limit for conventional SOT-23 PIN diodes. The HSMP-4810 diode is a low distortion attenuating PIN designed for operation to 3 GHz. The HSMP-4820 diode is ideal for limiting and low inductance switching applications up to 1.5 GHz. The HSMP-4890 is optimized for low current switching applications up to 3 GHz.

The HSMP-386X series of general purpose PIN diodes are designed for two classes of applications. The first is attenuators where current consumption is the most important design consideration. The second application for this series of diodes is in switches where low cost is the driving issue for the designer.

The HSMP-386X series Total Capacitance (C_T) and Total Resistance (R_T) are typical specifications. For applications that require guaranteed performance, the general purpose HSMP-383X series is recommended. For low distortion attenuators, the HSMP-380X or -381X series are recommended. For high performance switching applications, the HSMP-389X series is recommended.

A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

Package Lead Code Identification



Absolute Maximum Ratings[1] T_A = 25°C

Symbol	Parameter	Units	Absolute Maximum
I_f	Forward Current (1 ms Pulse)	Amp	1
P_t	Total Device Dissipation	mW[2]	250
P_{iv}	Peak Inverse Voltage	—	Same as V_{BR}
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. CW Power Dissipation at T_{LEAD} = 25°C. Derate to zero at maximum rated temperature.

PIN Attenuator Diodes
Electrical Specifications T_A = 25°C (Each Diode)

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)	Minimum High Resistance R_H (Ω)	Maximum Low Resistance R_L (Ω)
3800	D0	0	Single	3080	100	2.0	0.37	1000	8
3802	D2	2	Series						
3804	D4	4	Common Cathode						
3810	E0	0	Single	3081	100	3.0	0.35	1500	10
3812	E2	2	Series						
3813	E3	3	Common Anode						
3814	E4	4	Common Cathode						
Test Conditions					$V_R = V_{BR}$ Measure $I_R \leq 10\ \mu A$	I_F = 100 mA f = 100 MHz	V_R = 50 V f = 1 MHz	I_F = 0.01 mA f = 100 MHz	I_F = 20 mA f= 100 MHz

PIN Switching Diodes
Electrical Specifications T_A = 25°C

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)	Maximum Shunt Mode Harmonic Distortion Hmd (dBc)
3820	F0	0	Single	3188	50	0.6*	0.8*	—
3822	F2	2	Series					
3823	F3	3	Common Anode					
3824	F4	4	Common Cathode					
3880	S0	0	Single	—	100	6.5	0.40	–55
3890	G0	0	Single	—	100	2.5	0.30**	—
3892	G2	2	Series					
3893	G3	3	Common Anode					
3894	G4	4	Common Cathode					
3895	G5	5	Unconnected Pair					
Test Conditions					$V_R = V_{BR}$ Measure $I_R \leq 10\ \mu A$	I_F = 5 mA f = 100 MHz I_F = 10 mA*	V_R = 50 V f = 1 MHz V_R = 20 V* V_R = 5 V**	2 f_o, Z_o = 50 W f_o = 400 MHz P_{in} = +30 dBm 0 V bias

Note:

1. Package marking code is white.

PIN General Purpose Diodes, Electrical Specifications T_A = 25°C

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)
3830	K0	0	Single	3077	200	1.5	0.3
3832	K2	2	Series				
3833	K3	3	Common Anode				
3834	K4	4	Common Cathode				
Test Conditions					$V_R = V_{BR}$ Measure $I_R \leq 10$ mA	I_F = 100 mA f = 100 MHz	V_R = 50 V f = 1 MHz

High Frequency (Low Inductance, 500 MHz – 3 GHz) PIN Diodes, Electrical Specifications T_A = 25°C

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Typical Total Capacitance C_T (pF)	Maximum Total Capacitance C_T (pF)	Typical Total Inductance L_T (nH)	Application
4810	EB	B	Dual Cathode	100	3.0	0.35	0.4	1.0	Attenuator
4820	FA	A	Dual Anode	50	0.6*	0.75*	1.0	1.0*	Limiter
4890	GA	A	Dual Anode	100	2.5**	0.33	0.375	1.0	Switch
				$V_R = V_{BR}$ Measure $I_R \leq 10$ µA	I_F = 100 mA I_F = 10 mA* I_F = 5 mA**	V_R = 50 V f = 1 MHz V_R = 20 V*	V_R = 50 V f = 1 MHz V_R = 0 V	f = 500 MHz – 3 GHz V_R = 20 V*	

PIN General Purpose Diodes, Typical Specifications T_A = 25°C

Part Number HSMP-	Code Marking Code[1]	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Typical Series Resistance R_S (Ω)	Typical Total Capacitance C_T (pF)
3860	L0	0	Single	50	3.0/1.5*	0.20
3862	L2	2	Series			
3863	L3	3	Common Anode			
3864	L4	4	Common Cathode			
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ µA	I_F = 10 mA f = 100 MHz *I_F = 100 mA	V_R = 50 V f = 1 MHz

Typical Parameters at T_A = 25°C

Part Number HSMP-	Series Resistance R_S (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance C_T (pF)
380X	55	1800	500	0.32 @ 50 V
381X	75	1500	300	0.27 @ 50 V
382X	1.5	70*	7	0.60 @ 20 V
383X	20	500	80	0.20 @ 50 V
388X	3.8	2500	550	0.30 @ 50 V
389X	3.8	200*	–	0.20 @ 5 V
Test Conditions	I_F = 1 mA f = 100 MHz I_F = 10 mA*	I_F = 50 mA I_R = 250 mA I_F = 10 mA* I_R = 6 mA*	V_R = 10 V I_F = 20 mA 90% Recovery	

Note:
1. Package marking code is white.

Typical Parameters at T_A = 25°C (unless otherwise noted), Single Diode

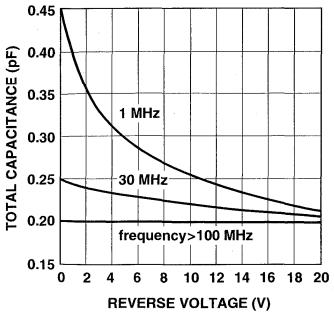


Figure 1. RF Capacitance vs. Reverse Bias, HSMP-3810 Series.

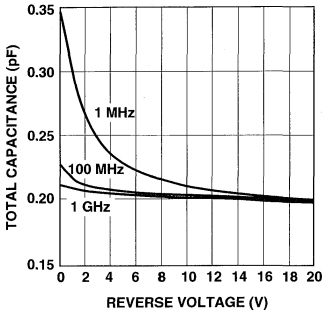


Figure 2. RF Capacitance vs. Reverse Bias, HSMP-3830 Series.

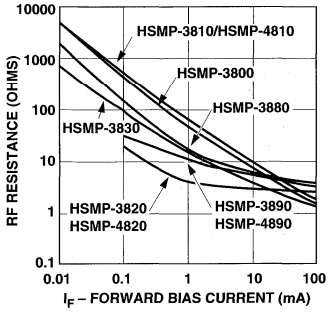


Figure 3. RF Resistance at 25°C vs. Forward Bias Current.

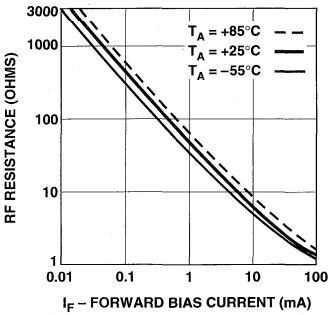


Figure 4. RF Resistance vs. Forward Bias Current for HSMP-3800.

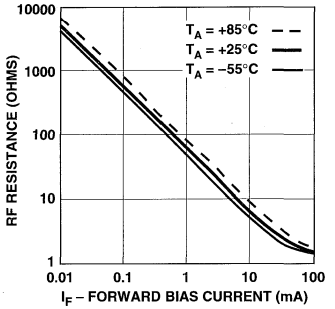


Figure 5. RF Resistance vs. Forward Bias Current for HSMP-3810/ HSMP-4810.

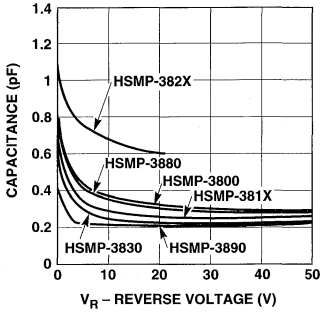


Figure 6. Capacitance vs. Reverse Voltage.

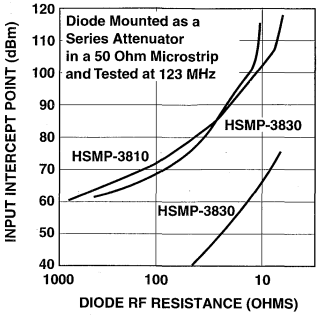


Figure 7. 2nd Harmonic Input Intercept Point vs. Diode RF Resistance for Attenuator Diodes.

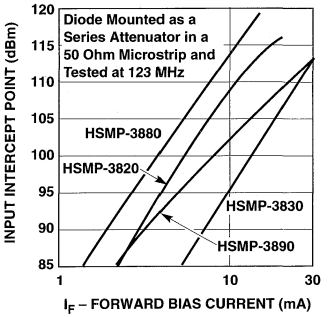


Figure 8. 2nd Harmonic Input Intercept Point vs. Forward Bias Current for Switch Diodes.

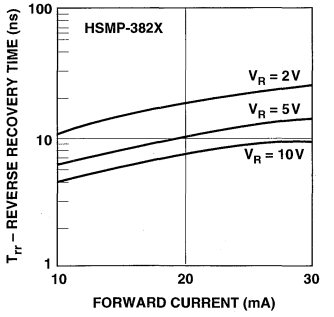


Figure 9. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages. HSMP-3820 Series.

Typical Parameters (continued)

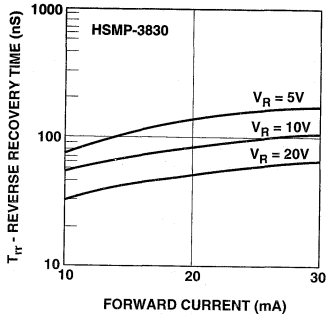


Figure 10. Reverse Recovery Time vs. Forward Current for Various Reverse Voltage. HSMP-3830 Series.

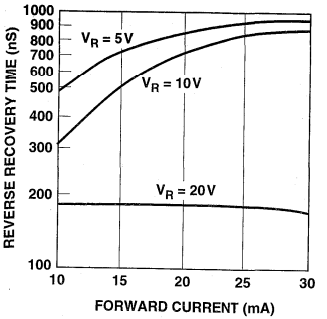


Figure 11. Typical Reverse Recovery Time vs. Reverse Voltage. HSMP-3880 Series.

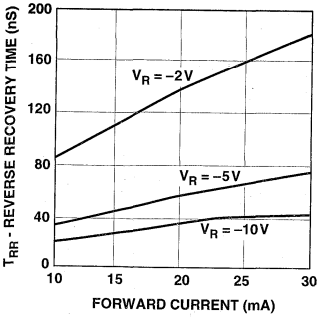


Figure 12. Typical Reverse Recovery Time vs. Reverse Voltage. HSMP-3890 Series.

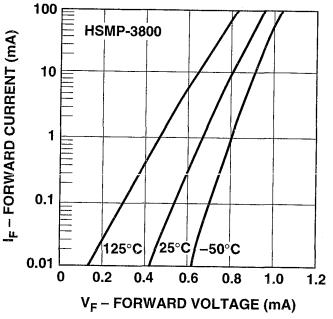


Figure 13. Forward Current vs. Forward Voltage. HSMP-3800 Series.

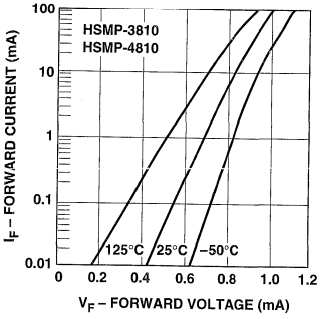


Figure 14. Forward Current vs. Forward Voltage. HSMP-3810 and HSMP-4810 Series.

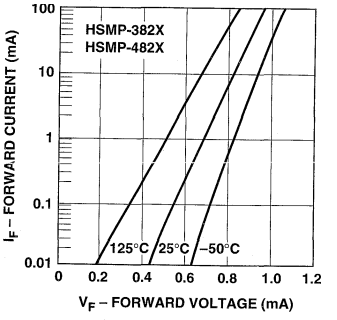


Figure 15. Forward Current vs. Forward Voltage. HSMP-3820 and HSMP-4820 Series.

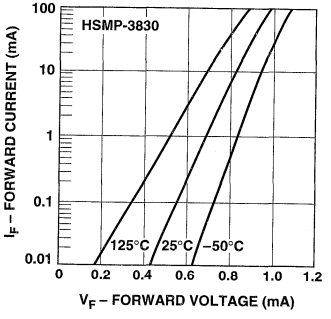


Figure 16. Forward Current vs. Forward Voltage. HSMP-3830 Series.

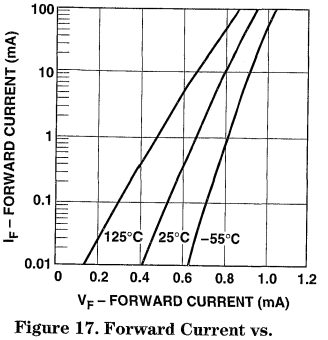


Figure 17. Forward Current vs. Forward Voltage. HSMP-3880 Series.

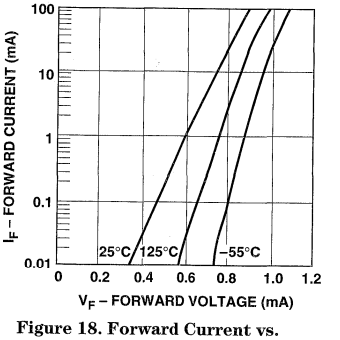


Figure 18. Forward Current vs. Forward Voltage. HSMP-3890 and HSMP-4890 Series.

Typical Parameters (continued)

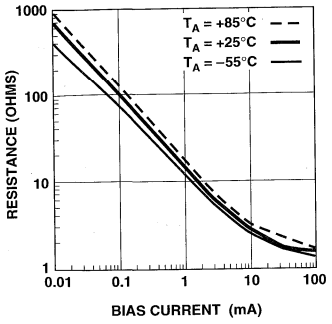


Figure 19. Typical RF Resistance vs. Forward Bias Current for HSMP-3860.

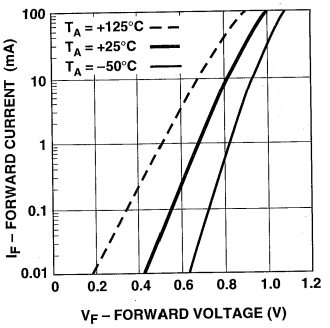


Figure 20. Forward Current vs. Forward Voltage for HSMP-3860.

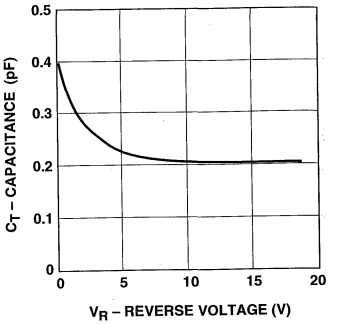
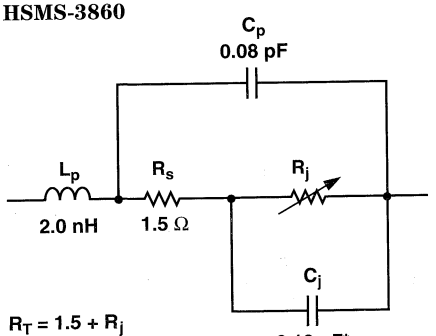


Figure 21. Typical Capacitance vs. Reverse Bias for HSMP-3860.

Equivalent Circuit Model

HSMS-3860



$R_T = 1.5 + R_j$

$C_T = C_P + C_j$

$R_j = \frac{12}{I^{0.9}}\ \Omega$

I = Forward Bias Current in mA

Typical Applications for Multiple Diode Products

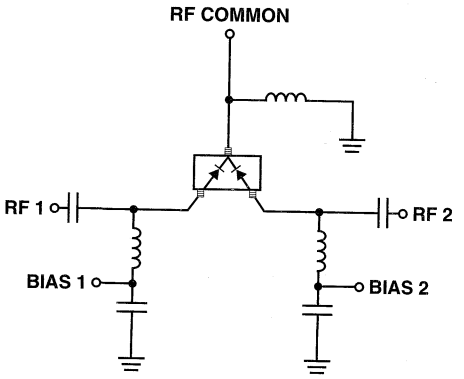


Figure 22. Simple SPDT Switch, Using Only Positive Current.

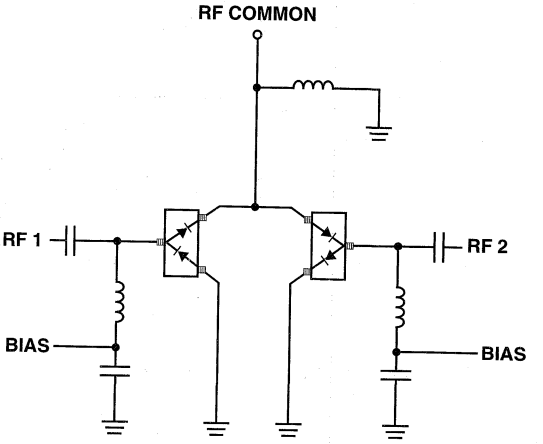


Figure 23. High Isolation SPDT Switch, Dual Bias.

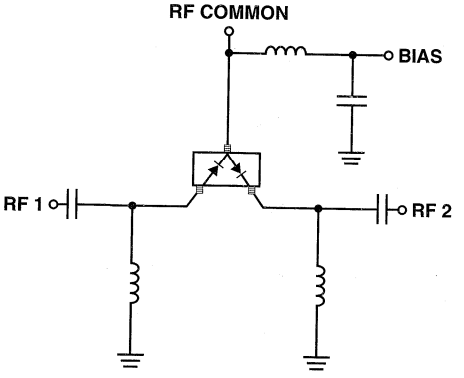


Figure 24. Switch Using Both Positive and Negative Bias Current.

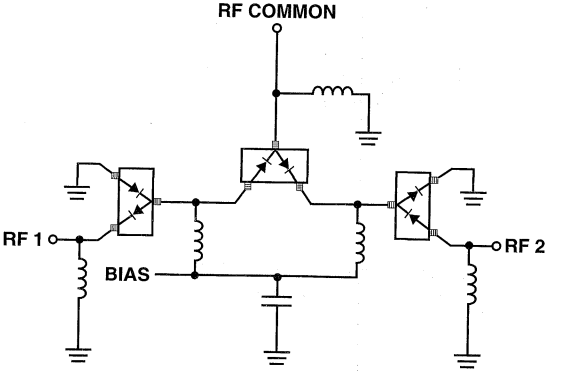


Figure 25. Very High Isolation SPDT Switch, Dual Bias.

Typical Applications for Multiple Diode Products (continued)

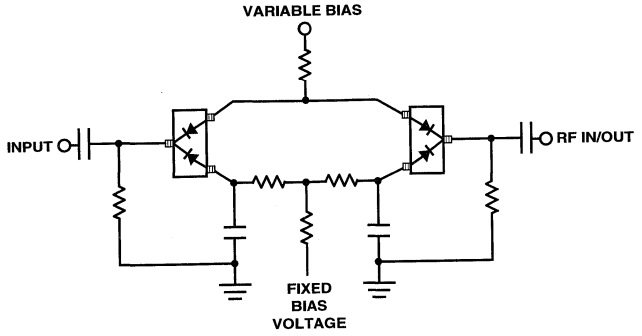


Figure 26. Four Diode π Attenuator.

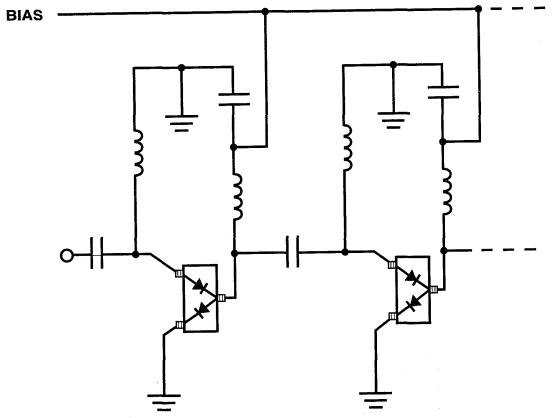


Figure 27. High Isolation SPST Switch (Repeat Cells as Required).

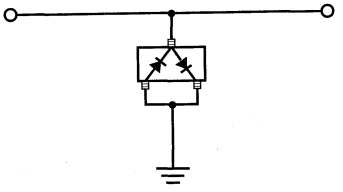
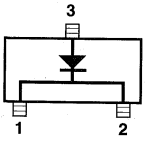
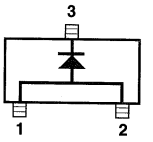


Figure 28. Power Limiter Using HSMP-3822 Diode Pair.

Typical Applications for HSMP-48XX Low Inductance Series

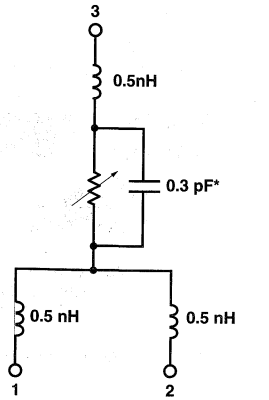


HSMP-4810



HSMP-4820 & HSMP-4890

Figure 29. Internal Connections.



*0.8pF TYPICAL FOR HSMP-3820

Figure 30. Equivalent Circuit.

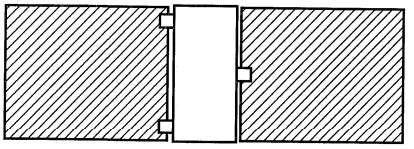
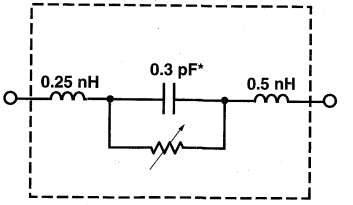


Figure 31. Circuit Layout.



*0.8 pF TYPICAL FOR HSMP-3820

Figure 32. Equivalent Circuit.

Microstrip Series Connection for HSMP-48XX Series

In order to take full advantage of the low inductance of the HSMP-48XX series when using them in series application, both lead 1 and lead 2 should be connected together, as shown above.

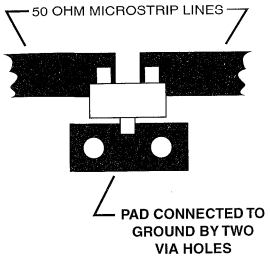


Figure 33. Circuit Layout.

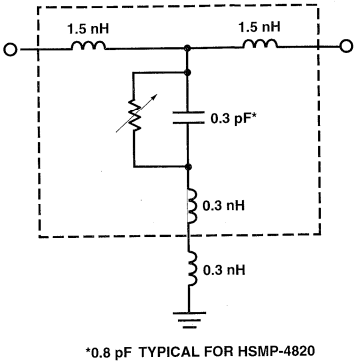


Figure 34. Equivalent Circuit.

Microstrip Shunt Connections for HSMP-48XX Series

In the diagram above, the center conductor of the microstrip line is interrupted and leads 1 and 2 of the HSMP-38XX series diode are placed across the resulting gap. This forces the 0.5 nH lead inductance of leads 1 and 2 to appear as part of a low pass filter, reducing the shunt parasitic inductance and increasing the maximum available attenuation. The 0.3 nH of shunt inductance external to the diode is created by the via holes, and is a good estimate for 0.032" thick material.

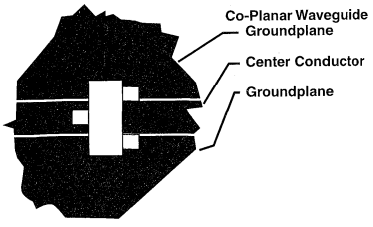


Figure 35. Circuit Layout.

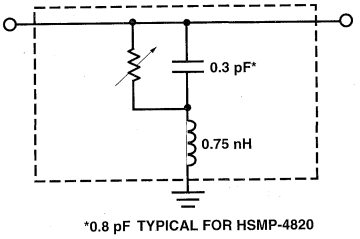


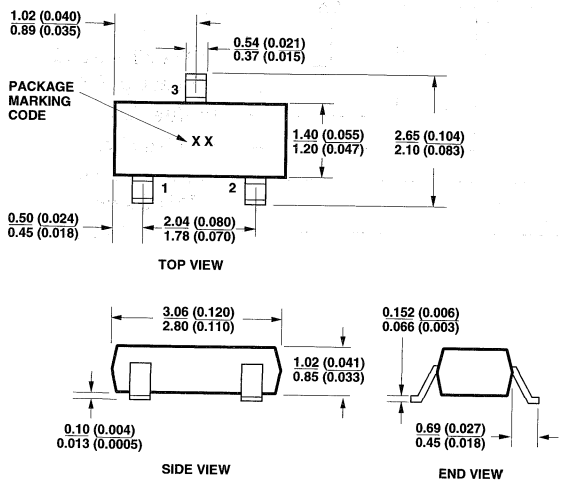
Figure 36. Equivalent Circuit.

Co-Planar Waveguide Shunt Connection for HSMP-48XX Series

Co-Planar waveguide, with ground on the top side of the printed circuit board, is shown in the diagram above. Since it eliminates the need for via holes to ground, it offers lower shunt parasitic inductance and higher maximum attenuation when compared to a microstrip circuit.

Package Dimensions

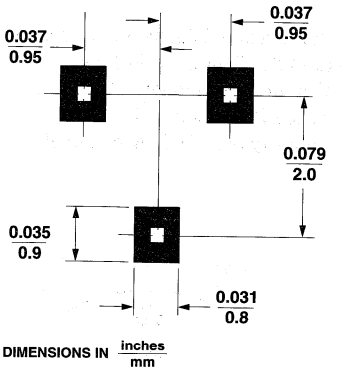
Outline 23 (SOT-23)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

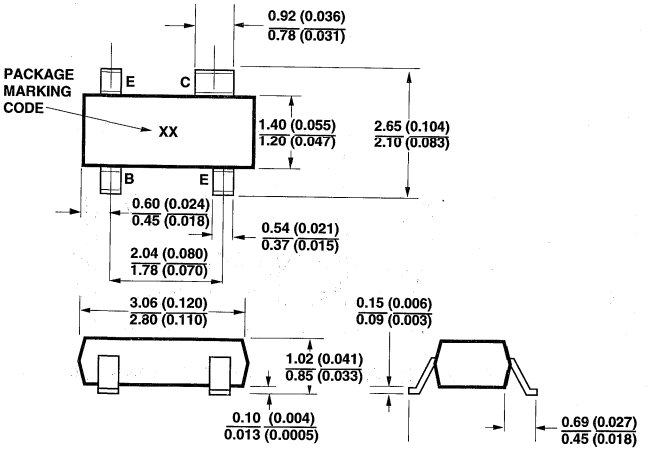
PC Board Footprints

SOT-23



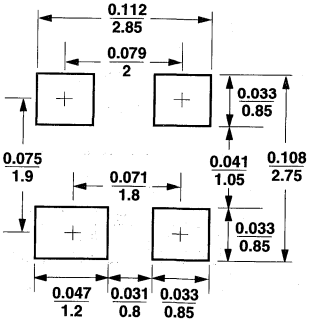
DIMENSIONS IN inches / mm

Outline 143 (SOT-143)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

SOT-143



DIMENSIONS IN inches / mm

Package Characteristics

Lead Material	Alloy 42
Lead Finish	Tin-Lead 85-15%
Maximum Soldering Temperature	260°C for 5 seconds
Minimum Lead Strength	2 pounds pull
Typical Package Inductance	2 nH
Typical Package Capacitance	0.08 pF (opposite leads)

Ordering Information

Option L30 = Bulk
Option L31 = Tape and Reel,
See Figures 37 and 38

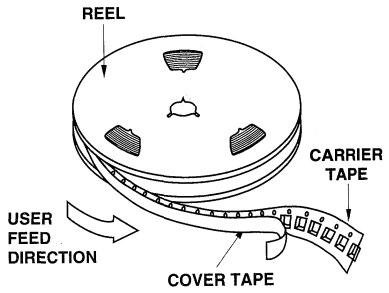
Conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement." Standard Quantity is 3,000 Devices/Reel.

Ordering Information

Specify part number followed by option under. For example:

H SMP - 38XX #L XX

- XX: Bulk or Tape and Reel Option
- #L: Profile: Low
- 38XX: Part Number
- SMP: Surface Mount PIN Diode
- H: Hewlett-Packard



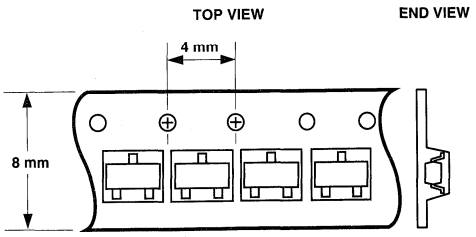


Figure 37. Option L31 for SOT-23 Packages.

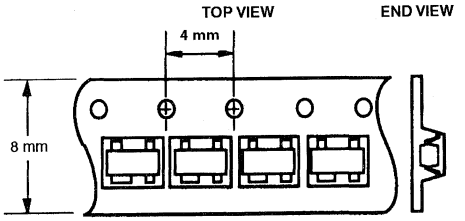


Figure 38. Option L31 for SOT-143 Packages.

HEWLETT® PACKARD

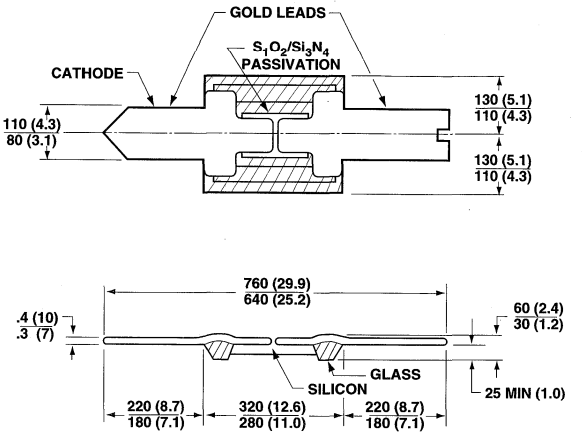
Beam Lead PIN Diode

Technical Data

HPND-4005

Features

- **High Breakdown Voltage 120 V Typical**
- **Low Capacitance 0.017 pF Typical**
- **Low Resistance 4.7 Ω Typical**
- **Rugged Construction 4 Grams Minimum Lead Pull**
- **Nitride Passivated**



DIMENSIONS IN μm (1/1000 inch)

Outline 21

Description

The HPND-4005 planar beam lead PIN diode is constructed to offer exceptional lead strength while achieving excellent electrical performance at high frequencies. High beam strength offers users superior assembly yield, while extremely low capacitance allows high isolation to be realized.

Nitride passivation and polyimide coating provide reliable device protection.

Applications

The HPND-4005 beam lead PIN diode is designed for use in stripline or microstrip circuits. Applications include switching, attenuating, phase shifting, limiting, and modulating at microwave frequencies. The extremely low capacitance of the HPND-4005 makes it ideal for circuits requiring high isolation in a series diode configuration.

Maximum Ratings

Operating Temperature ..... -65°C to +175°C
Storage Temperature ..... -65°C to +200°C
Power Dissipation at T_{CASE} = 25°C ..... 250 mW
(Derate linearly to zero at 175°C.)
Minimum Lead Strength ..... 4 grams pull on either lead
Diode Mounting Temperature ..... 220°C for 10 sec. max.

Electrical Specifications at T_A = 25°C

Part Number HPND-	Breakdown Voltage V_{BR} (V)		Series Resistance R_S (Ω)[2]		Capacitance C_T (pF)[1,2]		Forward Voltage V_F (V)	Reverse Current I_R (nA)	Minority Carrier Lifetime τ (ns)[2]	
	Min.	Typ.	Typ.	Max.	Typ.	Max.	Max.	Max.	Min.	Typ.
4005	100	120	4.7	6.5	0.017	0.02	1.0	100	50	100
Test Conditions	I_R = 10 mA		I_F = 20 mA I_F = 100 MHz		V_R = 10 V f = 10 GHz		I_F = 20 mA	V_R = 30 V	I_F = 10 mA I_R = 6 mA	

Notes:
1. Total capacitance calculated from measured isolation value in a series configuration.
2. Test performed on packaged samples.

Typical Parameters

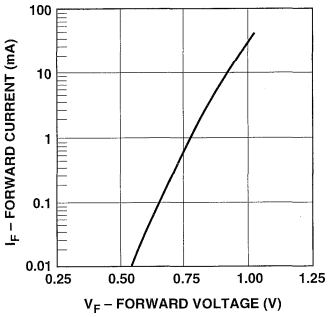


Figure 1. Typical Forward Conduction Characteristics.

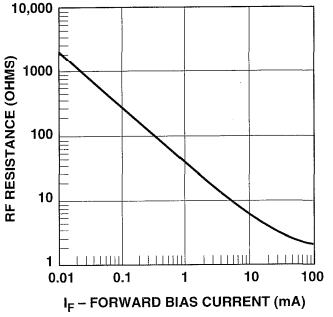


Figure 2. Typical RF Resistance vs. Forward Bias Current.

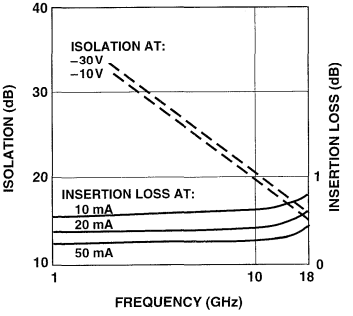


Figure 3. Typical Isolation and Insertion Loss in the Series Configuration (Z_O = 50 Ω).

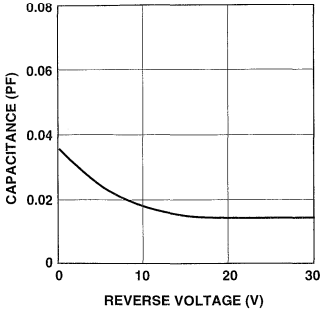


Figure 4. Typical Capacitance at 10 GHz vs. Reverse Bias.

Bonding and Handling Procedures for Beam Lead Diodes

1. Storage

Under normal circumstances, storage of beam lead diodes in HP supplied waffle/gel packs is sufficient. In particularly dusty or chemically hazardous environments, storage in an inert atmosphere desiccator is advised.

2. Handling

In order to avoid damage to beam lead devices, particular care must be exercised during inspection, testing, and assembly. Although the beam lead diode is designed to have exceptional lead strength, its small size and delicate nature requires that special handling techniques be observed so that the devices will not be mechanically or electrically damaged. A vacuum pickup is recommended for picking up beam lead devices, particularly larger ones, e.g., quads. Care must be exercised to assure that the vacuum opening of the needle is sufficiently small to avoid passage of the device through the opening. A #27 tip is recommended for picking up single beam lead devices. A 20X magnification is needed for precise positioning of the tip on the device. Where a vacuum pickup is not used, a sharpened wooden Q-tip dipped in isopropyl alcohol is very commonly used to handle beam lead devices.

3. Cleaning

For organic contamination use a warm rinse of trichloroethane, or its locally approved equivalent, followed by a cold rinse in acetone and methanol. Dry under infrared heat lamp for 5–10 minutes on clean filter paper. Freon degreaser, or its locally approved equivalent, may replace trichloroethane for light organic contamination.

- Ultrasonic cleaning is not recommended.
- Acid solvents should not be used.

4. Bonding

Thermocompression: See Application Note 979 "The Handling and Bonding of Beam Lead Devices Made Easy". This method is good for hard substrates only.

Wobble: This method picks up the device, places it on the substrate and forms a thermocompression bond all in one operation. This is described in the latest version of MIL-STD-883, Method 2017, and is intended for hard substrates only.

Resistance Welding or Parallel-GAP Welding: To make welding on soft substrates easier, a low pressure welding head is recommended. Suitable equipment is available from HUGHES, Industrial Products Division in Carlsbad, CA.

Epoxy: With solvent free, low resistivity epoxies (available from ABLESTIK and improvements in dispensing equipment, the quality of epoxy bonds is sufficient for many applications.

5. Lead Stress

In the process of bonding a beam lead diode, a certain amount of "bugging" occurs. The term *bugging* refers to the chip lifting away from the substrate during the bonding process due to the deformation of the beam by the bonding tool. This effect is beneficial as it provides stress relief for the diode during thermal cycling of the substrate. The coefficient of expansion of some substrate materials, specifically soft substrates, is such that some bugging is essential if the circuit is to be operated over wide temperature extremes.

Thick metal clad ground planes restrict the thermal expansion of the dielectric substrates in the X-Y axis. The expansion of the dielectric will then be mainly in the Z axis, which does not affect the beam lead device. An alternate solution to the problem of dielectric ground plane expansion is to heat the substrate to the maximum required operating temperature during the beam lead attachment. Thus, the substrate is at maximum expansion when the device is bonded. Subsequent cooling of the substrate will cause bugging, similar to bugging in thermocompression bonding or epoxy bonding. Other methods of bugging are preforming the leads during assembly or prestressing the substrate.

HEWLETT® PACKARD

Beam Lead PIN Diodes for Phased Arrays and Switches

Technical Data

HPND-4018
HPND-4028
HPND-4038

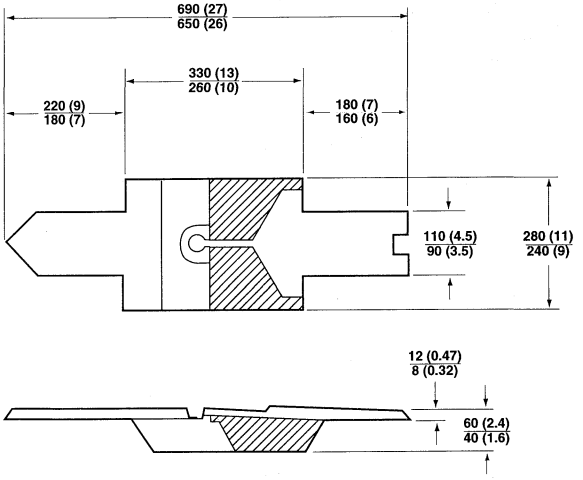
Features

- **Low Capacitance**
  0.025 pF Maximum at 1 MHz
  Guaranteed Min./Max.
- **Fast Switching**
  2.0 nsec
- **Low Resistance at Low Bias**
  1.5 Ω at I_F = 10 mA (Typical)
- **Rugged Construction**
  Typical 10 Gram Lead Pull
- **Silicon Nitride Passivation**

Description

The HPND-4018, 4028, and 4038 beam lead PIN diodes are designed for low capacitance, low resistance, and fast switching at microwave frequencies. These characteristics are achieved at low bias levels for minimal power consumption. Advanced processing techniques ensure uniform and consistent electrical performance, allowing guaranteed capacitance windows. This translates to improved performance in phased array applications.

Rugged construction and strong beams ensure high assembly yields while nitride passivation and polyimide coating ensure reliability. Standard Hi-Rel programs are available for all three devices.



Outline 83

Maximum Ratings

Operating Temperature ..... -65°C to +150°C
Storage Temperature ..... -65°C to +200°C
Power Dissipation at T_{CASE} = 25°C ..... 250 mW
(Derate linearly to zero at 150°C.)
Minimum Lead Strength ..... 4 grams pull on either lead per MIL-S-19500, LTPD = 20

Applications

These beam lead PIN diodes are designed for use in stripline, coplanar waveguide, or microstrip circuits. Applications include phase shifting and switching. The guaranteed capacitance windows ensure uniform performance in phased array radar. The low capacitance makes them ideal for circuits requiring high isolation in the series configuration. These devices have been fully characterized and S-parameters have been provided.

Electrical Specifications at T_A = 25°C

Part Number HPND-	Capacitance (pF)		Series Resistance R_S (Ω)		Breakdown Voltage V_{BR} (V)	Reverse Current I_R (nA)	Forward Voltage V_F (V)	Carrier Lifetime τ (ns)	Reverse Recovery t_{rr} (ns)	Series Resistance R_S (Ω)
	Min.	Max.	Typ.	Max.	Min.	Max.	Max.	Typ.	Typ.	Typ.
4018	0.015	0.025	4.0	4.6	60	100	1.1	26	2.0*	2.5
4028	0.025	0.045	2.3	3.0	60	100	1.1	36	2.6	2.0
4038	0.045	0.065	1.5	2.0	60	100	1.1	45	2.4	1.0
Test Conditions	V_R = 30 V f = 1 MHz		I_F = 10 mA f = 100 MHz		$V_R = V_{BR}$ Measure $I_R \leq 10$ mA	V_R = 50 V	I_F = 20 mA	I_F = 10 mA I_R = 6 mA	*I_F = 10 mA I_F = 5 mA V_R = 10 V 90% recovery	I_F = 50 mA f = 100 MHz

Typical Parameters

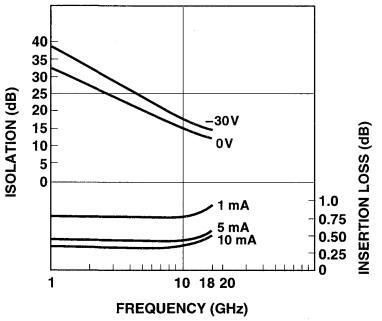


Figure 1. Typical Isolation and Insertion Loss, HPND-4018.

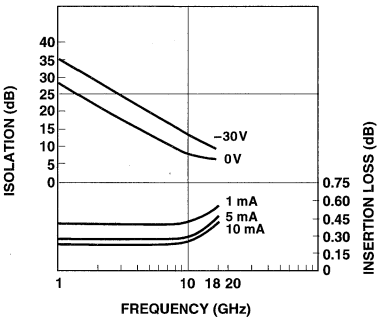


Figure 2. Typical Isolation and Insertion Loss, HPND-4028.

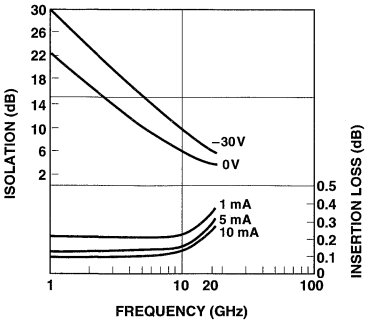


Figure 3. Typical Isolation and Insertion Loss, HPND-4038.

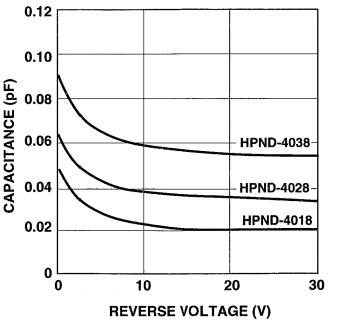


Figure 4. Typical Capacitance vs. Reverse Voltage (at 1 MHz).

Typical Parameters (cont.)

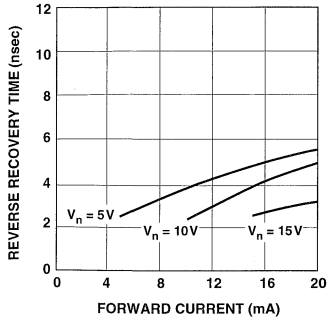


Figure 5. Typical Reverse Recovery Time vs. Forward Current (Series Configuration). HPND-4018.

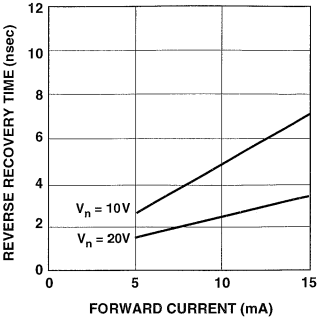


Figure 6. Typical Reverse Recovery Time vs. Forward Current (Series Configuration). HPND-4028, HPND-4038.

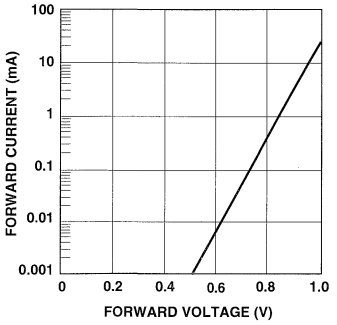


Figure 7. Typical Forward Characteristics.

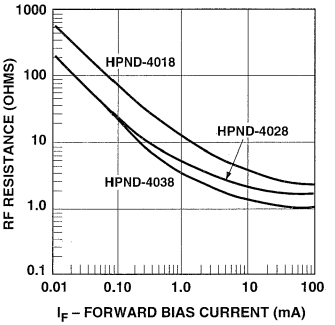


Figure 8. Typical RF Resistance vs. Forward Bias Current (at 100 MHz).

Typical S-Parameters (in series configuration) at Z_O = 50 Ω, 25°C
HPND-4018

Freq.	I_F = 1 mA					I_F = 5 mA					I_F = 10 mA				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
(MHz)	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.086	-1	-0.76	0.917	-1	0.046	8	-0.38	0.958	-1	0.037	11	-0.30	0.967	-1
2000	0.085	5	-0.76	0.917	-2	0.047	17	-0.40	0.957	-2	0.040	23	-0.32	0.965	-2
3000	0.085	10	-0.76	0.918	-4	0.051	25	-0.40	0.957	-4	0.043	32	-0.32	0.966	-4
4000	0.088	14	-0.74	0.919	-5	0.056	31	-0.40	0.957	-5	0.049	38	-0.32	0.966	-5
5000	0.090	18	-0.76	0.918	-6	0.060	36	-0.40	0.956	-6	0055	43	-0.32	0.965	-6
6000	0.093	20	-0.76	0.918	-7	0.066	39	-0.40	0.956	-7	0.061	46	-0.32	0.965	-7
7000	0.096	22	-0.76	0.918	-8	0.071	42	-0.40	0.957	-8	0.066	48	-0.32	0.965	-8
8000	0.100	24	-0.76	0.918	-10	0.076	43	-0.40	0.955	-10	0.072	50	-0.32	0.965	-10
9000	0.103	26	-0.76	0.918	-11	0.081	45	-0.40	0.955	-11	0.078	51	-0.32	0.965	-11
10000	0.106	27	-0.76	0.918	-12	0.086	46	-0.40	0.955	-12	0.083	51	-0.32	0.964	-12
11000	0.109	28	-0.74	0.919	-13	0.090	47	-0.40	0.956	-13	0.087	52	-0.32	0.965	-13
12000	0.114	28	-0.76	0.918	-14	0.096	46	-0.40	0.956	-14	0.093	52	-0.32	0.965	-15
13000	0.117	29	-0.76	0.917	-16	0.100	47	-0.40	0.956	-16	0.097	52	-0.32	0.965	-16
14000	0.121	30	-0.78	0.916	-17	0.105	48	-0.42	0.953	-17	0.103	53	-0.34	0.962	-17
15000	0.125	30	-0.80	0.913	-18	0.111	48	-0.42	0.953	-18	0.109	53	-0.34	0.963	-18
16000	0.129	31	-0.80	0.914	-19	0.116	49	-0.42	0.953	-19	0.114	53	-0.34	0.962	-19
17000	0.134	31	-0.80	0.914	-21	0.122	48	-0.44	0.952	-21	0.120	53	-0.36	0.961	-21
18000	0.140	32	-0.84	0.909	-22	0.130	49	-0.46	0.950	-22	0.129	53	-0.36	0.960	-22

HPND-4018

Freq.	V_R = 0 V					V_R = 10 V					V_R = 30 V				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
(MHz)	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.995	-3	-33.16	0.022	84	0.999	-2	-39.18	0.011	93	1.000	-2	-39.18	0.011	93
2000	0.990	-5	-27.54	0.042	76	0.998	-4	-32.78	0.023	85	0.998	-4	-33.16	0.022	87
3000	0.983	-7	-24.30	0.061	71	0.996	-6	-29.12	0.035	83	0.997	-6	-29.64	0.033	84
4000	0.975	-10	-22.28	0.077	68	0.993	-8	-26.76	0.046	81	0.995	-8	-27.14	0.044	82
5000	0.967	-12	-20.74	0.092	64	0.991	-10	-24.90	0.057	78	0.992	-10	-25.36	0.054	79
6000	0.959	-14	-19.50	0.106	62	0.987	-12	-23.24	0.069	76	0.988	-12	-23.76	0.065	77
7000	0.950	-16	-18.42	0.120	59	0.982	-14	-21.84	0.081	73	0.985	-14	-22.28	0.077	74
8000	0.942	-18	-17.60	0.132	57	0.979	-16	-20.74	0.092	71	0.982	-16	-21.22	0.087	72
9000	0.933	-21	-16.84	0.144	54	0.972	-18	-19.84	0.102	68	0.975	-18	-20.28	0.097	69
10000	0.924	-23	-16.32	0.153	52	0.966	-20	-19.10	0.111	67	0.969	-20	-19.50	0.106	68
11000	0.915	-25	-15.56	0.167	49	0.959	-23	-18.14	0.124	63	0.960	-22	-18.58	0.118	64
12000	0.904	-27	-15.00	0.178	48	0.951	-25	-17.40	0.135	62	0.953	-24	-17.80	0.129	63
13000	0.896	-29	-14.66	0.185	45	0.944	-27	-16.96	0.142	59	0.946	-26	-17.34	0.136	60
14000	0.886	-31	-14.04	0.199	43	0.936	-29	-16.20	0.155	55	0.940	-29	-16.60	0.148	56
15000	0.876	-33	-13.86	0.203	41	0.925	-31	-15.92	0.160	53	0.929	-31	-16.26	0.154	54
16000	0.870	-35	-13.44	0.213	37	0.920	-33	-15.46	0.169	48	0.924	-32	-15.82	0.162	49
17000	0.865	-36	-13.36	0.215	35	0.913	-34	-15.36	0.171	45	0.917	-34	-15.76	0.163	46
18000	0.859	-38	-13.44	0.213	32	0.907	-36	-15.50	0.168	41	0.911	-36	-15.92	0.160	42

Typical S-Parameters (cont.)
HPND-4028

Freq. (MHz)	I_F = 1 mA					I_F = 5 mA					I_F = 10 mA				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.046	7	-0.38	0.958	-1	0.031	17	-0.24	0.973	-1	0.027	19	-0.20	0.978	-1
2000	0.048	20	-0.40	0.956	-2	0.036	33	-0.26	0.971	-2	0.033	37	-0.22	0.975	-2
3000	0.052	29	-0.40	0.957	-4	0.041	43	-0.26	0.972	-4	0.040	47	-0.22	0.975	-4
4000	0.058	36	-0.40	0.957	-5	0.049	49	-0.26	0.971	-5	0.047	53	-0.22	0.975	-5
5000	0.063	42	-0.40	0.956	-6	0.057	54	-0.26	0.971	-6	0.055	58	-0.22	0.975	-6
6000	0.069	46	-0.40	0.956	-7	0.064	57	-0.26	0.971	-7	0.063	60	-0.24	0.974	-7
7000	0.075	48	-0.40	0.956	-8	0.070	60	-0.26	0.971	-8	0.070	62	-0.22	0.975	-8
8000	0.081	50	-0.40	0.955	-9	0.077	60	-0.28	0.970	-9	0.076	63	-0.24	0.974	-9
9000	0.087	51	-0.40	0.956	-11	0.084	61	-0.28	0.970	-11	0.083	63	-0.24	0.974	-11
10000	0.092	52	-0.40	0.956	-12	0.089	61	-0.28	0.970	-12	0.089	63	-0.24	0.974	-12
11000	0.097	53	-0.40	0.956	-13	0.095	61	-0.26	0.971	-13	0.095	63	-0.22	0.975	-13
12000	0.103	52	-0.40	0.956	-14	0.101	60	-0.26	0.971	-14	0.101	62	-0.22	0.975	-14
13000	0.107	51	-0.40	0.957	-15	0.106	59	-0.26	0.971	-15	0.105	62	-0.22	0.975	-15
14000	0.112	51	-0.42	0.954	-17	0.110	59	-0.30	0.968	-17	0.111	61	-0.24	0.973	-17
15000	0.119	51	-0.42	0.953	-18	0.117	58	-0.28	0.969	-18	0.117	60	-0.26	0.972	-18
16000	0.123	51	-0.44	0.952	-19	0.122	57	-0.28	0.969	-19	0.123	60	-0.26	0.972	-19
17000	0.129	49	-0.44	0.952	-20	0.130	56	-0.30	0.967	-20	0.129	57	-0.26	0.971	-20
18000	0.139	48	-0.46	0.950	-22	0.139	55	-0.32	0.965	-21	0.140	56	-0.28	0.970	-22

HPND-4028

Freq. (MHz)	V_R = 0 V					V_R = 10 V					V_R = 30 V				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.997	-4	-27.54	0.042	86	0.999	-3	-33.16	0.022	91	1.000	-2	-33.98	0.020	91
2000	0.988	-7	-21.74	0.082	79	0.997	-6	-27.34	0.043	86	0.998	-5	-28.18	0.039	86
3000	0.974	-11	-18.36	0.121	74	0.994	-8	-23.62	0.066	83	0.996	-7	-24.44	0.060	84
4000	0.958	-14	-16.10	0.157	69	0.991	-10	-21.12	0.088	81	0.992	-10	-21.94	0.080	82
5000	0.940	-17	-14.48	0.189	64	0.986	-13	-19.26	0.109	78	0.987	-13	-20.10	0.099	79
6000	0.921	-21	-13.20	0.219	70	0.979	-16	-17.66	0.131	75	0.982	-15	-18.42	0.120	76
7000	0.898	-24	-12.16	0.247	56	0.972	-19	-16.26	0.054	72	0.976	-18	-17.08	0.140	73
8000	0.879	-26	-11.36	0.271	52	0.965	-21	-15.20	0.174	70	0.970	-21	-15.92	0.160	71
9000	0.857	-29	-10.64	0.294	48	0.954	-24	-14.20	0.195	67	0.960	-23	-14.96	0.179	68
10000	0.836	-32	-10.12	0.312	46	0.942	-27	-13.44	0.213	65	0.950	-26	-14.20	0.195	66
11000	0.816	-35	-9.54	0.334	42	0.931	-30	-12.58	0.235	61	0.937	-29	-13.32	0.216	62
12000	0.795	-37	-9.10	0.351	40	0.917	-33	-11.84	0.256	59	0.926	-32	-12.62	0.234	60
13000	0.778	-40	-8.86	0.361	37	0.904	-36	-11.44	0.268	56	0.913	-34	-12.20	0.246	57
14000	0.761	-42	-8.44	0.379	33	0.892	-38	-10.80	0.289	52	0.903	-37	-11.52	0.266	54
15000	0.744	-44	-8.34	0.383	31	0.876	-41	-10.56	0.297	50	0.888	-39	-11.26	0.274	52
16000	0.733	-46	-8.04	0.397	28	0.867	-43	-10.12	0.312	46	0.881	-42	-10.80	0.289	48
17000	0.720	-48	-7.94	0.401	26	0.855	-45	-9.96	0.318	44	0.869	-44	-10.64	0.294	46
18000	0.709	-50	-8.00	0.399	24	0.846	-47	-9.94	0.319	42	0.861	-46	-10.64	0.294	44

Typical S-Parameters (cont.)
HPND-4038

Freq.	I_F = 1 mA					I_F = 5 mA					I_F = 10 mA				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
(MHz)	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.028	15	-0.22	0.976	-1	0.019	28	-0.12	0.987	-1	0.017	35	-0.10	0.989	-1
2000	0.032	34	-0.24	0.974	-2	0.026	50	-0.16	0.984	-2	0.024	56	-0.14	0.986	-2
3000	0.037	47	-0.22	0.975	-3	0.034	61	-0.14	0.985	-3	0.033	66	-0.12	0.988	-4
4000	0.045	55	-0.22	0.975	-5	0.042	67	-0.14	0.985	-5	0.042	70	-0.12	0.987	-5
5000	0.052	61	-0.24	0.974	-6	0.051	72	-0.16	0.984	-6	0.051	75	-0.14	0.986	-6
6000	0.060	65	-0.24	0.974	-7	0.059	74	-0.16	0.984	-7	0.059	77	-0.14	0.986	-7
7000	0.067	67	-0.24	0.974	-8	0.067	76	-0.16	0.984	-8	0.067	78	-0.12	0.987	-8
8000	0.073	69	-0.24	0.974	-9	0.074	76	-0.16	0.983	-9	0.073	78	-0.14	0.986	-9
9000	0.081	70	-0.24	0.973	-10	0.081	77	-0.16	0.984	-10	0.081	78	-0.14	0.986	-10
10000	0.087	71	-0.24	0.974	-11	0.088	77	-0.16	0.982	-11	0.089	79	-0.14	0.986	-11
11000	0.092	71	-0.22	0.975	-12	0.094	77	-0.16	0.984	-12	0.094	79	-0.14	0.986	-12
12000	0.099	70	-0.24	0.974	-14	0.100	76	-0.16	0.984	-14	0.101	77	-0.14	0.986	-14
13000	0.104	70	-0.22	0.975	-15	0.106	75	-0.14	0.985	-15	0.107	76	-0.12	0.987	-15
14000	0.110	69	-0.26	0.972	-16	0.112	74	-0.16	0.982	-16	0.113	75	-0.16	0.984	-16
15000	0.118	67	-0.24	0.973	-17	0.119	72	-0.16	0.983	-17	0.120	73	-0.14	0.985	-17
16000	0.123	66	-0.24	0.973	-18	0.125	71	-0.16	0.982	-18	0.126	72	-0.16	0.984	-18
17000	0.132	64	-0.26	0.972	-19	0.133	68	-0.16	0.982	-19	0.133	69	-0.16	0.984	-19
18000	0.141	62	-0.26	0.972	-20	0.143	66	-0.18	0.980	-20	0.143	67	-0.16	0.983	-20

HPND-4038

Freq.	V_R = 0 V					V_R = 10 V					V_R = 30 V				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
(MHz)	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.993	-5	-23.10	0.070	83	0.998	-3	-28.88	0.036	89	0.999	-3	-29.90	0.032	90
2000	0.976	-10	-17.28	0.137	76	0.995	-7	-22.86	0.072	84	0.996	-6	-23.76	0.065	85
3000	0.953	-15	-14.04	0.199	70	0.990	-10	-19.26	0.109	81	0.992	-9	-20.18	0.098	82
4000	0.923	-19	-11.88	0.255	64	0.982	-13	-16.78	0.145	78	0.986	-12	-17.74	0.130	79
5000	0.890	-23	-10.36	0.304	58	0.973	-16	-14.90	0.180	74	0.977	-15	-15.88	0.161	75
6000	0.857	-27	-9.20	0.347	53	0.962	-20	-13.40	0.214	71	0.968	-19	-14.30	0.193	73
7000	0.822	-31	-8.28	0.386	49	0.947	-23	-12.08	0.249	68	0.956	-22	-12.96	0.225	69
8000	0.790	-34	-7.58	0.418	45	0.933	-27	-11.06	0.280	65	0.945	-25	-11.92	0.254	66
9000	0.757	-38	-7.00	0.447	41	0.915	-30	-10.12	0.312	61	0.928	-29	-10.94	0.284	63
10000	0.727	-41	-6.54	0.471	38	0.897	-34	-9.40	0.339	58	0.912	-32	-10.22	0.309	61
11000	0.697	-44	-6.10	0.496	34	0.877	-37	-8.62	0.371	54	0.892	-35	-9.44	0.338	57
12000	0.668	-46	-5.74	0.517	32	0.854	-41	-8.00	0.399	52	0.874	-38	-8.76	0.365	54
13000	0.643	-49	-5.56	0.528	29	0.834	-44	-7.60	0.417	49	0.854	-42	-8.34	0.383	51
14000	0.620	-51	-5.22	0.549	26	0.813	-47	-7.04	0.445	45	0.839	-45	-7.76	0.410	48
15000	0.599	-53	-5.16	0.553	24	0.793	-50	-6.82	0.457	43	0.818	-48	-7.50	0.422	45
16000	0.584	-55	-4.90	0.569	21	0.778	-53	-6.42	0.478	39	0.805	-50	-7.10	0.442	42
17000	0.570	-57	-4.80	0.576	19	0.762	-55	-6.22	0.489	37	0.790	-53	-6.88	0.453	40
18000	0.556	-59	-4.84	0.574	17	0.747	-58	-6.18	0.491	35	0.776	-55	-6.86	0.454	37

Bonding and Handling Procedures for Beam Lead Diodes

1. Storage

Under normal circumstances, storage of beam lead diodes in HP supplied waffle/gel packs is sufficient. In particularly dusty or chemically hazardous environments, storage in an inert atmosphere desiccator is advised.

2. Handling

In order to avoid damage to beam lead devices, particular care must be exercised during inspection, testing, and assembly. Although the beam lead diode is designed to have exceptional lead strength, its small size and delicate nature requires that special handling techniques be observed so that the devices will not be mechanically or electrically damaged. A vacuum pickup is recommended for picking up beam lead devices, particularly larger ones, e.g., quads. Care must be exercised to assure that the vacuum opening of the needle is sufficiently small to avoid passage of the device through the opening. A #27 tip is recommended for picking up single beam lead devices. A 20X magnification is needed for precise positioning of the tip on the device. Where a vacuum pickup is not used, a sharpened wooden Q-tip dipped in isopropyl alcohol is very commonly used to handle beam lead devices.

3. Cleaning

For organic contamination use a warm rinse of trichloroethane, or its locally approved equivalent, followed by a cold rinse in acetone and methanol. Dry under infrared heat lamp for 5–10 minutes on clean filter paper. Freon degreaser, or its locally approved equivalent, may replace trichloroethane for light organic contamination.

- Ultrasonic cleaning is not recommended.
- Acid solvents should not be used.

4. Bonding

Thermocompression: See Application Note 979 "The Handling and Bonding of Beam Lead Devices Made Easy". This method is good for hard substrates only.

Wobble: This method picks up the device, places it on the substrate and forms a thermocompression bond all in one operation. This is described in the latest version of MIL-STD-883, Method 2017, and is intended for hard substrates only.

Resistance Welding or Parallel-GAP Welding: To make welding on soft substrates easier, a low pressure welding head is recommended. Suitable equipment is available from HUGHES, Industrial Products Division in Carlsbad, CA.

Epoxy: With solvent free, low resistivity epoxies (available from ABLESTIK and improvements in dispensing equipment, the quality of epoxy bonds is sufficient for many applications.

5. Lead Stress

In the process of bonding a beam lead diode, a certain amount of "bugging" occurs. The term *bugging* refers to the chip lifting away from the substrate during the bonding process due to the deformation of the beam by the bonding tool. This effect is beneficial as it provides stress relief for the diode during thermal cycling of the substrate. The coefficient of expansion of some substrate materials, specifically soft substrates, is such that some bugging is essential if the circuit is to be operated over wide temperature extremes.

Thick metal clad ground planes restrict the thermal expansion of the dielectric substrates in the X-Y axis. The expansion of the dielectric will then be mainly in the Z axis, which does not affect the beam lead device. An alternate solution to the problem of dielectric ground plane expansion is to heat the substrate to the maximum required operating temperature during the beam lead attachment. Thus, the substrate is at maximum expansion when the device is bonded. Subsequent cooling of the substrate will cause bugging, similar to bugging in thermocompression bonding or epoxy bonding. Other methods of bugging are preforming the leads during assembly or prestressing the substrate.

HEWLETT® PACKARD

Small Signal RF PIN Diode Chips for Hybrid Integrated Circuits

Technical Data

HPND-0001
HPND-0002

Features

- **Thermocompression/ Thermosonically Bondable**
- **Ideal for Hybrid Integrated Circuits**
- **Gold Metallization**
- **Silicon Nitride Passivation**
- **Uniform Electrical Characteristics**
- **Batch Matched Versions Available**
- **Planar Construction**

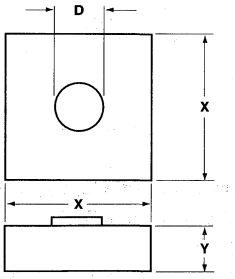
Description

These PIN/NIP diode chips are specifically designed for hybrid applications requiring thermosonic or thermocompression bonding techniques. The top metallization is a layer of gold for a tarnish free surface that allows either thermosonic or thermocompression bonding techniques. The bottom metallization is also gold, suitable for epoxy or eutectic die attach method.

Applications

These small signal, general purpose PIN/NIP diode chips are optimized for various analog and digital applications such as switches, digital phase shifters, pulse and amplitude modulators, limiters, leveling, and attenuating.

Outline 01B
Chip Dimensions



DIMENSIONS	FOR EPOXY OR EUTECTIC DIE ATTACH PART NO. HPND-	
	-0001	-0002
D (0.03) (1)	0.25 (10)	0.20 (8)
X (0.05) (2)	0.51 (20)	0.38 (15)
Y (0.03) (1)	0.15 (6)	0.15 (6)
TOP CONTACT	CATHODE	CATHODE
BOTTOM CONTACT	ANODE	ANODE

DIMENSIONS IN MILLIMETERS (1/1000 INCH).

Maximum Ratings

Junction Operating and Storage
Temperature Range ..... -65°C to +150°C
T_A = 25°C
P_D Power Dissipation ..... 250 mW
(Measured in an infinite heat sink derated linearly to zero at 150°C.)

Operation in excess of any one of these conditions may result in permanent damage to this device.

Electrical Specifications at T_A = 25°C

Chip for Epoxy or Eutectic Die Attach HPND-	Nearest Equivalent Surface Mount Part No. HSMP-	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Capacitance C_j (pF)	Typical Parameters		
					Series Resistance R_S (Ω)	Typical Carrier Lifetime τ (ns)	Typical Reverse Recovery Time t_{rr} (ns)
0001	3800	3080	100	0.20	2.0	1800	500
0002	3810	3081	100	0.20	3.5	1500	300
Test Conditions			$V_R = V_{BR}$ Measure $I_R \leq 10$ mA	V_R = 50 V *V_R = 20 V f = 1.0 MHz	I_F = 100 mA *I_F = 10 mA	I_F = 50 mA I_R = 250 mA *I_F = 10 mA *I_R = 6 mA	I_F = 20 mA V_R = 10 V 90% Recovery

Assembly and Handling Procedures for PIN Chips

1. Storage

Devices should be stored in a dry nitrogen purged dessicator or equivalent.

2. Cleaning

If required, surface contamination may be removed with electronic grade solvents. Typical solvents, such as freon (T.F. or T.M.C.), acetone, deionized water, and methanol, or their locally approved equivalents, can be used singularly or in combinations. Typical cleaning times per solvent are one to three minutes. DI water and methanol should be used (in that order) in the final cleans. Final drying can be accomplished by placing the cleaned dice on clean filter paper and drying with an infrared lamp for 5-10 minutes. Acids such as hydrofluoric (HF), nitric (HNO_3), and hydrochloric (HCl) should not be used.

The effects of cleaning methods/solutions should be verified on small samples prior to submitting the entire lot.

Following cleaning, dice should be either used in assembly (typically within a few hours) or stored in clean containers in a reducing atmosphere or a vacuum chamber.

3. Die Attach

a. Eutectic

Eutectic die attach can be accomplished by "scrubbing" the die with/without a preform on the header to combine with the silicon in the die. Temperature is approximately 400°C, with heating times of 5-10 seconds. (Note–times and temperature utilized may vary depending on the type, composition, and heat capacity of the header or substrate used.) This method is recommended for the HPND-000X series.

b. Epoxy

For epoxy die-attach, conductive silver-filled epoxies are recommended. This method can be used for all Hewlett-Packard PIN chips.

4. Wire Bonding

Either ultrasonic, thermosonic or thermocompression bonding techniques can be employed. Suggested wire is pure gold, 0.7 to 1.5 mil diameter.

HEWLETT® PACKARD

PIN Diode Chips for Hybrid MIC Switches/Attenuators

Technical Data

5082-0001
5082-0012

Features

- **Low Series Resistance 0.8 Ω Typical**
- **Nitride Passivated**

Description

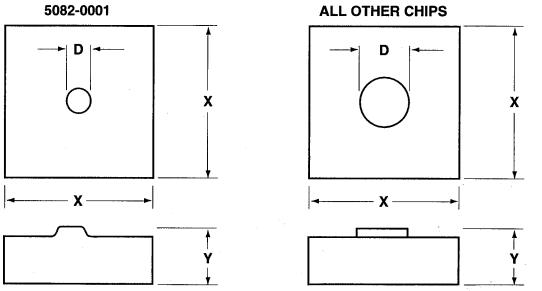
These PIN diode chips are silicon dioxide or nitride passivated. The 5082-0001 has a mesa construction and the 5082-0012 has a planar construction. The fabrication processes are optimized for long term reliability and tightly controlled for uniformity in electrical performance.

Applications

These general purpose PIN diodes are intended for low power switching applications such as duplexers, antenna switching matrices, digital phase shifters, time multiplex filters, TR switches, pulse and amplitude modulators, limiters, leveling circuits, and attenuators.

The 5082-0001 is optimized for applications requiring fast switching.

Outline 01B



DIMENSIONS	PART NO. 5082-	
	0012	0001
D ±0.03 (1)	0.10 (4)	0.06 (2.5)
X ±0.05 (2)	0.38 (15)	
Y ±0.03 (1)	0.10 (4.0)	0.11 (4.5)
Top Contact	Au. Cathode	Au. Anode
Bottom Contact	Au. Anode	Au. Cathode

Dimensions in millimeters (1/1000 inch)

Maximum Ratings

Junction Operating and Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature
5082-0001 ..... +300°C for 1 min. max.
5082-0012 ..... +425°C for 1 min. max.

Electrical Specifications at T_A = 25°C **Typical Parameters**

Chip Part Number 5082-	Nearest Equivalent Packaged Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Junction Capacitance C_j (pF)	Typical Series Resistance R_S (Ω)	Typical Lifetime τ (ns)	Typical Reverse Recovery Time t_{rr} (ns)
0001	3041	70	0.16*	0.8*	35*	5
0012	3001	150	0.12	1.0	400	100
Test Conditions		$V_R = V_{BR}$ Measure $I_R \leq 10$ mA	V_R = 50 V *V_R = 20 V f = 1 MHz	I_F = 100 mA *I_F = 20 mA f = 100 MHz	I_F = 50 mA I_R = 250 mA *I_R = 6 mA *I_F = 10 mA	I_F = 20 mA V_R = 10 V 90% Recovery

Assembly and Handling Procedures for PIN Chips

1. Storage

Devices should be stored in a dry nitrogen purged dessicator or equivalent.

2. Cleaning

If required, surface contamination may be removed with electronic grade solvents. Typical solvents, such as freon (T.F. or T.M.C.), acetone, deionized water, and methanol, or their locally approved equivalents, can be used singularly or in combinations. Typical cleaning times per solvent are one to three minutes. DI water and methanol should be used (in that order) in the final cleans. Final drying can be accomplished by placing the cleaned dice on clean filter paper and drying with an infrared lamp for 5-10 minutes. Acids such as hydrofluoric (HF), nitric (HNO_3) and hydrochloric (HCl) should not be used.

The effects of cleaning methods/solutions should be verified on small samples prior to submitting the entire lot.

Following cleaning, dice should be either used in assembly (typically within a few hours) or stored in clean containers in a reducing atmosphere or a vacuum chamber.

3. Die Attach

a. Eutectic

5082-0001

AuSn preform with stage temperature of 300°C for one minute max.

5082-0012

AuSn preform with stage temperature of 310°C for one minute max. AuGe preform with stage temperature of 390°C for one minute max.

b. Epoxy

For epoxy die-attach, conductive silver-filled or gold-filled epoxies are recommended. This method can be used for all Hewlett-Packard PIN chips.

4. Wire Bonding

Either ultrasonic or thermocompression bonding techniques can be employed. Suggested wire is pure gold, 0.7 to 1.5 mil diameter. Ultrasonic bonding method should be avoided for the 5082-0001 diode chip.

HEWLETT® PACKARD

Hermetic PIN Diodes for Stripline/Microstrip Switches/ Attenuators

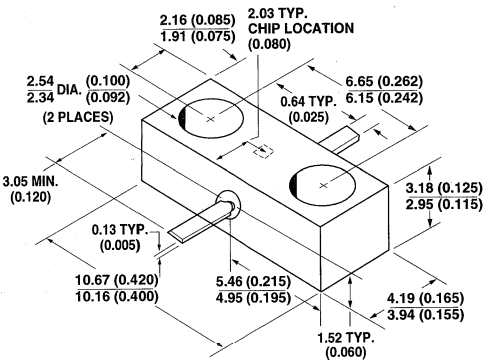
Technical Data

5082-3140
5082-3141

Features

- **Broadband Operation**
  HF through X-Band
- **Low Insertion Loss**
  Less than 0.5 dB to 10 GHz (5082-3140)
- **High Isolation**
  Greater than 20 dB to 10 GHz (5082-3140)
- **Fast Switching/Modulation**
  5 ns Typical (5082-3141)
- **Low Drive Current Required**
  Less than 20 mA for 20 dB Isolation (5082-3141)

Outline 60



DIMENSIONS IN MILLIMETERS AND (INCHES)

Description/Applications

The HP 5082-3140 is a passivated planar device and the 5082-3141 is a passivated mesa device. Both are in a shunt configuration in hermetic stripline packages. These diodes are optimized for good continuity of characteristic impedance which allows a continuous transition when used in 50 Ω microstrip or stripline circuits.

These diodes are designed for applications in microwave and HF-UHF systems using stripline or microstrip transmission line techniques.

Maximum Ratings

Part No. 5082-	-3140	-3141
Junction Operating and Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Power Dissipation [1]	1.75 W	0.75 W
Peak Incident Pulse Power [2]	225 W	50 W
Peak Inverse Voltage	150 V	70 V
Soldering Temperature	230°C for 5 sec.	

Notes:

1. Device properly mounted in sufficient heat sink at 25°C, derate linearly to zero at maximum operating temperature.
2. t_p = 1 µs, f = 10 GHz, Du = 0.001, Z_O = 50 Ω, T_A = 25°C.

5965-8882E

Typical circuit functions performed consist of switching, duplexing, multiplexing, leveling, modulating, limiting, or gain control functions as required in TR switches, pulse modulators, phase shifters, and amplitude modulators operating in the frequency range from HF through Ku-Band. These diodes provide nearly ideal transmission characteristics from HF through Ku-Band.

The 5082-3141 is recommended for applications requiring fast switching or high frequency modulation of microwave signals, or where the lowest bias current for maximum attenuation is required.

More information is available in HP Application Note 922 (Applications of PIN Diodes) and 929 (Fast Switching PIN Diodes).

Mechanical Specifications

Package Outline 60 is hermetically sealed and capable of meeting the stringent requirements of space level high reliability testing. Both the package and lead materials are gold plated Kovar.

Electrical Specifications at $T_A = 25°C$

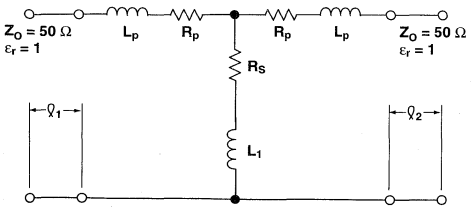
Part Number 5082-	Package Outline	Heat Sink	Min. Isolation (dB)	Max. Insertion Loss (dB)	Max. SWR	Max. Reverse Recovery Time t_{rr} (ns)	Typical Carrier Lifetime τ (ns)	Typical CW Power Switching Capability P_A (W)
3140	60	Anode	20	0.5	1.5	–	400	30
3141	60	Cathode	20	1.0	1.5	10	35*	13
Test[1] Conditions	–	–	I_F = 100 mA (Except 3141; I_F = 20 mA)	I_F = 0 P_{in} = 1 mW	I_F = 0 P_{in} = 1 mW	I_F = 20 mA V_R = 10 V Recovery to 90%	I_F = 50 mA I_R = 250 mA *I_F = 10 mA *I_R = 6 mA	–

Note:

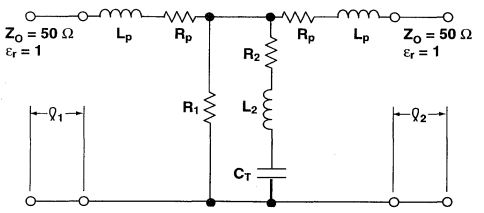
1. Test Frequencies: 8 GHz 5082-3141; 10 GHz 5082-3140.

Equivalent Circuits

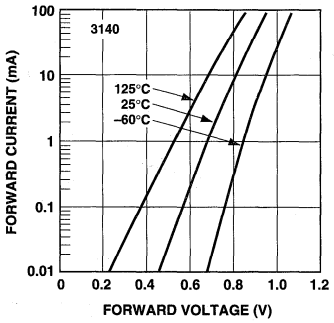
Forward Bias (Isolation State)



Zero Bias (Insertion Loss State)



Typical Parameters



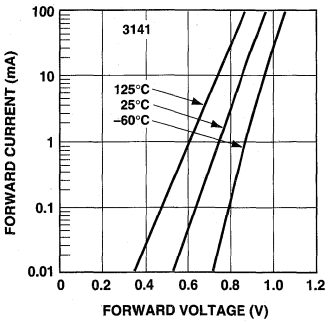


Figure 1. Typical Forward Characteristics.

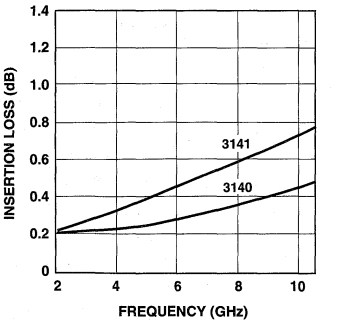


Figure 2. Typical Insertion Loss vs. Frequency.

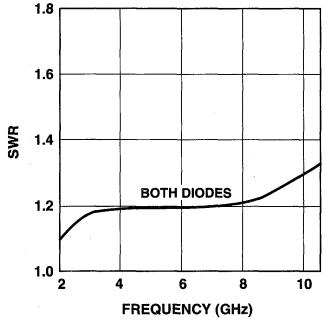


Figure 3. Typical SWR vs. Frequency.

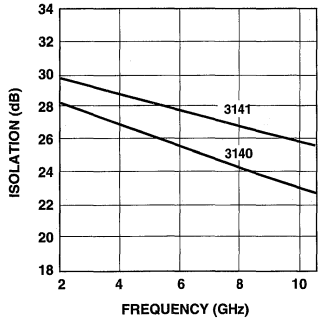


Figure 4. Typical Isolation vs. Frequency.

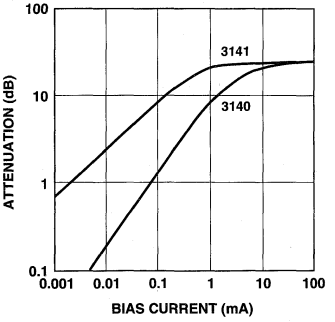


Figure 5. Typical Attenuation Above Zero Bias Insertion Loss vs. Bias Current at f = 8 GHz.

Typical Equivalent Circuit Parameters–Forward Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	Rs (Ω)	L_1 (pH)	ℓ_1 (mm)	ℓ_2 (mm)
3140	150	0.0	0.95	30	3.8	3.8
3141	150	0.0	0.8	20	3.8	3.8

Typical Equivalent Circuit Parameters–Zero Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	R_1 (KΩ)	L_2 (pH)	R_2 (KΩ)	C_T (pF)	ℓ_1 (mm)	ℓ_2 (mm)
3140	30	0.0	1.2	16	0.0	0.20	5.3	5.3
3141	200	0.0	∞	0	0.4	0.14	4.4	4.4

Typical Switching Parameters

RF Switching Speed HP 5082-3141

The RF switching speed of the HP 5082-3141 may be considered in terms of the change in RF isolation at 2 GHz. This switching speed is dependent upon the forward bias current, reverse bias drive pulse, and characteristics of the pulse source. The RF switching speed for the shunt-mounted stripline diode in a 50 Ω system is considered for two cases, one driving the diode from the forward bias state to the reverse bias state (isolation to insertion loss), second driving the diode from the reverse bias state to the forward bias state (insertion loss to isolation).

The total time it takes to switch the shunt diode from the isolation state (forward bias) to the insertion loss state (reverse bias) is shown in Figure 6. These curves are for three forward bias conditions with the diode driven in each case with three different reverse voltage pulses (V_{PR}). The total switching time for each case includes the delay time (pulse initiation to 20 dB isolation) and transition time (20 dB isolation to 0.9 dB isolation). Slightly faster switching times may be realized by spiking the leading edge of the pulse or using a lower impedance pulse driver.

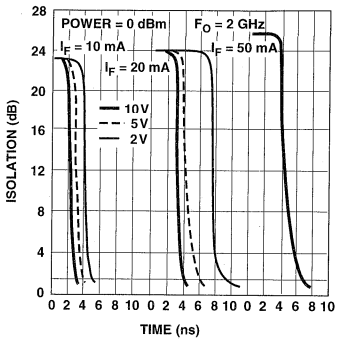


Figure 6. Isolation vs. Time (Turn-on) for HP 5082-3141. Frequency, 2 GHz.

The time it takes to switch the diode from zero or reverse bias to a given isolation is less than the time from isolation to the insertion loss case. For all cases of forward bias generated by the pulse generator (positive pulse), the RF switching time from the insertion loss state to the isolation state was less than 2 nanoseconds. A more detailed treatise on switching speed is published in AN929: "Fast Switching PIN Diodes".

Reverse Recovery Time

Figures 8 and 9 show reverse recovery time, (t_{rr}) vs. forward current, (I_F) for various reverse pulse voltages V_R. The circuit used to measure t_{rr} is shown in Figure 7.

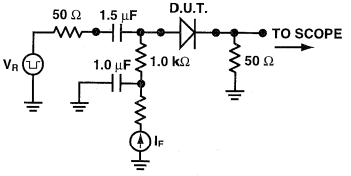


Figure 7. Basic t_{rr} Test Setup.

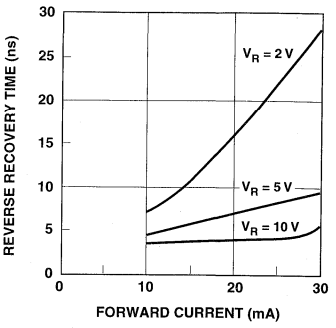


Figure 8. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3141.

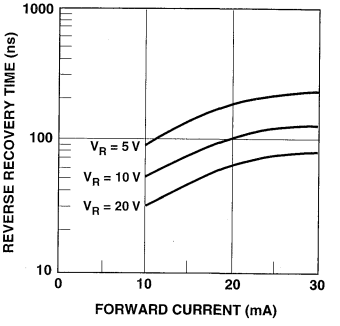


Figure 9. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3140.

HEWLETT® PACKARD

PIN Diodes for RF Switching and Attenuating

Technical Data

1N5719
1N5767
5082-3001
5082-3039
5082-3042/43
5082-3077
5082-3080/81
5082-3188
5082-3379

Features

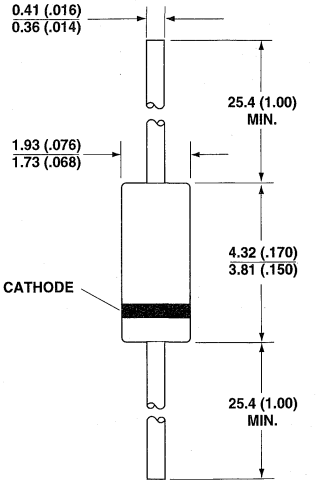
- **Low Harmonic Distortion**
- **Large Dynamic Range**
- **Low Series Resistance**
- **Low Capacitance**

Description/Applications

These general purpose switching diodes are intended for low power switching applications such as RF duplexers, antenna switching matrices, digital phase shifters, and time multiplex filters. The 5082-3188 is optimized for VHF/UHF bandswitching.

The RF resistance of a PIN diode is a function of the current flowing in the diode. These current controlled resistors are specified for use in control applications such as variable RF attenuators, automatic gain control circuits, RF modulators, electrically tuned filters, analog phase shifters, and RF limiters.

Outline 15 diodes are available on tape and reel. The tape and reel specification is patterned after RS-296-D.



DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline 15

Maximum Ratings

Junction Operating and
Storage Temperature Range ..... -65°C to +150°C
Power Dissipation 25°C ..... 250 mW
(Derate linearly to zero at 150°C)
Peak Inverse Voltage (PIV) ..... same as V_{BR}
Maximum Soldering Temperature ..... 260°C for 5 sec

Mechanical Specifications

The HP Outline 15 package has a glass hermetic seal with dumet leads. The lead finish is 95-5 tin-lead (SnPb) for all PIN diodes.

The leads on the Outline 15 package should be restricted so that the bend starts at least 1/16 inch (1.6 mm) from the glass body. Typical package inductance and capacitance are 2.5 nH and 0.13 pF, respectively. Marking is by digital coding with a cathode band.

General Purpose Diodes
Electrical Specifications at T_A = 25°C

Part Number 5082-	Maximum Total Capacitance C_T (pF)	Minimum Breakdown Voltage V_{BR} (V)	Maximum Residual Series Resistance R_S (Ω)	Effective Carrier Lifetime τ (ns)	Reverse Recovery Time t_{rr} (ns)
General Purpose Switching and Attenuating					
3001	0.25	200	1.0	100 (min.)	100 (typ.)
3039	0.25	150	1.25	100 (min.)	100 (typ.)
1N5719	0.3**	150	1.25	100 (min.)	100 (typ.)
3077	0.3	200	1.5	100 (min.)	100 (typ)
Fast Switching					
3042	0.4*	70	1.0*	35 (typ.)*	5 (max.)
3043	0.4*	50	1.5*	35 (typ.)*	10 (max.)
Band Switching					
3188	1.0*	35	0.6**	70 (typ.)*	12 (typ.)
Test Conditions	V_R = 50 V *V_R = 20 V **V_R = 100 V f = 1 MHz	$V_R = V_{BR}$ Measure $I_R \leq 10$ mA	I_F =100 mA *I_F = 20 mA **I_F = 10 mA f = 100 MHz	I_F = 50 mA I_R = 250 mA *I_F = 10 mA *I_R = 6 mA	I_F = 20 mA V_R = 10 V 90% Recovery

Notes:

Typical CW power switching capability for a shunt switch in a 50 Ω system is 2.5 W.

Part marking on glass package diodes, outline 15 is:

5082-xxxx

HPx
xxx
yww

For example, 1N5767 made in 1996 work week 35 would be marked:

HP5
767
635

RF Current Controlled Resistor Diodes
Electrical Specifications at T_A = 25°C

Part Number	Effective Carrier Lifetime t (ns)	Min. Breakdown Voltage V_{BR} (V)	Max. Residual Series Resistance R_S (Ω)	Max. Total Capacitance C_T (pF)	High Resistance Limit, R_H (W)		Low Resistance Limit, R_L (W)		Max. Difference in Resistance vs. Bias Slope, Dc
					Min.	Max.	Min.	Max.	
5082-3080	1300 (typ.)	100	2.5	0.4	1000			8**	
1N5767*	1300 (typ.)	100	2.5	0.4	1000			8**	
5082-3379	1300 (typ.)	50		0.4				8**	
5082-3081	2500 (typ.)	100	3.5	0.4	1500			8**	
Test Conditions	I_F = 50 mA I_R = 250 mA	$V_R = V_{BR}$, Measure $I_R \leq 10$ mA	I_F = 100 mA f = 100 MHz	V_R = 50 V f = 1 MHz	I_F = 0.01 mA f = 100 MHz		I_F = 1.0 mA I_F = 20 mA** f = 100 MHz		Batch Matched at I_F = 0.01 mA and 1.0 mA f = 100 MHz

*The 1N5767 has the additional specifications: τ = 1.0 msec minimum
I_R = 1 μA maximum at V_R = 50 V
V_F = 1 V maximum at I_F = 100 mA.

Typical Parameters at T_A = 25°C (unless otherwise noted)

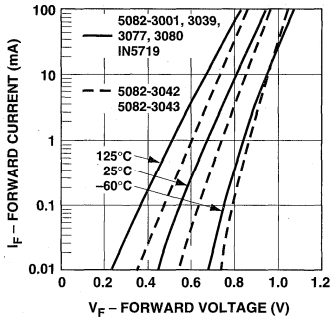


Figure 1. Forward Current vs. Forward Voltage.

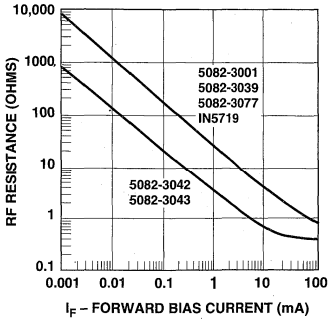


Figure 2. Typical RF Resistance vs. Forward Bias Current.

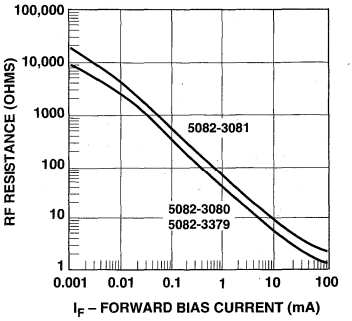


Figure 3. Typical RF Resistance vs. Forward Bias Current.

Typical Parameters at $T_A = 25°C$ (cont.)

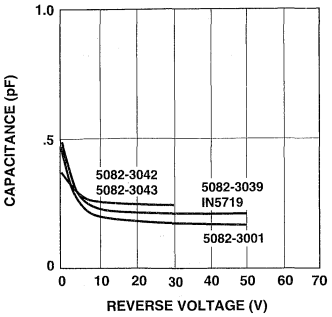


Figure 4. Typical Capacitance vs. Reverse Voltage.

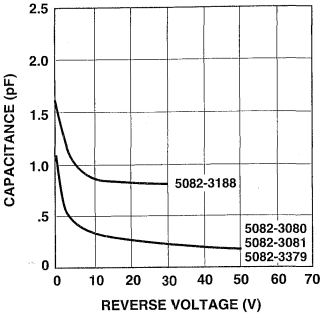


Figure 5. Typical Capacitance vs. Reverse Voltage.

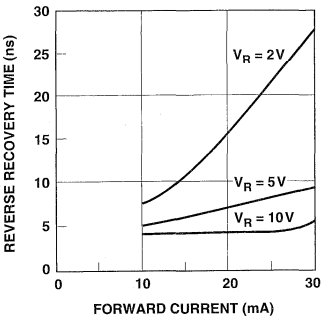


Figure 6. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3042, 3043.

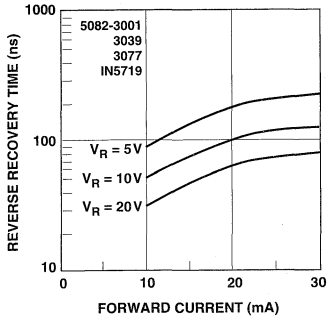


Figure 7. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages.

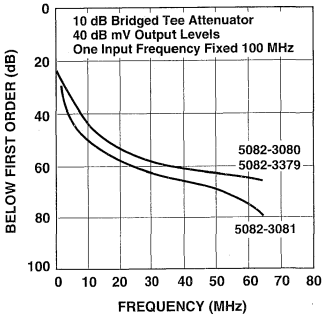


Figure 8. Typical Second Order Intermodulation Distortion.

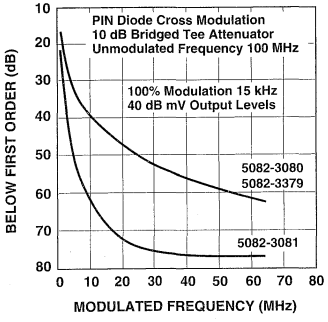


Figure 9. Typical Cross Intermodulation Distortion.

HEWLETT® PACKARD

Surface Mount PIN Diodes

Reliability Data

HPND-00XX
HSMP-38XA
HSMP-38XX
HSMP-48XX

Description

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation. For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in this catalog.

1. Life Test

A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hours	Total Failed	Failure Rate %/1K Hours
High Temp. Rev. Bias (HTRB)	V_R = 80% V_{BR}, T_A = 150°C	1,382	1,385,756	4	0.29
Operating Life (O.L.)	T_A = R.T., P_{FM} = Max. Rated Power, V_R = 80% V_{BR}, 60 Hz	2,162	2,084,325	0	0
High Temp. Storage (HTS)	T_A = 150°C	505	511,390	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated using the Arrhenius plot with activation energy of 1.2 eV and is listed in the following table.

Junction Temp. T_J** (°C)	Point[1] MTTF* (Hours)	Point[1] FIT[3]	90% Confidence Level[2] MTTF (Hours)	90% Confidence Level[2] FIT[3]
150	3.5×10^7	28.6	1.5×10^7	66.7
130	2.0×10^8	5.0	8.7×10^7	11.5
110	1.5×10^9	0.67	6.5×10^8	1.5
90	1.0×10^{10}	0.10	4.3×10^9	0.23
75	1.0×10^{11}	0.01	4.3×10^{10}	0.023
50	2.0×10^{12}	0.0005	8.7×10^{11}	0.0011

*MTTF data collected in Hermetic Package and Plastic Packages.
** T_J was calculated using a θ_{JC} of 500°C/W.

Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 50°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = 8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

$(7.7 \times 10^{-12}/hr) \times (25\%) \times (8760\ hrs/yr) = 1.69 \times 10^{-6}$ % per year.

Likewise, the 90% confidence level failure rate per year is:

$(1.8 \times 10^{-11}/hr) \times (25\%) \times (8760\ hrs/yr) = 3.94 \times 10^{-6}$ % per year.

2. Environmental and Mechanical Tests

Test Name	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	235°C, 5 seconds	746	0
Solder Heat	2031	260°C, 10 seconds	382	0
Resistance to Solvents	1022	4 Solvent Groups	332	0
Autoclave	HP GSS 12-109	121°C, 15 PSIG, 96 hrs.	2,064	10
Moisture Resistance	HP GSS 12-107, Method B	85°C/85% RH, 1000 hrs.	405	0
Thermal Shock	1056	-65/+150°C, 5 min. dwell, 200 cycles	1,447	2
Temperature Cycle	1051	-65/+150°C, 10 min. dwell, 200 cycles	1,209	1
Lead Integrity		2.0 pounds minimum	140	0

3. Flammability Test

(MIL-STD-202, Method 111):

Meets Needle Flame Test per UL Category D (Flaming Time <3 sec.) under material classifcation 94V0.

4. DOD-HDBK-1686 ESD Classification:

The PIN Diodes covered in this Reliability Data Sheet are Class I, with the following exceptions:

HPND-0002	Class II
HSMP-381X	Class II
HSMP-381A	Class II
HSMP-4810	Class II

HEWLETT® PACKARD

PIN Diodes

Reliability Data

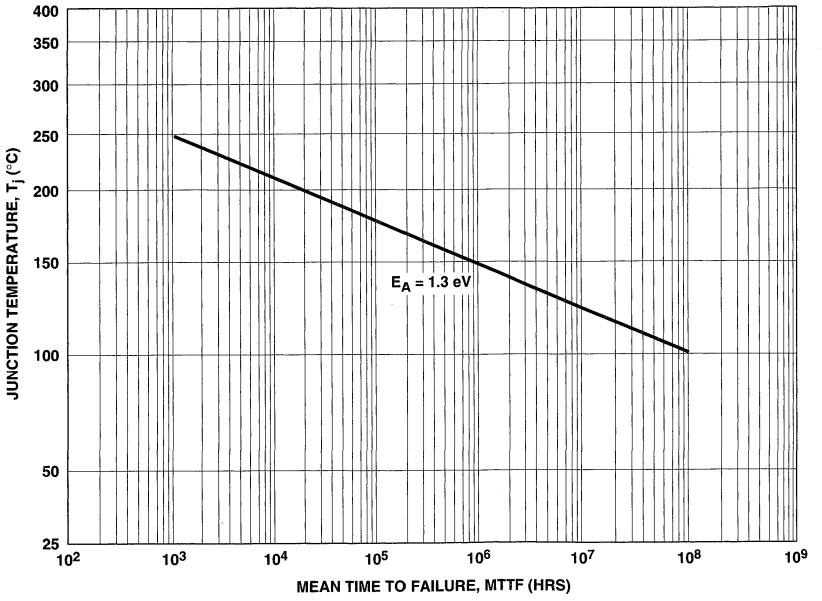
1N5719
5082-3001
5082-3039
5082-3077

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is initially compiled from reliability tests run prior to market introduction to demonstrate that a product meets design criteria. Additional tests are run periodically. The data on this sheet represents the latest review of accumulated test results.

Applications

This information represents the capabilities of the generic device. Failure rates and MTTF values presented here are achievable with normal MIL-S-19500 TX level screening. This reliability screening is no longer available from Hewlett-Packard. The screening tests, references, conditions, lot sizes, and LTPD are provided as references only.



Mean Time to Failure vs. Junction Temperature

Burn-In and Storage

Test	Test Conditions	LTPD/ 1000 Hours
High Temperature Life	1,000 hrs. min. storage time @ 150°C	3
Steady State Operating Life	1,000 hrs. min. operating time @ P_{FM} = 250 mW, V_{RM} = 150 V, f = 60 Hz, T_A = 25°C	3

Environmental

Test	MIL-STD-750 Reference	Test Conditions	LTPD
Solderability	2026	Sn 95, Pb 5, solder at 260°C	10
Temperature Cycling	1051	100 cycles from -65°C to +150°C, 0.5 hrs. at extremes, 5 min. transfer	7
Thermal Shock	1056	100 cycles from 0°C to +100°C, 3 sec. transfer	7
Moisture Resistance	1021	10 days, 90-98% RH, -10 to +65°C, non operating	7
Shock	2016	5 blows each X_1, Y_1, Y_2, 1500 G. 0.5 msec pulse	7
Vibration Variable Frequency	2056	4, 4 minute cycles each X, Y, Z at 20 G min. 100 to 2000 Hz	7
Constant Acceleration	2006	1 minute each X_1, Y_1, Y_2, at 20,000 G	7
Terminal Strength	2036	Miniature glass package, -3, 90° arcs, 2 leads, 8 oz., lead restriction	10
Hermeticity	1014	Fine and gross	2

DOD-HDBK-1686 ESD Classification:
The PIN diodes covered in this Reliability Data Sheet are Class I.

HEWLETT® PACKARD

PIN Diodes

Reliability Data

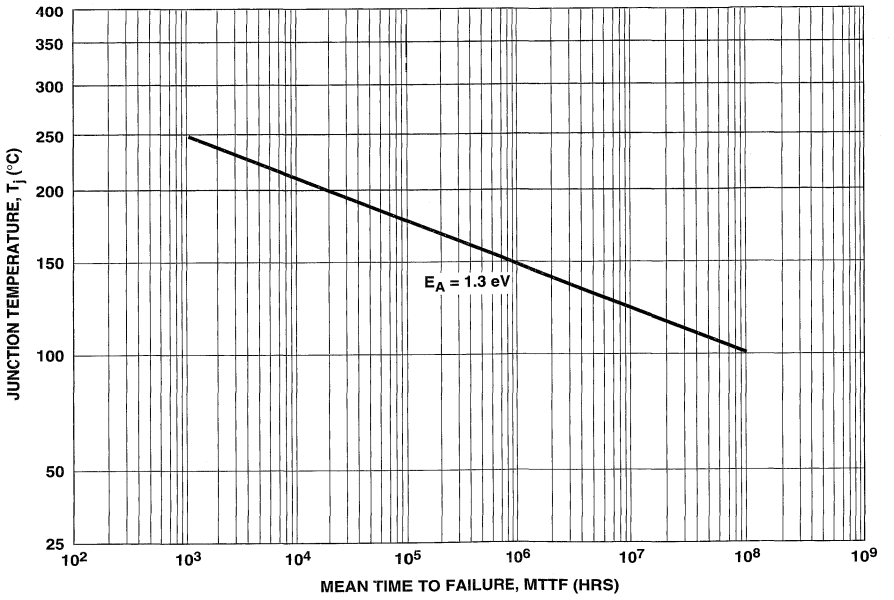
1N5767
5082-3080
5082-3188

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is initially compiled from reliability tests run prior to market introduction to demonstrate that a product meets design criteria. Additional tests are run periodically. The data on this sheet represents the latest review of accumulated test results.

Applications

This information represents the capabilities of the generic device. Failure rates and MTTF values presented here are achievable with normal MIL-S-19500 TX level screening. This reliability screening is no longer available from Hewlett-Packard. The screening tests, references, conditions, lot sizes, and LTPD are provided as references only.



Mean Time to Failure vs. Junction Temperature

Burn-In and Storage

Test	Test Conditions	LTPD/ 1000 Hours
High Temperature Life	1,000 hrs. min. storage time @ 150°C	3
Steady State Operating Life	1,000 hrs. min. operating time @ P_{FM} = 250 mW, V_{RM} = 20 V, f = 60 Hz, T_A = 25°C	3

Environmental

Test	MIL-STD-750	Tests Conditions	LTPD
Solderability	2026	Sn 95, Pb 5, solder at 260°C	10
Temperature Cycling	1051	100 cycles from -65°C to +150°C, 0.5 hrs. at extremes, 5 min. transfer.	7
Thermal Shock	1056	5 cycles from 0°C to +100°C, 3 sec. transfer	7
Moisture Resistance	1021	10 days, 90-98% RH, -10 to +65°C, non operating	7
Shock	2026	5 blows each X_1, Y_1, Y_2, 1500 G. 0.5 msec pulse	7
Vibration Fatigue	2046	32 ± 8 hrs., each X, Y, Z, 96 hr. total, 60 Hz, 20 G min.	7
Vibration Variable Frequency	2056	4, 4 minute cycles each X, Y, Z at 20 G min. 100 to 2000 Hz	7
Constant Acceleration	2006	1 minute each X_1, Y_1, Y_2, at 20,000 G	7
Terminal Strength	2036	Miniature glass package, -3, 90° arcs, 2 leads, 8 oz., lead restriction	7
Salt Atmosphere	1041	35° fog for 24 hours	7

DOD-HDBK-1686 ESD Classification:

IN5767	Class II
5082-3080	Class II
5082-3188	Class I

HEWLETT® PACKARD

Beam Lead PIN Diodes

Reliability Data

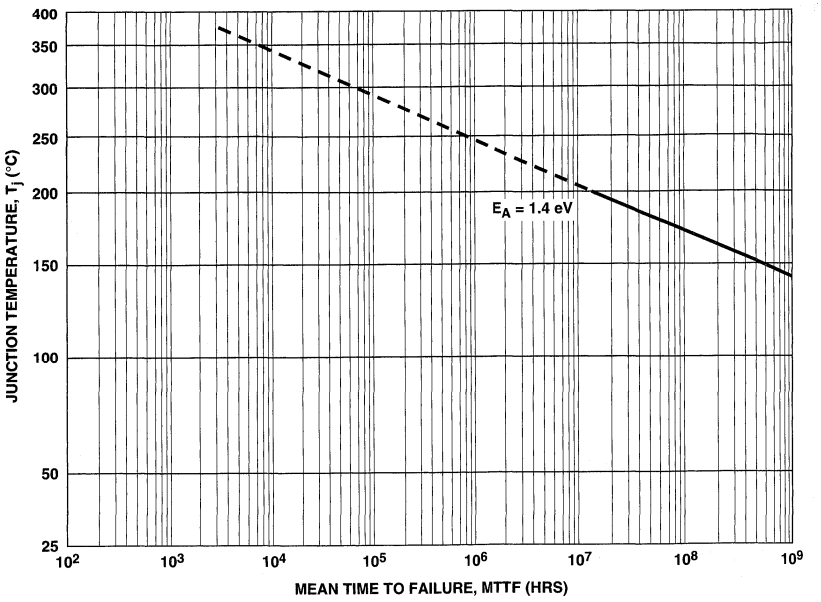
HPND-4005
HPND-4018
HPND-4028
HPND-4038

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is initially compiled from reliability tests run prior to market introduction to demonstrate that a product meets design criteria. Additional tests are run periodically. The data on this sheet represents the latest review of accumulated test results.

Applications

This information represents the capabilities of the generic device. Failure rates and MTTF values presented here are achievable with normal MIL-S-19500 TX level screening. This reliability screening is no longer available from Hewlett-Packard. The screening tests, references, conditions, lot sizes, and LTPD are provided as references only.



Mean Time to Failure vs. Junction Temperature

5965-8892E

Burn-In and Storage

Test	Test Conditions	LTPD/ 1000 Hours
High Temperature Life	1,000 hrs. min. storage time @ 200°C	3
Steady State Operating Life	1,000 hrs. min. operating time @ I_F = 30 mA, T_A = 150°C	3

Environmental

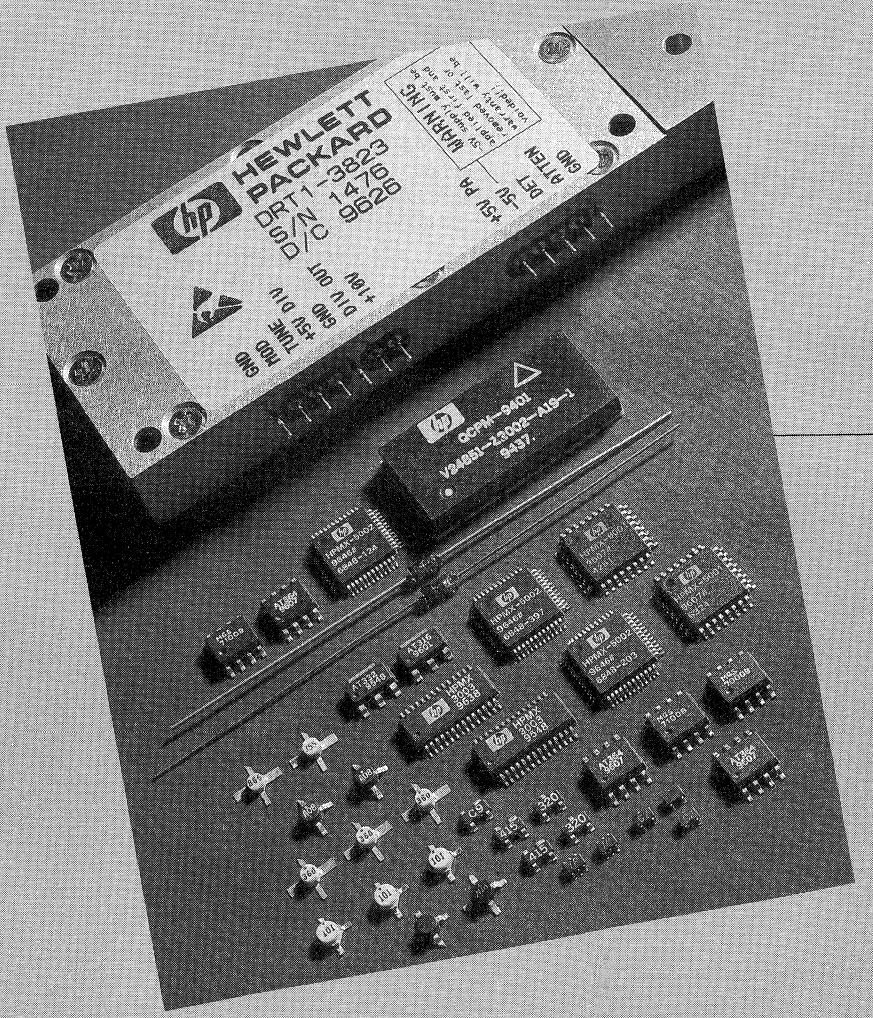
Test	MIL-STD-750 Reference	Test Conditions	LTPD
Temperature Cycling	1051	-65/+200°C, 100 cycles, 10 min. dwell, 5 min. transfer	7
Thermal Shock	1056	0/100°C, 100 cycles, 10 min. dwell, 10 sec. transfer	7
Moisture Resistance	1021	98% RH, -10°C/+65°C, 10 days	7
Constant Acceleration	2006	20 KGs, 1 min. each axis	7
Mechanical Shock	2016	5 blows each axis at X, Y, Z, 1500 Gs, 0.5 msec pulse	7
Vibration Variable Frequency	2056	20 Gs min., 100 to 2000 Hz, 4 minute cycles each axis X, Y, Z	7
Salt Atmosphere	1041	Salt Fog at 35°C for 24 hrs.	10

DOD-HDBK-1686 ESD Classification:

HPND-4005 Class I
HPND-4018 Class I
HPND-4028 Class I
HPND-4038 Class I

HEWLETT PACKARD

Schottky Diodes



Schottky Barrier Diodes

Characteristics

A Schottky barrier diode contains a metal-semiconductor barrier formed by deposition of a metal layer on a semiconductor. The resulting non-linear diode is similar to point contact diodes and p-n junction diodes. The Schottky diode is more rugged than the point contact diode because the contact is not subject to change under vibration. The advantage over p-n junction is the absence of minority carriers which limit the response speed in switching applications and the high frequency performance in mixing and detecting applications.

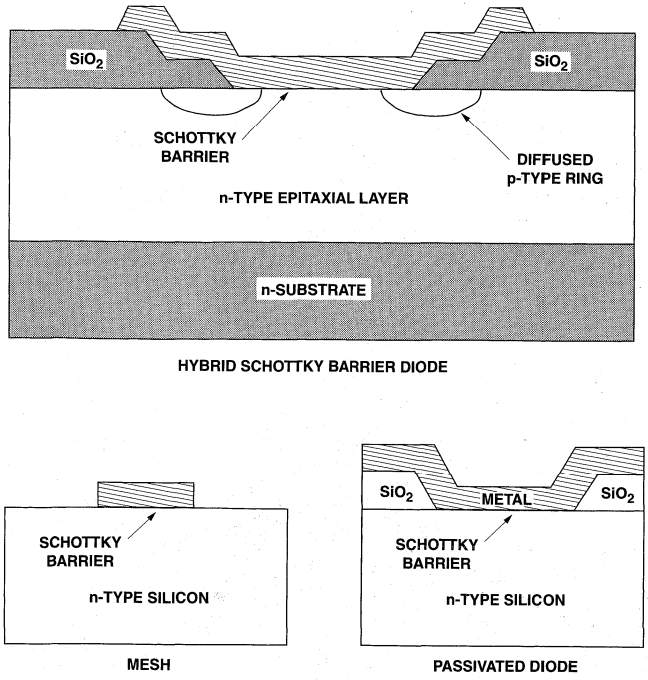


Figure 1. Three Types of Schottky Barrier Diodes.

Types of Diode Construction

There are several assembly geometries used for Schottky barrier diodes. Three types used in this catalog are shown in Figure 1.

Mesh Diodes

Hewlett-Packard's patented mesh diode is made by depositing metal through a screen to the semiconductor surface. Many closely spaced diodes are created on the chip. The diode contacts are too small for thermocompression bonding. Contact is made by pressing a sharp metal point against one of the metal contacts on the diode. The large number of contacts on the chip provide a good yield to this operation.

Although the mesh contacts are too small for thermocompression bonding, they are not small enough for operation at high microwave frequencies. It is not possible to deposit reliable contact areas small enough for operation at frequencies above 7 GHz; in fact, the highest test frequency is 3 GHz. The mesh devices have model numbers in the series 5082-2300 and 2900.

Passivated Diodes

The problem of creating small area contacts was solved by the development of the passivated diode process. An oxide layer is formed over the entire silicon area. Then photolithographic techniques are used to open a small hole in the oxide.

The appropriate metal is deposited in the hole to make the small area Schottky barrier. Then gold is deposited to provide a larger surface for the thermocompression bond in plastic packaged diodes or for the pressure contact in glass packaged diodes (outline 15). Passivated diodes include the 5082-2835, the HSMS-280X series, and zero bias detectors. These devices are used at frequencies up to 20 GHz.

This passivation process is also used in our beam lead diodes. The final gold layer becomes the beam lead itself. Beam lead diodes contain a nitride layer on the oxide to provide immunity from contaminants that could otherwise lead to reverse current drift. There is also a platinum layer between the barrier metal and the gold. This layer permits reliable operation at higher temperatures. Breakdown voltage for passivated type beam lead diodes is 4 volts minimum at 10 microamps.

Beam lead single diodes are included in the HSCH-5300 series and pairs in the HSCH-5500 series. These beam lead diodes are also available in package outlines C2, E4, and H2.

Hybrid Diodes

The breakdown voltage limitation was solved with the invention of the hybrid process. Hewlett-Packard's patented process combines a Schottky diode with a p-n junction, eliminating the premature breakdown of the passivated diode without sacrificing the picosecond switching response of the Schottky barrier. Breakdown voltage specifications as high as 70 volts are available. Hybrid diodes include the HSMS-280X and HSMS-281X families.

The dual nature of the hybrid diode limits the lowest capacitance to a picofarad. This limits the high frequency guaranteed performances of these diodes to 2 GHz.

The Height of the Schottky Barrier

The current-voltage characteristic of Schottky barrier diodes at room temperature is described by the following equation:

$$I = I_S \left(\exp \frac{V - IR_S}{0.026} - 1\right)$$

For currents below 0.1 mA, the IR_S term may be neglected. On semi-log graph paper, as plotted in this catalog, the current graph will be a straight line with inverse slope 2.3 x 0.026 = 0.060 volts per cycle. All curves have the same slope, but not necessarily the same value of current for a given voltage. This is determined by the saturation current, I_S, and is related to the type of metal deposited on the silicon and to the treatment of the silicon surface layer. The term "barrier height" is related to the voltage required for a given current. Low voltage corresponds to low barrier.

Study of the forward characteristics in this catalog shows that the lowest barrier diode is the HSMS-285X family of zero bias detectors. Detection at zero bias is possible for a range of barrier heights, but the voltage sensitivity is best for high barrier diodes. The other extreme is represented by medium barrier mixer diodes such as the HSMS-286X. However, this barrier height corresponds to a zero bias junction resistance that requires a load resistance above 10 megohms. Zero bias detection with these diodes is limited to single frequency applications.

Thermal Resistance

Thermal Resistance is normally designated by θ_{jc} "theta-j-c" or the thermal resistance from the junction to the case. It is specified in terms of °C per Watt (°C/W).

Using this number θ_{jc}, and knowing the amount of power being dissipated as heat in the diode, one can calculate the temperature rise of the junction with respect to the case. Conversely, one can reverse the process and use temperature rise and power data to compute θ_{jc}. This calculation is based upon the measurements which we made when we produced our diode data sheet.

The numbers to use are:

1. T_{jmax}, the maximum junction operating temperature
2. P_{max}, the maximum DC power dissipation
3. C_t, the case temperature = 25°C

Items 1 and 2 are found in the Maximum Ratings table on the diode's data sheet. The computation is as follows:

$$\theta_{jc} = (T_{jmax} - C_t) / P_{max}$$

As an example, consider the IN5711 Schottky diode. In this case,

T_{jmax} = 200°C
P_{max} = 250 mW
= 0.25 W

and our calculation yields

$\theta_{jc} = (200 - 25) / 0.25 = 700°C/W$

Applications of Schottky Barrier Diodes

Schottky barrier diodes are useful in a wide variety of applications over a broad frequency range from digital to microwave.

Mixers

The most sensitive receivers using Schottky barrier diodes make use of the nonlinear properties of the diode to produce a difference frequency by mixing the received signal with a local oscillator. Although this can be done with a single diode, it is more common to use multiple diodes in balanced or double balanced mixers. Balanced circuits reduce the effect of a noisy local oscillator and also reduce the level of high order mixing products that are not related to the desired input frequency. For multiple diode mixers, batch matched devices or matched pairs are available.

The most important property of mixer diodes is the noise figure—a measure of how small a signal can be received. The noise level for a perfect receiver is -114 dBm per MHz of bandwidth. A 6 dB noise figure mixer will degrade the noise level to -108 dBm per MHz. If the bandwidth of the receiver is 4 MHz, the noise level is raised to -102 dBm. If a 10 dB signal to noise level is required for proper operation of the receiver, the sensitivity is -92 dBm. In this section of the catalog, there are several groups of single diodes characterized for mixer applications. For stripline circuits the hermetic H2, broadband C2, and beam lead outlines are available. The best diodes at the highest frequency are guaranteed to have a noise figure less than 7.2 dB at 44 GHz.

The other group of mixer diodes uses outline 15, glass package, for 2 GHz. The best units have a 6 dB noise figure for 2 GHz.

Applications such as Doppler radar involving intermediate frequencies below 1 MHz will benefit by using the 5082-2303 or 5082-2900 with its lower noise at these output frequencies. The additional noise (flicker noise) varies inversely with difference frequency and may differ as much as 20 dB from one diode type to another. Since the lowest capacitance (passivated) diodes have the highest flicker noise, it is sometimes better to choose a Doppler mixer diode for lowest flicker noise rather than for lowest published noise figure.

Another type of mixer diode is the Schottky quad used for double balanced mixers. These quads are available in beam lead versions and in outline E4. These units contain a monolithic beam lead quad—four diodes connected in a ring configuration by gold deposited and plated on the wafer. Since the four diodes are made at the same time on the same portion of a wafer, they are nearly identical and ideally suited for double balanced mixers.

In most cases both medium and low barrier silicon models are available. The low barrier units have an impedance closer to 50 Ω. These models give better performance in broad band untuned circuits, particularly in those applications with local oscillator power below normal.

Detector Applications

For system applications with relaxed requirements on sensitivity, the video detector receiver is a good alternative to the superheterodyne receiver. The sensitivity is degraded about 50 dB, but the circuitry is simplified and broad bandwidth is easily attained without the problem of tracking the local oscillator frequency.

The important parameters are tangential signal sensitivity (TSS) and voltage (γ). Both of these, as well as video resistance (R_v), are guaranteed for these detector diodes. Typical detector performance is shown for mixer diodes, but detector diodes are designed for superior performance for this application.

Tangential signal sensitivity measures the ability of the diode to distinguish a small signal from noise. The name relates to a type of radar display with the bottom of the signal pulse tangent to the top of the noise level. There are subjective aspects to this measurement is now made with a voltmeter. The value depends on diode noise as well as detection capability.

In some applications, the detector is used as a monitor and the measurement level is well above the noise. For these applications, voltage sensitivity, voltage output for one microwatt input, is the important parameter.

The third specification, video resistance, R_v, is important for video amplifier and response time considerations. The video amplifier resistance, R_L, should be large compared to R_v because the maximum output voltage is degraded by the factor

$$R_L/(R_L + R_V)$$

However, response time is proportional to the RC product. If fidelity to pulse shape is important, the presence of pulses with steep edges requires a smaller value of load resistance. Sensitivity must be sacrificed for fidelity.

Zero bias Schottky detector diodes are available in plastic packages (outlines 23 and 323). Two types of metal to semiconductor junctions are used, resulting in two distinct ranges of junction resistance (video resistance). Since voltage sensitivity varies with resistance, the high resistance diodes have better voltage sensitivity. However, high resistance means higher noise so the TSS specifications are better for the low resistance diodes. All tests are done at 10 GHz.

The other type of detector (HSMS-282X and HSMS-286X series) requires a small forward bias. Production tests are made with 20 microamperes of bias which reduces the video resistance to about 1300 Ω. At zero bias the resistance is higher than for either one of the zero bias detectors. Although the statement has been made that high resistance corresponds to good sensitivity, the resistance is so high for these models that the sensitivity is degraded by normal load resistances. These diodes can be used without bias if the load resistance is comparable to the diode resistance. This is discussed in AN988, "All Schottky Diodes are Zero Bias Detectors."

Dynamic and Series Resistance

Schottky diode resistance may be expressed as series resistance, R_S, or as dynamic resistance, R_D. These two terms are related by the equation

$$R_D = R_S + R_j$$

where R_j is the resistance of the junction. Junction resistance of a diode with DC bias is quite accurately calculated by

$$R_j = 26/I_B \text{ where}$$

I_B is the bias current in milliamperes. The series resistance is independent of current.

The dynamic resistance is more easily measured. If series resistance is specified, it is usually obtained by subtracting the calculated junction resistance from the measured dynamic resistance.

Applications

The application notes represented by these abstracts are available from your local Hewlett-Packard sales office or nearest Hewlett-Packard authorized distributor or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

AN 923
Hot Carrier Diode Video Detectors
Describes the characteristics of HP Schottky barrier diodes intended for use in video detector or video receiver circuits, and discusses some design features of such circuits.

Though less sensitive than the heterodyne receiver, the many advantages of the video receiver make it extremely useful. The Schottky diode can be used to advantage in applications such as beacon, missile-guidance, fuse-activating, and countermeasure receivers, and as power-leveling and signal-monitoring detectors.

Among the subjects discussed are the performance characteristics of video detector diodes—tangential sensitivity, video resistance, voltage sensitivity and figure of merit; how these characteristics affect the bandwidth of a video detector, video detector design considerations; considerations that affect dynamic range; and considerations that vary the level at which *burnout* can occur.

Publication No. 5954-2079

AN 956-1
The Criterion for the Tangential Sensitivity Measurement
Discusses the meaning of Tangential Sensitivity and a recommended measurement technique.

Publication No. 5091-0169E

AN 956-3
Flicker Noise in Schottky Diodes
Treats the subject of flicker (1/f) noise in Schottky diodes, comparing four different types.

Publication No. 5952-0487

AN 956-4
Schottky Diode Voltage Doubler
Explains how Schottky detectors can be combined to achieve higher output voltages than would be produced by a single diode.

Publication No. 5964-4236E

AN 956-5
Dynamic Range Extension of Schottky Detectors
Discusses operation of two types of detectors: the small signal type, also known as square-law detectors; and the large signal type, also known as linear or peak detectors.

Techniques for raising the compression level are presented. An example is given illustrating the effect of bias current level on an HP 5082-2751 detector.

Publication No. 5952-8335

AN 956-6
Temperature Dependance of Schottky Detector Voltage Sensitivity
A discussion of the effects that temperature changes have on Schottky barrier diodes. Performance improves at lower temperatures in a predictable manner. Data presented was obtained using HP 5082-2750 detector diodes.

Publication No. 5964-3898E

AN 963
Impedance Matching Techniques for Mixers and Detectors
Presents a methodical technique for matching complex loads, such as Schottky diodes, to a transmission line. Direct application to broadband mixers and detectors is illustrated.

Publication No. 5952-0496

AN 969
The Zero Bias Schottky Detector Diode
A conventional Schottky diode detector such as the Hewlett-Packard HSMS-2860 requires no bias for high level input power—above one milliwatt. However, at low levels, a small amount of DC bias is required for detection to take place. Even though this bias current is at the microampere level, this requirement is often difficult to supply. This note describes the zero bias Schottky diode detector and offers design equations for its use.

Publication No. 5963–0951E

AN 976
Broadband Microstrip Mixer Design, the Butterfly Mixer
A microstrip mixer on RT/duroid substrate is designed for the frequency range 8 GHz to 12 GHz. Hewlett-Packard Schottky barrier diode model 5082-2207 is used. Low impedance shunt transmission lines are difficult to realize and present a problem in this type of circuit. Radial line stubs are used to avoid this problem.

Publication No. 5954-2126

AN 979
The Handling and Bonding of Beam Lead Devices Made Easy
Beam Lead devices are particularly attractive for hybrid circuits because of their low parasitics and small size. The availability of equipment and techniques specifically designed for their small size has facilitated the handling and bonding of these devices. This application note describes some of this equipment and techniques, and outlines suggestions for the proper handling and bonding of Beam Lead devices.

Publication No. 5953-4435

AN 986
Square Law and Linear Detection
Frequency, diode capacitance, breaksown voltage, and load resistance all have an effect on the slope of a microwave detector. At high input levels the linearity may be controlled by proper tuning.

Publication No. 5953-4444

AN 987
Is Bias Currrent Necessary?
Bias current is often necessary to reduce the impedance of detector diodes to a reasonable level. However, when the signal level is high, rectified current may reduce the impedance without the need for bias current. Measurements with the 5082-2755 diode are used to illustrate the effect.

Publication No. 5953-4446

AN 988
All Schottky Diodes are Zero Bias Detectors
Diodes which are normally biased make excellent detectors when the bias is eliminated. It is necessary to use a load with an impedance comparable to the diode impedance. This is shown with a 5082-2755 diode used with a 3469B multimeter as the load.

Publication No. 5953-4449

AN 991
Harmonic Mixing with the HSCH-5530 Series Dual Diode
The dual diode on coplanar waveguide forms an antiparallel pair. This arrangement is excellent for mixers with subharmonic local oscillators. A mixer for 34 GHz was designed and built. Conversion loss was measured as a function of frequency and local oscillator power level.

Publication No. 5953-4492

AN 992
Beam Lead Attachment Methods
This application bulletin gives a general description of various methods of attaching beam lead components to both hard and soft substrates. A table summarizes the most common attachment methods with advantages, disadvantages, and equipment costs.

Publication No. 5091-9074E

AN 993
Beam Lead Diode Bonding to Soft Substrate
The hard gold surface on standard PC boards with soft substrate material makes it almost impossible to successfully bond beam lead diodes onto the boards with normally recommended thermocompression bonding. Described in this application note is a new method of resistive spot welding or modified gap welding, which uses a single electrode to weld the beam while the conductor is contacted separately. This method allows tight pressure to be used on the weld probe, resulting in an effective bond without damaging the beam lead device.

Publication No. 5954-2227

AN 995
The Schottky Diode Mixer
A major application of the Schottky diode is the production of the difference frequency when the two frequencies are combined or mixed in the diode. Mixing efficiency is measured by the conversion loss, the ratio of signal input power to intermediate frequency output power. This application note studies the effect on mixing efficiency of diode parasitics, local oscillator power level, DC bias, barrier voltage, and local resistance. The advantage of

multiple diode mixers is considered. Distortion products are also discussed.

Publication No. 5954-2073

AN 997
A 2 GHz Balanced Mixer Using SOT-23 Surface Mount Schottky Diodes
The HSMS-2822 is a series diode pair in the SOT-23 package—ideal for use in a balanced mixer. The microstrip matching circuit consists of open stubs between the diodes and the IF port.

Publication No. 5954-2090

AN 1052
A Low Cost, Surface Mount X-Band Mixer
This note describes the design and performance of a balanced X-Band mixer. The surface mount design uses low capacitance, SOT-23 packaged Schottky diodes and is useful for high volume applications such as DBS and VSAT.

Publication No. 5091-4934E

AN 1069
Non-RF Applications for the Surface Mount Schottky Diode
Today's advanced wafer processing and packaging technologies make low cost Schottky diodes practical for many non-RF applications. Yhis note describes the use of this ultra-fast, low voltage diode in clipping, clamping, overvoltage protection and other applications.

Publication No. 5962-9465E

AN 1089
Designing Detectors for RF/ID Tags
Severe cost, size and DC power constraints in RF/ID tags have forced designers to abandon superheterodyne receivers for the older and simpler crystal video receiver. Consisting of a simple detector circuit and a printed antenna, this receiver can be built for pennies. This note describes two zero bias detector circuits for such applications, one operating at 915 MHz and the other at 2.45 GHz. Design equations for diode selection are given, as well as techniques for the realization of practical impedance matching networks.

Publication No. 5966-0786E

AN 1088
Designing the Virtual Battery
Many of today's portable RF products, such as RF/ID tags used in automotive electronic toll tag applications, are too small to contain a battery sufficient to power them over their expected lifetime. Where such devices operate in the presence of a RF field, a simple and inexpensive circuit consisting of a printed antenna, one or more Schottky diodes and a few passive components can be designed to convert part of the illuminating RF field into DC power. This note presents design techniques and illustrates them with data obtained on prototype circuits.

Publication No. 5966-0785E

AN 1090
The Zero Bias Schottky Diode Detector at Temperature Extremes—Problems and Solutions
The zero bias Schottky diode detector is ideal for RF/ID tag applications where it can be used to fabricate a receiver which consumes no primary power. However, its performance is heavily dependent upon its saturation current, which is a strong function of temperature. At both low and high temperature extremes, this dependance can lead to degradation in performance. The behavior of zero bias Schottky diodes is analyzed, experimental data is given, and a solution to the loss of performance at cold temperatures is presented.

Publication No. 5966-0784E

AN 1124
Linear Models for Diode Surface Mount Packages
When linear or non-linear analyses are performed on diode circuits, both the diode chip and its package must be accurately modeled. Included in this application note are linear models and element values for SOT-23, -143, -323, and -363 diode packages.

Publication No. 5966-0399E

Applications Note/Product Chart

Application Note Number/Title		Surface Mount							
		HSMS -280x	HSMS -281x	HSMS -282x	HSMS -285x	HSMS -286x	HSMs -8x0x	Pkg'd	Beam Lead
923	Hot Carrier Diode Video Detectors			X	X	X		X	X
956-1	Criterion for Tangential Sensitivity Measurement			X	X	X		X	X
956-3	Flicker Noise in Schottky Diodes		X		X			X	
956-4	Schottky Diode Voltage Doubler			X	X	X		X	X
956-5	Dynamic Range Extension of Schottky Detectors			X	X	X		X	X
956-6	Temperature Dependence of Schottky Detectors			X	X	X	X	X	X
963	Impedance Matching Techniques			X	X	X		X	X
969	The Zero Bias Schottky Detector Diode				X				X
976	The Butterfly Mixer			X					
979	Handling and Bonding of Beam Lead Devices								X
986	Square LAw and Linear Detection			X	X	X		X	X
987	Is Bias Current Necessary?			X		X		X	X
988	All Schottky Diodes are Zero Bias Detectors			X		X		X	X
991	Harmonic Mixing with the HSCH-5530								X
992	Beam Lead Attachment Methods								X
993	Beam Lead Diode Bonding to Soft Substrates								X
995	The Schottky Diode Mixer			X			X	X	X
997	2 GHz Balanced Mixer using SOT-23 SMD Diodes			X			X		
1052	Low Cost, Surface Mount X-Band Mixer						X		
1069	Non-RF Applications for the SMD Schottky	X	X	X		X		X	
1089	Designing Detectors for RF/ID Tags			X	X	X			
1088	Designing the Virtual Battery			X	X	X			
1090	Zero Bias Schottky Detector at Temperature				X				X

Applications Information

Schottky Diode Fundamentals

The Schottky diode is a rectifying metal-semiconductor contact formed between a metal and n-doped or p-doped semiconductor. When a metal-semiconductor junction is formed, free electrons flow across the junction from the semiconductor and fill the free-energy states in the metal. This flow of electrons builds a depletion potential across the junction. The difference in energy levels between semiconductor and metal is called a Schottky barrier.

P-doped Schottky barrier diodes excel at applications requiring ultra low turn-on voltage (such as zero biased RF detectors), but their very low breakdown voltage and high series resistance make them unsuitable for the applications discussed in this note. As a result, we will focus entirely on n-doped Schottky diodes.

Under forward bias (metal connected to positive in an n-doped Schottky), there are many electrons with enough thermal energy to cross the barrier potential into the metal. Once the applied bias exceeds the built-in potential of the junction the forward current I_f will increase rapidly with increase in V_f. See Figure 2.

When the Schottky diode is reverse biased, the potential barrier for electrons becomes large; hence there is a small probability that an electron will have sufficient thermal energy to cross the junction. The reverse leakage current will be in the nanoampere range.

In contrast to a conventional p-n junction, current in the Schottky diode is carried only by majority carriers. Because no minority carrier charge storage effects are present, Schottky diodes have carrier lifetimes of less than 100 ps and are extremely fast switching semiconductors.

Another significant difference between Schottky and p-n diodes is the forward voltage drop. Schottky diodes have a threshold of typically 0.3 V compared to 0.6 V of p-n junction diodes. See Figure 2.

Using computer-controlled precision doped and formulated epitaxial silicon wafers through the carefully defined diameter of the Schottky contact and the choice of metal deposited on the n-doped silicon, important characteristics of the diode (junction capacitance C_j, parasitic series resistance R_S, breakdown voltage V_{br} and forward voltage V_f) can be tailored to specific applications. The HSMS-280A series and HSMS-282A series of diodes are a case in point, as is illustrated by their SPICE parameters. See Table 1.

The differences in these two lines of Schottky diodes can also be seen by examining their forward characteristics, as shown in Figure 3.

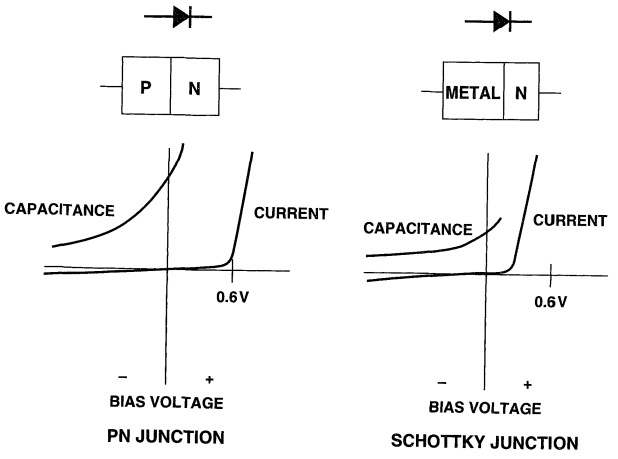


Figure 2.

Table 1.

Parameter	HSMS-280A	HSMS-282A
C_{J0}	1.6	0.7
V_{br}	75	15
R_S	30	6
E_G	0.69	0.69
I_{BV}	10.0E-5	10.0E-4
I_S	3.0E-8	2.2E-8
N	1.08	1.08
P_B	0.65	0.65
P_T	2	2
M	0.5	0.5

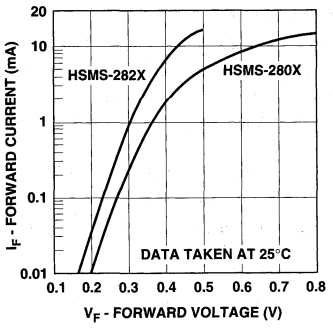


Figure 3. Forward Current vs. Forward Voltage.

It can be seen that, at low levels of forward current, the forward voltage of the HSMS-282A diode is slightly lower than that for the HSMS-280A. This is due to the lower barrier height of the former. At high values of forward current, V_f is lower for the HSMS-282A because of its lower R_S. The tradeoff, however, is a lower value of V_{br} for the HSMS-282A. Thus, the circuit designer has a choice of Schottky diode characteristics with which to optimize his circuit.

Clipping Circuits

Waveform Clipping

Illustrated in Figure 4 is a basic diode clipping circuit and its output waveform in response to a sinusoidal input. While the instantaneous value of the input voltage is less than the sum of the reference voltage V_{ref} and the diode turn-on voltage V_f, the diode is reverse-biased off, and the output waveform follows the input. When the input voltage becomes equal to or greater than $V_{ref} + V_f$, the corresponding output waveform exhibits clipping of the positive peak above the voltage $V_{ref} + V_f$. The flatness of this clipped portion is dependent upon the degree that the forward biased resistance R_d is less than the circuit resistance R, where R_d is the dynamic resistance of the diode.

Sine Wave to Square Wave Conversion

Double ended clipping (known as limiting) of signal waveforms can be accomplished with the use of a pair of diode clippers in a parallel series configuration shown in Figure 5. The use of the HSMS-28XC Schottky diode series pair helps to reduce the circuit layout size. If V_{ref1} is made equal to V_{ref2} and the amplitude of the sinusoidal input is sufficiently high, the output waveform will approach that of a square wave. This application represents in essence sine wave to square wave conversion.

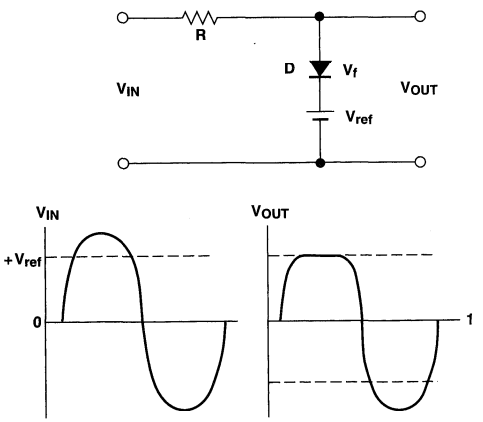


Figure 4.

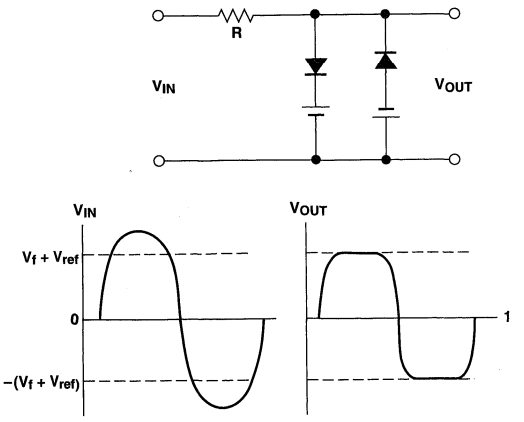


Figure 5.

Diode Requirements for Clipping Circuits

In clipping or limiting circuits, the forward bias diode resistance R_f must be much less than the circuit resistance R in order to maintain the flatness of the clipped portion of the waveform. The reverse bias resistance of the diode, R_T, must be much larger than R to avoid loading the circuit and distorting the waveform. These requirements are important in providing precise voltage reference in the circuits shown in Figures 4 and 5. Thus, the ratio of R_f/R_T can serve as a figure of merit for a clipping diode. The larger the ratio, the better the performance.

The low turn-on voltage of the HSMS-2800 series Schottky barrier diodes (particularly the HSMS-282A family) allows clipping and clamping closely to the desired reference level. The HSMS-280A family Schottky diodes has a high minimum breakdown voltage of 70 V and is suited for high voltage applications.

Voltage Protection of CMOS Gates

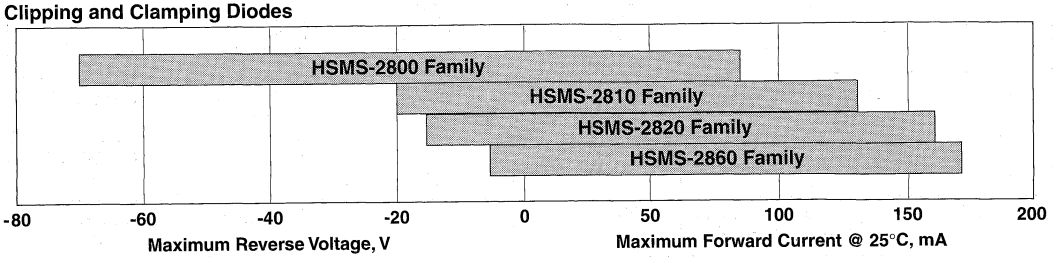
CMOS gates have a very high input resistance (typ. 50 MΩ) and a low output resistance of approximately 50 Ω. When an output gate is connected to an input gate using a microstrip transmission line, the line is terminated by the high input resistance of the input gate, thus it can be considered as "open". Due to the open transmission line a rising or falling signal will overshoot and can exceed the maximum or minimum allowed voltages (JEDEC) of the input gate. Usually "built-in" Schottky diodes are used to limit the input signal to V_{CC} + 0.5 V and –0.5 V because of its low turn-on voltage.

Quite often the "built-in" ESD protection diodes are too slow and connected via a resistor to the input pin of the integrated circuit. Therefore, external Schottky diodes connected to the power supply and ground line are necessary to provide a "dynamic" termination to the transmission line to clip the input signal below the JEDEC specification. It has been proved that the HSMS-282A series configuration Schottky diode pair, with its low turn-on voltage and fast switching response, is the best solution for such applications.

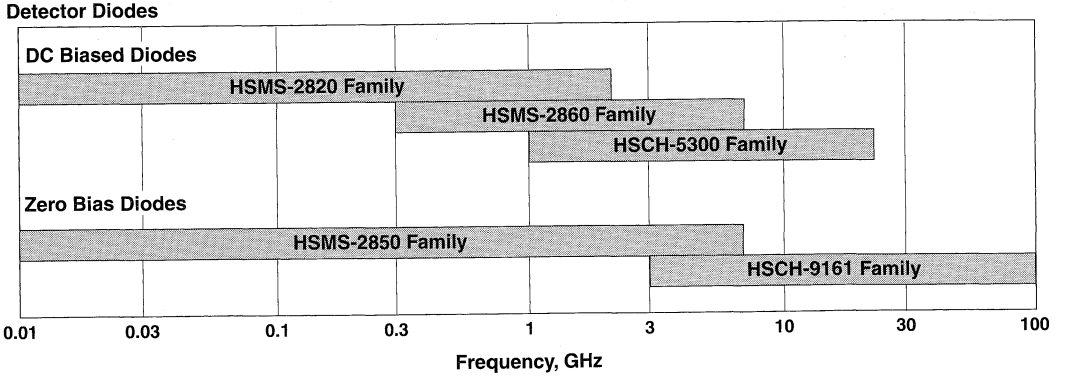
Schottky Diode Product Selection Guide

The following guides represent Hewlett-Packard's recommendations for most common applications. They do not include all the diodes described in this catalog. For detailed recommendations not covered in the following guides, contact the field sales office nearest you.

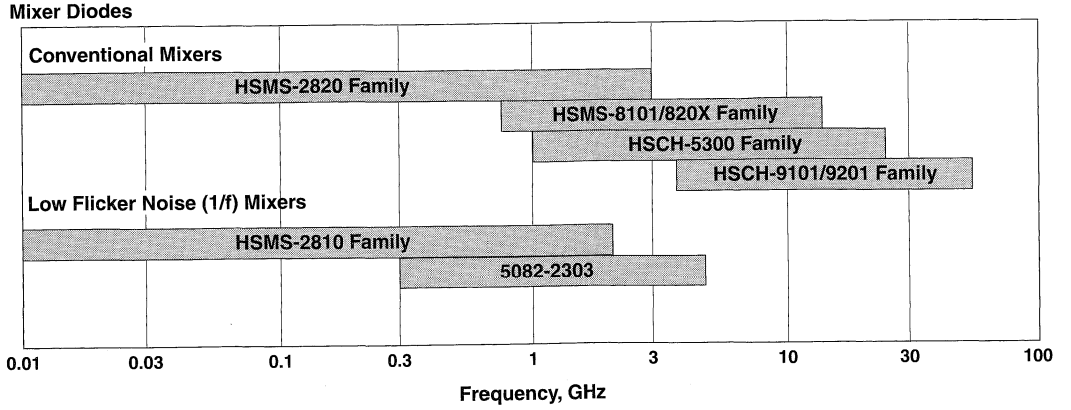
Clipping and Clamping Diodes



Detector Diodes



Mixer Diodes

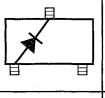
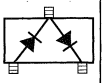
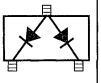
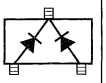
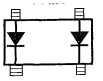
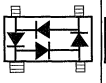
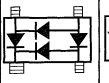
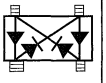
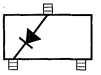
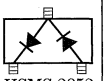
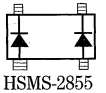
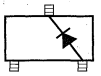
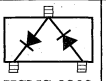
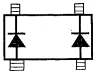
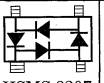


SOT-323 Surface Mount Schottky Diodes – Available Configurations

(also known as SC70 3-Lead)

SOT-23 Version	Application	Single 	Series Pair 	Common Anode 	Common Cathode 
HSMS-2800	High Breakdown Voltage	HSMS-280B A0	HSMS-280C A2	HSMS-280E A3	HSMS-280F A4
HSMS-2810	Low Flicker Noise Detector	HSMP-281B B0	HSMS-281C B2	HSMS-281E B3	HSMS-281F B4
HSMS-2820	Clipping/Clamping Switching, RF Detector & Mixer	HSMS-282B C0	HSMS-282C C2	HSMS-282E C3	HSMS-282F C4
HSMS-2850	High Frequency Zero Bias Detector	HSMS-285B P0	HSMS-285C P2	—	—
HSMS-2860	High Frequency Mixer, DC Biased Detector	HSMS-286B T0	HSMS-286C T2	HSMS-286E T3	HSMS-286F T4

SOT-23 and SOT-143 Surface Mount Schottky Diodes – Available Configurations

Application	SOT-23				SOT-143			
	Single	**Series Pair**	**Common Anode**	**Common Cathode**	**Unconnected Pair**	**Ring Quad**	**Bridge Quad**	**Crossover Quad**
								
High Breakdown Voltage	HSMS-2800 A0	HSMS-2802 A2	HSMS-2803 A3	HSMS-2804 A4	HSMS-2805 A5	HSMS-2807 A7	HSMS-2808 A8	
Low Flicker Noise Detector	HSMP-2810 B0	HSMS-2812 B2	HSMS-2813 B3	HSMS-2814 B4	HSMS-2815 B5	HSMS-2817 B7	HSMS-2818 B8	
Clipping/Clamping Switching, RF Detector & Mixer	HSMS-2820 C0	HSMS-2822 C2	HSMS-2823 C3	HSMS-2824 C4	HSMS-2825 C5	HSMS-2827 C7	HSMS-2828 C8	HSMS-2829 C9
High Frequency DC Biased	HSMS-2860 T0	HSMS-2862 T2	HSMS-2863 T3	HSMS-2864 T4	HSMS-2865 T5			
High Frequency Zero Bias Detector	 HSMS-2850 P0	 HSMS-2852 P2			 HSMS-2855 P5			
High Performance Mixer Diode	 HSMS-8101 R1	 HSMS-8202 2R			 HSMS-8205 R5	 HSMS-8207 R7		

Schottky Diode Selection Guides

SOT-23/-143 General Purpose Schottky-Barrier Diodes

Part Number	V_{BR} (V) (min)	V_F (mV) (max)	V_F @ I_F (V @ mA) (max)	C_t (pF) (max)	R_D (Ω) (typ)	Page
HSMS-282X	15	340	0.7 @ 30	1.0	12	3-36
HSMS-281X	20	400	1.0 @ 35	1.2	15	3-36
HSMS-280X	70	400	1.0 @ 15	2.0	35	3-36

The "X" in the above part numbers is replaced by "0" for a single diode configuration, "2" for a series pair, "3" for a common anode pair, "4" for a common cathode pair, all of the foregoing in SOT-23; and "5" for an unconnected pair, "7" for a ring quad, "8" for a bridge quad, and "9" (282X only) for a crossover quad in SOT-143.

SOT-23/-143 High Frequency Mixer Schottky-Barrier Diodes

Part Number	V_{BR} (V) (min)	V_F (mV) (min/max)	C_t (pF) (max)	R_D (Ω) (max)	Page
HSMS-8101 (single)	4	250/350	0.26	14	3-48
HSMS-820X	4	250/350	0.26	14	3-48

The "X" in the above part numbers is replaced by "2" for a series pair in SOT-23, and "5" for an unconnected pair, and "7" for a ring quad in SOT-143.

SOT-23/-143 Detector Schottky-Barrier Diodes

Part Number	V_{BR} (V) (min)	V_F (mV) (max)	C_t (pF) (typ)	Voltage Sensitivity (γ) (mV/μW) (typ @ 900 MHz)	R_V (KΩ) (typ)	Page
HSMS-285X	-	150	0.30	40	8.0	3-42
HSMS-286X	5	250	0.30	50	5.0	3-36, 42

The "X" in the above part numbers is replaced by "0" for a single diode configuration, "2" for a series pair, "3" for a common anode pair (286X only), "4" for a common cathode pair (286X only) all of the foregoing in SOT-23; and "5" for an unconnected pair in SOT-143.

Schottky Diode Selection Guide, continued

NEW SOT-323 Schottky-Barrier Diodes

Part Number	V_{BR} (V) (min)	V_F (mV) (max)	V_F @ I_F (V @ mA) (max)	C_t (pF) (typ)	R_D (Ω) (typ)	Volt. Sens. (γ) (mV/μW) (typ @ 900 MHz)	R_V (KΩ) (typ)	Page
HSMS-282A	15	340	0.7 @ 30	1.0	12	-	-	3-18
HSMS-281A	20	400	1.0 @ 35	1.2	15	-	-	3-18
HSMS-280A	70	400	1.0 @ 15	2.0	35	-	-	3-18
HSMS-285A	-	150	-	0.30	-	40	8.0	3-42
HSMS-286A	5	250	-	0.30	-	50	5.0	3-24

The "A" in the above part number is replaced by "B" for a single diode configuration, "C" for a series pair, "E" for a common anode pair, and "F" for a common cathode pair ("B" and "C" only for HSMS-285A).

Note:

1. See specific product data sheet for test conditions.

General Purpose Glass Schottky Diodes (Typical Specifications @ 25°C Case Temperature)

Part Number	V_{br} (V)	V_f @ 1 mA (mV)	C_t (pF)	Ir (nA)	Page
5082-2800 (1N5711)	70	410	2.0	200 @ 50 V	3-52
5082-2810 (1N5712)	20	410 (550)	1.2	100 (150) @ 15 V	3-52
5082-2811	15	410	1.2	100 @ 8 V	3-52
5082-2835	8	340	1.0	100 @ 1 V	3-52

Beam Lead Silicon Schottky Diodes (Typical Specifications @ 25°C Case Temperature)

Part Number	V_{br} (V)	R_s @ I_f = 5 mA (Ohms)	V_f @ 1 mA (mV)	Delta V_f (mV)	C_t (pF)	Delta C_t (pF)	Page
HSCH-5312 (single)	4	11	500	—	0.15	—	3-64
HSCH-5332 (single)	4	11	375	—	0.15	—	3-64
HSCH-5512 (series pair)	4	11	500	10	0.15	0.03	3-64
HSCH-5531 (series pair)	4	15	375	10	0.10	0.02	3-64

Beam Lead GaAs Schottky Barrier Diodes

Part Number	C_{total} (pF)	R_s (Ohms)	B_v @ -10 μA (V)	V_F @ 1 mA (mV)	Type	Page
HSCH-9101	0.040	6	> 4.5	700	single	3-76
HSCH-9201	0.040	6	> 4.5	700	series pair	3-76
HSCH-9251	0.040	6	> 4.5	700	antiparallel pair	3-76
HSCH-9301	0.075	6	> 4.5	700	ring quad	3-79
HSCH-9351	0.075	6	> 4.5	700	bridge quad	3-79

Zero-Bias Beam Lead GaAs Detector Diodes

Part Number	C_j (pF)	R_v Max. (kΩ)	Γ (mV/μW)	Functional through (GHz)	Page
HSCH-9161	0.035	7.5	0.5	110	3-83

HEWLETT® PACKARD

Surface Mount RF Schottky Diodes in SOT-323 (SC-70)

Technical Data

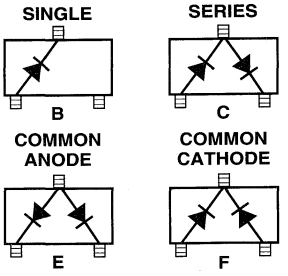
HSMS-280A Series
HSMS-281A Series
HSMS-282A Series

Features

- **Surface Mount SOT-323 Package**
- **Low Turn-On Voltage (As Low as 0.34 V at 1 mA)**
- **Low FIT (Failure in Time) Rate***
- **Six-sigma Quality Level**
- **Single and Dual Versions**
- **Tape and Reel Options Available**

* For more information see the Surface Mount Schottky Reliability Data Sheet.

Package Lead Code Identification (Top View)



Description/Applications

These Schottky diodes are specifically designed for analog and digital applications requiring devices in SOT-323 surface mount packages. This series offers a wide range of specifications and package configurations to give the designer wide flexibility. Typical applications of these Schottky diodes are mixing, detecting, switching, sampling, clamping, and wave shaping.

Absolute Maximum Ratings, T_C= 25°C

Symbol	Parameter	Unit	Absolute Maximum[1]
I_f	Forward Current (1μs Pulse)	Amp	1
P_{IV}	Peak Inverse Voltage	V	Same as V_{BR}
T_J	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	300

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications, T_C = +25°C, Single Diode[1]

Part Number HSMS-	Package Marking Code[2]	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	Maximum Forward Voltage V_F (V) @ I_F (mA)	Maximum Reverse Leakage I_R (nA) @ V_R (V)	Maximum Capacitance C_T (pF)	Typical Dynamic Resistance R_D (Ω)
280B	A0	B	Single	70	400	1.0 15	200 50	2.0	35
280C	A2	C	Series						
280E	A3	E	Common Anode						
280F	A4	F	Common Cathode						
281B	B0	B	Single	20	400	1.0 35	200 15	1.2	15
281C	B2	C	Series						
281E	B3	E	Common Anode						
281F	B4	F	Common Cathode						
282B	C0	B	Single	15	340	0.7 30	100 1	1.0	12
282C	C2	C	Series						
282E	C3	E	Common Anode						
282F	C4	F	Common Cathode						
Test Conditions				I_R = 10 µA	I_F = 1 mA[3]			V_F = 0 V f = 1 MHz[4]	I_F = 5 mA

Notes:

1. Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 5 mA, except HSMS-282X which is measured at 20 mA.
2. Package marking code is laser marked.
3. ΔV_F for diodes in pairs is 15.0 mV maximum at 1.0 mA.
4. ΔC_{TO} for diodes in pairs is 0.2 pF maximum.

Typical Performance, T_C = 25°C (unless otherwise noted), Single Diode

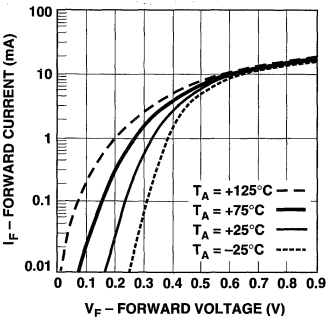


Figure 1. Forward Current vs. Forward Voltage at Temperatures—HSMS-280A Series.

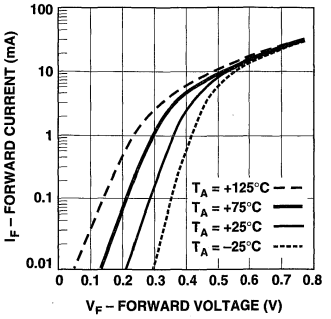


Figure 2. Forward Current vs. Forward Voltage at Temperatures—HSMS-281A Series.

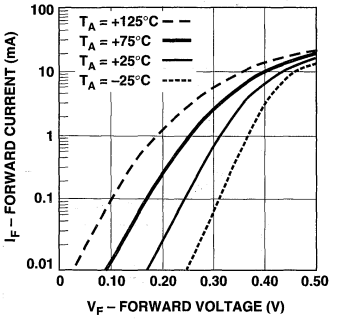


Figure 3. Forward Current vs. Forward Voltage at Temperatures—HSMS-282A Series.

Typical Performance, T_C = 25°C (unless otherwise noted), Single Diode, continued

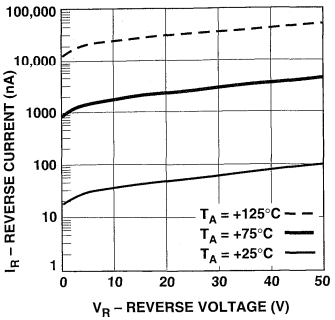


Figure 4. Reverse Current vs. Reverse Voltage at Temperatures—HSMS-280A Series.

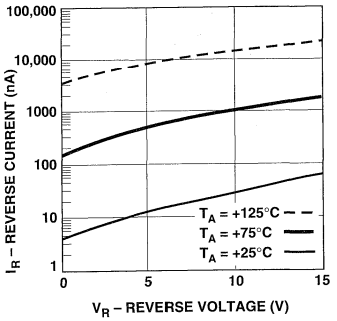


Figure 5. Reverse Current vs. Reverse Voltage at Temperatures—HSMS-281A Series.

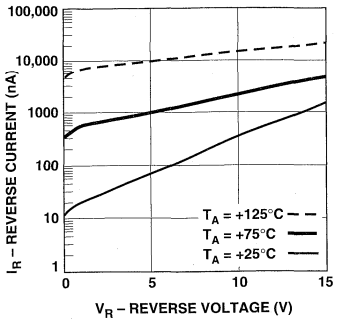


Figure 6. Reverse Current vs. Reverse Voltage at Temperatures—HSMS-282A Series.

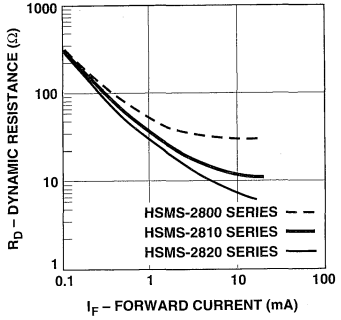


Figure 7. Dynamic Resistance vs. Forward Current.

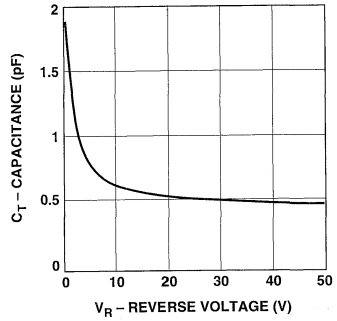


Figure 8. Total Capacitance vs. Reverse Voltage—HSMS-280A Series.

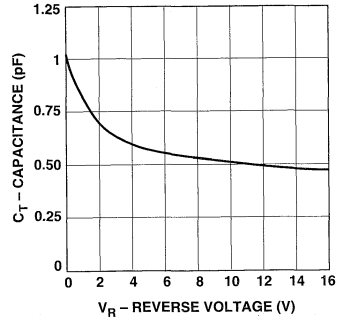


Figure 9. Total Capacitance vs. Reverse Voltage—HSMS-281A Series.

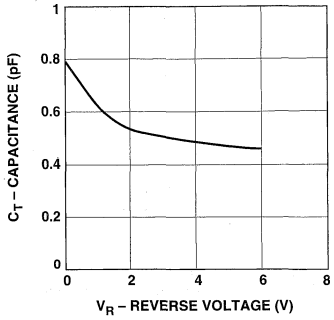


Figure 10. Total Capacitance vs. Reverse Voltage—HSMS-282A Series.

Assembly Instructions

SOT-323 PCB Footprint

A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 11 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.

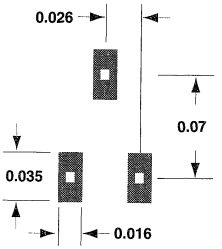


Figure 11. PCB Pad Layout (dimensions in inches).

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-323 package, will reach solder reflow temperatures faster than those with a greater mass.

HP's SOT-323 diodes have been qualified to the time-temperature profile shown in Figure 12. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235 °C.

These parameters are typical for a surface mount assembly process for HP SOT-323 diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

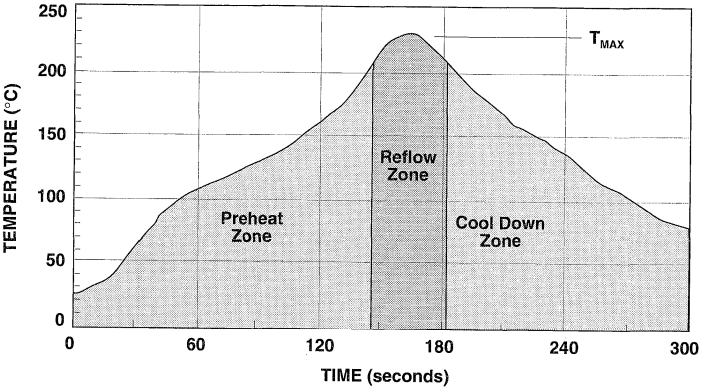
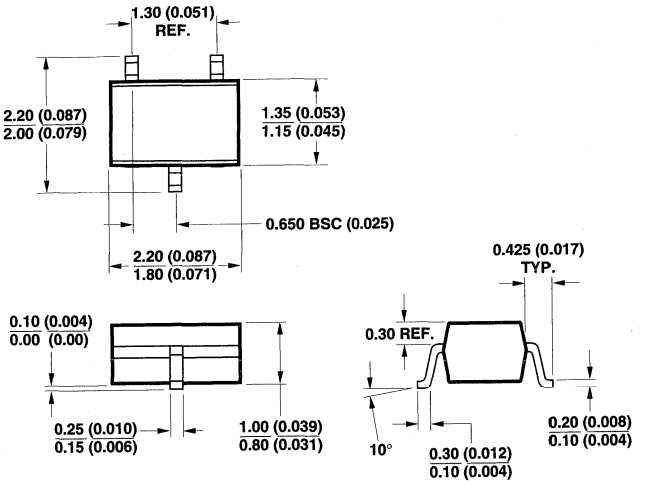


Figure 12. Surface Mount Assembly Profile.

Package Dimensions

Outline SOT-323 (SC-70 3 Lead)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

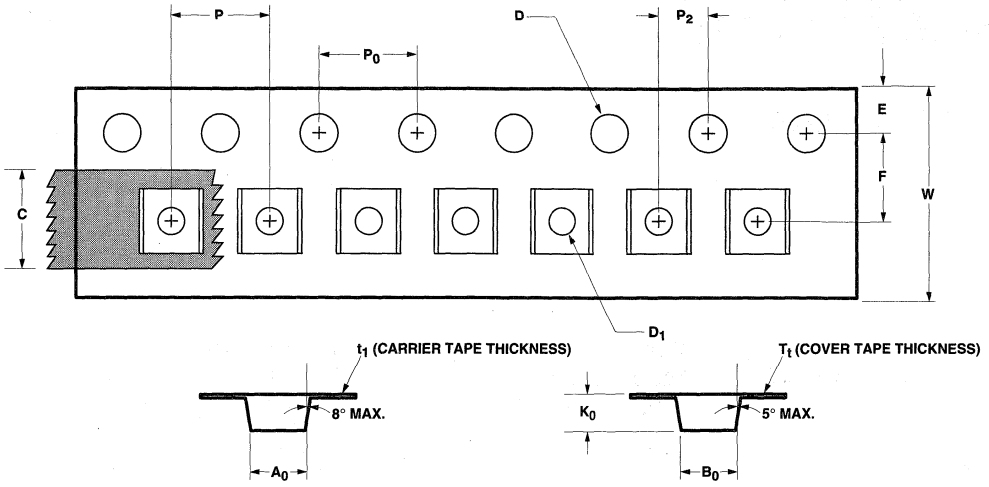
Part Number Ordering Information

Part Number	No. of Devices	Container
HSMS-28XA-TR1*	3000	7" Reel
HSMS-28XA-BLK*	100	antistatic bag

* where X = 0, 1, or 2; A = B, C, E, or F

Tape Dimensions and Product Orientation

For Outline SOT-323 (SC-70 3 Lead)



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

Surface Mount Microwave Schottky Detector Diodes in SOT-323 (SC-70)

Technical Data

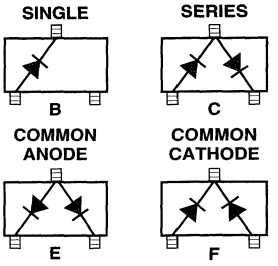
HSMS-285A Series
HSMS-286A Series

Features

- **Surface Mount SOT-323 Package**
- **High Detection Sensitivity:**
  Up to 50 mV/μW at 915 MHz
  Up to 35 mV/μW at 2.45 GHz
  Up to 25 mV/μW at 5.80 GHz
- **Low Flicker Noise:**
  -162 dBV/Hz at 100 Hz
- **Low FIT (Failure in Time) Rate***
- **Tape and Reel Options Available**

* For more information see the Surface Mount Schottky Reliability Data Sheet.

Package Lead Code Identification (Top View)



Description

Hewlett-Packard's HSMS-285A family of zero bias Schottky detector diodes and the HSMS-286A family of DC biased detector diodes have been designed and optimized for use from 915 MHz to 5.8 GHz. They are ideal for RF/ID and RF Tag, cellular and other consumer applications requiring small and large signal detection, modulation, RF to DC conversion or voltage doubling.

Available in various package configurations, these two families of detector diodes provide low cost solutions to a wide variety of design problems. Hewlett-Packard's manufacturing techniques assure that when two diodes are mounted into a single SOT-323 package, they are taken from adjacent sites on the wafer, assuring the highest possible degree of match.

DC Electrical Specifications, T_C = +25°C, Single Diode

Part Number HSMS-	Package Marking Code[1]	Lead Code	Configuration	Maximum Forward Voltage V_F (mV)		Typical Capacitance C_T (pF)
285B	P0	B	Single[2]	150	250	0.30
285C	P2	C	Series Pair[2,3]			
286B	T0	B	Single[4]	250	350	0.25
286C	T2	C	Series Pair[2,3]			
286E	T3	E	Common Anode[2,3]			
286F	T4	F	Common Cathode[2,3]			
Test Conditions				I_F = 0.1 mA	I_F = 1.0 mA	V_R = 0.5 V to -1.0 V f = 1 MHz

Notes:
1. Package marking code is laser marked.
2. ΔV_F for diodes in pairs is 15.0 mV maximum at 1.0 mA.
3. ΔC_T for diodes in pairs is 0.05 pF maximum at -0.5 V.

RF Electrical Parameters, T_C = +25°C, Single Diode

Part Number	Typical Tangential Sensitivity TSS (dBm) @ f =			Typical Voltage Sensitivity γ (mV/μW) @ f =			Typical Video Resistance R_v (KΩ)
HSMS-	915 MHz	2.45 GHz	5.8 GHz	915 MHz	2.45 GHz	5.8 GHz	
285B 285C	-57	-56	-55	40	30	22	8.0
Test Conditions	Video Bandwidth = 2 MHz Zero Bias			Power in = 40 dBm R_L = 100 LW, Zero Bias			
286B 286C 286E 286F	-57	-56	-55	50	35	25	5.0
Test Conditions	Video Bandwidth = 2 MHz I_b = 5 μA			Power in = −40 dBm R_L = 100 KΩ, I_b = 5 μA			

Absolute Maximum Ratings, T_C = 25°C, Single Diode

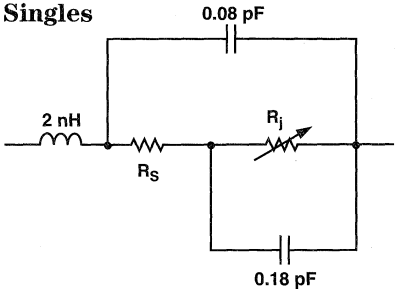
Symbol	Parameter	Unit	Absolute Maximum[1]
P_{IV}	Peak Inverse Voltage	V	2.0
T_J	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
T_{OP}	Operating Temperature	°C	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	350[2]

ESD WARNING: **Handling Precautions Should Be Taken To Avoid Static Discharge.**

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Equivalent Circuit Model HSMS-285B, HSMS-286B Singles



R_S = series resistance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5}\ nT}{I_b + I_s}$$

where
I_b = externally applied bias current in amps
I_s = saturation current (see table of SPICE parameters)
T = temperature, °K
n = identity factor (see table of SPICE parameters)

SPICE Parameters

Parameter	Units	HSMS-285A	HSMS-286A
B_V	V	3.8	7.0
C_{JO}	pF	0.18	0.18
E_G	eV	0.69	0.69
I_{BV}	A	3 x 10E-4	10E-5
I_S	A	3 x 10E-6	5 x 10E-8
N		1.06	1.08
R_S	Ω	25	5.0
P_B (V_J)	V	0.35	0.65
P_T (XTI)		2	2
M		0.5	0.5

Typical Parameters, Single Diode

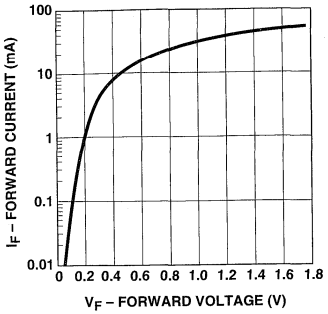


Figure 1. +25°C Forward Current vs. Forward Voltage, HSMS-285A Series.

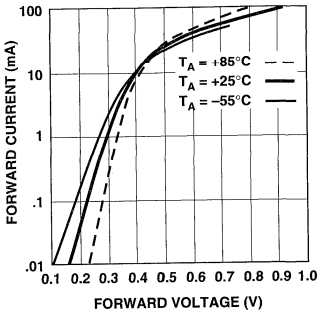


Figure 2. Forward Current vs. Forward Voltage at Temperature, HSMS-286A Series.

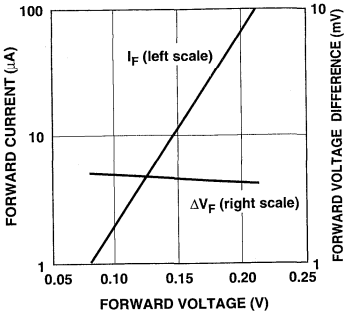


Figure 3. Forward Voltage Match, HSMS-286C, E and F Pairs.

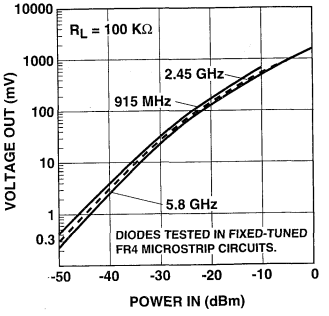


Figure 4. +25°C Output Voltage vs. Input Power, HSMS-285A Series at Zero Bias, HSMS-286A Series at 3 μA Bias.

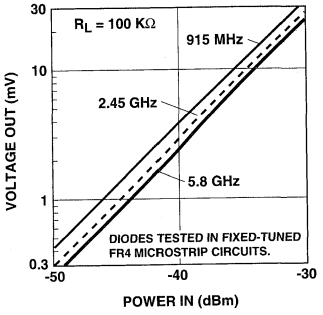


Figure 5. +25°C Expanded Output Voltage vs. Input Power. See Figure 4.

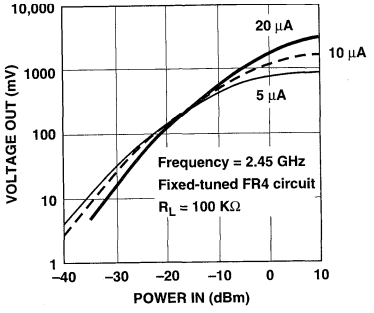


Figure 6. Dynamic Transfer Characteristic as a Function of DC Bias, HSMS-286A.

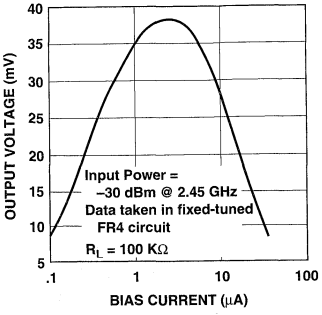


Figure 7. Voltage Sensitivity as a Function of DC Bias Current, HSMS-286A.

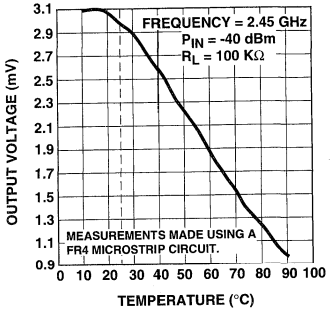


Figure 8. Output Voltage vs. Temperature, HSMS-285A Series.

Applications Information

Introduction

Hewlett-Packard's family of HSMS-285A zero bias Schottky diodes have been developed specifically for low cost, high volume detector applications where bias current is not available. The HSMS-286A family of DC Schottky diodes have been developed for low cost, high volume detector applications where stability over temperature is an important design consideration.

Schottky Barrier Diode Characteristics

Stripped of its package, a Schottky barrier diode chip consists of a metal-semiconductor barrier formed by deposition of a metal layer on a semiconductor. The most common of several different types, the passivated diode, is shown in Figure 9, along with its equivalent circuit.

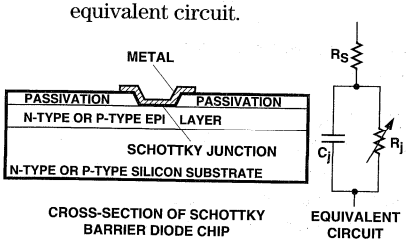


Figure 9. Schottky Diode Chip.

R_S is the parasitic series resistance of the diode, the sum of the bondwire and leadframe resistance, the resistance of the bulk layer of silicon, etc. RF energy coupled into R_S is lost as heat—it does not contribute to the rectified output of the diode. C_J is parasitic junction capacitance of the diode, controlled by the thickness of the epitaxial layer and the diameter of the Schottky contact. R_j is the junction resistance of the diode, a function of the total current flowing through it.

$$R_j = \frac{8.33 \times 10^{-5}\, n\, T}{I_S + I_b} = R_V - R_s$$

$$= \frac{0.026}{I_S + I_b} \text{ at } 25°C$$

where

n = ideality factor (see table of SPICE parameters)

T = temperature in °K

I_S = saturation current (see table of SPICE parameters)

I_b = externally applied bias current in amps

I_S is a function of diode barrier height, and can range from picoamps for high barrier diodes to as much as 5 μA for very low barrier diodes.

The Height of the Schottky Barrier

The current-voltage characteristic of a Schottky barrier diode at room temperature is described by the following equation:

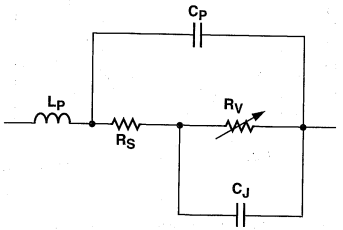
$$I = I_S \left(\exp\left(\frac{V - IR_S}{0.026}\right) - 1\right)$$

On a semi-log plot (as shown in the HP catalog) the current graph will be a straight line with inverse slope 2.3 X 0.026 = 0.060 volts per cycle (until the effect of R_S is seen in a curve that droops at high current). All Schottky diode curves have the same slope, but not necessarily the same value of current for a given voltage. This is determined by the saturation current, I_S, and is related to the barrier height of the diode.

Through the choice of p-type or n-type silicon, and the selection of metal, one can tailor the characteristics of a Schottky diode. Barrier height will be altered, and at the same time C_J and R_S will be changed. In general, very low barrier height diodes (with high values of I_S, suitable for zero bias applications) are realized on p-type silicon. Such diodes suffer from higher values of R_S than do the n-type. Thus, p-type diodes are generally reserved for detector applications (where very high values of R_V swamp out high R_S) and n-type diodes are used for mixer applications (where high L.O. drive levels keep R_V low).

Measuring Diode Parameters

The measurement of the five elements which make up the equivalent circuit for a packaged Schottky diode (see Figure 10) is a complex task. Various techniques are used for each element. The task begins with the elements of the diode chip itself.



FOR THE HSMS-285A or HSMS-286A SERIES
C_P = 0.08 pF
L_P = 2 nH
C_J = 0.18 pF
R_S = 25 Ω
R_V = 9 KΩ

Figure 10. Equivalent Circuit of a Schottky Diode.

R_S is perhaps the easiest to measure accurately. The V-I curve is measured for the diode under forward bias, and the slope of the curve is taken at some relatively high value of current (such as 5 mA). This slope is converted into a resistance R_d.

$$R_S = R_d - \frac{0.026}{I_f}$$

R_V and C_J are very difficult to measure. Consider the impedance of C_J = 0.16 pF when measured at 1 MHz — it is approximately 1 MΩ.

For a well designed zero bias Schottky, R_V is in the range of 5 to 25 KΩ, and it shorts out the junction capacitance. Moving up to a higher frequency enables the measurement of the capacitance, but it then shorts out the video resistance. The best measurement technique is to mount the diode in series in a 50 Ω microstrip test circuit and measure its insertion loss at low power levels (around -20 dBm) using an HP8753C network analyzer. The resulting display will appear as shown in Figure 11.

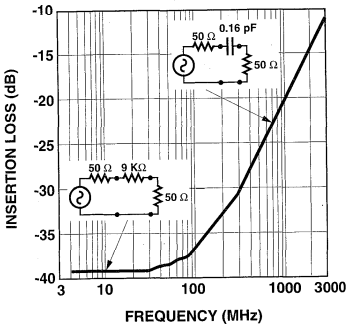


Figure 11. Measuring C_J and R_V.

At frequencies below 10 MHz, the video resistance dominates the loss and can easily be calculated from it. At frequencies above 300 MHz, the junction capacitance sets the loss, which plots out as a straight line when frequency is plotted on a log scale. Again, calculation is straightforward.

L_P and C_P are best measured on the HP8753C, with the diode terminating a 50 Ω line on the input port. The resulting tabulation of S_{11} can be put into a microwave linear analysis program having the five element equivalent circuit with R_V, C_J and R_S fixed. The optimizer can then adjust the values of L_P and C_P until the calculated S_{11} matches the measured values. Note that extreme care must be taken to de-embed the parasitics of the 50 Ω test fixture.

Detector Circuits

When DC bias is available, Schottky diode detector circuits can be used to create low cost RF and microwave receivers with a sensitivity of -55 dBm to -57 dBm.[1] Moreover, since external DC bias sets the video impedance of such circuits, they display classic square law response over a wide range of input power levels[2,3]. These circuits can take a variety of forms, but in the most simple case they appear as shown in Figure 12. This is the basic detector circuit used with the HSMS-286A family of diodes.

Where DC bias is not available, a zero bias Schottky diode is used to replace the conventional Schottky in these circuits, and bias choke L_1 is eliminated. The circuit then is reduced to a diode, an RF impedance matching network and (if required) a DC return choke and a capacitor. This is the basic detector circuit used with the HSMS-285A family of diodes.

In the design of such detector circuits, the starting point is the equivalent circuit of the diode, as shown in Figure 10.

Of interest in the design of the video portion of the circuit is the diode's video impedance—the other four elements of the equivalent circuit disappear at all reasonable video frequencies. In general, the lower the diode's video impedance, the better the design.

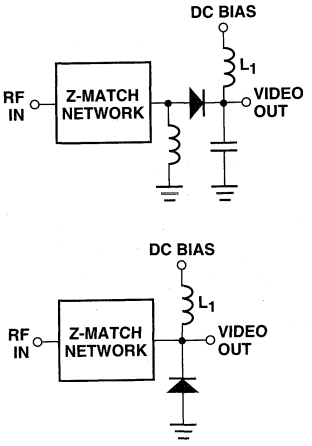


Figure 12. Basic Detector Circuits.

The situation is somewhat more complicated in the design of the RF impedance matching network, which includes the package inductance and capacitance (which can be tuned out), the series resistance, the junction capacitance and the video resistance. Of these five elements of the diode's equivalent circuit, the four parasitics are constants and the video resistance is a function of the current flowing through the diode.

[1] Hewlett-Packard Application Note 923, *Schottky Barrier Diode Video Detectors.*

[2] Hewlett-Packard Application Note 986, *Square Law and Linear Detection.*

[3] Hewlett-Packard Application Note 956-5, *Dynamic Range Extension of Schottky Detectors.*

$$R_V \approx \frac{26{,}000}{I_S + I_b}$$

where

I_S = diode saturation current in μA

I_b = bias current in μA

Saturation current is a function of the diode's design,[4] and it is a constant at a given temperature. For the HSMS-285A series, it is typically 3 to 5 μA at 25°C. For the medium barrier HSMS-2860 family, saturation current at room temperature is on the order of 50 nA.

Together, saturation and (if used) bias current set the detection sensitivity, video resistance and input RF impedance of the Schottky detector diode. Since no external bias is used with the HSMS-285A series, a single transfer curve at any given frequency is obtained, as shown in Figure 4. Where bias current is used, some tradeoff in sensitivity and square law dynamic range is seen, as shown in Figure 6 and described in reference [3].

The most difficult part of the design of a detector circuit is the input impedance matching network. For very broadband detectors, a shunt 60 Ω resistor will give good input match, but at the expense of detection sensitivity.

When maximum sensitivity is required over a narrow band of frequencies, a reactive matching network is optimum. Such networks can be realized in either lumped or distributed elements, depending upon frequency, size constraints and cost limitations, but certain general design principals exist for all types.[5] Design work begins with the RF impedance of the HSMS-285A series, which is given in Figure 13. Note that the impedance of the HSMS-286A series is very similar when bias current is set to 3 μA.

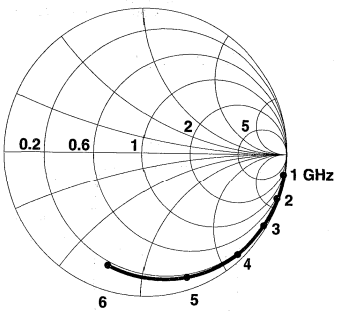


Figure 13. RF Impedance of the HSMS-285A Series at -40 dBm.

915 MHz Detector Circuit

Figure 14 illustrates a simple impedance matching network for a 915 MHz detector.

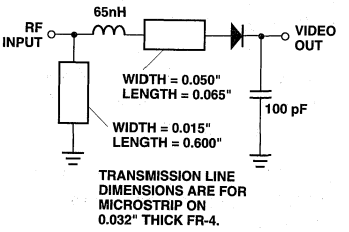


Figure 14. 915 MHz Matching Network for the HSMS-285A Series at Zero Bias or the HSMS-286A Series at 3 μA Bias.

A 65 nH inductor rotates the impedance of the diode to a point on the Smith Chart where a shunt inductor can pull it up to the center. The short length of 0.065" wide microstrip line is used to mount the lead of the diode's SOT-323 package. A shorted shunt stub of length <λ/4 provides the necessary shunt inductance and simultaneously provides the return circuit for the current generated in the diode. The impedance of this circuit is given in Figure 15.

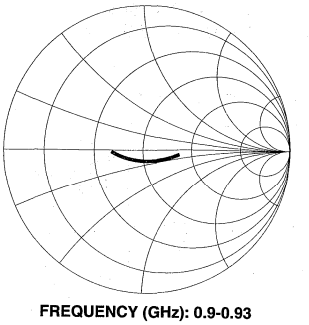


Figure 15. Input Impedance.

The input match, expressed in terms of return loss, is given in Figure 16.

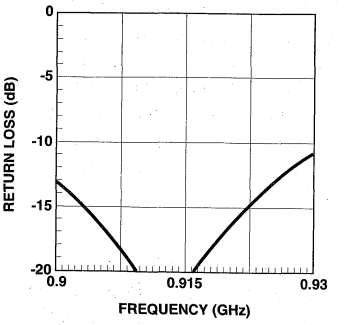


Figure 16. Input Return Loss.

As can be seen, the band over which a good match is achieved is more than adequate for 915 MHz RFID applications.

[4] Hewlett-Packard Application Note 969, *An Optimum Zero Bias Schottky Detector Diode.*

[5] Hewlett-Packard Application Note 963, *Impedance Matching Techniques for Mixers and Detectors.*

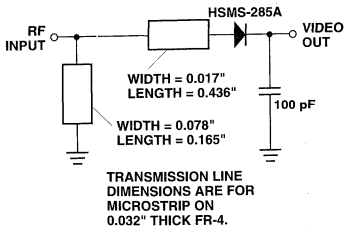


Figure 17. 2.45 GHz Matching Network for the HSMS-285A Series.

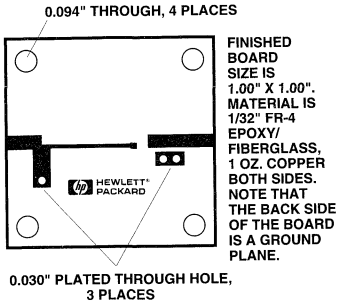


Figure 18. Physical Realization.

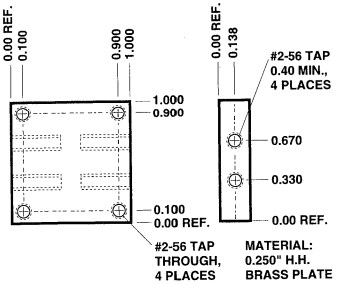


Figure 19. Mounting Plate.

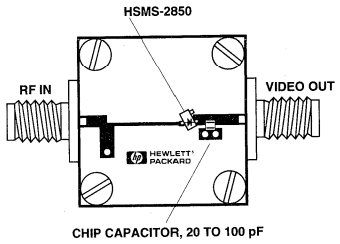


Figure 20. Test Detector.

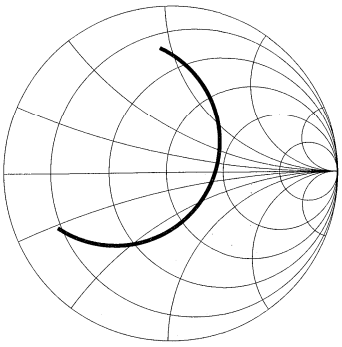


Figure 21. Input Impedance.

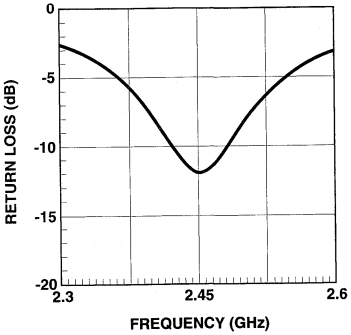


Figure 22. Input Return Loss.

2.45 GHz Detector Circuit

At 2.45 GHz, the RF impedance of the HSMS-285A series is closer to the line of constant susceptance which passes through the center of the chart, resulting in a design which is realized entirely in distributed elements — see Figure 17.

In order to save cost (at the expense of having a larger circuit), an open circuit shunt stub could be substituted for the chip capacitor. On the other hand, if space is at a premium, the long series transmission line at the input to the diode can be replaced with a lumped inductor.

A possible physical realization of such a network is shown in Figure 18.

This board is mounted on the brass or aluminum mounting plate shown in Figure 19.

Two SMA connectors (E.F. Johnson 142-0701-631 or equivalent), a high-Q capacitor (ATC 100A101MCA50 or equivalent), miscellaneous hardware and an HSMS-285B are added to create the test circuit shown in Figure 20.

The calculated input impedance for this network is shown in Figure 21.

The corresponding input match is shown in Figure 22. As was the case with the lower frequency design, bandwidth is more than adequate for the intended RFID application. Note that this same design applies to the HSMS-286A series when it is used with 3 to 5 μA of external bias.

A word of caution to the designer is in order. A glance at Figure 21 will reveal the fact that the circuit does not provide the optimum impedance to the diode at 2.45 GHz. The temptation will be to adjust the circuit elements to achieve an ideal single frequency match, as illustrated in Figure 23.

This does indeed result in a very good match at midband, as shown in Figure 24.

However, bandwidth is narrower and the designer runs the risk of a shift in the midband frequency of his circuit if there is any small deviation in circuit board or diode characteristics due to lot-to-lot variation or change in temperature. The matching technique illustrated in Figure 21 is much less sensitive to changes in diode and circuit board processing.

5.8 GHz Detector Circuit

A possible design for a 5.8 GHz detector is given in Figure 25.

As was the case at 2.45 GHz, the circuit is entirely distributed element, both low cost and compact. Input impedance for this network is given in Figure 26.

Input return loss, shown in Figure 27, exhibits wideband match.

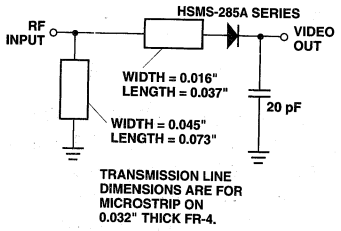


Figure 25. 5.8 GHz Matching Network for the HSMS-285A Series at Zero Bias or the HSMS-286A Series at 3 μA Bias.

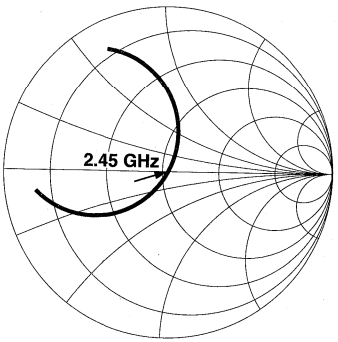


Figure 23. Input Impedance. Modified 2.45 GHz Circuit.

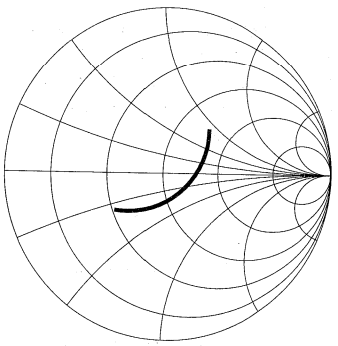


Figure 26. Input Impedance.

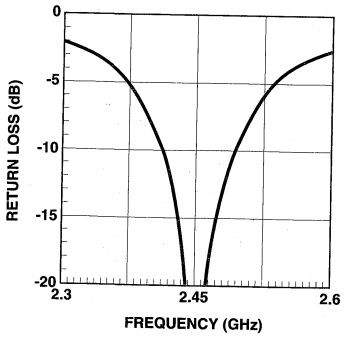


Figure 24. Input Return Loss. Modified 2.45 GHz Circuit.

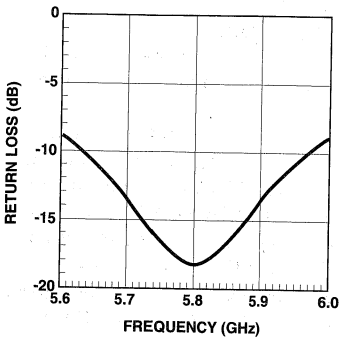


Figure 27. Input Return Loss.

Voltage Doublers

To this point, we have restricted our discussion to single diode detectors. A glance at Figure 12, however, will lead to the suggestion that the two types of single diode detectors be combined into a two diode voltage doubler[6] (known also as a full wave rectifier). Such a detector is shown in Figure 28.

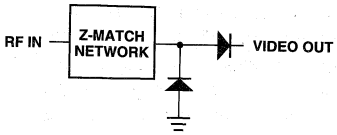


Figure 28. Voltage Doubler Circuit.

Such a circuit offers several advantages. First the voltage outputs of two diodes are added in series, increasing the overall value of voltage sensitivity for the network (compared to a single diode detector). Second, the RF impedances of the two diodes are added in parallel, making the job of reactive matching a bit easier. Such a circuit can easily be realized using the two series diodes in the HSMS-285C or the HSMS-286C.

The "Virtual Battery"

The voltage doubler can be used as a virtual battery, to provide power for the operation of an I.C. or a transistor oscillator in a tag. Illuminated by the CW signal from a reader or interrogator, the Schottky circuit will produce power sufficient to operate an I.C. or to charge up a capacitor for a burst transmission from an oscillator. Where such virtual batteries are employed, the bulk, cost, and limited lifetime of a battery are eliminated.

[6] Hewlett-Packard Application Note 956-4, *Schottky Diode Voltage Doubler.*

Flicker Noise

Reference to Figure 5 will show that there is a junction of metal, silicon, and passivation around the rim of the Schottky contact. It is in this three-way junction that flicker noise[7] is generated. This noise can severely reduce the sensitivity of a crystal video receiver utilizing a Schottky detector circuit if the video frequency is below the noise corner. Flicker noise can be substantially reduced by the elimination of passivation, but such diodes cannot be mounted in non-hermetic packages. p-type silicon Schottky diodes have the least flicker noise at a given value of external bias (compared to n-type silicon or GaAs). At zero bias, such diodes can have extremely low values of flicker noise. For the HSMS-285A series, the noise temperature ratio is given in Figure 29.

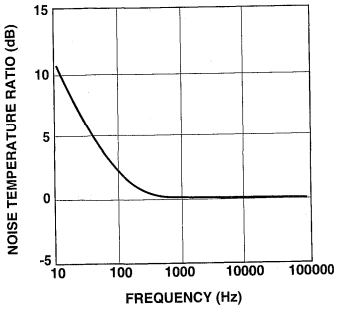


Figure 29. Typical Noise Temperature Ratio.

Noise temperature ratio is the quotient of the diode's noise power (expressed in dBV/Hz) divided by the noise power of an ideal resistor of resistance $R = R_V$.

For an ideal resistor R, at 300°K, the noise voltage can be computed from

$$v = 1.287 \times 10^{-10} \sqrt{R} \text{ volts/Hz}$$

which can be expressed as

$$20 \log_{10} v \quad \text{dBV/Hz}$$

Thus, for a diode with $R_V = 9$ KΩ, the noise voltage is 12.2 nV/Hz or -158 dBV/Hz. On the graph of Figure 26, -158 dBV/Hz would replace the zero on the vertical scale to convert the chart to one of absolute noise voltage vs. frequency.

Temperature Compensation

The compression of the detector's transfer curve is beyond the scope of this data sheet, but some general comments can be made. As was given earlier, the diode's video resistance is given by

$$R_V = \frac{8.33 \times 10^{-5} \text{ nT}}{I_S + I_b}$$

where T is the diode's temperature in °K.

As can be seen, temperature has a strong effect upon R_V, and this will in turn affect video bandwidth and input RF impedance. A glance at Figure 7 suggests that the proper choice of bias current in the HSMS-286A series can minimize variation over temperature.

The detector circuits described earlier were tested over temperature. The 915 MHz voltage doubler using the HSMS-286C series pair produced the output voltages as shown in Figure 30. The use of 3 μA of bias resulted in the highest voltage sensitivity, but at the cost of a wide variation over temperature. Dropping the bias to 1 μA produced a detector with much less temperature variation.

A similar experiment was conducted with the HSMS-286B in the 5.8 GHz detector. Once again, reducing the bias to some level under 3 μA stabilized the output of the detector over a wide temperature range.

It should be noted that curves such as those given in Figures 30 and 31 are highly dependent upon the exact design of the input impedance matching network. The designer will have to experiment with bias current using his specific design.

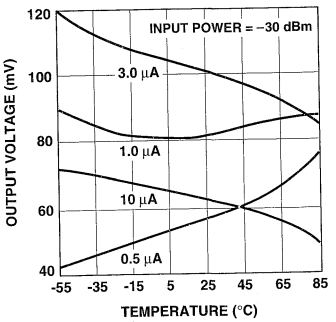


Figure 30. Output Voltage vs. Temperature and Bias Current in the 915 MHz Voltage Doubler using the HSMS-286C.

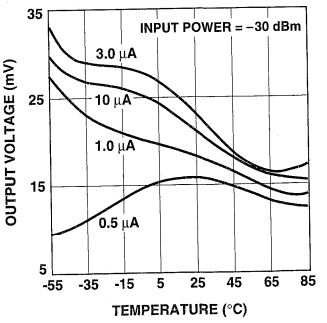


Figure 31. Output Voltage vs. Temperature and Bias Current in the 5.80 GHz Voltage Detector using the HSMS-286B Schottky.

[7] Hewlett-Packard Application Note 965-3, *Flicker Noise in Schottky Diodes.*

Diode Burnout

Any Schottky junction, be it an RF diode or the gate of a MESFET, is relatively delicate and can be burned out with excessive RF power. Many crystal video receivers used in RFID (tag) applications find themselves in poorly controlled environments where high power sources may be present. Examples are the areas around airport and FAA radars, nearby ham radio operators, the vicinity of a broadcast band transmitter, etc. In such environments, the Schottky diodes of the receiver can be protected by a device known as a limiter diode.[8] Formerly available only in radar warning receivers and other high cost electronic warfare applications, these diodes have been adapted to commercial and consumer circuits.

Hewlett-Packard offers a complete line of surface mountable PIN limiter diodes. Most notably, our HSMP-4820 (SOT-23) can act as a very fast (nanosecond) power-sensitive switch when placed between the antenna and the Schottky diode, shorting out the RF circuit temporarily and reflecting the excessive RF energy back out the antenna.

Assembly Instructions

SOT-323 PCB Footprint

A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 32 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.

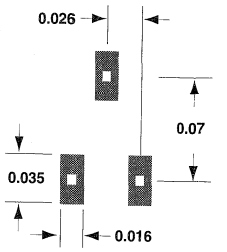


Figure 32. PCB Pad Layout (dimensions in inches).

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-323 package, will reach solder reflow temperatures faster than those with a greater mass.

HP's SOT-323 diodes have been qualified to the time-temperature profile shown in Figure 33. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235 °C.

These parameters are typical for a surface mount assembly process for HP SOT-323 diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

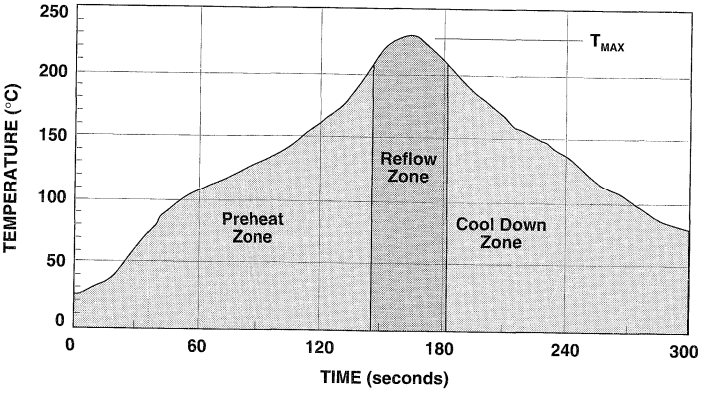
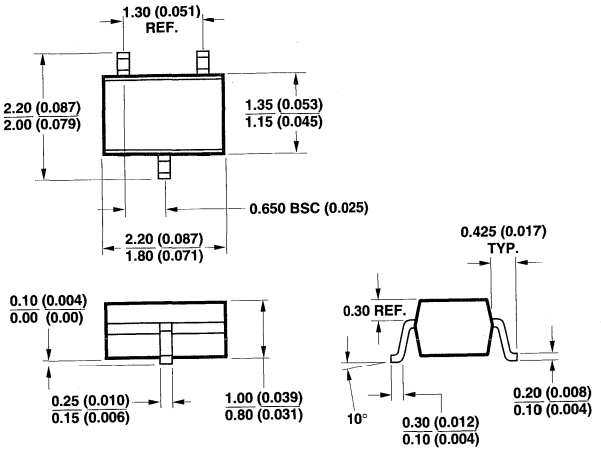


Figure 33. Surface Mount Assembly Profile.

[8] Hewlett-Packard Application Note 1050, *Low Cost, Surface Mount Power Limiters.*

Package Dimensions

Outline SOT-323 (SC-70, 3 Lead)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

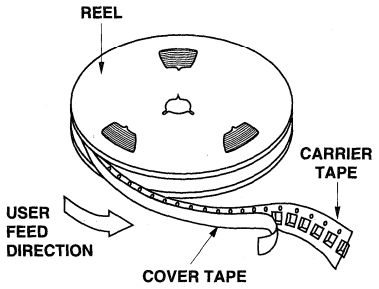
Part Number Ordering Information

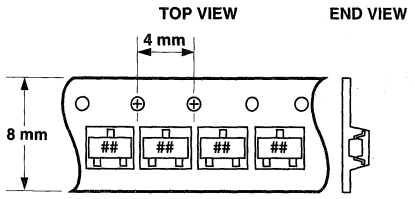
Part Number	No. of Devices	Container
HSMS-285A-TR1[1]	3000	7" Reel
HSMS-285A-BLK[1]	100	antistatic bag
HSMS-286A-TR1[2]	3000	7" Reel
HSMS-286A-BLK	100	antistatic bag

Notes:

1. "A" = B or C only
2. "A" = B, C, E or F

Device Orientation

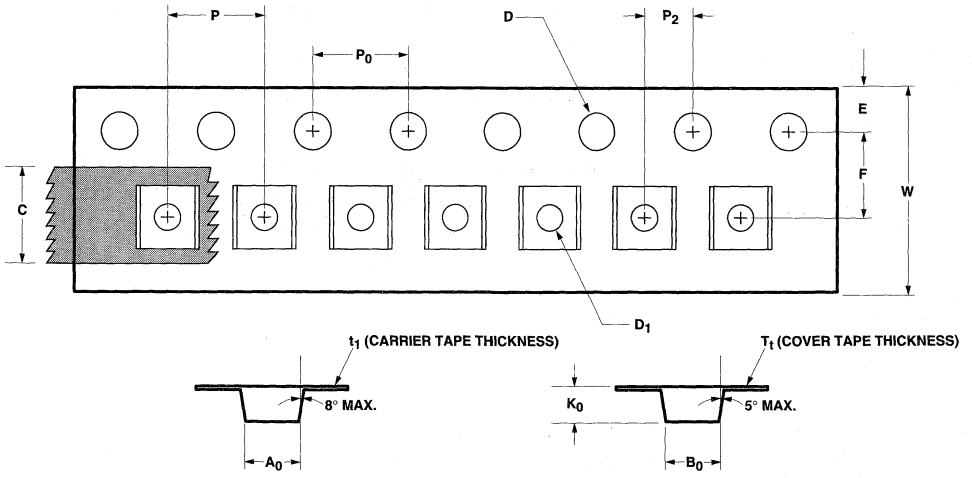




Note: "##" represents Package Marking Code.

Tape Dimensions and Product Orientation

For Outline SOT-323 (SC-70 3 Lead)



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

Surface Mount RF Schottky Barrier Diodes

Technical Data

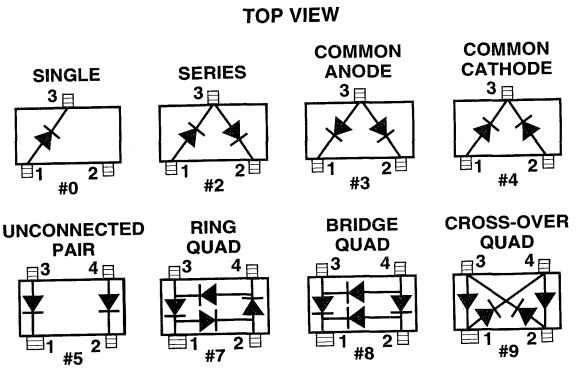
HSMS-28XX Series

Features

- **Surface Mount SOT-23/SOT-143 Package**
- **Low Turn-On Voltage (As Low as 0.34 V at 1 mA)**
- **Low FIT (Failure in Time) Rate***
- **Six-sigma Quality Level**
- **Single, Dual and Quad Versions**
- **Tape and Reel Options Available**

* For more information see the Surface Mount Schottky Reliability Data Sheet.

Package Lead Code Identification



Description/Applications

These Schottky diodes are specifically designed for both analog and digital applications. This series offers a wide range of specifications and package configurations to give the designer wide flexibility. Typical applications of these Schottky diodes are mixing, detecting, switching, sampling, clamping, and wave shaping. The HSMS-2800 series of diodes is optimized for high voltage applications. The HSMS-2810 series of diodes features very low flicker (1/f) noise. The HSMS-2820 series of diodes is the best all-around choice for most applications, featuring low series resistance, low forward voltage at all current levels and good RF characteristics. The HSMS-2860 series is a high performance diode offering superior V_f and ultra-low capacitance.

Note that HP's manufacturing techniques assure that dice found in pairs and quads are taken from adjacent sites on the wafer, assuring the highest degree of match.

Electrical Specifications T_A = 25°C, Single Diode[4]

Part Number HSMS[5]	Package Marking Code[3]	Lead Code	Configuration	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	Maximum Forward Voltage V_F (V) @ I_F (mA)	Maximum Reverse Leakage I_R (nA) @ V_R (V)	Maximum Capacitance C_T (pF)	Typical Dynamic Resistance R_D (Ω)[6]
2800	A0	0	Single	2800 (1N5711)	70	400	1.0 15	200 50	2.0	35
2802	A2	2	Series							
2803	A3	3	Common Anode							
2804	A4	4	Common Cathode							
2805	A5	5	Unconnected Pair							
2807	A7	7	Ring Quad[6]							
2808	A8	8	Bridge Quad[6]							
2810	B0	0	Single	2810 (1N5712)	20	400	1.0 35	200 15	1.2	15
2812	B2	2	Series							
2813	B3	3	Common Anode							
2814	B4	4	Common Cathode							
2815	B5	5	Unconnected Pair							
2817	B7	7	Ring Quad[6]							
2818	B8	8	Bridge Quad[6]							
2820	C0	0	Single	2835	15*	340	0.7 30	100 1	1.0	12
2822	C2	2	Series							
2823	C3	3	Common Anode							
2824	C4	4	Common Cathode							
2825	C5	5	Unconnected Pair							
2827	C7	7	Ring Quad[6]							
2828	C8	8	Bridge Quad[6]							
2829	C9	9	Cross-over Quad							
2860	T0	0	Single	None	5	320	0.6 30	—	0.30	10
2862	T1	2	Series Pair							
2863	T3	3	Common Anode							
2864	T4	4	Common Cathode							
2865	T5	5	Unconnected Pair							
Test Conditions					I_R = 10 µA *I_R = 100 µA	I_F = 1 mA[1]			V_F = 0 V f = 1.0 MHz[2]	I_F = 5 mA

Notes:

1. ΔV_F for diodes in pairs and quads in 15 mV maximum at 1 mA.
2. ΔC_{TO} for diodes in pairs and quads is 0.2 pF maximum.
3. Package marking code is in white.
4. Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 5 mA, except HSMS-282X which is measured at 20 mA.
5. See section titled "Quad Capacitance."
6. $R_D = R_S + 5.2\,\Omega$ at 25°C and I_f = 5 mA.

Absolute Maximum Ratings[1] T_A = 25°C

Symbol	Parameter	Value
I_f	Forward Current (1 ms Pulse)	1 Amp
P_t	Total Device Dissipation	250 mW[2]
P_{IV}	Peak Inverse Voltage	Same as V_{BR}
T_j	Junction Temperature	150°C
T_{stg}	Storage Temperature	-65 to 150°C

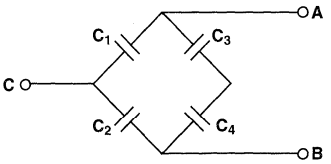
Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. CW Power Dissipation at T_{LEAD} = 25°C. Derate to zero at maximum rated temperature.

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches from the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. HP defines this measurement as "CM", and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capacitances can then be calculated by the formulas given below.

In a quad, the diagonal capacitance is the capacitance between points A and B as shown in the figure below. The diagonal capacitance is calculated using the following formula

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$



The equivalent adjacent capacitance is the capacitance between points A and C in the figure below. This capacitance is calculated using the following formula

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

This information does not apply to cross-over quad diodes.

SPICE Parameters

Parameter	Units	HSMS-280X	HSMS-281X	HSMS-282X	HSMS-286X
B_V	V	75	25	15	7.0
C_{J0}	pF	1.6	1.1	0.7	0.18
E_G	eV	0.69	0.69	0.69	0.69
I_{BV}	A	10E-5	10E-5	10E-4	10E-5
I_S	A	3x10E-8	4.8x10E-9	2.2x10E-8	5.0x10E-8
N		1.08	1.08	1.08	1.08
R_S	Ω	30	10	6.0	5.0
P_B	V	0.65	0.65	0.65	0.65
P_T		2	2	2	2
M		0.5	0.5	0.5	0.5

Typical Parameters at T_A = 25°C (unless otherwise noted), Single Diode

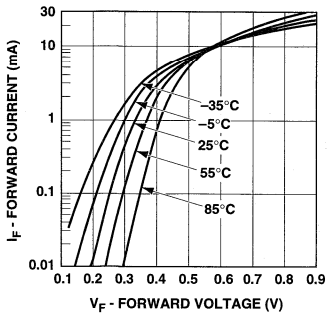


Figure 1. Typical Forward Current vs. Forward Voltage at Temperatures—HSMS-2800 Series

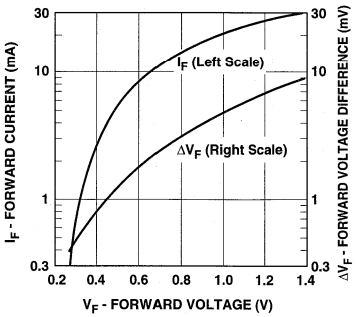


Figure 2. Typical V_f Match, HSMS-2800 Series Pairs and Quads.

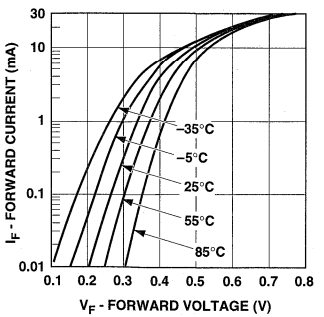


Figure 3. Typical Forward Current vs. Forward Voltage at Temperatures—HSMS-2810 Series.

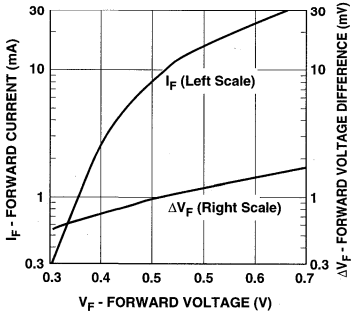


Figure 4. Typical V_f Match, HSMS-2810 Series Pairs and Quads.

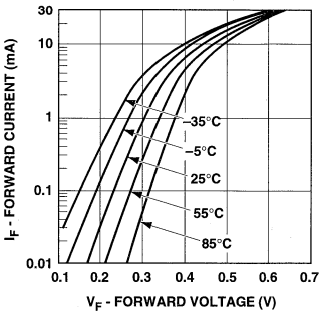


Figure 5. Typical Forward Current vs. Forward Voltage At Temperatures—HSMS-2820 Series.

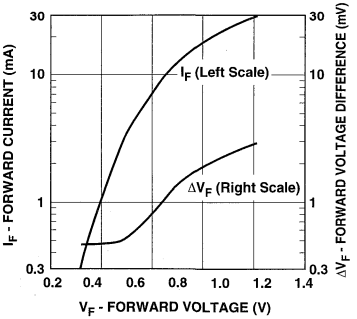


Figure 6. Typical V_f Match, HSMS-2820 Series Pairs and Quads at Mixer Bias Levels.

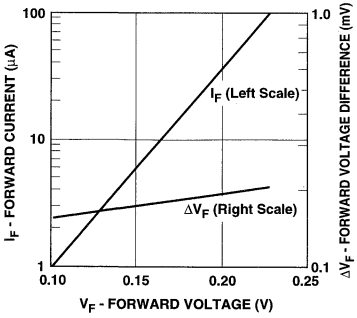


Figure 7. Typical V_f Match, HSMS-2820 Series Pairs at Detector Bias Levels.

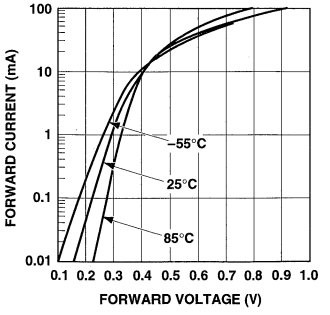


Figure 8. Typical Forward Current vs. Forward Voltage at Temperature, HSMS-2860 Series.

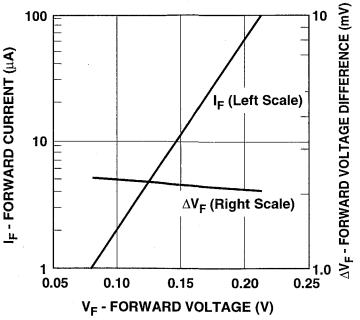


Figure 9. Typical V_f Match, HSMS-2860 Series Pairs at Detector Bias Levels.

Typical Parameters, continued

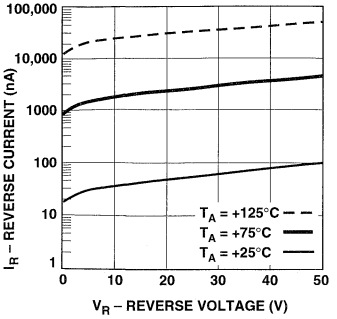


Figure 10. Reverse Current vs. Reverse Voltage at Temperatures—HSMS-2800 Series.

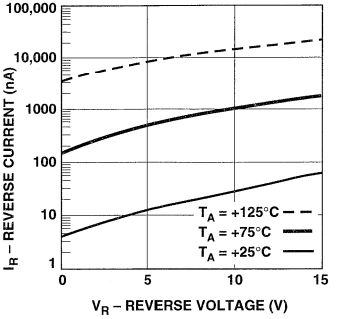


Figure 11. Reverse Current vs. Reverse Voltage at Temperatures—HSMS-2810 Series.

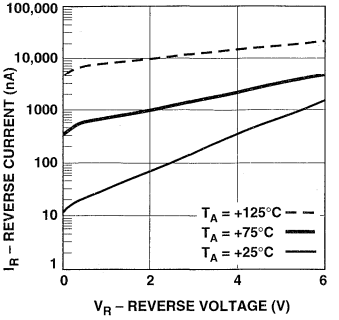


Figure 12. Reverse Current vs. Reverse Voltage at Temperatures—HSMS-2820 Series.

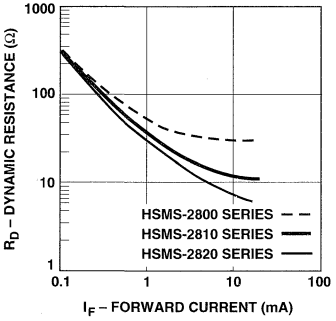


Figure 13. Dynamic Resistance vs. Forward Current—HSMS-2800 Series.

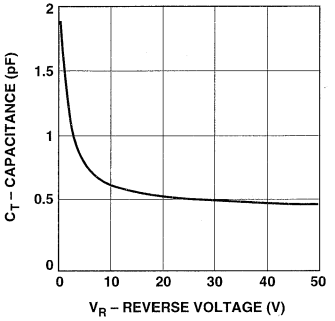


Figure 14. Total Capacitance vs. Reverse Voltage—HSMS-2800 Series.

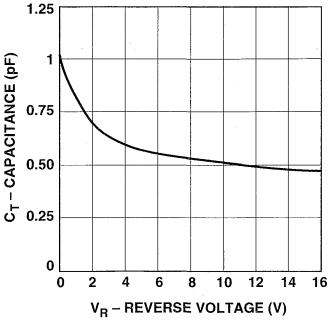


Figure 15. Total Capacitance vs. Reverse Voltage—HSMS-2810 Series.

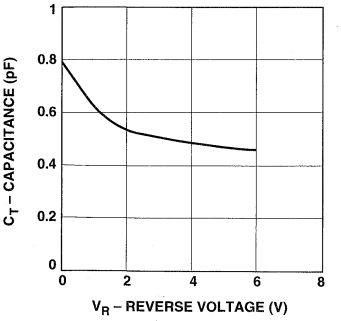


Figure 16. Total Capacitance vs. Reverse Voltage—HSMS-2820 Series.

Applications Information

Schottky Diode Fundamentals

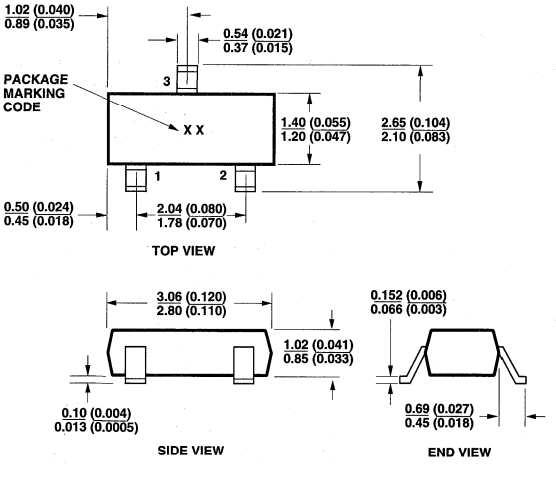
See the HSMS-280A series data sheet.

Package Characteristics

Lead Material ..... Alloy 42
Lead Finish ..... Tin-Lead 85/15%
Max. Soldering Temperature .... 260°C for 5 sec
Min. Lead Strength ..... 2 pounds pull
Typical Package
  Inductance ..... 2 nH (opposite leads)
Typical Package
  Capacitance ..... 0.08 pF (opposite leads)

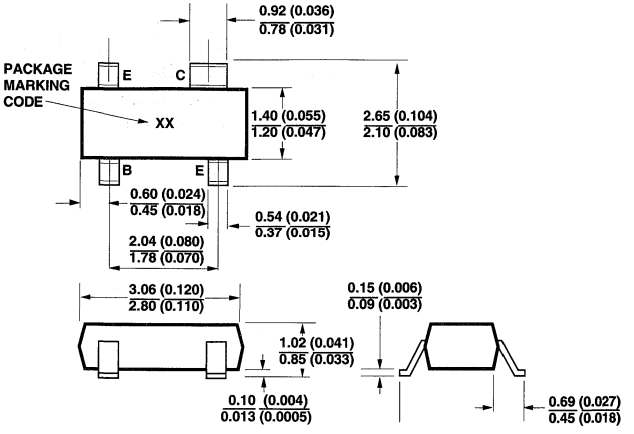
Package Dimensions

Outline 23 (SOT-23)



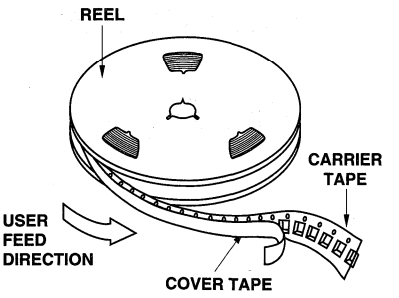
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 143 (SOT-143)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Device Orientation



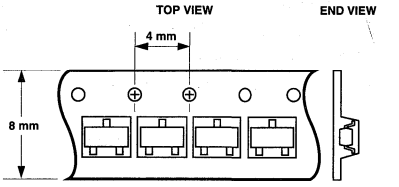


Figure 17. Option L31 for SOT-23 Packages.

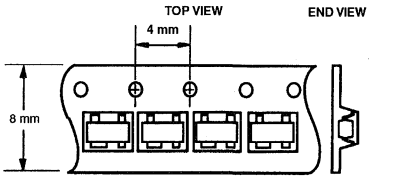


Figure 18. Option L31 for SOT-143 Packages.

HEWLETT® PACKARD

Surface Mount Microwave Schottky Detector Diodes

Technical Data

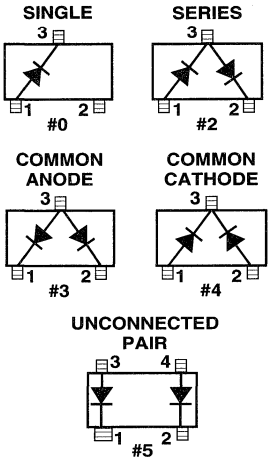
HSMS-2850 Series
HSMS-2860 Series

Features

- **Surface Mount SOT-23/ SOT-143 Package**
- **High Detection Sensitivity:**
  up to 50 mV/μW at 915 MHz
  up to 35 mV/μW at 2.45 GHz
  up to 25 mV/μW at 5.80 GHz
- **Low Flicker Noise:**
  -162 dBV/Hz at 100 Hz
- **Low FIT (Failure in Time) Rate***
- **Tape and Reel Options Available**

* For more information see the Surface Mount Schottky Reliability Data Sheet.

Package Lead Code Identification



Description

Hewlett-Packard's HSMS-2850 family of zero bias Schottky detector diodes and the HSMS-2860 family of DC biased detector diodes have been designed and optimized for use from 915 MHz to 5.8 GHz. They are ideal for RF/ID and RF Tag applications requiring small and large signal detection, modulation, RF to DC conversion or voltage doubling.

Available in various package configurations, these two families of detector diodes provide low cost solutions to a wide variety of design problems. Hewlett-Packard's manufacturing techniques assure that when two diodes are mounted into a single SOT-23 or SOT-143 package, they are taken from adjacent sites on the wafer, assuring the highest possible degree of match.

DC Electrical Specifications, T_A = +25°C, Single Diode

Part Number HSMS-	Package Marking Code[1]	Lead Code	Configuration	Maximum Forward Voltage V_F (mV)		Typical Capacitance C_T (pF)
2850	P0	0	Single	150	250	0.30
2852	P2	2	Series Pair [2,3]			
2855	P5	5	Unconnected Pair [2,3]			
2860	T0	0	Single	250	320	0.30
2862	T2	2	Series Pair [2,3]			
2863	T3	3	Common Anode [2,3]			
2864	T4	4	Common Cathode [2,3]			
2865	T5	5	Unconnected Pair [2,3]			
Test Conditions				I_F = 0.1 mA	I_F = 1.0 mA	V_R = –0.5 V to –1.0 V f = 1 MHz

Notes:
1. Package marking code is in white.
2. ΔV_F for diodes in pairs is 15.0 mV maximum at 1.0 mA.
3. ΔC_T for diodes in pairs is 0.05 pF maximum at –0.5 V.

RF Electrical Specifications, T_A = +25°C, Single Diode

Part Number HSMS-	Typical Tangential Sensitivity TSS (dBm) @ f =			Typical Voltage Sensitivity γ (mV/μW) @ f =			Typical Video Resistance RV (KΩ)
	915 MHz	2.45 GHz	5.8 GHz	915 MHz	2.45 GHz	5.8 GHz	
2850 2852 2855	–57	–56	–55	40	30	22	8.0
Test Conditions	Video Bandwidth = 2 MHz Zero Bias			Power in = –40 dBm R_L = 100 KΩ, Zero Bias			
2860 2862 2863 2864 2865	–57	–56	–55	50	35	25	5.0
Test Conditions	Video Bandwidth = 2 MHz I_b = 5 μA			Power in = –40 dBm R_L = 100 KΩ, I_b = 5 μA			

Absolute Maximum Ratings, T_A = +25°C, Single Diode

Symbol	Parameter	Absolute Maximum[1]
P_T	Total Device Dissipation[2]	75 mW
P_{IV}	Peak Inverse Voltage	2.0 V
T_J	Junction Temperature	150°C
T_{STG}	Storage Temperature	-65°C to 150°C
T_{OP}	Operating Temperature	-65°C to 150°C

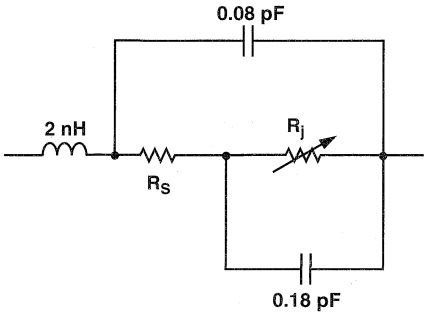
Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. CW Power Dissipation at T_{LEAD} = +25°C. Derate linearly to zero at maximum rated temperature.

ESD WARNING: Handling Precautions Should Be Taken To Avoid Static Discharge.

Equivalent Circuit Model

HSMS-2850, HSMS-2860; Singles



R_S = series resistance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5}\ nT}{I_b + I_s}$$

where

I_b = externally applied bias current in amps

I_s = saturation current (see table of SPICE parameters)

T = temperature, °K

n = identity factor (see table of SPICE parameters)

SPICE Parameters

Parameter	Units	HSMS-285X	HSMS-286X
B_V	V	3.8	7.0
C_{J0}	pF	0.18	0.18
E_G	eV	0.69	0.69
I_{BV}	A	3 x 10E-4	10E-5
I_S	A	3 x 10E-6	5.0 x 10E-8
N		1.06	1.08
R_S	Ω	25	5.0
P_B(VJ)	V	0.35	0.65
P_T(XTI)		2	2
M		0.5	0.5

Typical Parameters, Single Diode

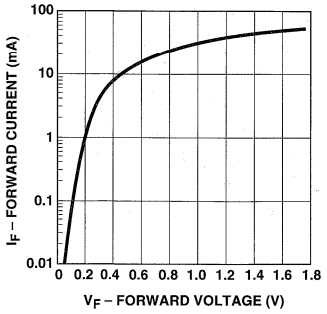


Figure 1. Typical Forward Current vs. Forward Voltage, HSMS-2850 Series.

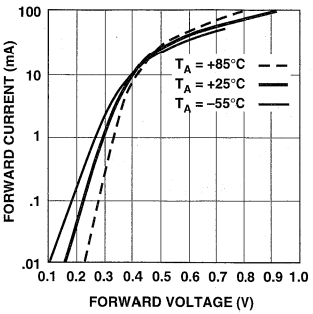


Figure 2. Typical Forward Current vs. Forward Voltage at Temperature, HSMS-2860 Series.

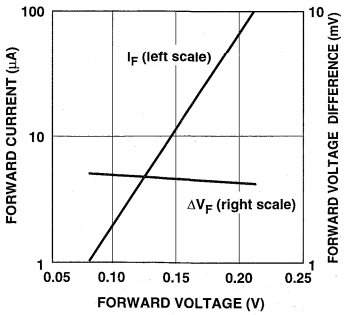


Figure 3. Typical Forward Voltage Match, HSMS-2860 Pairs.

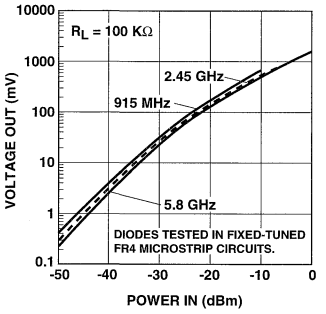


Figure 4. +25°C Output Voltage vs. Input Power, HSMS-2850 at Zero Bias, HSMS-2860 at 3 μA Bias.

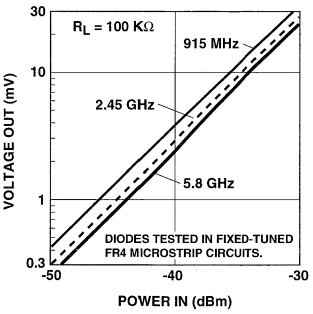


Figure 5. +25°C Expanded Output Voltage vs. Input Power. See Figure 4.

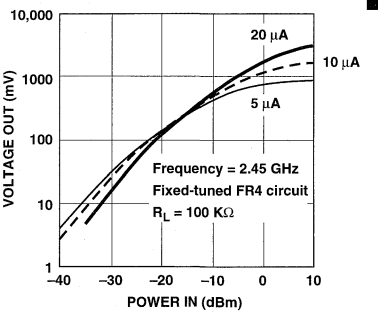


Figure 6. Dynamic Transfer Characteristic as a Function of DC Bias, HSMS-2860.

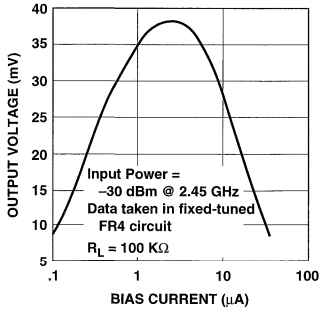


Figure 7. Voltage Sensitivity as a Function of DC Bias Current, HSMS-2860.

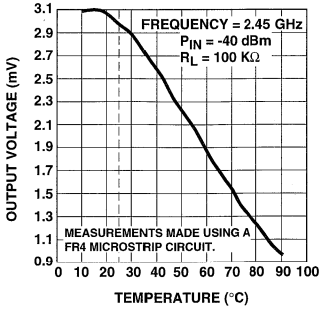


Figure 8. Output Voltage vs. Temperature, HSMS-2850 Series.

Applications Information

See the HSMS-285A data sheet.

Ordering Information

Specify part number followed by option. For example:

H SMS-285X #X XX

- XX: Bulk or Tape and Reel Option
- #X: Profile: Low = L
- SMS-285X: Part Number
- SMS: Surface Mount Schottky
- H: Hewlett-Packard

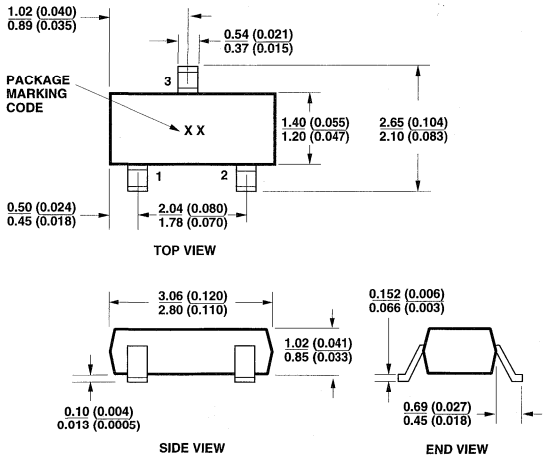
Profile Option Descriptions

#L30 = Bulk

#L31 = 3K pc. Tape and Reel, Device Orientation Figures 9, 10

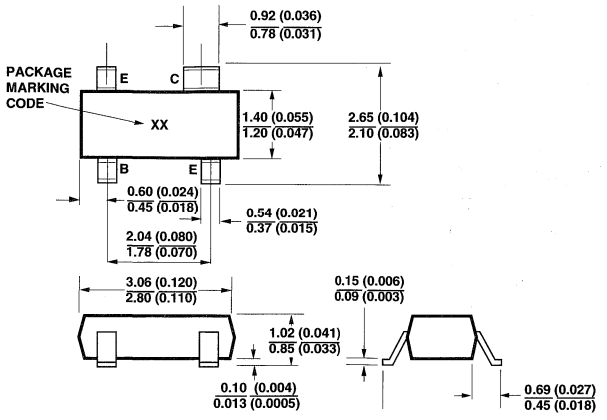
Tape and Reeling conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement."

Package Dimensions
Outline 23 (SOT-23)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 143 (SOT-143)

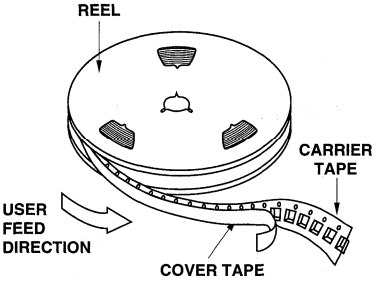


DIMENSIONS ARE IN MILLIMETERS (INCHES)

Package Characteristics

Lead Material	Alloy 42
Lead Finish	Tin-Lead 85/15%
Max. Soldering Temp.	260°C for 5 sec.
Min. Lead Strength	2 pounds pull
Typical Package Inductance	2 nH (opposite leads)
Typical Package Capacitance	0.08 pF (opposite leads)

Device Orientation



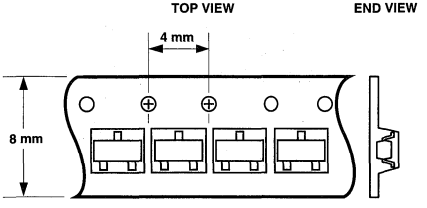


Figure 9. Option L31 for SOT-23 Packages.

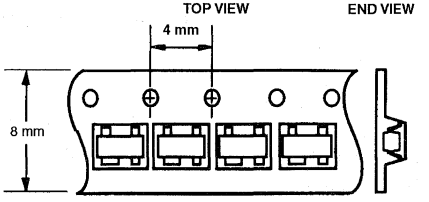


Figure 10. Option L31 for SOT-143 Packages.

HEWLETT® PACKARD

Surface Mount Microwave Schottky Mixer Diodes

Technical Data

HSMS-8101 Single
HSMS-8202 Pair
HSMS-8205 Pair
HSMS-8207 Quad

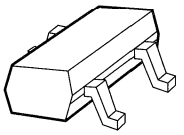
Features

- **Optimized for use at 10-14 GHz**
- **Low Capacitance**
- **Low Conversion Loss**
- **Low RD**
- **Low Cost Surface Mount Plastic Package**

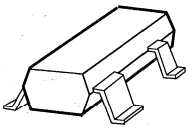
Description/Applications

These low cost microwave Schottky diodes are specifically designed for use at X/Ku-bands and are ideal for DBS and VSAT downconverter applications. They are available in SOT-23 and SOT-143 standard package configurations.

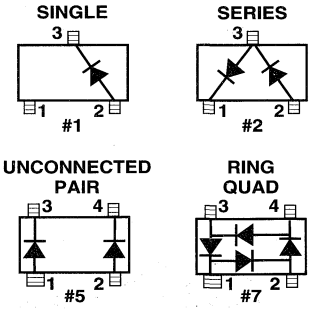
Plastic SOT-23 Package



Plastic SOT-143 Package



Package Lead Code Identification (Top View)



Absolute Maximum Ratings[1], T_A = +25°C

Symbol	Parameter	Unit	Min.	Max.
P_T	Total Device Dissipation[2]	mW	—	75
P_{IV}	Peak Inverse Voltage	V	—	4
T_J	Junction Temperature	°C	—	+150
T_{STG}, T_{op}	Storage and Operating Temperature	°C	-65	+150

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. Measured in an infinite heat sink at T_{CASE} = 25°C. Derate linearly to zero at 150°C per diode.

DC Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	HSMS-8101		HSMS-8202		HSMS-8205		HSMS-8207	
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{BR}	Breakdown Voltage	I_R = 10 µA	V	4		4		4		4	
C_T	Total Capacitance	V_R = 0 V, f = 1 MHz	pF		0.26		0.26		0.26		0.26
ΔC_T	Capacitance Difference	V_R = 0 V, f = 1 MHz	pF		—		0.04		0.04		0.04
R_D	Dynamic Resistance	I_F = 5 mA	Ω		14		14		14		14
ΔR_D	Dynamic Resistance Difference	I_F = 5 mA	Ω		—		2		2		2
V_F	Forward Voltage	I_F = 1 mA	mV	250	350	250	350	250	350	250	350
ΔV_F	Forward Voltage Difference	I_F = 1 mA	mV		—		20		20		20
	Lead Code			1		2		5		7	
	Package Marking Code in White			R1		2R		R5		R7	

RF Electrical Parameters, T_A = 25°C

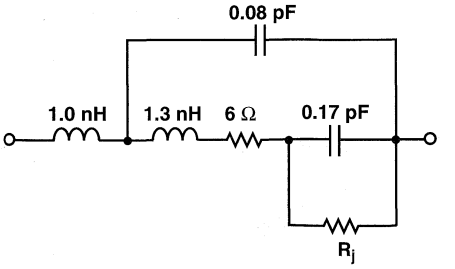
Symbol	Parameter	Units	Typical
L_c	Conversion Loss at 12 GHz	dB	6.3
Z_{IF}	IF Impedance	Ω	150
SWR	SWR at 12 GHz		1.2

Note:
DC Load Resistance = 0 Ω; LO Power = 1 mW.

SPICE Parameters

I_S = 4.6 E-8	E_G = 0.69	TT = 0
R_S = 6	C_{JO} = 0.18 E-12	
N = 1.09	P_B (V_J) = 0.5	
B_V = 7.3	M = 0.5	
I_{BV} = 10E-5	FC = 0.5	

Linear Equivalent Circuit



Self Bias

	1 mA	2.5 mA
R_j	263	142

Typical Performance, T_C = 25°C

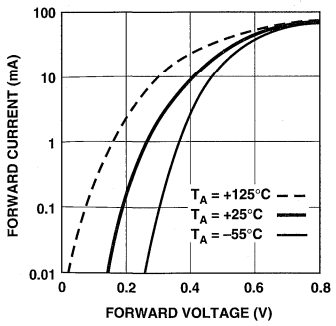


Figure 1. Typical Forward Current vs. Forward Voltage at Three Temperatures.

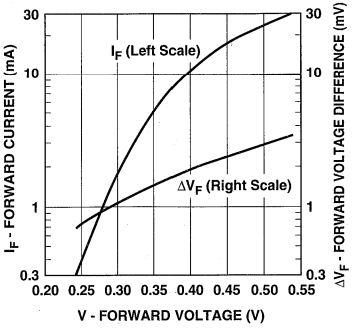


Figure 2. Typical VF Match, HSMS-820X Pairs and Quads.

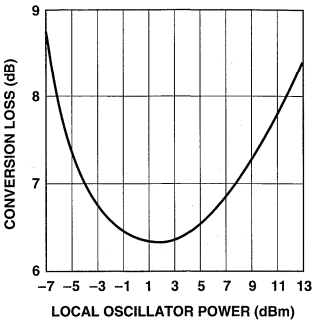


Figure 3. Typical Conversion Loss vs. Local Oscillator Power.

Ordering Information

Specify part number followed by option. For example:

H SMS-8101 #X XX

- XX — Bulk or Tape and Reel Option
- #X — Profile: Low = L
- 8101 — Part Number
- SMS — Surface Mount Schottky
- H — Hewlett-Packard

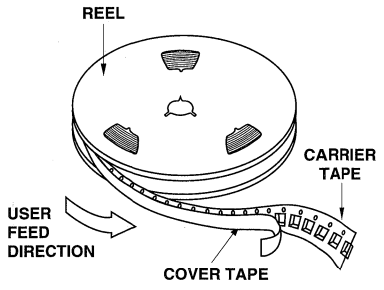
Profile Option Descriptions

#L30 = Bulk

#L31 = 3K pc. Tape and Reel, Device Orientation Figures 4, 5

Tape and Reeling conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement."

Device Orientation



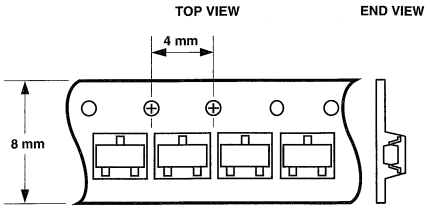


Figure 4. Option L31 for SOT-23 Packages.

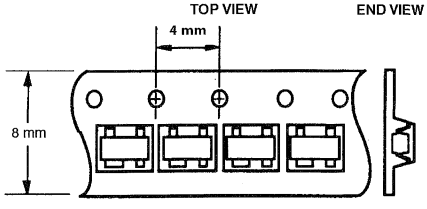
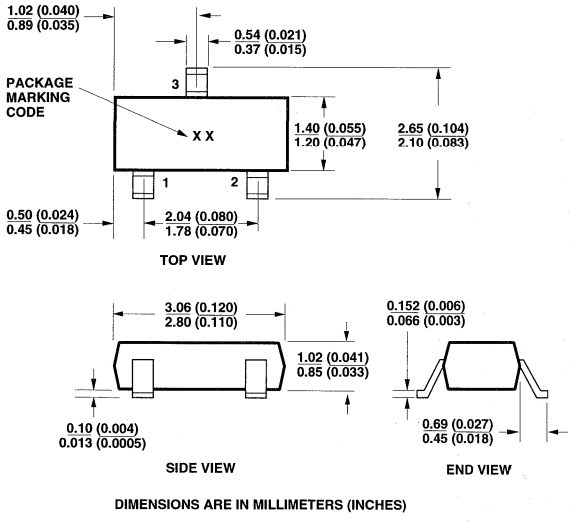


Figure 5. Option L31 for SOT-143 Packages.

Package Characteristics

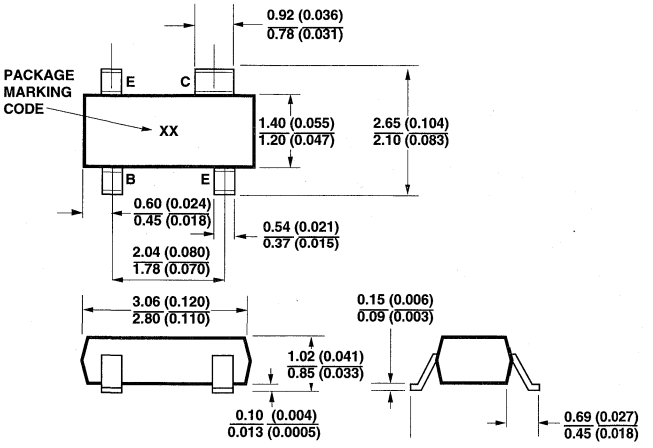
Lead Material ..... Alloy 42
Lead Finish ..... Tin-Lead 85-15%
Maximum Soldering Temperature ..... 260°C for 5 seconds
Minimum Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)

Package Dimensions
Outline 23 (SOT-23)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 143 (SOT-143)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Schottky Barrier Diodes for General Purpose Applications

Technical Data

1N5711
1N5712
5082-2300 Series
5082-2800 Series
5082-2900 Series

Features

- **Low Turn-On Voltage**
  As Low as 0.34 V at 1 mA
- **Pico Second Switching Speed**
- **High Breakdown Voltage**
  Up to 70 V
- **Matched Characteristics Available**

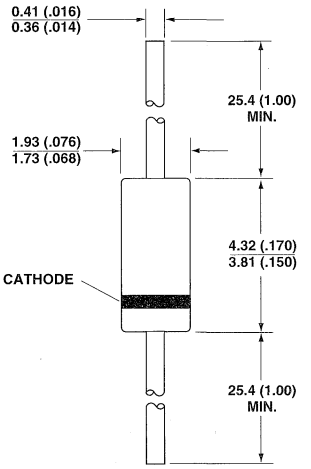
Description/Applications

The 1N5711, 1N5712, 5082-2800/10/11 are passivated Schottky barrier diodes which use a patented "guard ring" design to achieve a high breakdown voltage. Packaged in a low cost glass package, they are well suited for high level detecting, mixing, switching, gating, log or A-D converting, video detecting, frequency discriminating, sampling, and wave shaping.

The 5082-2835 is a passivated Schottky diode in a low cost glass package. It is optimized for low turn-on voltage. The 5082-2835 is particularly well suited for the UHF mixing needs of the CATV marketplace.

The 5082-2300 and 2900 Series devices are unpassivated Schottky diodes in a glass package. These diodes have extremely low 1/f noise and are ideal for low noise mixing, and high sensitivity detecting. They are particularly well suited for use in Doppler or narrow band video receivers.

Outline 15



DIMENSIONS IN MILLIMETERS AND (INCHES).

Maximum Ratings

Junction Operating and Storage Temperature Range
- 5082-2303, -2900 ..... -60°C to +100°C
- 1N5711, 1N5712, 5082-2800/10/11 ..... -65°C to +200°C
- 5082-2835 ..... -60°C to +150°C

DC Power Dissipation
(Measured in an infinite heat sink at T_{CASE} = 25°C)
Derate linearly to zero at maximum rated temperature
- 5082-2303, -2900 ..... 100 mW
- 1N5711, 1N5712, 5082-2800/10/11 ..... 250 mW
- 5082-2835 ..... 150 mW

Peak Inverse Voltage ..... V_{BR}

Package Characteristics

	Outline 15
Lead Material	Dumet
Lead Finish	95-5% Tin-Lead
Max. Soldering Temperature	260°C for 5 sec
Min. Lead Strength	4 pounds pull
Typical Package Inductance	
1N5711, 1N5712:	2.0 nH
2800 Series:	2.0 nH
2300, 2900 Series:	3.0 nH
Typical Package Capacitance	
1N5711, 1N5712:	0.2 pF
2800 Series:	0.2 pF
2300, 2900 Series:	0.07 pF

The leads on the Outline 15 package should be restricted so that the bend starts at least 1/16 inch from the glass body.

Outline 15 diodes are available on tape and reel. The tape and reel specification is patterned after RS-296-D.

Electrical Specifications at T_A = 25°C

General Purpose Diodes

Part Number	Package Outline	Min. Breakdown Voltage V_{BR} (V)	Max. Forward Voltage V_F (mV)	V_F = 1 V Max. at Forward Current I_F (mA)	Max. Reverse Leakage Current I_R (nA) at V_R (V)		Max. Capacitance C_T (pF)
5082-2800	15	70	410	15	200	50	2.0
1N5711	15	70	410	15	200	50	2.0
5082-2810	15	20	410	35	100	15	1.2
1N5712	15	20	550	35	150	16	1.2
5082-2811	15	15	410	20	100	8	1.2
5082-2835	15	8*	340	10*	100	1	1.0
Test Conditions		I_R = 10 μA *I_R = 100 μA	I_F = 1 mA	*V_F = 0.45 V			V_R = 0 V f =1.0 MHz

Note: Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 5 mA except for 5082-2835 which is measured at 20 mA.

Low 1/f (Flicker) Noise Diodes

Part Number 5082-	Package Outline	Min. Breakdown Voltage V_{BR} (V)	Max. Forward Voltage V_F (mV)	V_F = 1 V Max. at Forward Current I_F (mA)	Max. Reverse Leakage Current I_R (nA) at V_R (V)		Max. Capacitance C_T (pF)
2303	15	20	400	35	500	15	1.0
2900	15	10	400	20	100	5	1.2
Test Conditions		I_R = 10 µA	I_F = 1 mA				V_R = 0 V f =1.0 MHz

Note: Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 20 mA.

Matched Pairs and Quads

Basic Part Number 5082-	Matched Pair Unconnected	Matched Quad Unconnected	Batch Matched[1]	Test Conditions
2900	5082-2912 ΔV_F = 30 mV	5082-2970 ΔV_F = 30 mV		ΔV_F at I_F = 1.0, 10 mA
2800	5082-2804 ΔV_F = 20 mV	5082-2805 ΔV_F = 20 mV		ΔV_F at I_F = 0.5, 5 mA *I_F = 10 mA ΔC_O at f = 1.0 MHz
2811			5082-2826 ΔV_F = 10 mV ΔC_O = 0.1 pF	ΔV_F at I_F = 10 mA ΔC_O at f = 1.0 MHz
2835			5082-2080 ΔV_F = 10 mV ΔC_O = 0.1 pF	ΔV_F at I_F =10 mA ΔC_O at f = 1.0 MHz

Note:
1. Batch matched devices have a minimum batch size of 50 devices.

SPICE Parameters

Parameter	Units	5082-2800	5082-2810	5082-2811	5082-2835	5082-2303	5082-2900
B_V	V	75	25	18	9	25	10
C_{J0}	pF	1.6	0.8	1.0	0.7	0.7	1.1
E_G	eV	0.69	0.69	0.69	0.69	0.69	0.69
I_{BV}	A	10E-5	10E-5	10E-5	10E-5	10E-5	10E-5
I_S	A	2.2 x 10E-9	1.1 x 10E-9	0.3 x 10E-8	2.2 x 10E-8	7 x 1.0E-9	10E-8
N		1.08	1.08	1.08	1.08	1.08	1.08
R_S	Ω	25	10	10	5	10	15
P_B	V	0.6	0.6	0.6	0.56	0.64	0.64
P_T		2	2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5	0.5

Typical Parameters

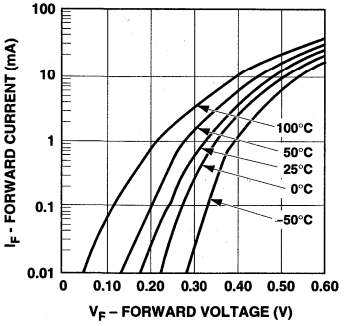


Figure 1. I-V Curve Showing Typical Temperature Variation for 5082-2300 and 5082-2900 Series Schottky Diodes.

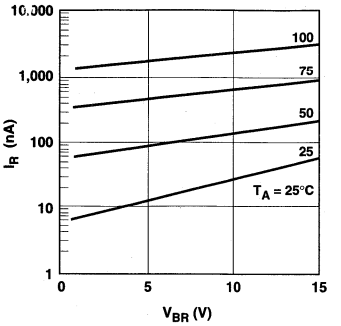


Figure 2. 5082-2300 Series Typical Reverse Current vs. Reverse Voltage at Various Temperatures.

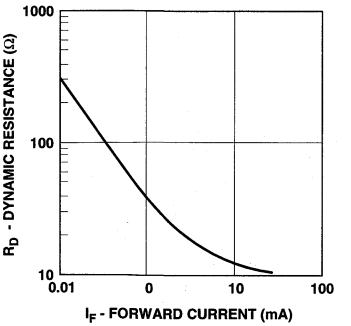


Figure 3. 5082-2300 Series and 5082-2900 Series Typical Dynamic Resistance (R_D) vs. Forward Current (I_F).

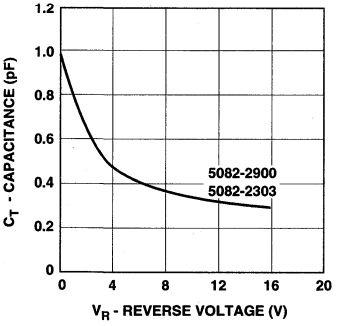


Figure 4. 5082-2300 and 5082-2900 Series Typical Capacitance vs. Reverse Voltage.

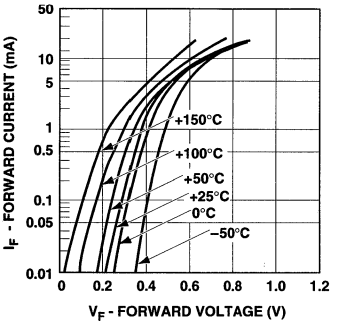


Figure 5. I-V Curve Showing Typical Temperature Variation for 5082-2800 or 1N5711 Schottky Diodes.

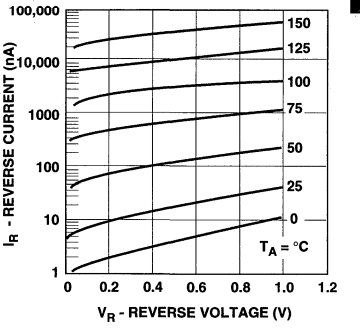


Figure 6. (5082-2800 OR 1N5711) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

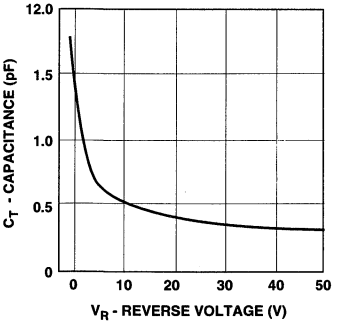


Figure 7. (5082-2800 or 1N5711) Typical Capacitance (C_T) vs. Reverse Voltage (V_R).

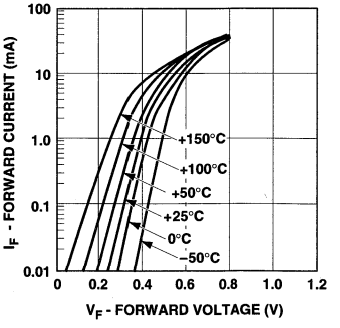


Figure 8. I-V Curve Showing Typical Temperature Variation for the 5082-2810 or 1N5712 Schottky Diode.

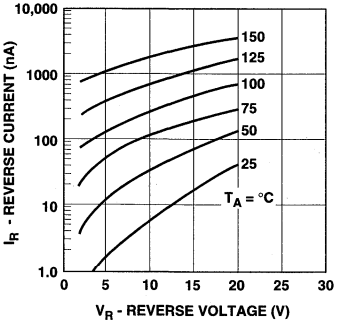


Figure 9. (5082-2810 or IN5712) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

Typical Parameters, continued

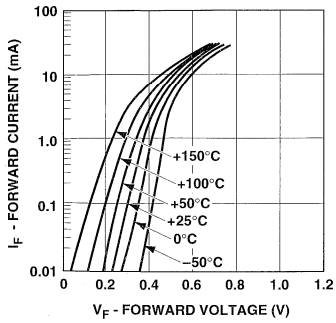


Figure 10. I-V Curve Showing Typical Temperature Variation for the 5082-2811 Schottky Diode.

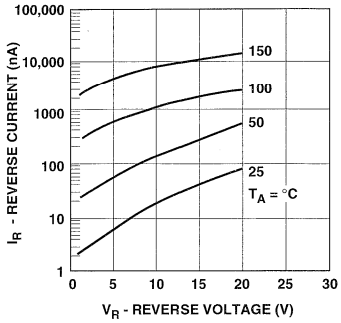


Figure 11. (5082-2811) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

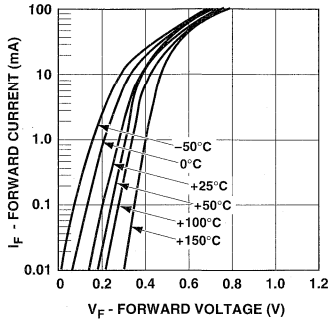


Figure 12. I-V Curve Showing Typical Temperature Variations for 5082-2835 Schottky Diode.

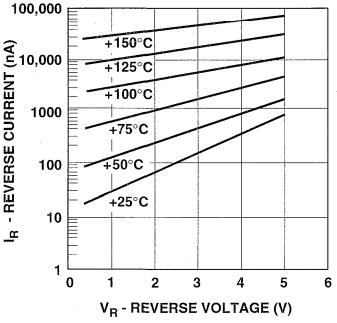


Figure 13. (5082-2835) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

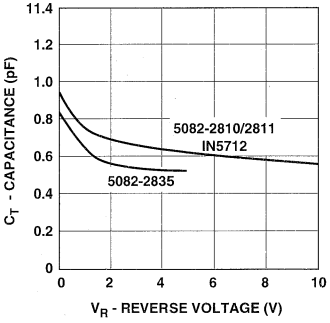


Figure 14. Typical Capacitance (C_T) vs. Reverse Voltage (V_R).

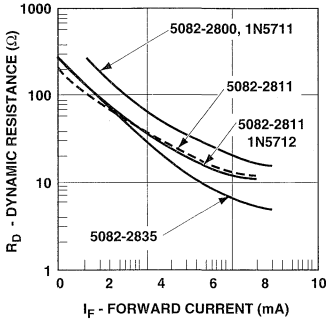


Figure 15. Typical Dynamic Resistance (R_D) vs. Forward Current (I_F).

Diode Package Marking

HPX

XXX

YZZ

where XXX are the last three digits of the 5082-XXXX part number, Y is the last digit of the calendar year, and ZZ is the work week of manufacture.

For example, a 5082-2811 manufactured during the 35th work week of 1996 would be marked

HP2

811

635

HEWLETT® PACKARD

Schottky Barrier Diodes for Stripline, Microstrip Mixers and Detectors

Technical Data

5082-2207/09
5082-2765/85
5082-2774/94

Features

- **Small Size**
- **Low Noise Figure**
  6 dB Typical at 9 GHz
- **Rugged Design**
- **High Uniformity**
- **High Burnout Rating**
  1 W RF Pulse Power Incident
- **Both Medium and Low Barrier Available**

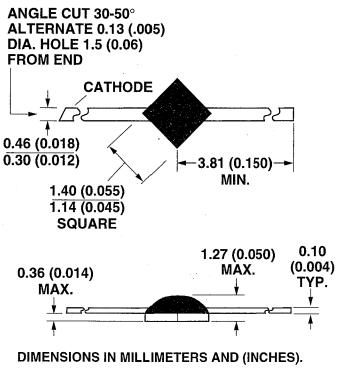
Description/Applications

This family consists of medium barrier and low barrier beam lead diodes mounted in easily handled carrier packages. Low barrier diodes provide optimum noise figure at low local oscillator drive levels. Medium barrier diodes provide a wider dynamic range for lower distortion mixer designs. Application Note 976 presents design techniques for an X-Band mixer.

Note: For new designs, the HSMS-286X and HSMS-820X series of surface mount microwave diodes are recommended.

Outline C2

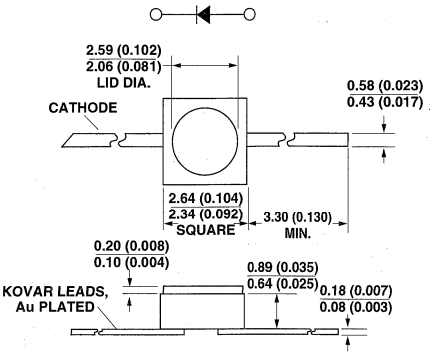
C_P = 0.055 pF



DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline H2

C_P = 0.175 pF



DIMENSIONS IN MILLIMETERS AND (INCHES).

Package Characteristics

These diodes are designed for microstrip and stripline use. The kovar leads provide good continuity of transmission line impedance to the diode. Outline C2 is a plastic on ceramic package. Outline H2 has a metal ceramic hermetic seal. The ceramic is alumina. Metal parts are gold plated kovar.

The hermetic package, outline H2, is capable of passing many of the environmental tests of MIL-STD-750. The applicable solderability test is reference 2031.1: 260°C, 10 seconds.

Maximum Ratings

Operating and Storage Temperature Range
- C2 Packaged Diodes ..... -65°C to +150 °C
- H2 Packaged Diodes ..... -65°C to +175 °C

Pulse Power Incident at T_{CASE} = 25°C ..... 1 W
(1 μs pulse, Du = 0.001)

CW Power Dissipation at T_{CASE} = 25°C
(Measured in an infinite heat sink) ..... 125 mW
Derate linearly to zero at maximum operating temperature.

Diode Mounting Temperature in Packages
- C2 ..... 235°C for 10 sec max.
- H2 ..... 260°C for 10 sec max.

Peak Inverse Voltage ..... 4 V

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

RF Electrical Specifications at T_A = 25°C

Part Number 5082-	Test Freq. (GHz)	Barrier	Maximum Noise Figure NF (dB)	IF Impedance Z_{IF} (Ω) Min.	IF Impedance Z_{IF} (Ω) Max.	Maximum SWR	Package	Typical Junction Capacitance C_j (pF)
2765 2785	9.375	Low Low	6.0 6.5	150	350	1.5:1 2.0:1	Hermetic H2	0.18
2207 2209		Medium Medium	6.0 6.5	200	400	1.5:1 2.0:1	Broadband C2	
2774 2794		Low Low	6.0 6.5	150	350	1.5:1 2.0:1		
Test Conditions			DC Load Resistance = 0 Ω L.O. Power = 1 mW IF = 30 MHz, 1.5 dB NF					V = 0

*Minimum batch size 20 units.

Typical Detector Characteristics at T_A = 25°C

Medium Barrier and Low Barrier (DC Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	T_{SS}	-54	dBm	20 μA Bias, R_L = 100 KΩ P_{in} = - 40 dBm Video Bandwidth = 2 MHz f = 10 GHz
Voltage Sensitivity	γ	6.6	mV/μW	
Video Resistance	R_V	1400	Ω	

Low Barrier (Zero Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	T_{SS}	-44	dBm	Zero Bias, R_L = 10 MΩ P_{in} = - 30 dBm Video Bandwidth = 2 MHz f = 10 GHz
Voltage Sensitivity	γ	10	mV/μW	
Video Resistance	R_V	1.8	MΩ	

SPICE Parameters

Parameter	Units	5082-2207 5082-2209	5082-2765 5082-2774 5082-2785 5082-2794
B_V	V	5	5
C_{J0}	pF	0.20	0.20
E_G	eV	0.69	0.69
I_{BV}	A	10E-5	10E-5
I_S	A	3 x 10E-10	4 x 10E-8
N		1.08	1.08
R_S	Ω	5	6
P_B	V	0.65	0.5
P_T		2	2
M		0.5	0.5

Typical Parameters

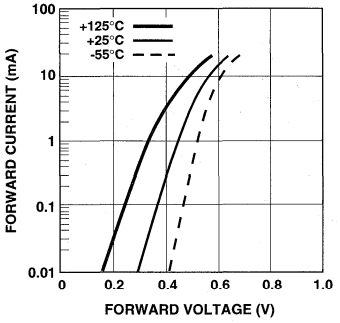


Figure 1. Typical Forward Characteristics for Medium Barrier Diodes.

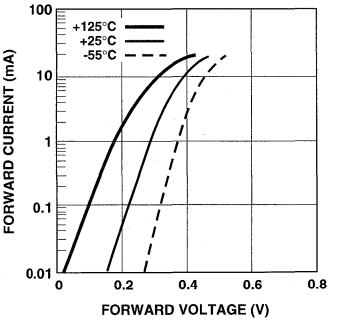


Figure 2. Typical Forward Characteristics for Low Barrier Diodes.

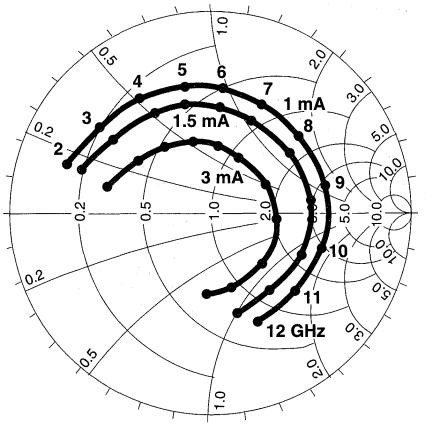


Figure 3. Typical Admittance Characteristics, 5082-2765 with Self Bias.

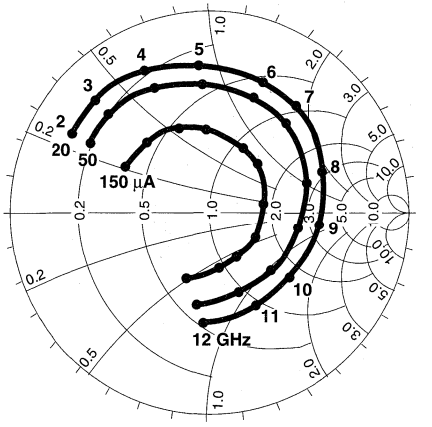


Figure 4. Typical Admittance Characteristics, 5082-2765 with External Bias.

Typical Parameters, continued

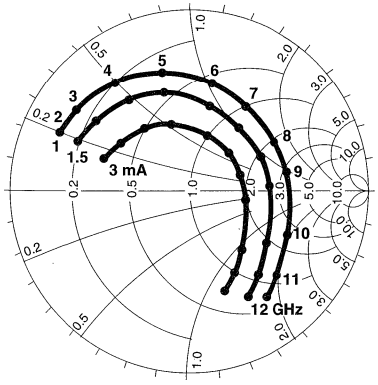


Figure 5. Typical Admittance Characteristics 5082-2785 with Self Bias.

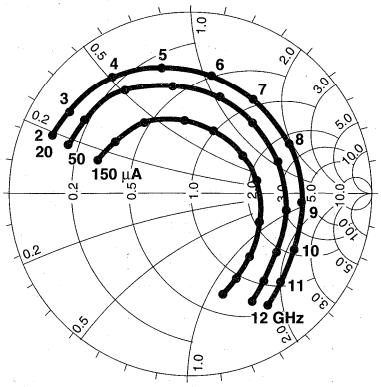


Figure 6. Typical Admittance Characteristics 5082-2785 with External Bias.

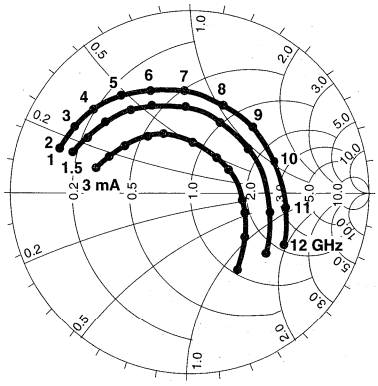


Figure 7. Typical Admittance Characteristics, 5082-2207 and 5082-2774 with Self Bias.

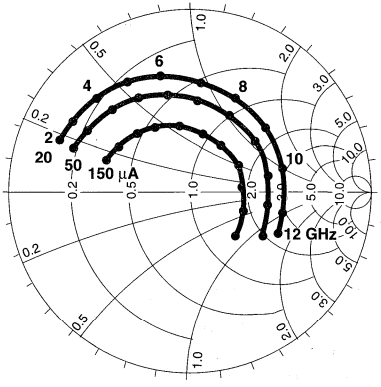


Figure 8. Typical Admittance Characteristics, 5082-2207 and 5082-2774 with External Bias.

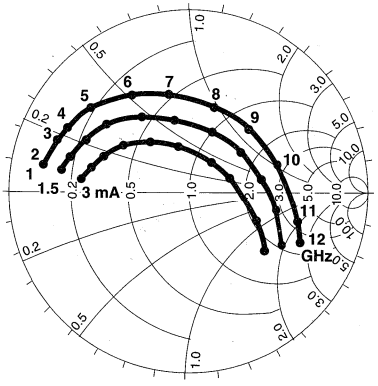


Figure 9. Typical Admittance Characteristics, 5082-2209 and 5082-2794 with Self Bias.

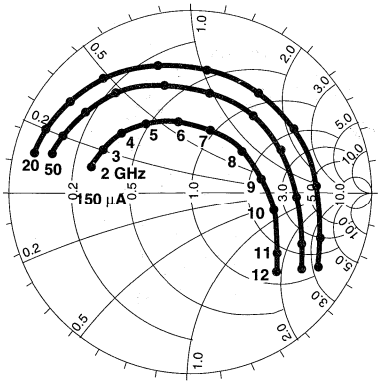


Figure 10. Typical Admittance Characteristics, 5082-2209 and 5082-2794 with External Bias.

Typical Parameters, continued

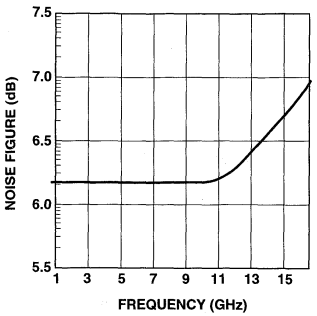
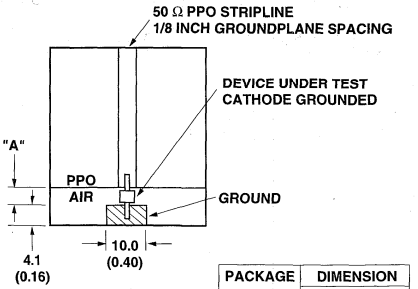


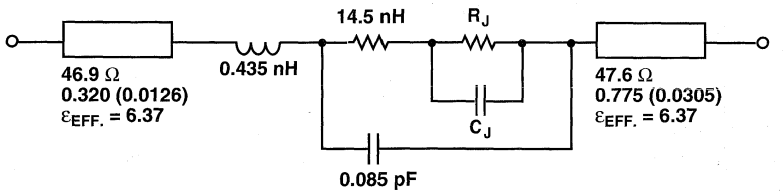
Figure 11. Typical Noise Figure vs. Frequency for 5082-2209, -2794.



PACKAGE	DIMENSION "A"
C2	1.91 ± 0.05 (0.075 ± 0.002)
H2	2.67 ± 0.05 (0.105 ± 0.002)

Figure 12. Admittance Test Circuit.

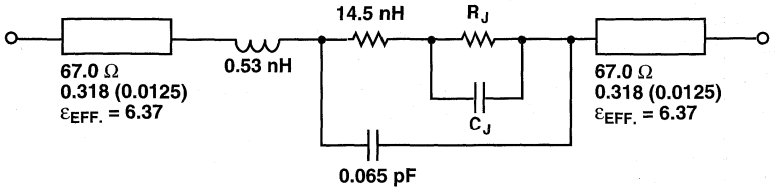
MODEL FOR H2 DIODES



DIMENSIONS IN MILLIMETERS (INCHES)

Parameter	Symbol	1 mA Rect. Current 5082-2765	20 μA Ext. Bias 5082-2765	Units
Junction Resistance	R_J	258	545	Ω
Junction Capacitance	C_J	0.255	0.302	pF

MODEL FOR C2 DIODES



DIMENSIONS IN MILLIMETERS (INCHES)

Parameter	Symbol	1 mA Rect. Current 5082-2207, 5082-2774	20 μA Ext. Bias 5082-2207, 5082-2774	Units
Junction Resistance	R_J	338	421	Ω
Junction Capacitance	C_J	0.189	0.195	pF

HEWLETT® PACKARD

Schottky Barrier Diode Quads for Double Balanced Mixers

Technical Data

5082-2830

Features

- **Small Size**
  Eases Broad Band Designs
- **Tight Match**
  Improves Mixer Balance
- **Improved Balance over Temperature**
- **Rugged Design**

Description/Applications

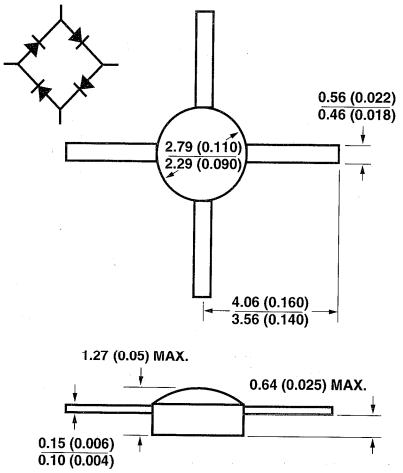
This matched diode quad uses a monolithic array of Schottky diodes interconnected in ring configuration. The relative proximity of the diode junction on the wafer assures uniform electrical characteristics and temperature tracking.

These diodes are designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators requiring wideband operation and small size. the low barrier diodes allow for optimum mixer noise figure at lower than conventional local oscillator levels. the wider dynamic range of the medium barrier diodes allows for better distortion performance.

Note: For new designs, the HSMS-820X series of surface mount microwave diodes are recommended.

Outline E4

C_P = 0.07 pF diagonal C_P = 0.09 pF adjacent



DIMENSIONS IN MILLIMETERS AND (INCHES).

Maximum Ratings

Operating and Storage Temperature Range
E4 ..... -65°C to +125°C

DC Power Dissipation ..... 75 mW per Junction
Derated linearly to zero at maximum rated temperatures (measured in infinite heat sink at T_{CASE} = 25°C).

Soldering Temperature
E4 ..... 220°C for 10 sec

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Electrical Specifications at T_A = 25°C

Part Number 5082-	Package	Barrier	Maximum Capacitance C_M (pF)	Maximum Measured Capacitance Difference ΔC_M (pF)	Maximum V_F Difference ΔV_F (mV)	Maximum Dynamic Resistance R_D (Ω)	Typical Parameters: Forward Voltage V_F (V)
2830	E4	Medium	0.5 Typ.	0.20	20	12	0.40
Test Conditions			V_R = 0 f = 1 MHz		I_F = 5 mA between Adjacent Leads		I_F = 1 mA Measured between Adjacent Leads

Package Characteristics

The HP outline E4 package is designed for MIC, Microstrip, and Stripline use from dc through C-Band. The leads provide a good continuity of transmission line impedance to the monolithic diode array. The leads are tin plated copper.

Dynamic and Series Resistance

Schottky diode resistance may be expressed as series resistance, R_S, or as dynamic ressitance, R_D. These two terms are related by the equation

$$R_D = R_S = R_j$$

where R_j is the resistance of the junction. Junction resistance of a diode with DC bias is quite accurately calculated by

$$R_j = 26/I_B$$

where I_B is the bias current in milliamperes. The series resistance is independent of current.

The dynamic resistance is more easily measured. If series resistance is specified, it is usually obtained by subtracting the calculated junction resistance from the measured dynamic resistance.

SPICE Parameters

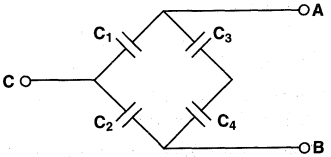
Parameter	Units	5082-2830
B_V	V	10
C_{J0}	pF	4
E_G	eV	0.69
I_{BV}	A	10E-5
I_S	A	2 x 10E-10
N		1.08
R_S	Ω	6
P_B	V	0.65
P_T		2
M		0.5

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches from the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. HP defines this measurement as "CM", and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capacitances can then be calculated by the formulas given below.

In a quad, the diagonal capacitance is the capacitance between points A and B as shown in figure below. The diagonal capacitance is calculated using the following formula

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$



The equivalent adjacent capacitance is the capacitance between points A and C in figure below. This capacitance is calculated using the following formula

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

HEWLETT® PACKARD

Beam Lead Schottky Diodes for Mixers and Detectors (1–26 GHz)

Technical Data

HSCH-5300 Series

Features

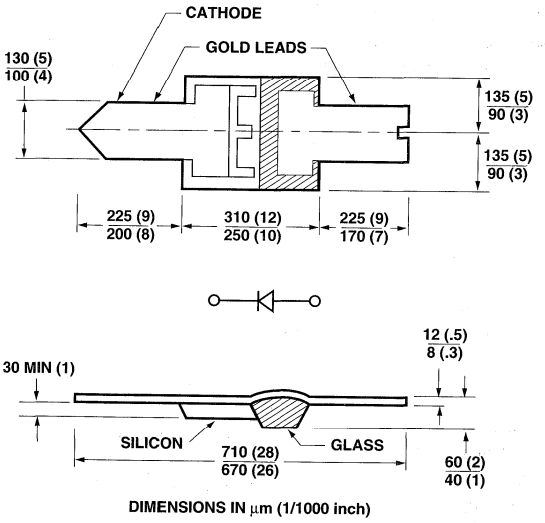
- **Platinum Tri-Metal System**
  High Temperature Stability
- **Silicon Nitride Passivation**
  Stable, Reliable Performance
- **Low Noise Figure**
  Guaranteed 7.5 dB at 26 GHz
- **High Uniformity**
  Tightly Controlled Process Insures Uniform RF Characteristics
- **Rugged Construction**
  4 Grams Minimum Lead Pull
- **Low Capacitance**
  0.10 pF Max. at 0 V
- **Polyimide Scratch Protection**

Description

These beam lead diodes are constructed using a metal-semiconductor Schottky barrier junction. Advanced epitaxial techniques and precise process control insure uniformity and repeatability of this planar passivated microwave semiconductor. A nitride passivation layer provides immunity from contaminants which could otherwise lead to I_R drift.

The HP beam lead process allows for large beam anchor pads for rugged construction (typical 6 gram pull strength) without degrading capacitance.

Outline 07



Maximum Ratings

Pulse Power Incident at T_A = 25°C ..... 1 W
Pulse Width = 1 µs, Du = 0.001
CW Power Dissipation at T_A = 25°C ..... 150 mW
Measured in an infinite heat sink derated linearly to zero at maximum rated temperature
T_{OPR} – Operating Temperature Range ..... -65°C to +175 °C
T_{STG} – Storage Temperature Range ..... -65°C to +200°C
Minimum Lead Strength ..... 4 grams pull on any lead
Diode Mounting Temperature ..... +350°C for 10 sec. max.

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Applications

The beam lead diode is ideally suited for use in stripline or microstrip circuits. Its small physical size and uniform dimensions give it low parasitics and repeatable RF characteristics through K-band.

The basic medium barrier devices in this family are DC tested HSCH-5310, -5312, and -5316. A batch matched version is available as the HSCH-5317. Equivalent low barrier devices are HSCH-5330, -5332, and -5336. Batch matched versions are available as HSCH-5331 and -5333.

For applications requiring guaranteed RF-tested performance up to 26 GHz, the HSCH-5340 is selected with batch match units available as the HSCH-5341. The HSCH-5318 is selected for 6.2 dB maximum noise figure at 9.375 GHz; with RF batch match units available as the HSCH-5319. The HSCH-5314 is rated at 7.2 dB maximum noise figure at 16 GHz with RF batch match units available as the HSCH-5315.

Assembly Techniques

Thermocompression bonding is recommended. Welding or conductive epoxy may also be used. For additional information see Application Note 979, "The Handling and Bonding of Beam Lead Devices Made Easy," or Application Note 993, "Beam Lead Device Bonding to Soft Substrates."

Table IA. Electrical Specifications for RF Tested Diodes at T_A = 25°C

Part Number HSCH-	Batch* Matched HSCH-	Barrier	Max. Noise Figure NF (dB)	I_F Impedance Z_{IF} (Ω) Min.	I_F Impedance Z_{IF} (Ω) Max.	Max. SWR	Min. Breakdown Voltage V_{BR} (V)	Max. Dynamic Resistance R_D (Ω)	Max. Total Capacitance C_T (pF)	Max. Forward Voltage V_F (mV)	Max. Leakage Current I_R (nA)
5318	5319	Medium	6.2 at 9.375 GHz	200	400	1.5:1	4	12	0.25	500	100
5314	5315		7.2 at 16 GHz					16	0.15		
5340	5341	Low	7.5 at 26 GHz	150	350	1.5:1	4	20	0.10	375	400
Test Conditions	ΔNF ≤ 0.3 dB $\Delta Z_{IF} \leq$ 25 Ω		DC Load Resistance - 0 Ω LO Power = 1 mW I_F = 30 MHz, 1.5 dB NF				$I_R \leq 10$ μA	I_F = 5 mA	V_R = 0 V f = 1 MHz	I_F = 1 mA	V_R = 1 V

*Minimum batch size 20 units.

Note:
1. $C_T = C_J + 0.02$ pF (fringing cap).

Table IB. Electrical Specifications for DC Tested Diodes at T_A = 25°C

Part Number HSCH-	Batch* Matched HSCH-	Barrier	Minimum Breakdown Voltage V_{BR} (V)	Maximum Dynamic Resistance R_D (Ω)	Maximum Total Capacitance C_T (pF)	Maximum Forward Voltage V_F (mV)	Maximum Leakage Current I_R (nA)
5316 5312 5310	5317	Medium	4	12 16 20	0.25 0.15 0.10	500	100
5336 5332 5330	5333 5331	Low	4	12 16 20	0.25 0.15 0.10	375	400
Test Conditions	$\Delta V_F \leq 15$ mV @ 5 mA		$I_R \leq 10$ µA	I_F = 5 mA	V_R = 0 V f = 1 MHz	I_F = 1 mA	V_R = 1 V

*Minimum batch size 20 units.

Typical Detector Characteristics at T_A = 25°C

Medium Barrier and Low Barrier (DC Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-54	dBm	20 µA Bias, R_L = 100 KΩ Video Bandwidth = 2 MHz f = 10 GHz
Voltage Sensitivity	γ	6.6	mV/µW	
Video Resistance	R_V	1400	Ω	

Low Barrier (Zero Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-44	dBm	Zero Bias, R_L = 10 MΩ Video Bandwidth = 2 MHz f = 10 GHz
Voltage Sensitivity	γ	10	mV/µW	
Video Resistance	R_V	1.8	MΩ	

SPICE Parameters

Parameter	Units	HSCH-5316 HSCH-5318	HSCH-5312 HSCH-5314	HSCH-5310	HSCH-5330 HSCH-5340	HSCH-5332	HSCH-5336
B_V	V	5	5	5	5	5	5
C_{J0}	pF	0.2	0.13	0.09	0.09	0.13	0.20
E_G	eV	0.69	0.69	0.69	0.69	0.69	0.69
I_{BV}	A	10E-5	10E-5	10E-5	10E-5	10E-5	10E-5
I_S	A	3 x 10E-10	3 x 10E-10	3 x 10E-10	4 x 10E-10	4 x 10E-8	4 x 10E-8
N		1.08	1.08	1.08	1.08	1.08	1.08
R_S	Ω	5	9	13	13	9	6
P_B	V	0.65	0.65	0.65	0.5	0.5	0.5
P_T		2	2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5	0.5

Typical Parameters

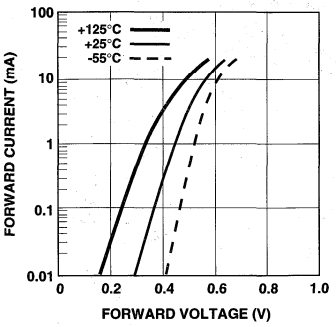


Figure 1. Typical Forward Characteristics for Medium Barrier Beam Lead Diodes. HSCH-5310 Series.

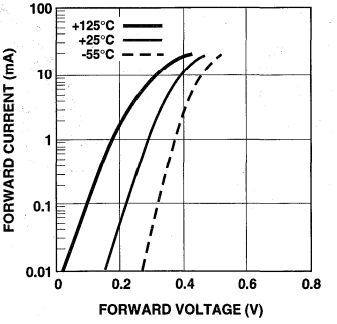


Figure 2. Typical Forward Characteristics for Low Barrier Beam Lead Diodes. HSCH-5330, -5340 Series.

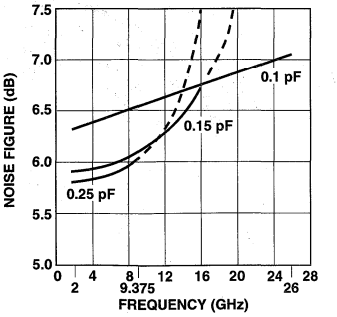


Figure 3. Typical Noise Figure vs. Frequency.

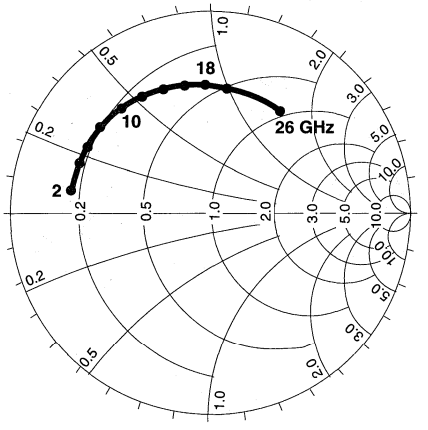


Figure 4. Typical Admittance Characteristics with 1 mA Self Bias. HSCH-5340 and -5341.

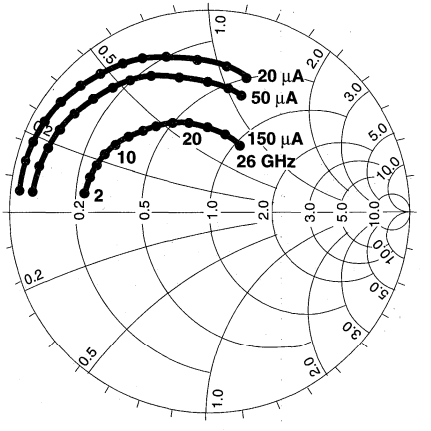


Figure 5. Typical Admittance Characteristics with External Bias. HSCH-5340 and -5341.

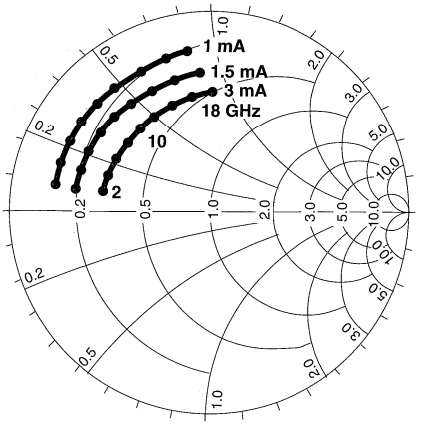


Figure 6. Typical Admittance Characteristics with Self Bias. HSCH-5314 and -5315.

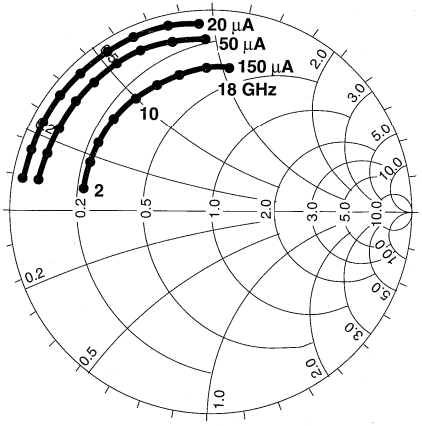


Figure 7. Typical Admittance Characteristics with External Bias. HSCH-5314 and -5315.

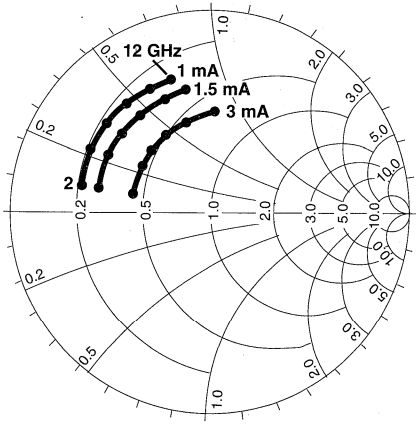


Figure 8. Typical Admittance Characteristics with Self Bias. HSCH-5318 and -5319.

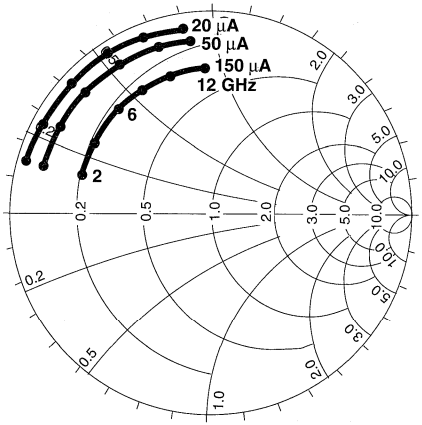
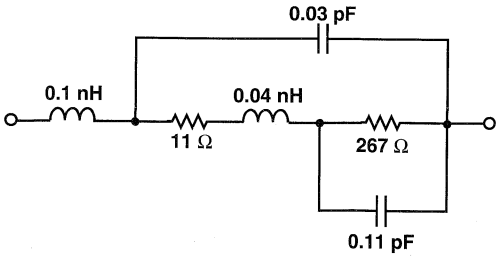


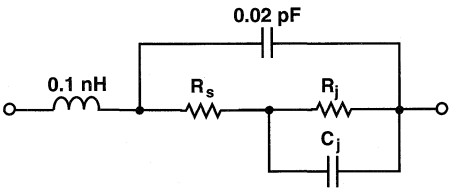
Figure 9. Typical Admittance Characteristics with External Bias. HSCH-5318 and -5319.

Models for Each Beam Lead Schottky Diode

HSCH-5340, -5341
1 mA Self Bias

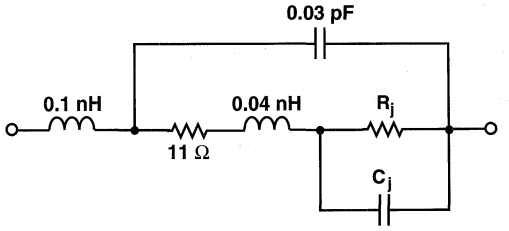


Other HSCH-53XX
Self Bias



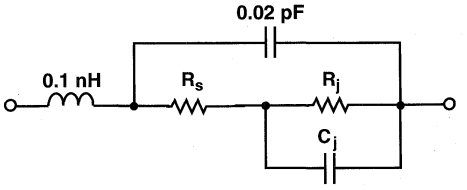
Part Numbers	1.0 mA Self Bias			1.5 mA Self Bias			3.0 mA Self Bias		
	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)
HSCH-5314, -5315	5.0	393	0.11	5.2	232	0.11	5.0	150	0.12
HSCH-5318, -5319	5.1	244	0.16	5.0	178	0.16	5.0	109	0.19

HSCH-5340, -5341
External Bias



Part Numbers	20 μA DC Bias		50 μA DC Bias		150 μA DC Bias	
	R_j (Ω)	C_j (pF)	R_j (Ω)	C_j (pF)	R_j (Ω)	C_j (pF)
HSCH-5340, -5341	1300	0.09	560	0.09	187	0.10

Other HSCH-53XX
External Bias



Part Numbers	20 μADC Bias			50 μADC Bias			150 μADC Bias		
	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)
HSCH-5314, -5315	2.8	1300	0.11	4.7	520	0.12	2.7	180	0.13
HSCH-5318, -5319	5.1	1300	0.18	3.9	520	0.19	4.7	180	0.20

HEWLETT® PACKARD

Beam Lead Schottky Diode Pairs for Mixers and Detectors

Technical Data

HSCH-5500 Series

Features

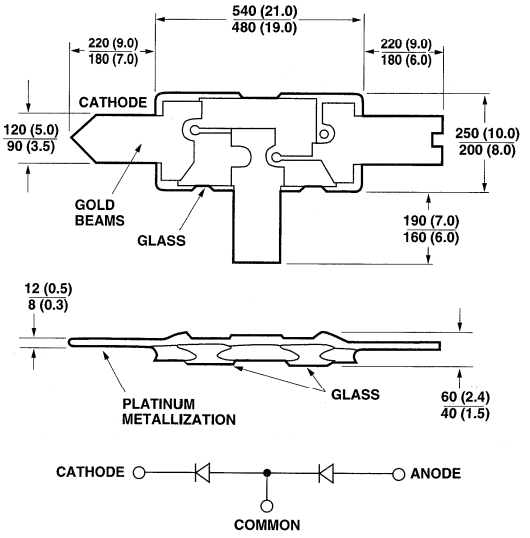
- **Monolithic Pair**
  Closely Matched Electrical Parameters
- **Low Capacitance**
  0.1 pF Maximum at 0 Volts
- **Low Noise Figure**
  Typical 7.5 dB at 26 GHz
- **Rugged Construction**
  4 Grams Minimum Lead Pull
- **Platinum Tri-Metal System**
  High Temperature Stability
- **Polyimide Scratch Protection**
- **Silicon Nitride Passivation**
  Stable, Reliable Performance

Description

These dual beam lead diodes are constructed using a metal-semiconductor Schottky barrier junction. Advanced epitaxial techniques and precise process control insure uniformity and repeatability of this planar passivated microwave semiconductor. A nitride passivation layer provides immunity from contaminants which could otherwise lead to I_R drift.

The HP beam lead process allows for large beam anchor pads for rugged construction (typical 6 gram pull strength) without degrading capacitance.

Outline 04B



DIMENSIONS IN μm (1/1000 inch)

Maximum Ratings (for Each Diode)

Pulse Power Incident at T_A = 25°C ..... 1 W
Pulse Width = 1 μs, Du = 0.001
CW Power Dissipation at T_A = 25°C ..... 150 mW
Measured in an infinite heat sink derated linearly to zero at maximum rated temperature
T_{OPR} – Operating Temperature Range .....-65°C to +175 °C
T_{STG} – Storage Temperature Range .....-65°C to +200°C
Minimum Lead Strength ..... 4 grams pull on any lead
Diode Mounting Temperature ..... 350°C for 10 sec. max.

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Applications

The beam lead diode is ideally suited for use in stripline or microstrip or coplanar waveguide circuits. Its small physical size and uniform dimensions give it low parasitics and repeatable RF characteristics through K-band.

These dual beam leads are intended for use in balanced mixers and in even harmonic anti-parallel pair mixers. By using several of these devices in the proper configuration it is easy to assemble bridge quads, star quads, and ring quads for Class I, II, or III type double balanced mixers.

Assembly Techniques

Thermocompression bonding is recommended. Welding or conductive epoxy may also be used. For additional information see Application Note 979, "The Handling and Bonding of Beam Lead Devices Made Easy," or Application Note 993, "Beam Lead Device Bonding to Soft Substrates."

Electrical Specifications for DC Tested Diodes at T_A = 25°C

Part Number HSCH-[1]	Barrier	Minimum Breakdown Voltage V_{BR} (V)	Maximum Dynamic Resistance R_D (Ω)	Max. ΔR_D (Ω)	Maximum Total Capacitance C_T (pF)	Max. ΔC_T (pF)	Maximum Forward Voltage V_F (mV)	Max. ΔV_F (mV)	Max. I_R (nA)
5511	Medium	4	20	3	0.10	0.02	500	10	100
5512			16	2	0.15	0.03			
5531	Low		20	3	0.10	0.02	375		400
Test Conditions		I_R = 10 μA	I_F = 5 mA		V_R = 0 V, f = 1 MHz		I_F = 1 mA		V_R = 1 V

Note:
1. Standard Hi-Rel program available on HSCH-5511 and HSCH-5531. Others are available upon request.

Typical Detector Characteristics at T_A = 25°C

Medium Barrier and Low Barrier (DC Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-55	dBm	20 μA Bias, Zero Bias, P_{in} = -40 dBm, R_L = 100 KΩ, Video Bandwidth = 2 MHz, f = 10 GHz
Voltage Sensitivity	γ	9.0	mV/μW	
Video Resistance	R_V	1350	Ω	

Low Barrier (Zero Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-46	dBm	Zero Bias, Zero Bias, P_{in} = -30 dBm, R_L = 10 MΩ, Video Bandwidth = 2 MHz, f = 10 GHz
Voltage Sensitivity	γ	17	mV/μW	
Video Resistance	R_V	1.4	MΩ	

SPICE Parameters

Parameter	Units	HSCH-5512	HSCH-5511	HSCH-5531
B_V	V	5	5	5
C_{J0}	pF	0.13	0.09	0.09
E_G	eV	0.69	0.69	0.69
I_{BV}	A	10E-5	10E-5	10E-5
I_S	A	3 x 10E-10	3 x 10E-10	4 x 10E-8
N		1.08	1.08	1.08
R_S	Ω	9	13	13
P_B	V	0.65	0.65	0.5
P_T		2	2	2
M		0.5	0.5	0.5

Typical Parameters

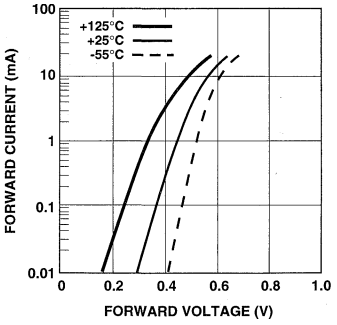


Figure 1. Typical Forward Characteristics for Medium Barrier Beam Lead Diodes. HSCH-551X Series.

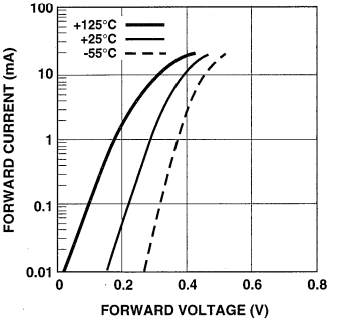


Figure 2. Typical Forward Characteristics for Low Barrier Beam Lead Diodes. HSCH-553X Series,

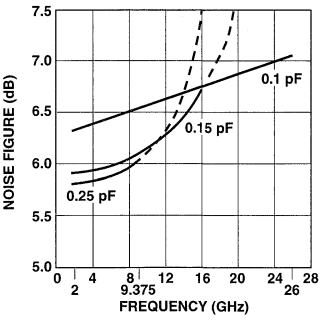


Figure 3. Typical Noise Figure vs. Frequency.

Figure 4. Typical Admittance Characteristics with 1 mA Self Bias. HSCH-5511 and -5331.

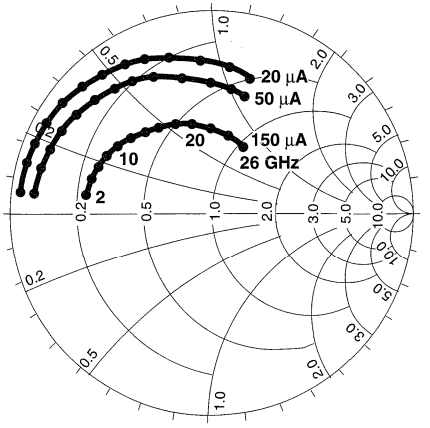


Figure 5. Typical Admittance Characteristics with External Bias. HSCH-5511 and -5531.

Typical Parameters, continued

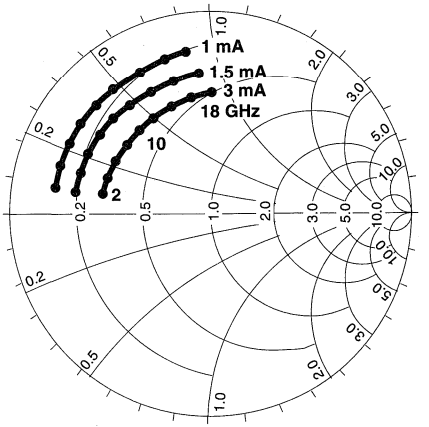


Figure 6. Typical Admittance Characteristics with Self Bias. HSCH-5512.

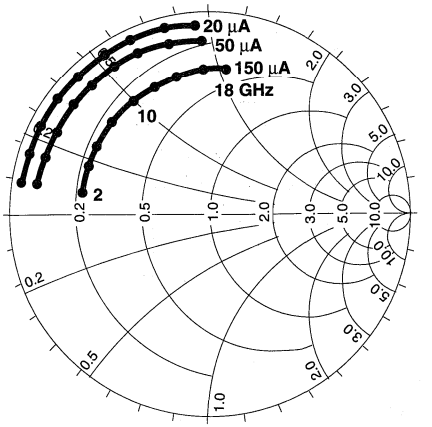


Figure 7. Typical Admittance Characteristics with External Bias. HSCH-5512.

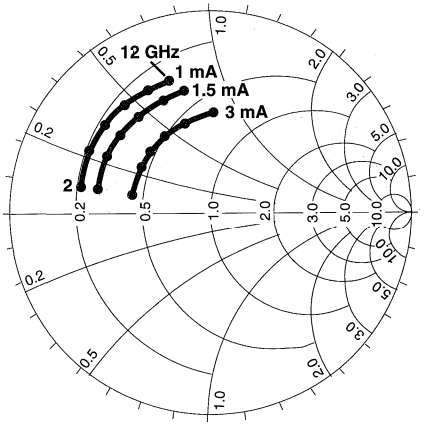


Figure 8. Typical Admittance Characteristics with Self Bias. HSCH-5536.

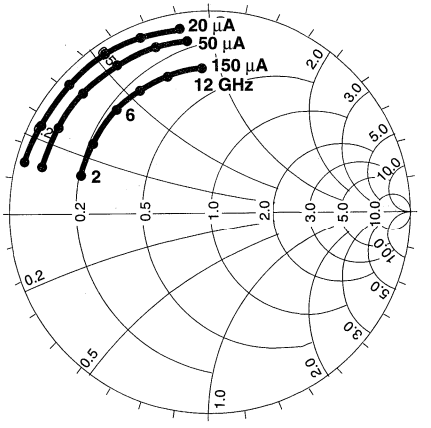
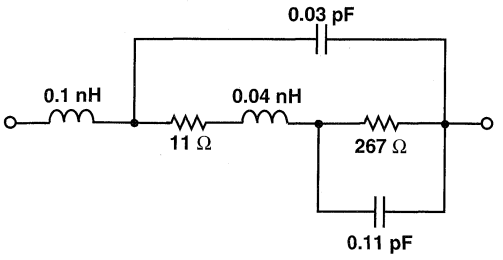


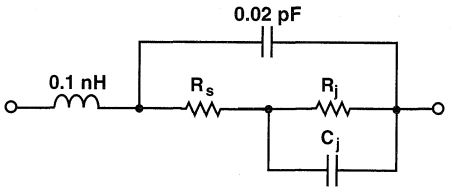
Figure 9. Typical Admittance Characteristics with External Bias. HSCH-5536.

Models for Each Beam Lead Schottky Diode

HSCH-5511, -5531
1 mA Self Bias



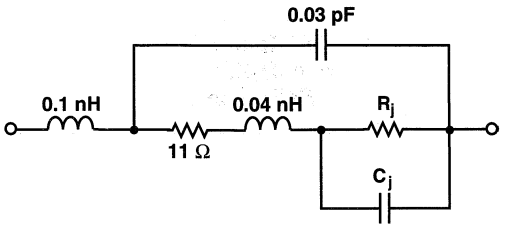
HSCH-5512
Self Bias



Part Number	1.0 mA Self Bias			1.5 mA Self Bias			3.0 mA Self Bias		
	R_1 (Ω)	R_2 (Ω)	C (pF)	R_1 (Ω)	R_2 (Ω)	C (pF)	R_1 (Ω)	R_2 (Ω)	C (pF)
HSCH-5512	5.0	393	0.11	5.2	232	0.11	5.0	150	0.12

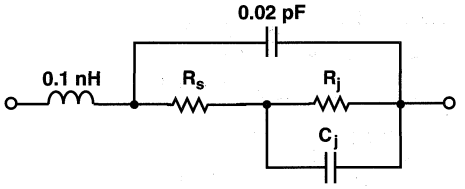
Models for Each Beam Lead Schottky Diode, continued

HSCH-5511, -5531
External Bias



Part Numbers	20 μA DC Bias		50 μA DC Bias		150 μA DC Bias	
	R_j (Ω)	C_j (pF)	R_j (Ω)	C_j (pF)	R_j (Ω)	C_j (pF)
HSCH-5511, -5531	1400	0.09	560	0.09	187	0.10

HSCH-5512
External Bias



Part Numbers	20 μA DC Bias			50 μA DC Bias			150 μA DC Bias		
	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)
HSCH-5512	2.8	1240	0.11	4.7	550	0.12	2.7	180	0.13

HEWLETT® PACKARD

GaAs Beam Lead Schottky Barrier Diodes

Technical Data

HSCH-9101
HSCH-9201
HSCH-9251

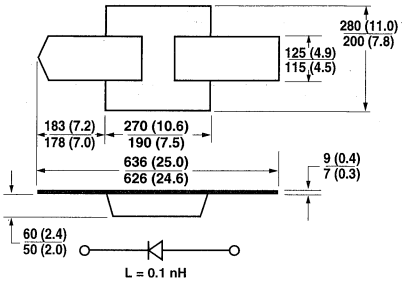
Features

- **Gold Tri-Metal System**
  For Improved Reliability
- **Low Capacitance**
- **Low Series Resistance**
- **High Cutoff Frequency**
- **Polyimide Passivation**
- **Multiple Configurations**

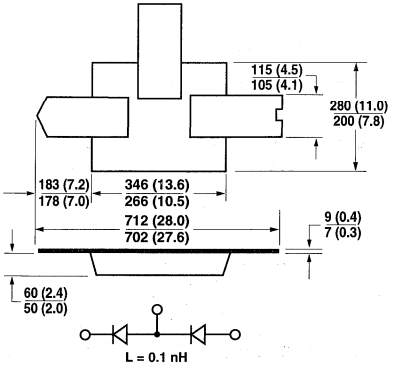
Description

The HSCH-9101 single, the HSCH-9201 series pair, and the HSCH-9251 anti-parallel pair are advanced gallium arsenide Schottky barrier diodes. These devices are fabricated utilizing molecular beam epitaxy (MBE) manufacturing techniques and feature rugged construction and consistent electrical performance. A polyimide coating provides scratch protection and resistance to contamination.

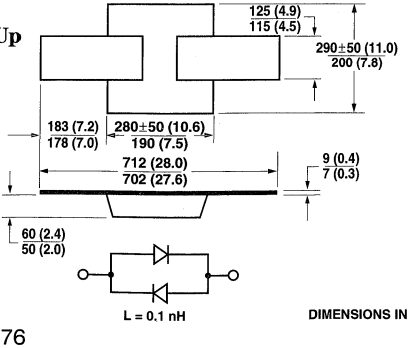
HSCH-9101



HSCH-9201



HSCH-9251
Junction Side Up



DIMENSIONS IN μm (1/1000 inch)

Applications

This line of Schottky diodes is optimized for use in mixer applications at millimeter wave frequencies. Some suggested mixer types are single ended and single balanced for the single and series pair. The anti-parallel pair is ideal for harmonic mixers.

Assembly Techniques

Thermocompression bonding is recommended. Welding or conductive epoxy may also be used. For additional information see Application Note 979, "The Handling and Bonding of Beam Lead Devices Made Easy," or Application Note 992, "Beam Lead Attachment Methods," or Application Note 993, "Beam Lead Device Bonding to Soft Substrates."

GaAs diodes are ESD sensitive. Proper precautions should be used when handling these devices.

Maximum Ratings

Power Dissipation at T_{LEAD} = 25°C ..... 75 mW per junction
Measured in an infinite heat sink derated linearly to zero at maximum rated temperature
Operating Temperature ..... -65°C to +150°C
Storage Temperature ..... -65°C to +150°C
Mounting Temperature ..... 235°C for 10 seconds
Minimum Lead Strength ..... 6 grams

Electrical Specifications at T_A = 25°C

Part Number			HSCH-9101			HSCH-9201			HSCH-9251		
Symbol	**Parameters and Test Conditions**	**Units**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
C_j[1]	Junction Capacitance V_R = 0 V, f = 1 MHz	pF		0.040	0.050		0.040	0.050		0.040	
ΔC_j[1]	Junction Capacitance Difference V_R = 0 V, f = 1 MHz	pF					0.005	0.010			
R_S[2]	Series Resistance	Ω			6			6			6
V_{F1}	Forward Voltage I_F = 1 mA	mV		700	800		700	800		700	800
V_{F10}	Forward Voltage I_F = 10 mA	mV		800	850		800	850		800	850
ΔV_F	Forward Voltage Difference I_F = 1 mA and 10 mA	mV						15			15
V_{BR}	Reverse Breakdown Voltage $V_R = V_{BR}$ measure $I_R \leq 10$ μA (per junction)	V	4.5			4.5					

Notes:
1. Junction capacitance is determined by measuring total device capacitance and subtracting the calculated parasitic capacitance (0.035 pF).
2. Series resistance is determined by measuring the dynamic resistance and subtracting the calculated junction resistance of 6 Ω.

Typical Parameters

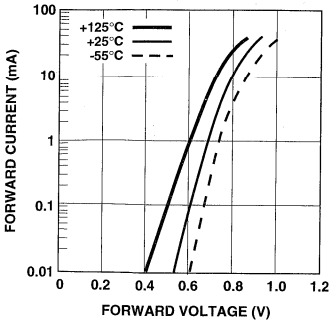


Figure 1. Typical Forward Characteristics for HSCH-9101, HSCH-9201, and HSCH-9251.

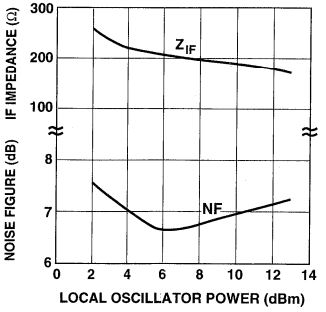


Figure 2. Typical Noise Figure and I.F. Impedance vs. Local Oscillator Power, for HSCH-9101 and HSCH-9201.

SPICE Parameters

Parameter	Units	HSCH-9XXX
B_V	V	5
C_{J0}	pF	0.04
E_G	eV	1.43
I_{BV}	A	10E-5
I_S	A	1.6 x 10E-13
N		1.20
R_S	Ω	5
P_B	V	0.7
P_T		2
M		0.5

HEWLETT® PACKARD

GaAs Beam Lead Schottky Barrier Ring and Bridge Diodes

Technical Data

HSCH-9301
HSCH-9351

Features

- **Gold Tri-Metal System**
  For Improved Reliability
- **Low Capacitance**
- **Low Series Resistance**
- **High Cutoff Frequency**
- **Polyimide Passivation**

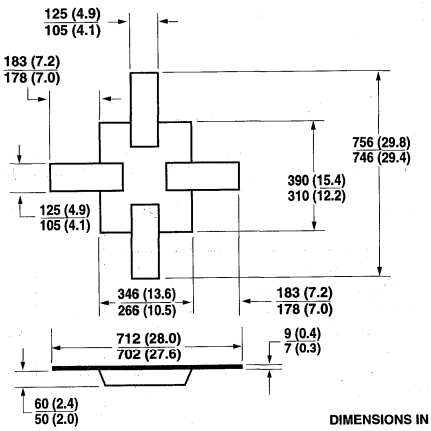
Description

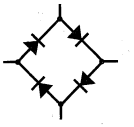
The HSCH-9301 ring quad and the HSCH-9351 bridge quad are advanced gallium arsenide Schottky barrier diodes. These devices are fabricated utilizing molecular beam epitaxy (MBE) manufacturing techniques and feature rugged construction and consistent electrical performance. A polyimide coating provides scratch protection and resistance to contamination.

Applications

This line of Schottky diodes is optimized for use in mixer applications at millimeter wave frequencies. Some suggested mixer types are double balanced for the ring quad and biased double balanced for the bridge quad. The bridge quad can also be used in sampling circuits.

HSCH-9301 (Junction Side Up)

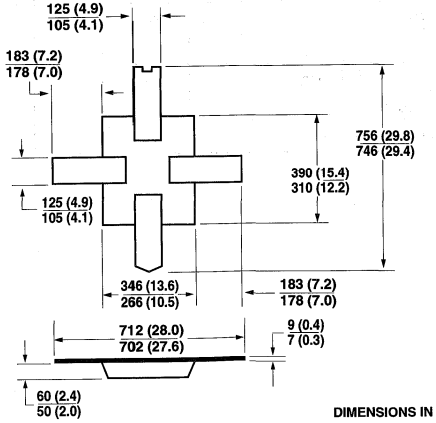


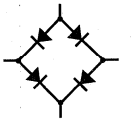


L = 0.1 nH

DIMENSIONS IN μm (1/1000 inch)

HSCH-9351 (Junction Side Up)





L = 0.1 nH

DIMENSIONS IN μm (1/1000 inch)

Assembly Techniques

Thermocompression bonding is recommended. Welding or conductive epoxy may also be used. For additional information see Application Note 979, "The Handling and Bonding of Beam Lead Devices Made Easy," or Application Note 992, "Beam Lead Attachment Methods," or Application Note 993, "Beam Lead Device Bonding to Soft Substrates."

GaAs diodes are ESD sensitive. Proper precautions should be used when handling these devices.

Maximum Ratings

Power Dissipation at T_{LEAD} = 25°C ..... 75 mW per junction
Measured in an infinite heat sink derated linearly to zero at maximum rated temperature
Operating Temperature ..... -65°C to +150°C
Storage Temperature ..... -65°C to +150°C
Mounting Temperature ..... 235°C for 10 seconds
Minimum Lead Strength ..... 6 grams

Electrical Specifications at T_A = 25°C

Part Number			HSCH-9301			HSCH-9351		
Symbol	**Parameters and Test Conditions**	**Units**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
C_M	Measured Capacitance V_R = 0 V, f = 1 MHz	pF		0.075	0.100		0.075	0.100
C_{TA}	Total Adjacent Capacitance V_R = 0 V, f = 1 MHz	pF		0.110			0.110	
C_{TD}	Total Diagonal Capacitance V_R = 0 V, f = 1 MHz	pF		0.075			0.075	
ΔC_M	Measured Capacitance Difference V_R = 0 V, f = 1 MHz	pF		0.015	0.025		0.015	0.025
R_S	Series Resistance	Ω			6			6
V_F	Forward Voltage I_F = 1 mA	mV		700	800		700	800
ΔV_F	Forward Voltage Difference I_F = 1 mA	mV			20			20
V_{BR}	Reverse Breakdown Voltage $V_R = V_{BR}$ measure $I_R \leq 10$ µA (per junction)	V				4.5		

Typical Parameters

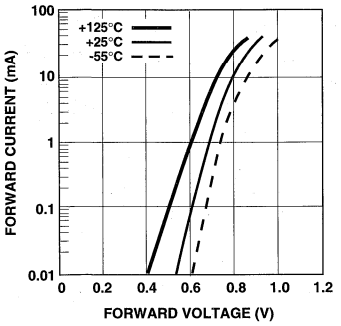


Figure 1. Typical Forward Characteristics for HSCH-9301, HSCH-9351.

SPICE Parameters

Parameter	Units	HSCH-9XXX
B_V	V	5
C_{J0}	pF	0.04
E_G	eV	1.43
I_{BV}	A	10E-5
I_S	A	1.6 x 10E-13
N		1.20
R_S	Ω	5
P_B	V	0.7
P_T		2
M		0.5

Dynamic and Series Resistance

Schottky diode resistance may be expressed as series resistance, R_S, or as dynamic resistance, R_D. These two terms are related by the equation

$$R_D = R_S + R_j$$

where R_j is the resistance of the junction. Junction resistance of a diode with DC bias is quite accurately calculated by

$$R_j = 26/I_B$$

where I_B is the bias current in milliamperes. The series resistance is independent of current.

The dynamic resistance is more easily measured. If series resistance is specified it is usually obtained by subtracting the calculated junction resistance from the measured dynamic resistance.

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches from the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. HP defines this measurement as "C_M," and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capacitances can then be calculated by the formulas given below.

In a quad, the diagonal capacitance is the capacitance between points A and B as shown in Figure 2. The diagonal capacitance is calculated using the following formula

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$

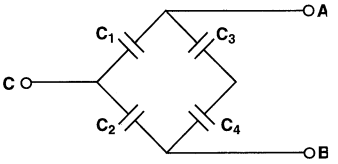


Figure 2.

The equivalent capacitance is the capacitance between points A and C in Figure 2. This capacitance is calculated using the following formula

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

Bonding and Handling Procedures for Beam Lead Diodes

1. Storage

Under normal circumstances, storage of beam lead diodes in HP supplied waffle/gel packs is sufficient. In particularly dusty or chemically hazardous environments, storage in an inert atmosphere desiccator is advised.

2. Handling

In order to avoid damage to beam lead devices, particular care must be exercised during inspection, testing, and assembly. Although the beam lead diode is designed to have exceptional lead strength, its small size and delicate nature requires that special handling techniques be observed so that the devices will not be mechanically or electrically damaged. A vacuum pickup is recommended for picking up beam lead devices, particularly larger ones, e.g., quads. Care must be exercised to assure that the vacuum opening of the needle is sufficiently small to avoid passage of the device through the opening. A #27 tip is recommended for picking up single beam lead devices. A 20X magnification is needed for precise positioning of the tip on the device. Where a vacuum pickup is not used, a sharpened wooden Q-tip dipped in isopropyl alcohol is very commonly used to handle beam lead devices.

3. Cleaning

For organic contamination use a warm rinse of trichloroethane followed by a cold rinse in acetone and methanol. Dry under infrared heat lamp for 5-10 minutes on clean filter paper. Freon degreaser may replace trichloroethane for light organic contamination.

- Ultrasonic cleaning is not recommended.
- Acid solvents should not be used.

4. Bonding

See Application Note 992, "Beam Lead Attachment Methods", for a general description of the various methods for attaching beam lead diodes to both hard and soft substrates.

Thermocompression: See Application Note 979 "The Handling and Bonding of Beam Lead Devices Made Easy". This method is good for hard substrates only.

Wobble: This method picks up the device, places it on the substrate and forms a thermocompression bond all in one operation. This is described in MIL-STD-883, Method 2017 and is intended for hard substrates only. Equipment specifically designed for beam lead wobble bonding is available from KULICKE and SOFFA in Horsham, PA.

Ultrasonic: Not recommended.

Resistance Welding or Parallel-GAP Welding: To make welding on soft substrates easier, a low pressure welding head is recommended. Suitable equipment is available from HUGHES, Industrial Products Division in Carlsbad, CA.

For more information, see Application Note 993, "Beam Lead Diode Bonding to Soft Substrates".

Epoxy: With solvent free, low resistivity epoxies (available from ABLESTIK in Gardena, CA, MICON in Lexington, MA, and many others) and improvements in dispensing equipment, the quality of epoxy bonds is sufficient for many applications. Equipment is available from ADVANCED SEMICONDUCTOR MATERIALS AMERICA, INC., Assembly Products Group in Chandler, AZ (Automatic), and WEST BOND in Orange, CA (Manual).

Reflow: Not recommended.

HEWLETT® PACKARD

Zero Bias Beamlead Detector Diode

Technical Data

HSCH-9161

Features

- **Low Junction Capacitance**
- **Lower Temperature Coefficient than Silicon**
- **Durable Construction— Typical 6 gram beamlead strength**
- **Operation to 110 GHz**

Description

Hewlett-Packard's HSCH-9161 detector diode is a beamlead, GaAs device fabricated using the modified barrier integrated diode (MBID) process[1]. This diode is designed for zero bias detecting applications at frequencies through 110 GHz. It can be mounted in ceramic microstrip (MIC), finline and coplanar waveguide circuits.

[1] The diode structure and process are covered by U.S. Patent No. 4,839,709 issued to Mark Zurakowski on June 13, 1989, and assigned to Hewlett-Packard.

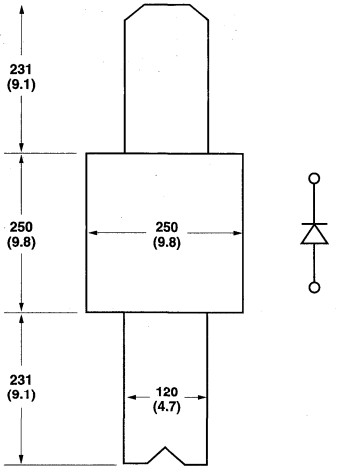
Applications

At room temperature and frequencies under 10 GHz, the silicon zero bias Schottky detectors HSMS-0005 and HSMS-2850 offer comparable performance. However, the HSCH-9161 yields virtually flat detection sensitivity from 10 to 30 GHz with good performance from 30 to 110 GHz. In a wideband matched detector, in which a shunt 50 Ω resistor is used in front of the diode, voltage sensitivity (γ) is calculated to be 1 mV/μW. Where a high-Q reactive impedance matching network is substituted for the shunt 50 Ω resistor, values of γ approaching 25 mV/μW can be expected.

In applications below 10 GHz where DC bias is not available and where temperature sensitivity is a design consideration, the HSCH-9161 offers superior stability when compared to silicon zero bias Schottky diodes.

Bonding and Handling

For more detailed information, see HP Application Note 999, "GaAs MMIC Assembly and Handling Guidelines."



ALL DIMENSIONS IN MICRONS.

HSCH-9161 Absolute Maximum Ratings, T_A = 25°C

Symbol	Parameters/Conditions	Units	Min.	Typ.	Max.
T_{op}	Operating Temp. Range	°C	-65		175
T_{stg}	Storage Temp. Range	°C	-65		200
P_B	Burnout Power	dBm		20	

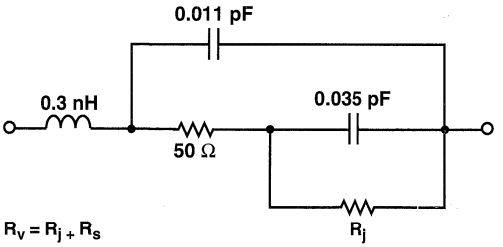
DC Specifications/Physical Properties, T_A = 25°C

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
C_j	Junction Capacitance Test Conditions: f = 1 GHz	pF		.035	
R_V	Video Resistance Test Conditions: Zero Bias	kΩ	1.8		7.5
γ	Voltage Sensitivity Test Conditions: Zero Bias, 10 GHz, shunt 50 Ω input matching resistor	mV/μW	0.5		
—	Beamlead Strength	grams	3		

Assembly Techniques

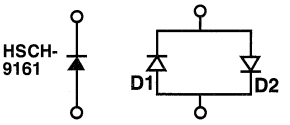
Thermocompression bonding is recommended. Welding or conductive epoxy may also be used. For additional information see Application Note 979, "The Handling and Bonding of Beam Lead Devices Made Easy," or Application Note 992, "Beam Lead Attachment Methods," or Application Note 993, "Beam Lead Device Bonding to Soft Substrates."

Small Signal Linear Model



SPICE Parameters

Because of the high leakage of this diode under reverse bias, it must be modelled as an anti-parallel pair.



D1 represents the characteristic of the HSCH-9161 under forward bias and D2 (in the forward direction) gives the V-I curve of the HSCH-9161 under reverse bias.

Parameter	Units	D1	D2
B_V	V	10	10
C_{JO}	pF	0.030	0.030
E_G	eV	1.42	1.42
I_{BV}	A	10E-12	10E-12
I_S	A	12 x 10E-6	84 x 10E-6
N		1.2	40.0
R_S	Ω	50	10
P_B (V_J)	V	0.26	0.26
P_T (XTI)		2	2
M		0.5	0.5

HSCH-9161 Typical Performance

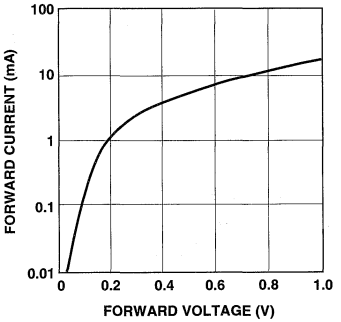


Figure 1. Forward Current vs. Forward Voltage.

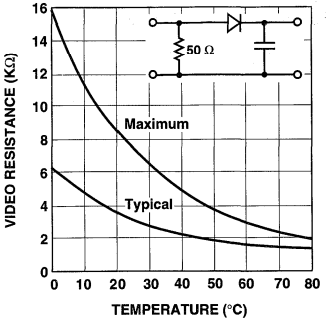


Figure 2. Typical Variation of Video Resistance vs. Temperature.

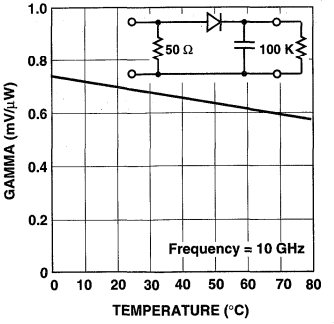


Figure 3. Calculated Variation of Voltage Sensitivity vs. Temperature.

HEWLETT® PACKARD

Schottky Barrier Chips for Hybrid Integrated Circuits

Technical Data

HSMS-0005/06
HSMS-8002/12

Features

- **Thermocompression/ Thermosonically Bondable**
- **Gold Metallization**
- **Silicon Nitride Passivation**
- **Uniform Electrical Characteristics**
- **Batch Matched Versions Available**
- **Planar Construction**
- **Available in Many Electrical Selections**
- **Ideal for Hybrid Integrated Circuits**

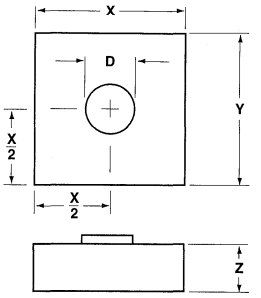
Description/Applications

These Schottky chips are designed for hybrid applications at DC through K-band frequencies. The passivated planar construction of these Schottky chips provides a wide temperature range capability combined with broad bandwidth performance.

A variety of chips are provided which are optimized for various analog and digital applications. Typical applications of Schottky chips are mixing, detecting, switching, gating, sampling, and wave shaping.

This series of Schottky diode chips are specifically designed for analog and digital hybrid applications requiring thermosonic or thermocompression bonding techniques. The large bonding pad allows easy bonding. The top metallization is a layer of gold deposited on adhesive metal layers for a tarnish-free surface that allows either thermosonic or thermocompression bonding techniques. The bottom metallization is also gold, suitable for epoxy or eutectic die attach methods.

Chip Dimensions



DIMENSIONS	PART NO. HSMS-	
	-0006/-8002	-0005
D	75 (3)	55 (2)
X	250 (10)	250 (10)
Y	275 (11)	250 (10)
Z	150 (8)	150 (6)
Top Contact	Anode	Cathode

NOTES:
1. Dimensions in microns (1/1000 inch).
2. Dimension tolerance is ±30μ.
3. All contact metallization is gold.

Absolute Maximum Ratings, T_A = 25°C

Symbol	Parameter	Units	HSMS-8002	HSMS-0005
P_T	Total device dissipation, measured in an infinite heatsink. Derate linearly to zero at maximum rated temperature	mW	75	75
P_{IV}	Peak Inverse Voltage	V	4.0	2.0
TJ	Junction Temperature (maximum)	°C	150	200
T_{STG}	Storage Temp. Range	°C	−65 to 150	−65 to 200
T_{OP}	Operating Temperature	°C	−65 to 150	−65 to 200

Note: Operation in excess of any one of these conditions may result in permanent damage to the device.

DC Electrical Specifications at T_A = 25°C

Schottky Barrier Chips for Microwave and RF Mixers

Part Number HSMS-	Batch Matched[1] HSMS-	Nearest Equivalent Packaged Part: HSMS-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	Maximum Forward Voltage V_F (mV)	Maximum Capacitance C_T (pF)	Maximum Dynamic Resistance R_D (Ω)[2]
8002	8012	8101	4	250	350	0.16	14
Test Conditions	ΔV_F = 15 mV I_F = 1 mA		I_R = 10 μA	I_F = 1 mA		V_R = 0 V f = 1.0 MHz	I_F = 5 mA

Notes:
1. Standard batch match size, 100 units.
2. To obtain R_S, subtract 26/5 = 5.2 Ω.

RF Electrical Parameters at T_A = 25°C

Part Number HSMS-	Typical Conversion Loss L_C (dB)	Typical IF Impedance Z_{IF} (Ω)	Typical SWR	Typical Tangential Sensitivity T_{SS} (dBm)
8002	5.5	150	1.2:1	-46
Test Conditions	f = 16 GHz DC load resistance = 0 Ω, LO power = 1 mW			f = 10 GHz BW = 2 MHz I_{BIAS} = 20 μA

DC Electrical Specifications at T_A = 25°C

Schottky Barrier Chips for Microwave and RF Detectors

Part Number HSMS-	Nearest Equivalent Packaged Part No. HSMS-	Maximum Forward Voltage V_F (mV)	Minimum Breakdown Voltage V_{BR} (V)	Typical Capacitance C_T (pF)
0005	2850	250	—	0.20
0006	2860	350	4.0	0.17
Test Conditions		I_F = 1 mA	I_R = 10 μA	V_R = 0.5 V, f = 1 MHz

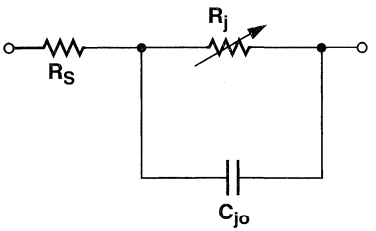
Typical RF Electrical Parameters at T_A = 25°C

Part Number HSMS-	DC Bias	Voltage Sensitivity γ (mV/μW)			Video Resistance R_V (KΩ)
		915 MHz	2.45 GHz	5.8 GHz	
0005	zero	40	30	22	8.0
0006	5 μA	40	32	25	5.5
Test Conditions		P_{in} = -40 dBm	R_L = 100 KΩ		

SPICE Parameters

Parameter	Units	HSMS-8002	HSMS-0005	HSMS-0006
B_V	V	7.0	3.8	6.0
C_{J0}	pF	0.16	0.16	0.17
E_G	eV	0.69	0.69	0.69
I_{BV}	A	10E-5	10E-5	10E-5
I_S	A	4.6 x 10E-8	3 x 10E-6	3 x 10E-8
N		1.08	1.15	1.10
R_S	Ω	5.0	20	7.0
P_B	V	0.65	0.65	0.65
P_T		2	2	2
M		0.5	0.5	0.5

Equivalent Circuit Model



$$R_j \approx \frac{.026}{I_s + I_b}$$

I_b = bias current in A

Assembly and Handling Procedures for Schottky Chips

1. Storage

Devices should be stored in a dry nitrogen purged desiccator or equivalent.

2. Cleaning

If required, surface contamination may be removed with electronic grade solvents such as freon (T.F. or T.M.C.), acetone, deionized water, and methanol used singularly or in combinations. Typical cleaning times per solvent are one to three minutes. DI water and methanol should be used (in that order) in the final cleansing. Final drying can be accomplished by placing the cleaned dice on clean filter paper and drying with an infrared lamp for 5–10 minutes. Acids such as hydrofluoric (HF), nitric (HNO_3) and hydrochloric (HCl) must not be used.

The effects of cleaning methods/solutions should be verified on small samples prior to submitting the entire lot.

Following cleaning, dice should either be used in assembly (typically within a few hours) or stored in clean containers in an inert atmosphere or a vacuum chamber.

3. Die Attach

a. Eutectic

Eutectic die attach can be accomplished by "scrubbing" the die with a preform on the header. (Note—times and temperature utilized vary depending on the type of preform.) For example, 310°C is suitable for a Au/Sn preform.

b. Epoxy

For epoxy die-attach, conducive silver-filler epoxies are recommended. This method can be used for all Hewlett-Packard Schottky chips.

4. Wire Bonding

Thermocompression wire bonding is recommended. Suggested wire is pure gold, 0.7 to 1.5 mil diameter.

HEWLETT® PACKARD

Tri Metal Beam Lead Schottky Diodes

Reliability Data

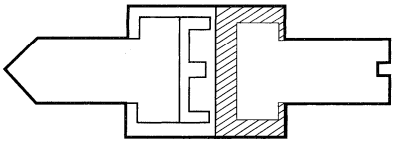
HSCH-5300 Series
HSCH-5500 Series

Conclusion

Hewlett-Packard's beam lead diodes have successfully passed stringent environmental testing. Hewlett-Packard beam lead diodes may be used in military and space applications without the necessity of hermetically sealed packaging.

General

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is compiled from reliability tests run to demonstrate that a product meets the specified design criteria. All Schottky beam lead families have fulfilled the standard requirements of reliability qualification.



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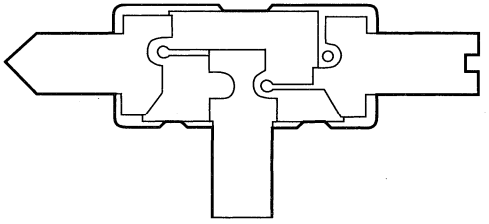


PAIR

Program Description

The purpose of this program is to qualify all beam lead diodes for operation in extreme environmental conditions which may be encountered during military and space operations.

The following test sequence has been designed to assess the endurance of beam lead diodes through relevant environmental stresses such as heat and humidity. To qualify a device as hermetic, the conventional procedure is to perform dye-penetrant and Radiflo tests. However, because of the absence of an enclosed cavity in the unique design of the beam lead diode, these tests are not directly applicable. Therefore, this program utilizes reliability tests such as moisture resistance, salt atmosphere, and immersion to verify that the passivation layer on the beam lead acts as a seal to protect the active area of the diode.

To perform these tests, various Schottky diodes were mounted in non-hermetic, open packages and tested as exposed beam lead devices.

Applicable Part Numbers

Schottky Beam Leads
HSCH-5300 Series
HSCH-5500 Series

Test Sequence

Test	MIL-STD-750	Tests Condition	Units Tested	Failed	LTPD
Moisture Resistance[1,2]	1021	98% R.H. -10°C to 65°C, 10 days			
Temperature Cycling	1051	-65°C to 200°C, 100 cyc.	80	0	<7
Constant Acceleration	2006	20 KG, 1 min. each axis	(40 per lot)		
Salt Atmosphere[2]	1041	35° fog, 24 hours	25	0	<10
Salt Water Immersion[2]	(MIL-STD-883, M1002B)	65°C saturated NaCl solution, 2 cycles	25	0	<10

Notes:
1. The sequence of moisture resistance and temperature cycling followed by constant acceleration assures a thorough evaluation of the effect of exposure to high humidity and heat conditions. End points were taken after each test.
2. End points were: Visual at 100X magnification and D.C. testing to MIL-STD-19500.

Results

As demonstrated by these tests, Hewlett-Packard's beam lead diodes exhibit superior performance when subjected to severe environmental conditions. This proven reliability is achievable because of Hewlett-Packard's unique beam lead design. These beam lead diodes are made of tri-metal (Ti-Pt-Au or NiCr-Pt-Au) which extends both the operating and storage temperature range. In addition, a nitride passivation layer acts as a sealant and provides immunity from contaminants which could lead to I_R drift. Conductive particle protection is provided by a layer of polyimide, which also functions as scratch protection. Therefore, it is recommended that Hewlett-Packard beam lead diodes be used in military and space applications without the necessity of hermetically sealed packaging.

DOD-HDBK-1686 ESD Classification:
HSCH-5300 Series Class I
HSCH-5500 Series Class I

Tri Metal Beam Lead Schottky Diodes and Hermetic Packaged Devices

Reliability Data

HSCH-5300 Series
HSCH-5500 Series
5082-2765
5082-2785

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Hewlett-Packard Communications Components Designer's Catalog.

1. Life Test

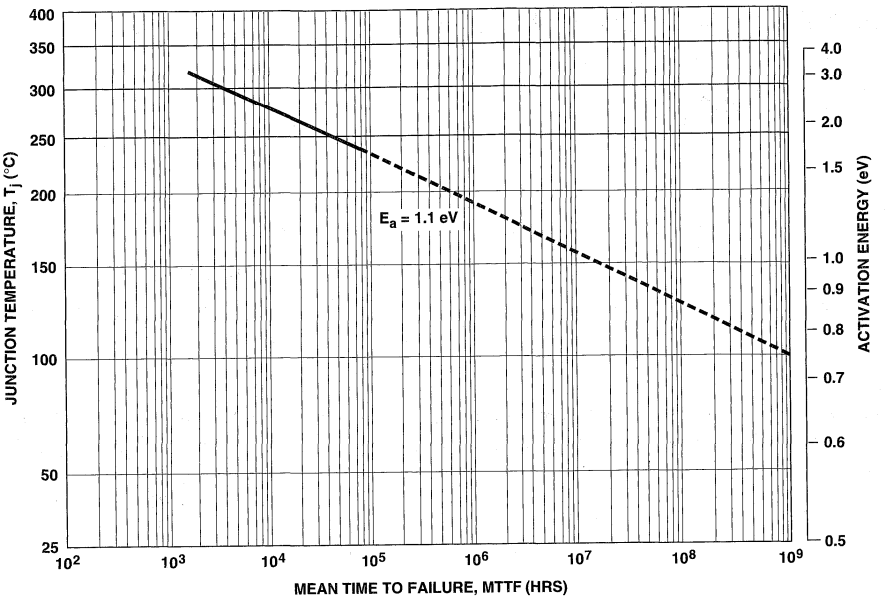
A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Rev. Bias (HTRB)	V_R = 80% V_{BR}, T_A = 150°C	482	482,000	0	0
Operating Life (OL)	I_P = 50 mA A-C, T_A = 125°C	1052	1,050,000	0	0
Room Temp. Operating Life (RTOL)	P_{fm} = 125 mW, T_A = 25°C V_R = 80% V_{BR}, 60 Hz	297	297,000	0	0
High Temp. Operating Life (HTOL)	10 mA DC, T_A = 150°C	287	287,500	0	0
High Temp. Storage (HTS)	T_A = 200°C	191	191,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1 eV, and listed in the following table.

Junction Temp. T_J (°C)	Point[1]		90% Confidence Level[2]	
	MTTF (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
200°C	5.0×10^5	2000.0	2.2×10^5	4545.0
175°C	2.3×10^6	435.0	1.0×10^6	1000.0
150°C	1.2×10^7	83.0	5.2×10^6	192.0
125°C	6.5×10^7	15.0	2.8×10^7	35.0
100°C	7.0×10^8	1.4	3.0×10^8	3.3
75°C	8.2×10^9	0.12	3.6×10^9	0.27



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures which can only be generated at elevated temperature. Data in the above table is obtained by extrapolation to lower temperature.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 75°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

$(1.2 \times 10^{-10}/\text{hr.}) \times (25\%) \times (8760\ \text{hrs/yr}) = 2.6 \times 10^{-5}\%$ per year

Likewise, the 90% confidence level failure rate per year is:

$(2.7 \times 10^{-10}/\text{hrs.}) \times (25\%) \times (8760\ \text{hrs/yr}) = 5.9 \times 10^{-5}\%$ per year

2. DOD-HDBK-1686 ESD Classification:

HSCH-5300 Series	Class I
HSCH-5500 Series	Class I
5082-2765	Class I
5082-2785	Class I

GaAs Schottky Diode

Reliability Data

HSCH-9XXX

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Hewlett-Packard Communications Components Designer's Catalog.

1. Life Test

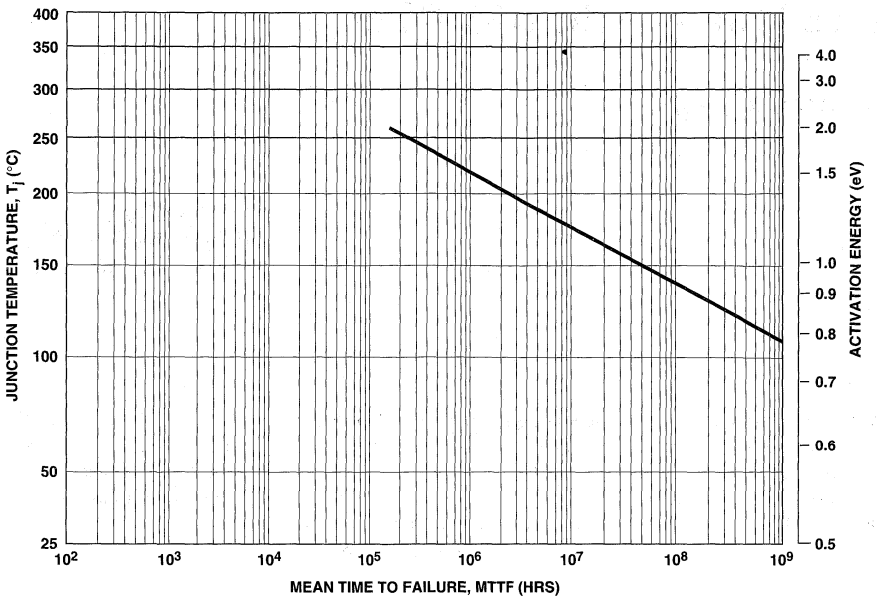
A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp Reverse Bias (HTRB)	80% of V_{BR} @ T_A = 150°C	128	128,000	0	0
Operating Life (O.L.)	I_f = 55 mA D.C @ T_A = 55°C	134	122,150	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.0 eV, and listed in the following table.

Junction Temp. Tj (°C)	Point[1]		90% Confidence Level[2]	
	MTTF (hours)	FIT[3]	MTTF (hours)	FIT[3]
150	$5x10^7$	25	2.2×10^7	45
125	$2.5x10^8$	4	$1.1x10^8$	9
100	$2.0x10^9$	0.50	$9x10^8$	1.10
75	$1.5x10^{10}$	0.07	$6.5x10^9$	0.15
50	$2.0x10^{11}$	0.005	$9x10^{10}$	0.01



Notes:

1. The point MTTF is extrapolated from High Temperature Storage at 150, 200, 250°C.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 50°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

($5x10^{-12}$ hrs.) x (25%) x (8760 hrs/yr) = $1.1x10^{-6}$% per year

Likewise, the 90% confidence level failure rate per year is:

($1x10^{-11}$%/1000 hrs. x (25%) x (8760 hrs/yr) = $2x10^{-6}$% per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Moisture Resistance		80-98% RH @ -10/+65°C, 10 Days	22	0
Salt Atmosphere	1041	10-50 gr/m^2 @ 35°C, 24 hrs.	22	0

3. DOD-HDBK-1686 ESD Classification:

HSCH-9XXX – Class I

HEWLETT® PACKARD

Surface Mount Schottky Diodes

Reliability Data

HSMS-000X
HSMS-280X/1X/2X
HSMS-280A/1A/2A

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Hewlett-Packard Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

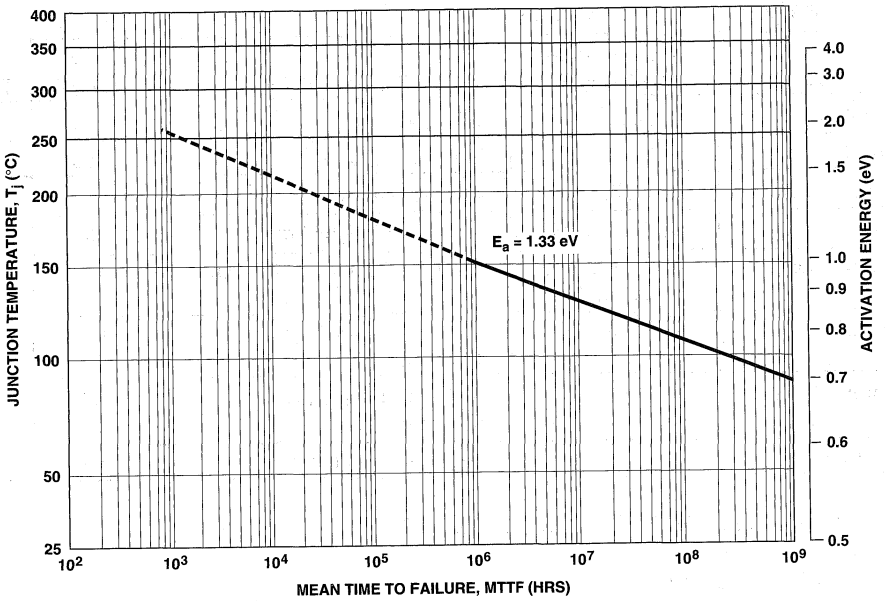
Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Rev. Bias (HTRB)	V_R = 80% V_{BR}, T_A = 150°C	804	828,045	0	0
Operating Life (O.L.)	T_A = 25°C, P_{FM} = 250 mW V_R = 80% V_{BR}, 60 Hz	1,068	999,884	0	0
High Temp. Operating Life (HTOL)	10 mA DC, T_A = 150°C	250	251,900	0	0
High Temp. Storage (HTS)	T_A = 150°C	2,917	1,836,660	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.33 eV, and listed in the following table.

Junction Temp. T_J** (°C)	Point[1]		90% Confidence Level[2]	
	MTTF* (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
150	1.8×10^6	556.0	7.8×10^5	1282.0
140	4.4×10^6	227.0	1.9×10^6	526.0
130	1.1×10^6	91.0	4.8×10^6	208.0
120	2.9×10^7	34.0	1.3×10^7	77.0
100	2.4×10^8	4.0	1.0×10^8	10.0
75	4.8×10^9	0.20	2.1×10^9	0.48
50	1.5×10^{11}	0.007	6.5×10^{10}	0.015

*MTTF data collected in Hermetic and Plastic Packages.
**T_J was calculated using a θ_{JA} of 500°C/W.
(Notes on reverse side.)



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 50°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk ≅ 25%

Then the point failure rate per year is:

(7.0 x 10^{-12}/hr) x (25%) x (8760 hrs/yr) = 1.5 x 10^{-6}% per year

Likewise, the 90% confidence level failure rate per year is:

(1.5 x 10^{-11}/hr) x (25%) x (8760 hrs/yr) = 3.3 x 10^{-6}% per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	215°C, 5 seconds	500	0
Solder Heat	2031	260°C, 10 seconds	426	0
Resistance to Solvent	1022	4 Solvent Groups	98	0
Autoclave	HP GSS 12-109	121°C, 15 PSIG, 96 hrs.	1204	0
Moisture Resistance	HP GSS 12-107, Method B	85°C/85% RH, biased, 1000 hrs.	311	0
Thermal Shock	1056	-65/150°C, 5 min dwell, 200 cycles	615	0
Temperature Cycle	1051	-65/150°C, 10 min dwell, 200 cycles	637	0
Lead Integrity		2.0 pounds minimum	140	0

3. Flammability Test (MIL-STD-202, Method 111):

Meets Needle Flame Test per UL Category D
(Flaming Time <3 sec.) under material classification 94V0.

4. DOD-HDBK-1686A ESD Classification:

HSMS-000X	Class I
HSMS-280X/1X/2X	Class I
HSMS-280A/1A/2A	Class I

HEWLETT® PACKARD

Passivated P-Type Microwave Schottky Diodes

Reliability Data

HSMS-285A/5X

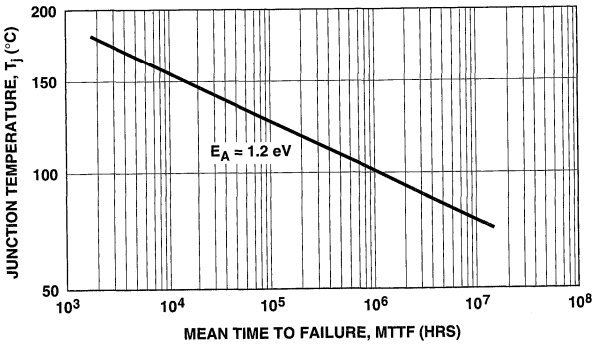
Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is compiled from reliability tests run to demonstrate that a product meets the specified design criteria.

Periodically, additional tests are run. The data on this sheet represents the latest review of accumulated test results. All data recorded here is for P-type passivated microwave Schottky diodes mounted in non-hermetic sealed unsealed 44 packages.

Applications

This information represents the capabilities of the generic device. Failure rate and MTTF values presented here are achievable with normal MIL-S-19500 test screening. Reliability can be guaranteed only under specified conditions and LTPD levels.



Mean Time to Failure vs. Junction Temperature.

1. Burn-In and Storage

Test	Test Conditions[1]	LTPD per 1000 Hours
High Temperature Life	Storage at 125°C	4.0
Steady State Operating Life	P_{FM} = 100 mW V_{RM} = 80% of V_{BR} T_A = 25°C f = 60 Hz	3.0

Note:
1. 1000 hours minimum on all life tests.

2. Environmental

Test	MIL-STD-750 Reference	Test Conditions	LTPD
Temperature Cycle	1051C	10 cycles from -65°C to 200°C, 5 hours at extremes, 5 min. transfer	10
Thermal Shock	1056	10 cycles from 0°C to 100°C, 3 sec. transfer	10
Mechanical Shock	2016	5 blows each at X1, X2, Y, 1500 G, 0.5 msec pulse	10
Vibration Fatigue	2046	20 G min., 60 Hz	10
Vibration Variable Frequency	2056	four 4 min. cycles each X, Y, Z at 20 G min., 100 to 2000 Hz	10
Moisture Resistance	1021	240 hours, 90-98% relative humidity	10
Salt Atmosphere	1041	35°C fog for 24 hours	12

DOD-HDBK-1686 ESD Classification:

HSMS-285A/5X Class I

HEWLETT® PACKARD

Surface Mount Schottky Diodes

Reliability Data

HSMS-8002/12
HSMS-8101
HSMS-820X
HSMS-286A/6X

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Hewlett-Packard Communications Components Designer's Catalog.

1. Life Test

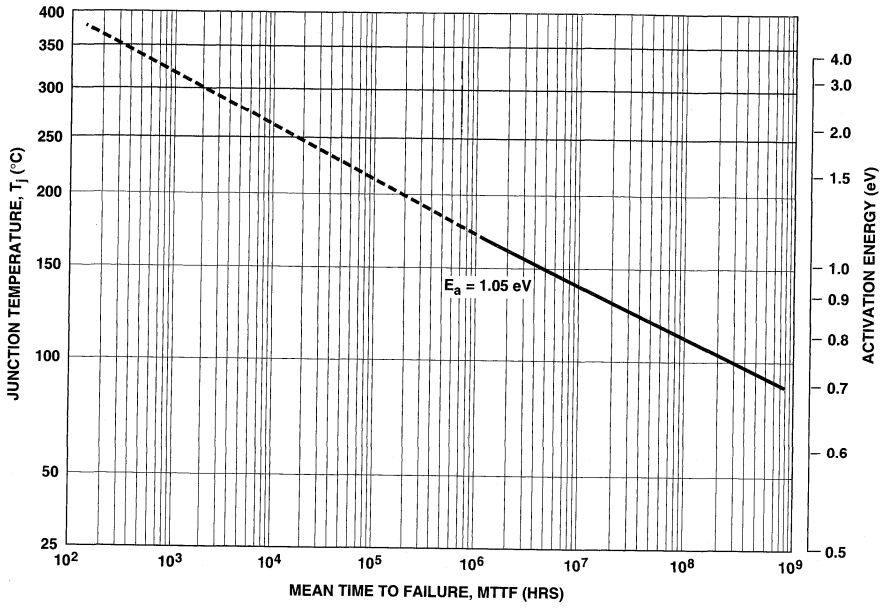
A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Rev. Bias (HTRB)	V_R = 80% V_{BR}, T_A = 150°C	127	127,000	0	0
High Temp. Operating Life (HTOL)	P_{fm} = 75 mW, T_A = 65°C V_R = 80% V_{BR}	129	129,000	0	0
High Temp. Storage (HTS)	T_A = 150°C	129	129,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.05 eV, and listed in the following table.

Junction Temp. T_J (°C)	Point[1]		90% Confidence Level[2]	
	MTTF (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
150	3.6×10^6	278.0	1.6×10^6	625.0
140	7.3×10^6	137.0	3.2×10^6	312.0
130	1.5×10^7	67.0	6.5×10^6	153.0
120	3.2×10^7	31.0	1.4×10^7	71.0
100	1.7×10^8	6.0	7.4×10^7	14.0
75	1.8×10^9	0.56	7.8×10^8	1.3
50	2.6×10^{10}	0.04	1.1×10^{10}	0.09



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 50°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

(4.0 x 10^{-11}/1000 hrs.) x (25%) x (8760 hrs/yr) = 8.76 x 10^{-6}% per year

Likewise, the 90% confidence level failure rate per year is:

(9.0 x 10^{-11}/1000 hrs.) x (25%) x (8760 hrs/yr) = 1.97 x 10^{-5}% per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	215°C, 5 seconds	500	0
Solder Heat	2031	260°C, 10 seconds	426	0
Resistance to Solvent	1022	4 solvent groups	98	0
Autoclave		121°C, 15 PSIG, 96 hrs.	116	0
Moisture Resistance		85°C/85% RH, biased, 1000 hrs.	118	0
Thermal Shock	1056	-65/150°C, 5 min dwell, 200 cycles	163	0
Temperature Cycle	1051	-65/150°C, 10 min dwell, 200 cycles	169	0
Lead Integrity			140	0

3. Flammability Test:

Meets Needle Flame Test Category D (Flaming Time <3 sec.) under material classification 94V0.

4. DOD-HDBK-1686A ESD Classification:

HSMS-8002/8012/8101/820X/286X/286A Class I

HEWLETT® PACKARD

Passivated General Purpose Schottky Diodes

Reliability Data

1N5711/12
5082-2800/04/05
5082-2810/11
5082-2826
5082-2835
5082-2080

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Hewlett-Packard Communications Components Designer's Catalog.

1. Life Test

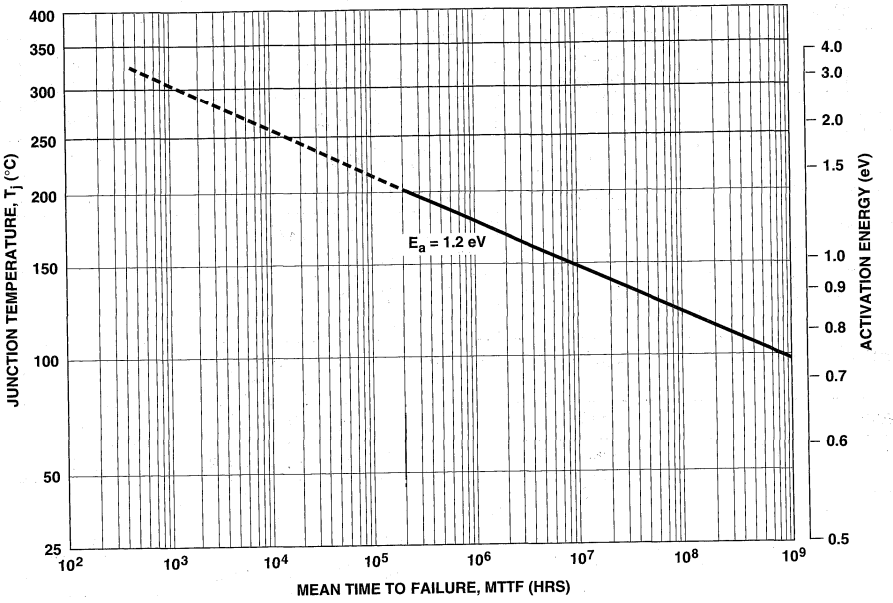
A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Rev. Bias (HTRB)	V_R = 80% V_{BR}, T_A = 200°C	676	598,000	0	0
Room Temp. Operating Life (RTOL)	P_{fm} = 250 mW, T_A = 25°C V_R = 80% V_{BR}, 60 Hz	364	364,000	0	0
High Temp. Storage (HTS)	T_A = 200°C	367	271,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.2 eV, and listed in the following table.

Junction Temp. T_J (°C)	Point[1]		90% Confidence Level[2]	
	MTTF (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
200	2.7×10^5	3704.0	1.2×10^5	8333.0
175	1.4×10^6	714.0	6.1×10^5	1639.0
150	8.9×10^6	112.0	4.0×10^6	250.0
125	7.1×10^7	14.0	3.1×10^7	32.0
100	7.4×10^8	1.3	3.2×10^8	3.1
75	1.0×10^{10}	0.10	4.3×10^9	2.3



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 75°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

(1.0 x 10^{-10}/hr.) x (25%) x (8760 hrs/yr) = 2.2 x 10^{-5}% per year

Likewise, the 90% confidence level failure rate per year is:

(2.3 x 10^{-10}/hrs.) x (25%) x (8760 hrs/yr) = 5.1 x 10^{-5}% per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	260°C, 5 seconds	198	0
Solder Heat	2031	260°C, 10 seconds	44	0
Resistance to Solvent	1022	4 solvent groups	126	0
Thermal Shock	1056	-65/200°C, 5 min dwell, 200 cycles	116	0
Temperature Cycle	1051	-55/100°C, 10 min dwell, 200 cycles	416	0
Mechanical Shock	2016	1500 g's, 0.5 msec pulse 5 blows each X1, Y1, Y2	272	0
Acceleration	2006	20,000 g's, 1 min, X1, Y, Y2	116	0
Vibration Variable Freq.	2056	20–2000 Hz, 20 g, 4 min all axis	116	0
Hermeticity	1017	Fine And Gross	416	0
Lead Integrity		4 lbs Minimum	176	0
Salt Atmosphere	1041	10–50 gr/m^2 @ 35°C, 24 hrs.	45	0

3. DOD-HDBK-1686 ESD Classification:

5082-28XX Class I

HEWLETT® PACKARD

Tri Metal Beam Lead Schottky Diodes (Non-Hermetic Packaged)

Reliability Data

5082-2207/09
5082-2774/94
5082-2830

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Hewlett-Packard Communications Components Designer's Catalog.

1. Life Test

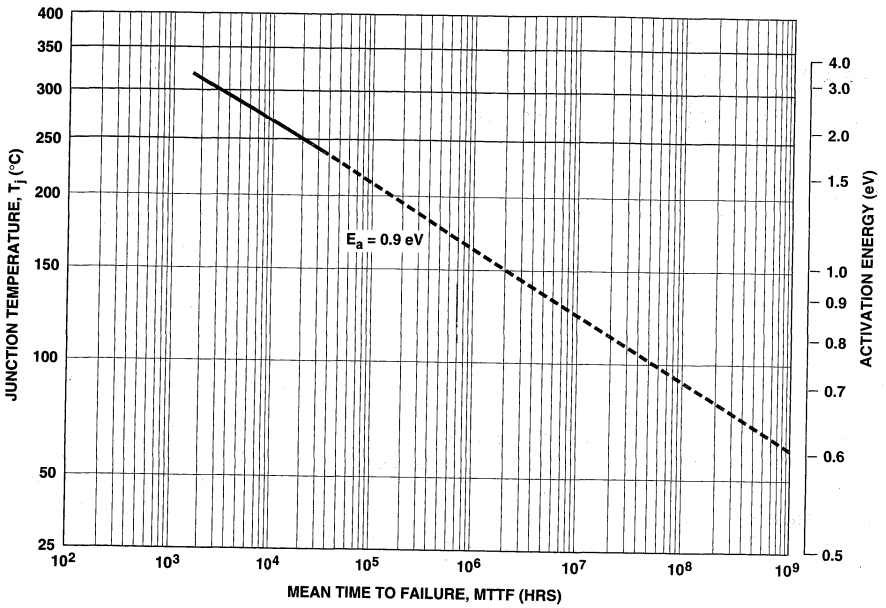
A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Reverse Bias (HTRB)	$V_R = 80\%\ V_{BR}$, $T_A = 150°C$	482	482,000	0	0
High Temp. Operating Life (OL)	$I_P = 50$ mA AC, $T_A = 125°C$	1052	1,050,000	0	0
Room Temp. Operating Life (OL)	$P_{fm} = 125$ mW, 25°C $V_R = 80\%\ V_{BR}$, 60 Hz	297	297,000	0	0
High Temp. Storage (HTS)	$T_A = 125°C$	319	319,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 0.9 eV, and listed in the following table.

Junction Temp. T_J (°C)	Point[1]		90% Confidence Level[2]	
	MTTF (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
150	1.7×10^6	588.0	7.4×10^5	1351.0
140	3.1×10^6	322.0	1.3×10^6	769.0
130	5.7×10^6	175.0	2.5×10^6	402.0
120	1.1×10^7	91.0	5.0×10^6	200.0
100	4.7×10^7	21.0	2.0×10^7	50.0
75	3.5×10^8	2.8	1.5×10^8	6.7
50	3.6×10^9	0.28	1.56×10^9	0.64



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures which can only be generated as elevated temperature. Data in the above table is obtained by extrapolation at low temperatures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 50°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure per year is:

(2.8 x 10^{-10}/hr) x (25%) x (8760 hrs/yr) = 6.1 x 10^{-5}% per year

Likewise, the 90% confidence level failure rate per year is:

(6.4 x 10^{-10}/hr) x (25%) x (8760 hrs/yr) = 1.4 x 10^{-4}% per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	260°C, 5 seconds	144	0
Solder Heat	2031	260°C, 10 seconds	115	0
Moisture Resistance		85°C/85% RH, biased, 1000 hrs.	845	0
Thermal Shock	1056	-65°C/125°C, 5 min. dwell, 200 cycles	744	0
Temperature Cycle	1051	-65°C/125°C, 10 min. dwell, 200 cycles	1784	0
Lead Integrity		>3 oz	214	0

3. DOD-HDBK-1686 ESD Classification:

5082-2207/09	Class I
5082-2774/94	Class I
5082-2830	Class I

HEWLETT® PACKARD

Mesh Schottky Diodes

Reliability Data

5082-2303
5082-2900

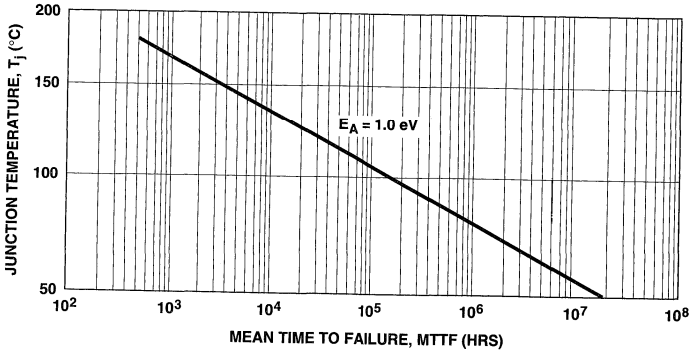
Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is compiled from reliability tests run to demonstrate that a product meets the specified design criteria.

Periodically, additional tests are run. The data on this sheet represents the latest review of accumulated test results. All data recorded here is for mesh Schottky diodes mounted in hermetically sealed glass packages.

Applications

This information represents the capabilities of the generic device. Failure rate and MTTF values presented here are achievable with normal MIL-S-19500 test screening. Reliability can be guaranteed only under specified conditions and LTPD levels.



Mean Time to Failure vs. Junction Temperature.

1. Burn-In and Storage

Test	Test Conditions[1]	LTPD per 1000 Hours
High Temperature Life	Storage at 125°C	4.0
Steady State Operating Life	P_{FM} = 100 mW V_{RM} = 80% of V_{BR} T_A = 25°C f = 60 Hz	3.0

Note:
1. 1000 hours minimum on all life tests.

2. Environmental

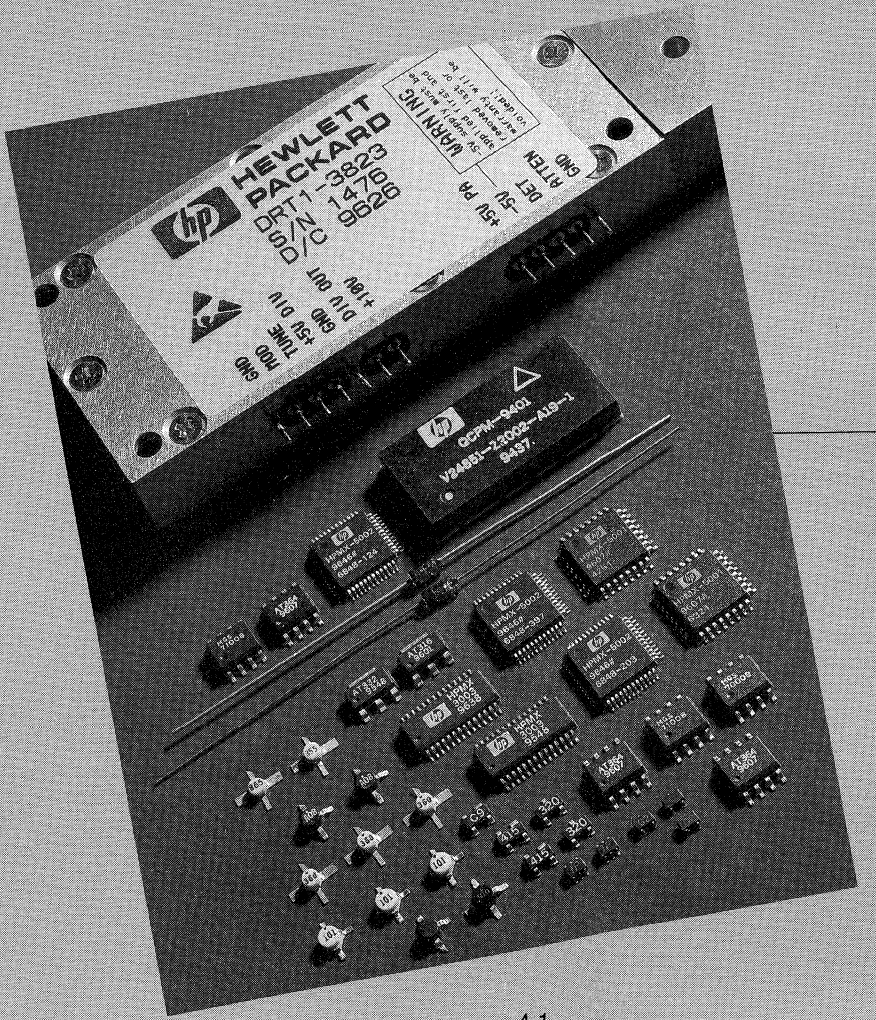
Test	MIL-STD-750 Reference	Test Conditions	LTPD
Temperature Cycle	1051C	10 cycles from -65°C to 200°C, 5 hours at extremes, 5 min. transfer	10
Thermal Shock	1056	10 cycles from 0°C to 100°C, 3 sec. transfer	10
Mechanical Shock	2016	5 blows each at X1, X2, Y, 1500 G, 0.5 msec pulse	10
Vibration Fatigue	2046	20 G min., 60 Hz	10
Vibration Variable Frequency	2056	four 4 min. cycles each X, Y, Z at 20 G min., 100 to 2000 Hz	10
Moisture Resistance	1021	240 hours, 90-98% relative humidity	10
Salt Atmosphere	1041	35°C fog for 24 hours	12

3. DOD-HDBK-1686 ESD Classification:

5082-2303 Class I
5082-2900 Class I

HEWLETT® PACKARD

RF and Microwave Silicon Bipolar Transistors



RF and Microwave Silicon Bipolar Transistors

Characteristics

The silicon bipolar transistor is a semiconductor device, with amplification due to current gain. The advantages silicon bipolar transistors have over other transistor types include mature technology (both in the understanding of the device physics and the device design), low cost, and proven reliability. Therefore, silicon bipolar transistors offer designers a familiar, reliable, cost effective solution to many of their design needs.

Hewlett-Packard manufactures bipolar junction transistors using the Self-Aligned Transistor (SAT) process. This state-of-the-art silicon process yields and f_T of 10 GHz and an f_{MAX} of 25 GHz. Other process features include ion-implantation, the use of gold metallization, and nitride surface passivation. Transistors manufactured with this proprietary process have excellent performance, repeatability, and reliability.

The performance capabilities of an interdigitated microwave bipolar junction transistor are strongly related to two design parameters. The pitch, or emitter-to-emitter center line spacing, controls the "high performance" aspects of the transistor. Finer pitches result in more gain and lower noise figure at higher frequencies. Devices with coarser pitches are typically easier to manufacture, but are limited to lower frequency applications. The number of emitter fingers controls the current handling ability of the device and is a measure of output power capability. Devices with larger numbers of fingers are suitable for power applications such as transmit stages; devices with small numbers of fingers operate at lower biases and are often the best choice for battery operated applications.

Product Families

Hewlett-Packard uses a numbering scheme based on the pitch and number of emitter fingers. Discrete bipolar transistors have part numbers starting with the alpha characters "AT". In general, the first numerical digit of the part number is the emitter to emitter pitch, to the nearest micron. The second and third digits represent the number of emitter fingers. The final two digits represent package style, with the code "00" being reserved for chip form. Devices are manufactured with pitches from 2 to 6 microns (a 6 micron pitch device is designated by a first digit of "6").

6 micron pitch

The AT-640 devices are capable of producing 0.5W at frequencies up to 4 GHz with gains as high as 12.5 dB at 2 GHz.

4 micron pitch

The AT-414/415 are general purpose parts with excellent noise, gain, and power capabilities, and is the starting place for most designs. The AT-420 supplies the same high performance, but with improved output power capability.

3 micron pitch

The AT-3 series of devices has been optimized for high performance at very low bias voltage and current. The AT-3 devices provide 1 dB noise figures at a V_{CE} of 1 V and I_C of 1 mA.

Application Information

The following application information is either published in this catalog or available from your local Hewlett-Packard sales office, authorized distributor, or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

Application Notes

Abstracts

HEWLETT® PACKARD

900 and 2400 MHz Amplifiers Using the AT-3 Series Low Noise Silicon Bipolar Transistors

Application Note 1085

1. Introduction

Discrete transistors offer low cost solutions for commercial applications in the VHF through microwave frequency range. Today's silicon bipolar transistors offer state-of-the-art noise figure and gain performance with low power consumption.

This application note discusses the design techniques and performance of the Hewlett-Packard AT-3 series of silicon bipolar transistors as used in typical low noise amplifiers for use in the various commercial markets.

Although specific designs are presented for 900 and 2400 MHz, the techniques are applicable to other applications in the VHF through S Band frequency range. This would include the 450 MHz (Mobile Radio), 900 MHz (Cellular and Pager), 1.2 and 1.5 GHz (GPS), 1.9 GHz (PCN), 2.1 to 2.7 GHz (MMDS and ITFS) and the 2.4 GHz (ISM) markets.

Generally, silicon bipolar devices are easier to work with at the lower frequencies because of their inherently lower impedances. However, today's state-of-the-art low current bipolar transistors have considerably higher impedances making them comparable to GaAs FETs at these frequencies. Similar design techniques must be used with these devices to assure good performance. Appropriate design techniques will be presented.

This application note will begin with an overview of noise parameters and definitions and then lead into general design considerations for building low noise amplifiers. Two amplifier designs will be presented along with measured results. The application note will finish with a discussion of matching network losses and their effect on amplifier noise figure. Touchstone™ circuit files and simulated results for both amplifiers are included in the Appendix.

2. Noise Parameter Measurements

A typical test set-up for measuring noise parameters is shown in Figure 1. The device under test (DUT) is normally inserted into a test fixture that includes 50 ohm input and output transmission lines whose effect can be calibrated out for the particular frequency. As a minimum, a double stub tuner or

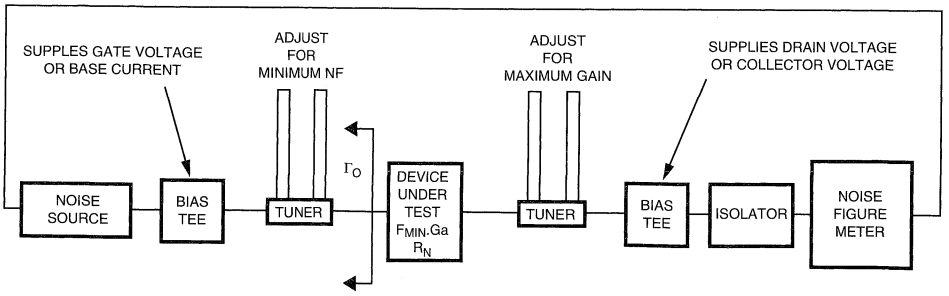


Figure 1. Typical Noise Parameter Measuring Test Set-up.

equivalent must be used at the input to the DUT to present the required Gamma Opt., Γ_O, to the device for it to achieve its minimum noise figure. Although not always required, a tuner can be inserted at the output of the DUT. Providing a conjugate match at the output of the DUT while the input is presented with Γ_O provides a means of measuring associated gain at minimum noise figure. One particular manufacturer of automatic noise measuring equipment uses a tuner on the input and terminates the output in 50 Ω and then measures the resultant S_{22}. A calculation then provides the associated DUT gain. Bias Tees are used at the input and output of the DUT to bias the device. A noise source with a low Excess Noise Ratio, ENR, such as the Hewlett-Packard HP346A, is desired as it minimizes test error by minimizing the range over which the noise figure meter must remain linear. The HP346A noise source also has minimal change in reflection coefficient between the "on" and "off" states. This minimizes the ability of the DUT to change its gain with varying input termination. Any change in DUT gain will increase the measurement error. An isolator placed at the input of the noise figure meter is always desirable but may not be possible at the lower frequencies where size becomes more of an issue.

The noise figure of a linear two port is given by equation (1) shown in the table below.

In equation (1),
NF_{min} is the device minimum noise figure when terminated in Y_{on},
Y_{on} is the generator admittance at which minimum noise figure occurs,
Y_g is the generator admittance presented to the input of the device,
R_n is the noise resistance which gives an indication of the sensitivity of noise figure to termination, and
G_g is the real part of the generator impedance.

The equation can be transformed into an equivalent equation involving the source reflection coefficient, Γ_S, and the reflection coefficient required for minimum noise figure, Γ_O. See equation (2) below.

Once Γ_O has been determined and NF_{min} determined, the R_n can be determined by making a 50 Ω noise figure measurement and calculating R_n. This procedure only works well if Γ_O can be determined by a single measurement. A more accurate method would be to pick 4 reflection coefficients (4 terminating impedances) in the vicinity of where one believes Γ_O to be and then solve 4 equations and 4 unknowns. This method has become a more accurate industry standard.

The input tuner must be capable of transforming the customary 50 ohm source impedance to that required for the device to achieve its rated noise figure. As an example, for the Hewlett-Packard AT-30511 operated at a V_{CE} of 1 volt and I_C of 1 mA, Γ_O has a magnitude of 0.76 increasing to 0.96 at 500 MHz. These numbers represent impedances that can be increasingly difficult to match with low loss. Losses of the tuner become more questionable as the Γ_O increases, plus the ability to design and build a low loss matching network becomes more of a challenge. An early paper by Strid[1] discusses tuner losses as well as losses in matching networks. The problem with tuner losses is that the tuner has a different loss for every tuner setting and this effect is more pronounced at higher reflection coefficients. The user must rely on calibration data supplied by the manufacturer and this data may not be guaranteed much above a reflection coefficient of 0.6 to 0.7.

If the tuner's calibration were accurately known and relatively constant with tuner setting then it would be a simple matter to adjust the tuner and DUT for lowest noise figure and then subtract out the tuner loss to obtain the DUT minimum noise figure, NF_{min}. With varying loss in the tuner, it is difficult to determine if adjusting the tuner and DUT for minimum noise figure minimizes the DUT noise figure or the tuner loss. The alternative of presenting 4 known impedances to the device and solving 4 equations and 4 unknowns is preferred.

Equations

$$NF = NF_{min} + \frac{R_n}{G_g} \left| Y_g - Y_{on} \right|^2 \qquad (1)$$

$$NF = NF_{min} + \frac{4 R_n}{Z_o} \frac{|\Gamma_s - \Gamma_o|^2}{(|1 + \Gamma_o|^2)(1 - |\Gamma_s|^2)} \qquad (2)$$

3. General Design Considerations

Implementing the input match can take on any of a variety of circuit topologies depending on the frequency and the space allowed for implementing the network. Alternatives may include:

- Lumped element network,
- Microstripline network, or
- Cavity filter match

A lumped element network can be either high pass, low pass, or bandpass and generally 2 or 3 elements. Below 2 GHz these networks will generally be lower loss than a microstripline circuit because of substrate losses. Above 2 GHz, the lumped element topology will be very difficult to synthesize with realizable components. The cavity filter approach is probably the lowest loss matching network but cost and size generally make it prohibitive for most commercial applications.

Losses of actual input matching circuits have been measured at nearly 0.5 dB at VHF frequencies when attempting to match the high impedances of MESFETs. Similar impedances can be encountered when using low current silicon bipolar transistors. Matching a device for lowest noise performance does not necessarily guarantee the best input VSWR and performance tradeoffs need to be made. A solution is the use of inductance in the emitter leads to create negative feedback which can bring Γ_O and S_{11}* closer in value[2,3,4]. The amount of inductance must be carefully weighed against its effect on other circuit parameters such as gain and stability. An improperly chosen amount of inductance can cause out-of-band oscillations that can prohibit an amplifier from delivering its rated performance. Other techniques such as resistive feedback and resistive loading can improve stability but can limit power output capability.

An often overlooked part of an amplifier is the bias decoupling network that must be invisible to the RF matching networks. Generally they provide a low loss method of biasing the devices but in some situations can actually be used to provide some resistive loading for stability both in-band and out-of-band. Properly designed bias decoupling networks can also be used to provide some form of band pass or high pass filtering that could help reduce low frequency out-of-band gain. A poorly designed amplifier with very high low-frequency gain that may be unconditionally stable according to the computer simulation may actually oscillate if the output can radiate back to the input. The enclosure that houses the amplifier must be designed to offer enough isolation around the circuit such that it does not make the amplifier circuit unstable at any frequency.

The manner in which circuit elements are implemented will affect the overall amplifier performance. The use of etched circuit elements as opposed to surface mount discrete elements offers a cost benefit but may affect losses. Surface mount components offer small size but parasitics and device Q must be understood if their effect on circuit performance is to be properly analyzed.

4. 900 MHz Silicon Bipolar Amplifier

The 900 MHz amplifier uses an AT-32033 which is in the industry standard SOT-23 package. The AT-32033 is one of a series of silicon bipolar transistors that are fabricated using an optimized version of Hewlett-Packard's 10 GHz f_t Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device-to-device uniformity is guaranteed in fabrication by the use of ion-implantation, self aligned techniques, and gold metalization.

The AT-3 series of devices has a 3.2 micron emitter-to-emitter pitch and has been fabricated in a variety of geometries for various applications. The 20 emitter finger interdigitated geometry yields an easy to match device capable of moderate power at low to moderate current. The 10 emitter finger geometry offers higher gain at low current while the 5 emitter finger geometry offers the highest gain at lowest current consumption. The smaller devices at very low current present very high impedances that can make them more of a challenge to design with. The impedances associated with very low current transistors at 900 MHz are very similar to those presented by 500 micron MESFETs at 900 MHz.

The 900 MHz AT-32033 amplifier is designed for a nominal 1 dB noise figure and 10 dB associated gain at 2 mA collector current. Although the device is capable of sub 1 dB noise figures, most applications do not require much below 1.5 dB. Starting out with a device that has such a low NF_{min} allows the designer to make tradeoffs between noise figure, gain, stability, etc.

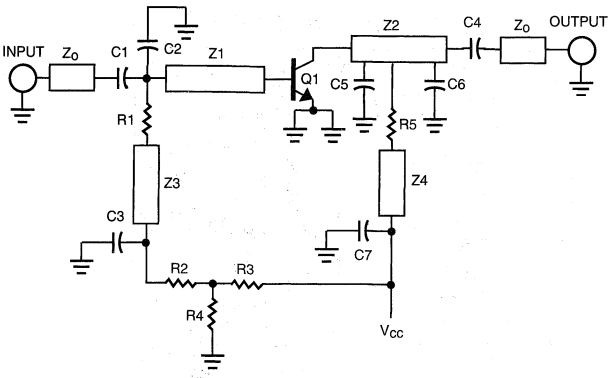
The schematic diagram of the 900 MHz amplifier is shown in Figure 2. The input noise match consisting of a low pass network in the form of C2 and Z1 provides a low Q broad band match. A small wound inductor could replace

transmission line Z1. A value in the range of 15 to 20 nH would be a good substitute. In the actual circuit it was found that the input shunt capacitor was not required. Adding a shunt capacitor at this point will allow the designer to make tradeoffs between noise figure and input VSWR.

The output match consists of a 3 element low pass network. The 3 element network allowed a shorter length of series transmission line to be used as compared to a 2 element match. The series inductive element can be etched onto the printed circuit board or a low cost wound inductor can be used if board space is limited. A suggested value would be in the range of 20 to 25 nH. The artwork and component placement guide are shown in Figures 3 and 4. A small amount of emitter inductance is used to improve in-band stability. This value must be carefully chosen such that an excessive amount is not used, otherwise high frequency oscillations could be produced. Out-of-band oscillations will severely limit the ability of the device to produce its rated performance. Resistor R1 provides very low frequency stability while resistor R5 enhances overall stability, including in-band performance. A current source consisting of resistor R2 connected to the resistive divider consisting of resistors R3 and R4 provide the necessary base current to produce the desired 2 mA collector current.

Actual measured noise figure of the amplifier with a micro-stripline input is shown in Figure 5. The amplifier provides a nominal 1.25 dB noise figure from 800 to 1000 MHz. The noise figure will improve slightly with the use of a wound inductor in place of the microstripline. Pay careful attention to the parasitic capacitance of the wound inductor as it could limit amplifier noise figure and affect out-of-band stability. Actual measurements of the microstripline input match circuit indicates a 0.26 dB loss. Subtracting this loss from the measured amplifier noise figure suggests a 1 dB device noise figure which is as predicted by the computer simulation. One of the advantages of using a device with a 0.78 dB NF_{min} is that compromises can be made between noise figure, gain, and input match.

Actual measured amplifier gain is shown in Figure 6. The amplifier has a nominal 11 dB gain from 750 to 900 MHz.



C1–10 pF CHIP CAPACITOR
C2 – 1 pF CHIP CAPACITOR (ADJ FOR NF/VSWR)
C3, C7–1,000 pF CHIP CAPACITOR
C4–100 pF CHIP CAPACITOR
C5–1 pF CHIP CAPACITOR
C6–2.7 pF CHIP CAPACITOR
Q1 – HEWLETT-PACKARD AT-32033 SILICON BIPOLAR TRANSISTOR
R1 – 50 OHM CHIP RESISTOR
R2 – 47 K OHM CHIP RESISTOR (ADJ FOR RATED Ic)
R3, R4 – 15 K OHM CHIP RESISTOR
R5, – 150 – 180 OHM CHIP RESISTOR (ADJ FOR STABILITY/POUT)
Z_o – 50 OHM MICROSTRIPLINE
Z1–Z2 – ETCHED MICROSTRIPLINE CIRCIITRY (MAY SUBSTITUTE INDUCTOR)
Z3–Z4 – MICROSTRIP BIAS DECOUPLING LINES

Figure 2. Schematic Diagram of AT-30233 900 MHz Amplifier.

The etched microstriplines can be replaced by a pair of lumped inductors as shown in Figure 7 with a 0.1 dB improvement in noise figure.

Once the circuit has been optimized for best noise figure, gain and input/output VSWR, it is then necessary to take a look at output power. The 900 MHz amplifier was first tested for P_{1dB} and then for IP_3. Initial results for P_{1dB} were less than those as specified on the data sheet. The major difference is that the amplifier being evaluated was conjugately matched at the output. Most device manufacturers specify P_{1dB} at a "power match" and not a "conjugate match". This implies that tuners are used at the input and output of the device to maximize

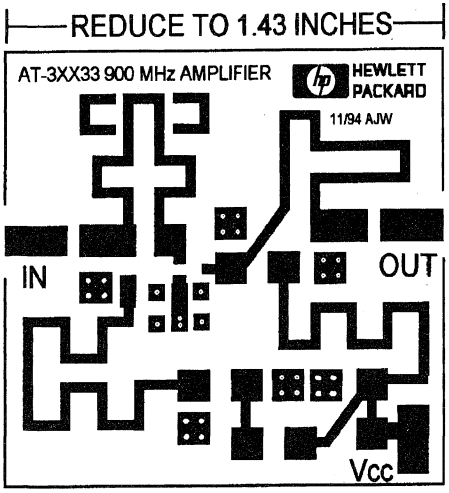


Figure 3. 2X artwork for 900 MHz Amplifier using 0.062 inch thick FR-4.

gain and power output. Maximum power output rarely occurs when any device's output port is conjugately matched. How much improvement can be achieved by power matching?

Initially, the 900 MHz amplifier was tuned for best output VSWR at 850 MHz. Greater than 20 dB return loss was obtained. The measured 1 dB compression point referenced to the output was -5.5 dBm with the device biased at a V_{CE} of 2.7 volts and 2 mA I_C. Close examination of the output matching network suggested that possibly the 180 Ω resistor used in the output bias decoupling line might be

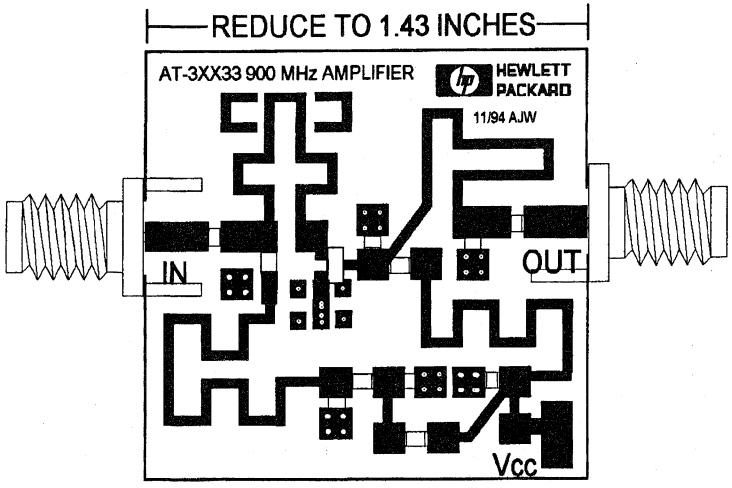


Figure 4. Component Placement for 900 MHz Amplifier using 0.062 inch thick FR-4.

WARNING: DO NOT USE PHOTOCOPIES OR FAX COPIES OF THIS ARTWORK TO FABRICATE PRINTED CIRCUITS.

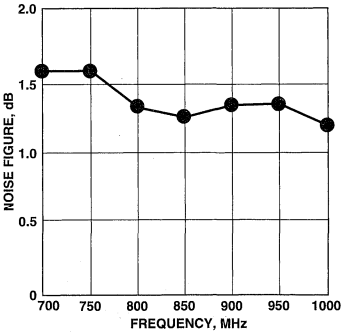


Figure 5. AT-32033 Amplifier Noise Figure.

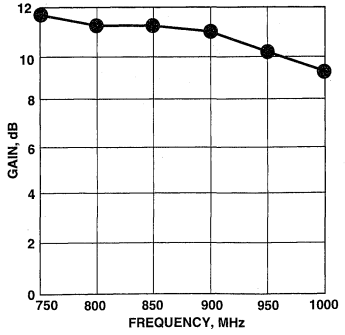


Figure 6. AT-32033 Amplifier Gain.

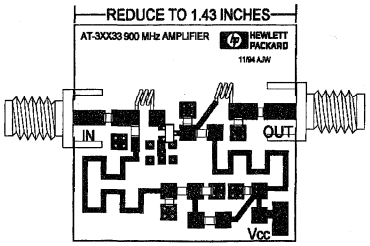


Figure 7. 900 MHz Amplifier showing the Placement of Wound Inductors in place of Microstripline Networks.

absorbing some of the power. This resistor was placed in the circuit to raise in-band stability. Placing a short across this resistor and re-measuring the 1 dB compression point showed an improvement of 3.5 dB! Also observed was an increase in collector current when the device is driven toward compression. An increase in current causes an increase in the voltage drop across the 180 Ω resistor causing the collector voltage to sag. Minimizing the value of this resistor will tend to keep V_{CE} high when the device is driven hard and will also minimize power absorption in the circuit. The drawback could be decreased stability. Some compromise with respect to output loads may have to be instituted if additional power output is desired.

A P_{1dB} of -2 dBm is still slightly lower than the data sheet specification. However, the output is still conjugately matched and not power matched. In order to provide a power match, one must provide an alternative output match. In order to prove that a power match will provide greater power output, a lab exercise can be set-up. A double stub tuner is connected in series with the existing conjugately matched amplifier output circuitry and the power meter. The tuner is then adjusted for greatest power output while driving the input circuit higher. A spectrum analyzer can be useful here to determine that harmonics are not high enough in level to distort the power meter measurement. In small steps increase the input power and then retune the output tuner for maximum fundamental power. After retuning the output for a power match, it was found that the P_{1dB} increased to nearly 2 dBm with a reduction in gain of 1 dB over the small signal conjugate match. In order to revise the output match to provide a power match would require breaking the circuit at the collector port of the device and measuring the new Gamma Load (Γ_L) presented by the existing circuit plus the external tuner. It is interesting to note that the output return loss which was greater than 20 dB at 850 MHz is now only 8.5 dB at the power match condition.

In addition to measuring P_{1dB} at all output matches, the two tone third order intercept point (IP_3) was also measured. For each test, two tones were introduced at the input to the amplifier which are separated by 10 MHz. The resultant third order products were then measured and averaged and IP_3 was calculated. The results are shown in Table 1.

The results show a consistent 20 to 21 dB of difference between P_{1dB} and IP_3. This is somewhat greater than has been measured on other larger geometry small signal devices but it does appear to be repeatable.

5. 2400 MHz Silicon Bipolar Amplifier

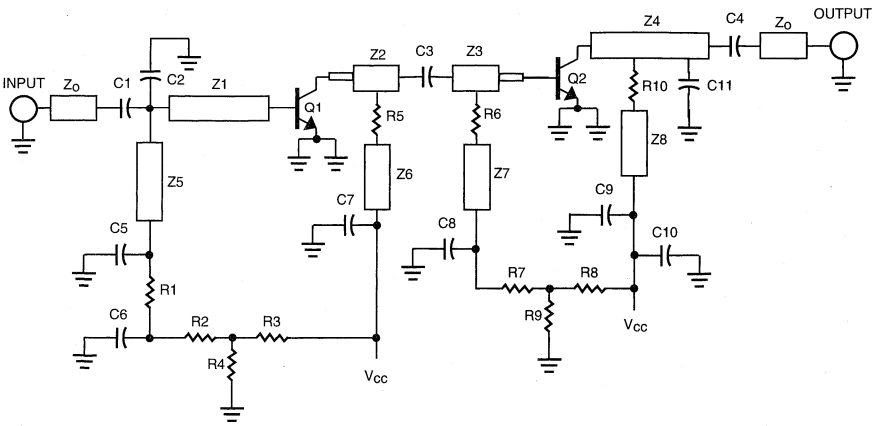
The 2400 MHz amplifier is designed around the Hewlett-Packard AT-31011. The 10 emitter finger geometry plus the SOT-143 package with the two emitter leads offers improved performance at frequencies above 2 GHz. At a rated current of 1 mA, the AT-31011 provides a device noise figure of 1.7 dB at 2400 MHz with an associated gain of 10 dB.

The schematic diagram of the 2400 MHz amplifier is shown in Figure 8. The input noise match consisting of a low pass network in the form of C2 and Z1 provides a low Q broad band match. The capacitor at C2 can be optimized for either a noise or conjugate match.

The output match consists of a 2 element low pass network while the interstage network consists of two short transmission lines and a series capacitor. The artwork and component placement guide are shown in Figures 9 and 10. Minimal emitter inductance is used to preserve in-band gain without sacrificing stability. Resistor R1 provides low frequency stability while resistors R5 and R10 enhance overall stability, including in-band performance. Two current sources (resistor R2 connected to the resistive divider consisting of resistors R3 and R4 and R7 connected to the resistive divider consisting of R8 and R9) provide the necessary base current to produce the desired 1 mA collector current in each device.

Table 1. 900 MHz Amplifier Power Output Summary.

Condition	P_{1dB}	IP_3
Conjugate Match	-5.5 dBm	+16 dBm
Conjugate Match w/o resistor	- 2.0 dBm	+18 dBm
Power Match	+2 dBm	+23 dBm



C1, C4, C5, C9 –10 pF CHIP CAPACITOR
C2 – 1.3 pF CHIP CAPACITOR
C3–1.5 pF CHIP CAPACITOR
C6, C7, C8, C10,–1,000 pF CHIP CAPACITOR
C11– 2 pF CHIP CAPACITOR (ADJUST FOR MIN OUTPUT VSWR)
Q1, Q2 – HEWLETT-PACKARD AT-31011 SILICON BIPOLAR TRANSISTOR
R1, R10 – 50 OHM CHIP RESISTOR
R5, R7 – 47 K OHM CHIP RESISTOR (ADJUST FOR RATED Ic)
R3, R4, R8, R9, 15 K OHM CHIP RESISTOR
R5, 16 OHM CHIP RESISTOR
R6, 1 K OHM CHIP RESISTOR
Z_O – 50 OHM MICROSTRIPLINE
Z1–Z4 – ETCHED MICROSTRIPLINE CIRCIITRY
Z5–Z8 – MICROSTRIP BIAS DECOUPLING LINES

Figure 8. Schematic Diagram of AT-31011 2400 MHz Amplifier.

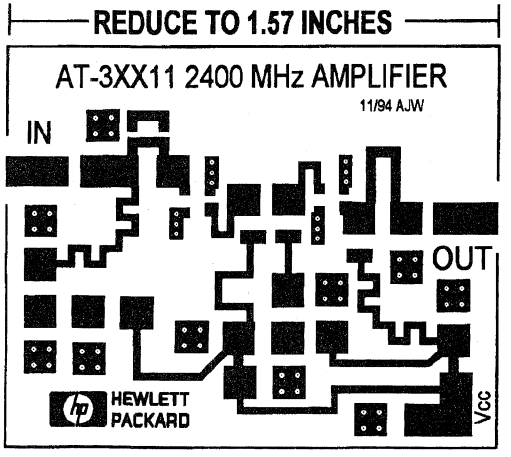


Figure 9. 2X artwork for 2400 MHz Amplifier using 0.062 inch thick FR-4.

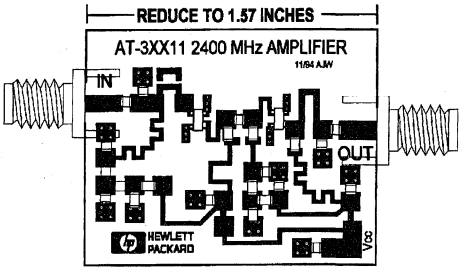


Figure 10. Component placement for 2400 MHz Amplifier (Drawing not to scale).

The amplifier has a measured noise figure between 1.9 and 1.95 dB from 2400 to 2500 MHz with a nominal associated gain of 20 dB at a total current consumption of 2 mA for both devices. Measured output 1 dB gain compression point is -4.5 dBm with an associated IP_3 of +7 dBm. See Figures 11 and 12.

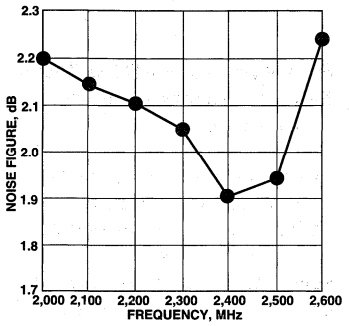


Figure 11. AT-31011 Amplifier Noise Figure.

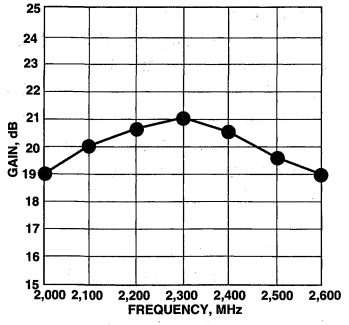


Figure 12. AT-31011 Amplifier Gain.

6. Other Applications

The low current bipolar transistors can also be used in frequency converter applications. Although not optimum, the 900 MHz amplifier circuit shown in Figure 4 can be used to demonstrate mixer operation. The amplifier circuit can be modified for use as a downconverter to a 10.7 MHz IF by simply coupling out the IF by attaching a 0.1 to 0.3 µH coil to the output circuit. The point to couple to should be at the junction of C4 and C6 (reference Figure 2). Ultimately, the IF should also have a dc blocking capacitor but it was not required for this simple test. The LO is injected into the output port of the amplifier and the amplifier input port is the RF input port. With a nominal +3 dBm LO, the circuit without any optimization provides a nominal 6 dB conversion gain and less than 12 dB noise figure. Optimization of the bias and matching structures will improve performance. Generally, higher LO increases conversion gain but there is generally a nominal LO power that produces the lowest noise figure. Bias voltage and current can be critical, especially for lowest noise operation.

7. Matching Circuit Losses

The losses associated with the input matching structure can be calculated with the help of equation (3) shown in the table below. The available gain of a two port is shown.

The power delivered to the load is simply the power that would be delivered if the load were conjugately matched to the network. With the input to the network being 50 ohms, $\Gamma_S = 0$, equation (3) reduces to equation (4).

The measurement of S_{21} is nothing more than a 50 ohm available gain measurement. It is imperative that the source and load presented to the device be as near a perfect 50 ohm impedance as possible as this is the reference impedance for the reflection coefficient. Both the numerator and the denominator use only the magnitude of S_{21} and Γ_L or S_{11} so it is only necessary to measure accurately the magnitude and not phase. With a network with a very high reflection coefficient, S_{22} becomes very large and S_{21} very lossy. With a low reflection coefficient, S_{22} is smaller and loss becomes very low.

Several circuits are analyzed for loss and the results are shown in Table 2. The first circuit is a simple series inductor and blocking capacitor providing a noise match for a 900 MHz amplifier. Loss calculated to be 0.23 dB. The second circuit is a simple L network consisting of a variable series capacitor and a shunt inductor which transforms a 50 ohm source impedance to an S_{22} of 0.94 at 500 MHz. This is a typical reflection coefficient required to match both silicon and GaAs devices for lowest

Equations

$$G_a = \frac{|S_{21}|^2 \ (1 - |\Gamma_S|^2)}{|1 - S_{11}\,\Gamma_S|^2 \ (1 - |\Gamma_L|^2)} \qquad (3)$$

$$G_a = |S_{21}|^2 / (1 - |\Gamma_L|^2) \qquad (4)$$

Table 2. Losses of Various Matching Networks.

Circuit Number	Freq. (MHz)	Circuit	S21 (dB)	S21	S22 (dB)	S22	Loss (dB)
1	900	L	-5.8	0.513	-1.4	0.85	0.23
2	500	L/C	-9.8	0.324	-0.54	0.94	0.45
3	150	Cap coupled tank	-5.8	0.513	-1.4	0.85	0.23
4	900	AT-32033 Microstrip	-0.5	0.944	-12.7	0.23	0.26
5	2400	AT-31011 Microstrip	-2.2	0.776	-4.75	0.58	0.44
6	2400	ATF-10236 Microstrip	-1.1	0.881	-7.0	0.45	0.14

noise figure at 500 MHz. Compared to circuit number 1, the measured loss has increased 0.2 dB because of the losses associated with matching to a higher impedance. The third circuit is a parallel tuned circuit with a series input capacitor used to provide the high impedance transformation to a reflection coefficient of 0.85 at 150 MHz. Notice that the measured loss is the same as circuit number 1 with a similar reflection coefficient but at a different frequency. Circuits 4, 5, and 6 are micro-stripline designs for 900 and 2400 MHz.. Circuit 4 is the input network for the 900 MHz amplifier using the AT-32033 previously described. Subtracting the 0.26 dB for the input loss reduces the noise figure to 1 dB which is the noise figure as predicted without circuit losses. The loss of the input match for the 2400 MHz AT-31011 amplifier was measured at 0.44 dB. This is as a result of using lossy FR-4/G-G10 at 2 GHz and a higher reflection coefficient. Contrast this result with circuit number 6 which is a noise match for the ATF-10236 FET etched on ER = 2.2 material[6].

8. Calculating Circuit Losses

The calculation of circuit losses is only as accurate as the models of the individual circuit elements. The inductor in matching circuit #1 will be analyzed.

The inductor used is an air wound solenoid with 5 turns #26 guage enamel wire with a 0.075" I.D. The inductance is calculated as [7,8]:

$$L\ (\mu H) = \frac{n^2 \bullet r^2}{9\,r + 10\,l}$$

where n = number of turns
r = radius
l = length

Solving yields L ~ 20 nH

The unloaded Q can be calculated as follows:

$$Qu = 2\,r\,A\,f^{1/2}$$

where r = radius
A = 100 - 130 for 1/r from 2 to 20
f = frequency in MHz

Solving yields Qu = 259.

Actual measurements of Q suggest that a Qu of 100 to 200 might be a better value for maximum Qu. The equivalent series R_S can now be calculated. Based on a Qu of 200 :

$$Qu = \frac{j\,\omega\,l}{Rs}$$

$$\text{Therefore } Rs = \frac{j\,\omega\,l}{Qu}$$

Solving yields R_S = 0.565 Ω. This is the equivalent series resistance of the 5 turn coil.

The loaded Q of the circuit, Ql, can now be calculated or measured with the device terminating the matching network and a 50 Ω source termination. The loaded Q can be found by dividing the 3 dB bandwidth into the nominal center frequency, f_O. Another alternative is to plot Z_{in} of the network terminated with the device. Any point on the Smith Chart represents an impedance consisting of both real and reactive components. Dividing the reactive part into the real part provides the Q of the network. The Ql is approximately 1 for this network. Network insertion loss can now be calculated with the following equation:

Insertion Loss I.L. =
-20 log [(Qu - Ql) / Qu]

Solving yields an insertion loss of 0.043 dB. If the Qu of the inductor is only 100 then the loss would calculate at 0.087 dB, which is probably more consistent with the measured results. Other factors such as radiation loss, microstripline loss and capacitor Q can make up the difference in the calculated versus measured loss.

Some packaged and molded inductors have a Qu of only 25 and with a higher Ql the loss can approach 0.5 dB!

9. Conclusions

At low bias currents, the AT-3 series of devices can have a Γ_O as high as 0.94 at sub 1 dB noise figures. This allows the designer more flexibility in making tradeoffs and still achieving 1 to 1.5 dB noise figures at 900 MHz with silicon. In addition to concern over tuner losses and their effect ultimately on the accuracy of the noise parameter measurement, the losses associated with actual noise matching structures can approach 0.5 dB unless attention is paid to component Q.

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3. G.D. Vendelin, "Feedback Effects on the Noise Performance of GaAs MESFETs," Low Noise Microwave Transistors and Amplifiers, H. Fukui, Editor, IEEE Press, 1981, pp. 294-296.

4. D. Williams, W. Lum, S. Weinreb, "L-Band Cryogenically Cooled GaAs FET Amplifiers," Microwave Journal, October 1980, p. 73.

5. "Using the ATF-10236 in Low Noise Amplifier Applications in the UHF Through 1.7 GHz Frequency Range", Hewlett-Packard Application Note 1076, Newark, Ca.11/94

6. "S-Band Low Noise Amplifiers", Hewlett-Packard Applications Note AN-G004, 5091-9311E (10/93)

7. R.W. Rhea, "Oscillator Design and Computer Simulation" Prentice Hall, 1990, pp 140-143

8. Reference Data for Radio Engineers, 6 th ed., Howard W. Sams, 1975, p 6-3

Appendix I.

AT-32033 900 MHz Low Noise Amplifier Touchstone Circuit File

```
!SINGLE STAGE DESIGN
 !A.J.WARD 11-28-94
!REVISED 06-15-95
DIM
        FREQ    GHZ
        IND     NH
        CAP     PF
        LNG     IN
VAR
        W1=.03                  !INPUT LINE WIDTH
        L1\1.11529 !INPUT LINE LENGTH
        C1=0.7          !INPUT SHUNT CAPACITOR,
        !               TRADEOFF NOISE FIGURE AND INPUT VSWR
        W3=.03          !OUTPUT LINE WIDTH
        L3=1                    !OUTPUT LINE LENGTH
        LL1=.05         !EMITTER LEAD LENGTH, UP TO .1
                        STILL OK ON STABILITY
CKT
        MSUB    ER=4.8 H=.062 T=.0014 RHO=1 RGH=0
        TAND    TAND=.002
        MLIN    1       2       W=.1 L=.05
        SLC     2       3       L=.25 C=10
        MLIN    3       4       W=.1 L=.2
        SLC     4       5       L=.25 C^C1
        VIA     5       0       D1=.03 D2=.03 H=.062 T=.0014
        MSTEP   4       6       W1=.1 W2^W1
        MLIN    6       7       W^W1 L^L1
        !IND    6       7       L#0 14.82035 30  !OPTIONAL INDUCTOR
        RES     4       10      R=50
        MLIN    10      11      W=.1 L=.1
        MSTEP   11      12      W1=.1 W2=.03
        MLIN    12      13      W=.03 L=1.5
        SLC     13      14      L=.4 C=1000
        VIA     14      0       D1=.03 D2=.03 H=.062 T=.0014
        MSTEP   7       16      W1^W1 W2=.1
        MLIN    16      17      W=.1          L=.1
        MSTEP   17      18      W1=.1 W2=.02
        MLIN    18      19      W=.02 L=.01
        DEF2P   1       19      INPUT

        S2PA    1       2       3 C:\S_DATA\BJT\T320333A.S2P
        DEF3P   1       2       3 DEVICE

        MLIN    1       2       W=.02  L^LL1
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        DEF1P 1                 EMITTER

        MLIN    1       2       W=.02 L=.030
        MSTEP   2       3       W1=.02 W2=.1
        MLIN    3       4       W=.1 L=.1
        CAP     3       5       C=1
        VIA     5       0       D1=.03 D2=.03 H=.062 T=.0014
        MSTEP   4       6       W1=.1         W2^W3
        MLIN    6       7       W^W3 L^L3!OUTPUT SERIES
                                MICROSTRIPLINE
```

Appendix I. (continued)

```
        CAP     7       8 C=3.3
        VIA     8       0 D1=.03 D2=.03 H=.062 T=.0014
        MSTEP   7       9 W1=.03 W2=.1
        MLIN    9       10 W=.1 L=.2
        SLC     10      11 L=.25 C=100   !OUTPUT BLOCKING CAPACITOR
        MLIN    11      12 W=.1 L=.2
        !IND    6       7 L=19           !OPTIONAL INDUCTOR
        RES     4       15 R=180         !OUTPUT BIAS RESISTOR
        MLIN    15      16 W=.1 L=.1
        MSTEP   16      17 W1=.1 W2=.03
        MLIN 17 18 W=.03 L=1.1           !OUTPUT BIAS DECOUPLING LINE
        SLC     18      19 L=.4 C=1000
        VIA     19      0 D1=.03 D2=.03 H=.062 T=.0014
        DEF2P   1       12 OUTPUT

        INPUT   1       2
        DEVICE  2       3       4
        EMITTER 4
        OUTPUT  3       5
        DEF2P   1       5       AMP

FREQ
        !SWEEP  .8      .95     .05
        SWEEP   1       6       .05
        !STEP   .9
OUT
        AMP     DB[S11]
        AMP     DB[S21]
        AMP     DB[S12]
        AMP     DB[S22]
        AMP     NF
        AMP     K
        AMP     B1
```

Appendix II.
AT-32033 900 MHz Low Noise Amplifier Touchstone Output File

FREQ	DB[S11]	DB[S21]	DB[S12]	DB[S22]	NF	K	B1
GHz	AMP	AMP	AMP	AMP	AMP	AMP	AMP
0.10000	-1.498	3.372	-48.108	-4.199	130.814	15.358	1.061
0.20000	-4.645	8.046	-38.108	-4.383	116.859	6.328	0.874
0.30000	-5.827	10.157	-32.273	-4.526	9.236	2.837	0.850
0.40000	-5.057	11.257	-28.176	-4.861	4.600	1.600	0.891
0.50000	-5.110	11.791	-25.061	-5.606	3.035	1.301	0.885
0.60000	-6.812	11.983	-23.273	-6.637	2.162	1.350	0.830
0.70000	-10.037	11.955	-21.702	-8.525	1.483	1.396	0.810
0.80000	-11.427	11.658	-20.392	-12.403	1.076	1.375	0.879
0.85000	-9.606	11.353	-19.889	-15.993	0.998	1.342	0.945
0.90000	-7.482	10.904	-19.526	-20.742	0.988	1.303	1.018
0.95000	-5.781	10.462	-19.357	-19.366	1.038	1.247	1.081
1.00000	-4.585	9.866	-19.343	-14.305	1.141	1.199	1.120
1.10000	-3.556	8.190	-19.893	-7.571	1.602	1.136	1.059
1.20000	-4.059	5.508	-21.451	-4.013	2.792	1.228	0.814
1.30000	-5.057	2.124	-23.713	-2.238	5.002	1.539	0.549
1.40000	-5.778	-1.342	-26.059	-1.382	7.892	2.089	0.367

Appendix II. (continued)

FREQ GHz	DB[S11] AMP	DB[S21] AMP	DB[S12] AMP	DB[S22] AMP	NF AMP	K AMP	B1 AMP
1.50000	-6.267	-4.557	-28.154	-0.931	10.447	2.849	0.254
1.60000	-6.700	-7.319	-29.959	-0.663	10.898	3.700	0.182
1.70000	-7.272	-9.781	-31.482	-0.485	9.234	4.597	0.132
1.80000	-8.057	-11.963	-32.742	-0.359	7.568	5.409	0.096
1.90000	-9.156	-13.736	-33.692	-0.267	7.705	5.855	0.070
2.00000	-10.786	-15.080	-34.236	-0.200	8.002	5.759	0.050
2.10000	-13.299	-15.845	-34.236	-0.152	7.700	5.023	0.037
2.20000	-17.541	-16.048	-33.689	-0.119	6.549	3.940	0.028
2.30000	-20.689	-15.868	-32.776	-0.099	5.263	2.960	0.023
2.40000	-14.810	-15.587	-31.776	-0.088	4.265	2.305	0.020
2.50000	-10.236	-15.354	-30.873	-0.082	3.532	1.907	0.019
2.60000	-7.580	-15.320	-30.189	-0.078	3.052	1.695	0.017
2.70000	-6.082	-15.405	-29.640	-0.073	2.768	1.574	0.016
2.80000	-5.301	-15.439	-29.055	-0.071	2.674	1.488	0.015
2.90000	-4.989	-15.228	-28.241	-0.074	2.759	1.417	0.015
3.00000	-5.043	-14.562	-26.985	-0.087	2.998	1.356	0.017
3.10000	-5.584	-13.034	-24.930	-0.129	3.383	1.297	0.026
3.20000	-7.307	-10.196	-21.582	-0.287	4.065	1.281	0.062
3.30000	-15.000	-5.276	-16.166	-1.248	5.426	1.335	0.274
3.40000	-2.598	-5.918	-16.327	-1.502	8.299	1.488	0.355
3.50000	-2.766	-12.438	-22.380	-0.413	14.667	1.770	0.117
3.60000	-3.838	-17.043	-26.530	-0.195	110.890	2.230	0.058
3.70000	-5.109	-20.831	-29.874	-0.114	114.890	3.038	0.034
3.80000	-6.263	-24.588	-33.198	-0.073	118.632	4.665	0.022
3.90000	-7.069	-28.352	-36.539	-0.053	122.715	8.177	0.015
4.00000	-7.852	-31.840	-39.612	-0.044	127.408	15.485	0.012
4.10000	-8.982	-34.760	-42.171	-0.041	131.902	28.677	0.011
4.20000	-10.107	-37.081	-44.142	-0.041	135.443	48.112	0.010
4.30000	-8.786	-39.067	-45.788	-0.041	139.553	71.206	0.011
4.40000	-5.200	-41.421	-47.811	-0.042	148.837	96.903	0.012
4.50000	-2.572	-44.864	-50.932	-0.043	164.320	135.388	0.015
4.60000	-1.317	-49.706	-55.460	-0.044	182.941	238.949	0.017
4.70000	-0.831	-56.880	-62.327	-0.045	206.724	820.446	0.019
4.80000	-0.676	-83.878	-89.025	-0.046	230.000	999.900	0.020
4.90000	-0.655	-59.586	-64.440	-0.048	216.606	1.2e+03	0.020
5.00000	-0.688	-53.587	-58.153	-0.049	198.890	317.261	0.021
5.10000	-0.746	-49.788	-54.070	-0.050	187.575	142.025	0.021
5.20000	-0.820	-46.540	-50.543	-0.052	177.777	73.514	0.022
5.30000	-0.924	-43.271	-47.000	-0.053	167.832	38.986	0.022
5.40000	-1.100	-39.630	-43.087	-0.056	156.799	20.311	0.023
5.50000	-1.501	-35.333	-38.519	-0.061	144.303	10.651	0.024
5.60000	-2.652	-30.545	-33.463	-0.077	132.566	6.353	0.027
5.70000	-3.785	-27.790	-30.441	-0.103	128.475	4.930	0.035
5.80000	-2.526	-28.273	-30.658	-0.106	130.063	4.583	0.038
5.90000	-1.797	-28.389	-30.506	-0.114	130.625	4.174	0.042
6.00000	-1.406	-26.574	-28.423	-0.153	128.556	3.283	0.058

Appendix III.
AT-31011 2400 MHz Low Noise Amplifier Touchstone Circuit File

```
!AT-31011 2400 MHz LOW NOISE AMPLIFIER !
!A.J.WARD 9-12-94
!REVISED 06-15-95

DIM
        FREQ    GHZ
        IND     NH
        CAP     PF
        LNG     IN

VAR
        W1=.03                  !INPUT LINE WIDTH
        L1=.15                  !INPUT LINE LENGTH
        C1=1.3                  !INPUT SHUNT CAPACITOR
        C2=1.5                  !INTERSTAGE BLOCKING CAPACITOR
        W2=.02                  !INTERSTAGE LINE WIDTH
        L2=.178                 !INTERSTAGE LINE LENGTH
        W3=.03                  !OUTPUT LINE WIDTH
        L3=.4                   !OUTPUT LINE LENGTH
        LL1=.02
        LL2=.02

CKT
        MSUB ER=4.8 H=.062 T=.0014 RHO=1 RGH=0
        TAND TAND=.002
        MLIN    1       2       W=.1 L=.05
        SLC     2       3       L=.25 C=10
        MLIN    3       4       W=.1 L=.05
        MCROS   4 5 6 7         W1=.1 W2=.02 W3^W1 W4=.1
        MLIN    6       8       W^W1 L^L1
        MLIN    7       14      W=.1 L=.03
        SLC     14      15      L=.25 C^C1
        VIA     15      0       D1=.03 D2=.03 H=.062 T=.0014
        MLIN    5       16      W=.02 L=.68
        MSTEP   16      17      W1=.02 W2=.1
        MLIN    17      18      W=.1 L=.1
        SLC     18      19      L=.25 C=10
        VIA     19      0       D1=.03 D2=.03 H=.062 T=.0014
        RES     18      20      R=50
        SLC     20      21      L=.4 C=1000
        VIA     21      0       D1=.03 D2=.03 H=.062 T=.0014
        MSTEP   8       9       W1^W1 W2=.1
        MLIN    9       10      W=.1        L=.1
        MSTEP   10      11      W1=.1 W2=.02
        DEF2P   1       11      INPUT

        S2PA    1 2 3           C:\S_DATA\BJT\T310113A.S2P
        DEF3P   1 2 3 DEV1

        MLIN    1       2       W=.02  L^LL1
        MLIN    1       3       W=.02  L^LL1
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     3       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     3       0       D1=.030 D2=.030 H=.062 T=.001
        DEF1P   1               Q1EM
```

Appendix III. (continued)

```
        MLIN    1       2       W=.03 L=.03
        MSTEP   2       3       W1=.03 W2^W2
        MLIN    3       4       W^W2        L^L2
        MSTEP   4       5       W1^W2       W2=.1
        MLIN    5       6       W=.1        L=.1
        RES     6       7       R=20                        !Q1 OUTPUT BIAS RESISTOR
        MLIN    7       8       W=.08 L=.04
        MSTEP   8       9       W1=.08 W2=.02
        MLIN    9       10      W=.02 L=.45         !Q1 BIAS DECOUPLING LINE
        MSTEP   10      11      W1=.02 W2=.1
        MLIN    11      12      W=.1 L=.1
        SLC     12      13      L=.4 C=1000
        VIA     13      0       D1=.03 D2=.03 H=.062 T=.0014
        SLC     6       20      L=.25 C^C2          !INTERSTAGE BLOCKING CAP
        MLIN    20      21      W=.1        L=.1
        MSTEP   21      22      W1=.1       W2^W2
        MLIN    22      23      W^W2        L^L2
        MSTEP   23      24      W1^W2 W2=.03
        MLIN    24      25      W=.03 L=.03
        RES     20      30      R=1000 L=1          !Q2 INPUT BIAS RESISTOR
        MLIN    30      31      W=.08 L=.04
        MSTEP   31      32      W1=.08 W2=.02
        MLIN    32      33      W=.02 L=.1 !Q2 BIAS DECOUPLING LINE
        SLC     33      35      L=.4 C=1000
        VIA     35      0       D1=.03 D2=.03 H=.062 T=.0014
        DEF2P   1       25      INTER

        S2PA    1 2 3
        DEF3P   1 2 3           DEV2

        MLIN    1       2       W=.02 L^LL2
        MLIN    1       3       W=.02 L^LL2
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     3       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     3       0       D1=.030 D2=.030 H=.062 T=.001
        DEF1P   1               Q2EM

        MLIN    1       2       W=.03 L=.01
        MSTEP   2       3       W1=.03 W2^W3
        MLIN    3       4       W^W3 L^L3           !OUTPUT SERIES MICROSTRIPLINE
CAP     4       0       C=2
        SRL     3       5       R=50 L=1    !OUTPUT BIAS RESISTOR
        MLIN    5       6       W=.08 L=.04
        MSTEP   6       7       W1=.08 W2=.02
        MLIN    7       8       W=.02 L=.68  !OUTPUT BIAS DECOUPLING LINE
        SLC     8       9       L=.4 C=1000
        VIA     9       0       D1=.03 D2=.03 H=.062 T=.0014
        SLC     4       10      L=.25 C=10  !OUTPUT BLOCKING CAPACITOR
        MLIN    10      11      W=.1  L=.1
        DEF2P   1       11      OUTPUT

        INPUT   1       2
        DEV1    2 3 4
        Q1EM    4
        INTER   3 5
        DEV2    5 6 7
        Q2EM    7
```

Appendix III. (continued)

```
        OUTPUT 6  8
        DEF2P  1  8  AMP

FREQ
        !SWEEP  .8  .95 .05
        SWEEP   .1  6  .1
        !STEP   2.4
        !SWEEP 2.3  2.5  .05

OUT
        AMP     DB[S11]
        AMP     DB[S21]
        AMP     DB[S12]
        AMP     DB[S22]
        AMP     NF
        AMP     K
        AMP     B1
```

Appendix IV
AT-31011 2400 MHz Low Noise Amplifier Touchstone Output File

FREQ GHZ	DB[S11] AMP	DB[S21] AMP	DB[S12] AMP	DB[S22] AMP	NF AMP	K AMP	B1 AMP
0.10000	-1.062	-25.182	-127.386	-1.469	187.514	1.3e+06	0.512
0.20000	-2.238	-17.107	-107.059	-5.097	167.325	2.2e+05	1.103
0.30000	-3.106	-14.030	-96.733	-9.769	157.806	7.9e+04	1.332
0.40000	-4.179	-11.418	-88.924	-11.791	147.718	3.0e+04	1.291
0.50000	-6.116	-5.838	-79.275	-9.303	125.694	6.0e+03	1.098
0.60000	-9.158	1.884	-68.806	-6.720	9.221	767.412	0.883
0.70000	-5.916	8.755	-59.488	-4.902	6.045	86.657	0.849
0.80000	-1.510	13.302	-52.728	-3.672	3.465	8.081	0.969
0.90000	-0.759	15.839	-48.162	-2.926	3.126	2.195	0.874
1.00000	-3.086	16.219	-47.144	-2.533	3.617	4.467	0.630
1.10000	-6.211	15.194	-46.967	-2.233	4.244	6.010	0.494
1.20000	-6.775	13.557	-47.433	-1.901	4.767	6.667	0.439
1.30000	-6.028	12.114	-47.732	-1.606	5.052	6.605	0.400
1.40000	-5.436	11.090	-47.632	-1.372	5.045	6.050	0.361
1.50000	-5.146	10.504	-47.111	-1.189	4.777	5.198	0.326
1.60000	-5.020	10.311	-46.304	-1.062	4.350	4.298	0.298
1.70000	-5.087	10.495	-45.119	-0.970	3.884	3.392	0.275
1.80000	-5.332	11.064	-43.545	-0.909	3.469	2.560	0.256
1.90000	-5.833	12.146	-42.197	-0.880	3.131	1.993	0.242
2.00000	-6.630	13.619	-40.444	-0.908	2.882	1.547	0.236
2.10000	-7.811	15.390	-38.208	-1.045	2.689	1.228	0.250
2.20000	-9.439	17.534	-35.567	-1.562	2.498	1.096	0.329
2.30000	-10.168	19.528	-33.040	-3.547	2.290	1.218	0.602
2.40000	-8.117	19.730	-32.267	-10.820	2.112	1.677	1.043
2.50000	-6.692	17.784	-33.774	-13.923	2.025	2.396	1.159
2.60000	-6.057	14.779	-36.308	-7.421	2.002	3.569	1.039
2.70000	-5.351	11.596	-38.988	-4.821	2.072	5.294	0.889
2.80000	-4.538	8.423	-41.626	-3.415	2.260	7.682	0.753
2.90000	-3.765	5.290	-44.192	-2.529	2.595	10.856	0.637
3.00000	-3.103	2.218	-46.669	-1.934	3.095	14.941	0.540
3.10000	-2.538	-0.665	-49.149	-1.506	3.745	19.792	0.458
3.20000	-2.079	-3.453	-51.487	-1.209	4.545	25.637	0.394
3.30000	-1.706	-6.114	-53.649	-0.999	5.455	32.402	0.345
3.40000	-1.401	-8.621	-55.612	-0.849	6.469	39.855	0.306
3.50000	-1.151	-10.953	-57.357	-0.740	7.804	47.556	0.277

Appendix IV. (continued)

FREQ GHZ	DB[S11] AMP	DB[S21] AMP	DB[S12] AMP	DB[S22] AMP	NF AMP	K AMP	B1 AMP
3.60000	-0.944	-13.090	-58.869	-0.662	8.831	54.827	0.255
3.70000	-0.772	-15.018	-60.137	-0.606	10.646	60.822	0.239
3.80000	-0.628	-16.729	-61.158	-0.567	23.033	64.789	0.228
3.90000	-0.510	-18.237	-61.950	-0.542	108.229	66.692	0.221
4.00000	-0.424	-19.592	-62.567	-0.529	115.275	68.719	0.218
4.10000	-0.415	-20.849	-62.734	-0.525	121.982	78.852	0.217
4.20000	-0.885	-21.223	-62.032	-0.532	123.681	154.792	0.209
4.30000	-0.164	-22.151	-61.899	-0.545	129.046	35.679	0.232
4.40000	-0.112	-23.504	-62.207	-0.566	135.252	30.737	0.241
4.50000	-0.096	-24.905	-62.579	-0.589	141.063	33.882	0.251
4.60000	-0.092	-26.441	-63.104	-0.613	146.946	42.347	0.260
4.70000	-0.092	-28.146	-63.815	-0.630	153.040	56.771	0.267
4.80000	-0.092	-30.047	-64.740	-0.635	159.418	78.833	0.269
4.90000	-0.091	-32.170	-65.904	-0.622	166.132	111.562	0.264
5.00000	-0.089	-34.519	-67.313	-0.590	173.204	159.859	0.252
5.10000	-0.086	-37.057	-68.927	-0.544	180.576	230.188	0.233
5.20000	-0.082	-39.651	-70.616	-0.490	187.968	325.612	0.212
5.30000	-0.077	-42.024	-72.099	-0.435	194.686	428.636	0.189
5.40000	-0.073	-43.798	-73.002	-0.384	199.757	486.771	0.168
5.50000	-0.068	-44.848	-73.196	-0.339	202.939	467.729	0.149
5.60000	-0.064	-45.563	-73.071	-0.300	205.529	420.440	0.132
5.70000	-0.062	-46.692	-73.375	-0.265	209.831	424.844	0.117
5.80000	-0.063	-49.524	-75.397	-0.232	219.639	657.731	0.103
5.90000	-0.068	-58.864	-83.940	-0.198	230.000	4.8e+03	0.088
6.00000	-0.078	-50.536	-74.829	-0.166	224.833	618.737	0.074

Applications

The application notes represented by these abstracts are available from your local Hewlett-Packard sales office or nearest Hewlett-Packard authorized distributor or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

Applications Literature

High Frequency Transistor Primer Series

Primer 1
Silicon Bipolar Electrical Characteristics

Publication No. 300120

Primer 2
Noise and S-Parameter Characterization

Publication No. 5091-8350E

Primer 3
Thermal Properties

Publication No. 300124

Primer 3A
Thermal Resistance

Publication No. 300126

General Application Notes

AN A001
Notes on Choke Network Design

Designing bias decoupling networks for bipolar transistors and GaAs FET devices that provide stable device performance.

Publication No. 5091-8824E

AN A004R
Electrostatic Discharge Damage and Control

Identifying and preventing ESD damage to semiconductor devices

Publication No. 5091-8803E

AN A005
Transistor Chip Use

Discussion of procedures for proper storage, die attach, and bonding for discrete transistors

Publication No. 5091-8802E

AN A006
Mounting Considerations for Packaged Microwave Semiconductors

Mechanical, thermal, and soldering information

Publication No. 5091-8696E

AN A008
Microwave Oscillator Design

Using S-Parameters to predict frequency of oscillation

Publication No. 5964-3431E

AN A009
Direct Broadcast Satellite Systems

This note takes a system level look at the individual components that make up a low noise block downconverter

Publication No. 5091-8819E

AN S014
750 – 1250 MHz Voltage Controlled Oscillator

This application note uses S parameter analysis to determine the negative resistance region of the oscillator circuit and resultant resonant frequency when mated with a tuned circuit

Publication No. 5966-0935E

AN 1084
2 Stage 800 – 1000 MHz Amplifier Using the AT-41511 Silicon Bipolar Transistor

A two stage amplifier is described that provides 2 dB noise figure and 30 dB gain. Power output performance versus bias voltage is also discussed.

Publication No. 5964-3853E

AN 1131
Low Noise Amplifiers for 320 MHz and 850 MHz using the AT-32063 Dual Transistor

The application note discusses the design of cascode low noise amplifiers for 320 and 850 MHz using the AT-32063 dual transistor.

Publication No. 5966-0781E

Silicon Bipolar Transistors Selection Guide

NF_o and G_a are specified at a low noise bias point, while $P_{1\,dB}$, $G_{1\,dB}$, and $|S_{21E}|^2$ are specified at bias points which optimize these parameters.

Low Noise Transistors (Typical Specifications @ 25°C Case Temperature)

Part Number	Frequency (GHz)	V_{CE} (V)	NF_o (dB)	G_a (dB)	$P_{1\,dB}$ (dBm)	$G_{1\,dB}$ (dBm)	$\|S_{21E}\|^2$ @ 1.0 GHz (dB)	Package	Page No.
AT-30511	0.9	2.7	1.1	16.0	+7.0	16.5	17.9[1]	SOT-143 plastic SM	4-23
AT-30533	0.9	2.7	1.1	13.0	+7.0	15.0	15.2[1]	SOT-23 plastic SM	4-23
AT-31011	0.9	2.7	0.9	13.0	+9.0	14.0	19.1[1]	SOT-143 plastic SM	4-33
AT-31033	0.9	2.7	0.9	11.0	+9.0	12.0	15.8[1]	SOT-23 plastic SM	4-33
AT-32011	0.9	2.7	1.0	14.0	+13.0	16.5	18.9[1]	SOT-143 plastic SM	4-53
AT-32033	0.9	2.7	1.0	12.5	+13.0	14.5	15.1[1]	SOT-23 plastic SM	4-53
AT-32063[2]	0.9	2.7	1.1	14.5	+12.0	16.0	17.0[1]	SOT-363 plastic SM	4-63
AT-41410	2.0	8.0	1.6	14.0	+19.0	14.0	17.7	100 mil stripline	4-104
AT-41411	2.0	8.0	1.8	13.0	+17.0	13.0	16.7	SOT-143 plastic SM	4-109
AT-41435	2.0	8.0	1.7	14.0	+19.0	14.0	17.2	micro-X SM	4-114
AT-41485	1.0	8.0	1.4	18.5	+18.5	14.0[3]	17.5	85 mil plastic	4-124
AT-41486	1.0	8.0	1.4	18.0	+18.0	13.5[3]	17.5	85 mil plastic SM	4-129
AT-41511	0.9	5.0	1.0	15.5	+14.5	17.5	15.8[1]	SOT-143 plastic SM	4-134
AT-41533	0.9	5.0	1.0	14.5	+14.5	14.5	13.9[1]	SOT-23 plastic SM	4-134
AT-41586	1.0	8.0	1.4	17.0	+18.0	13.0[3]	17.0	85 mil plastic SM	4-144
AT-42010	2.0	8.0	1.9	13.5	+21.0	14.0	17.0	100 mil stripline	4-154
AT-42035	2.0	8.0	1.9	13.5	+21.0	14.0	16.6	micro-X SM	4-159
AT-42070	2.0	8.0	1.9	14.0	+21.0	15.0	17.3	70 mil stripline	4-164
AT-42085	2.0	8.0	1.9	13.5	+20.5	14.0	17.0	85 mil plastic	4-169
AT-42086	2.0	8.0	1.9	13.0	+20.5	13.5	16.5	85 mil plastic SM	4-174

Notes:

1. Typical at 900 MHz
2. Dual transistor — All data is per individual transistor.
3. Typical $G_{1\,dB}$ at 2 GHz

Silicon Bipolar Transistors Selection Guide, continued

Medium Power Transistors (Typical Specifications @ 25°C Case Temperature)

Part Number	V_{CE} (V)	$P_{1\,dB}$ @ 2 GHz (dBm)	$G_{1\,dB}$ @ 2 GHz (dBm)	$P_{1\,dB}$ @ 4 GHz (dBm)	$G_{1\,dB}$ @ 4 GHz (dBm)	Package	Page No.
AT-64020	16.0	+28	10.0	+27	6.5	200 mil BeO disk	4-179
AT-64023	16.0	+28	12.5	+27	9.5	230 mil flange BeO	4-183

Medium/High Power Transistors (Typical Specifications @ 25°C Case Temperature)

Part Number	Frequency (GHz)	V_{CE} (V)	P_{out} (dBm)	Power Gain (dB)	Collector Efficiency (%)	Package	Page No.
AT-31625	0.9	4.8	+28, CW	9	70	MSOP-3	4-43
AT-33225	0.9	4.8	+31, CW	9	70	MSOP-3	4-71
AT-36408	0.9	4.8	+35, pulsed	9	60	SOIC-8	4-81
AT-38086	0.9	4.8	+28, pulsed	11	60	85 mil plastic	4-89

HEWLETT® PACKARD

Low Current, High Performance NPN Silicon Bipolar Transistor

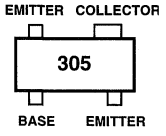
Technical Data

AT-30511
AT-30533

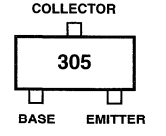
Features

- **High Performance Bipolar Transistor Optimized for Low Current, Low Voltage Operation**
- **900 MHz Performance:**
  AT-30511: 1.1 dB NF, 16 dB G_A
  AT-30533: 1.1 dB NF, 13 dB G_A
- **Characterized for End-Of-Life Battery Use (2.7 V)**
- **SOT-23 and SOT-143 SMT Plastic Packages**
- **Tape-And-Reel Packaging Option Available[1]**

Outline Drawing



SOT-143 (AT-30511)



SOT-23 (AT-30533)

Note:
1. Refer to "Tape-and-Reel Packaging for Semiconductor Devices".

Description

Hewlett-Packard's AT-30511 and AT-30533 are high performance NPN bipolar transistors that have been optimized for maximum f_T at low voltage operation, making them ideal for use in battery powered applications in wireless markets. The AT-30533 uses the 3 lead SOT-23, while the AT-30511 places the same die in the higher performance 4 lead SOT-143. Both packages are industry standard, and compatible with high volume surface mount assembly techniques.

The 3.2 micron emitter-to-emitter pitch and reduced parasitic design of these transistors yields extremely high performance products that can perform a multiplicity of tasks. The 5 emitter finger interdigitated geometry yields an extremely fast transistor with high gain and low operating currents.

Optimized performance at 2.7 V makes these devices ideal for use in 900 MHz, 1.8 GHz, and 2.4 GHz battery operated systems as an LNA, gain stage, buffer, oscillator, or active mixer. Typical amplifier designs at 900 MHz yield 1.3 dB noise figures with 13 dB or more associated gain at a 2.7 V, 1 mA bias. Voltage breakdowns are high enough for use at 5 volts. High gain capability at 1 V, 1 mA makes these devices a good fit for 900 MHz pager applications.

The AT-3 series bipolar transistors are fabricated using an optimized version of Hewlett- Packard's 10 GHz f_T, 30 GHz f_{MAX} Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices.

AT-30511, AT-30533 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	11
V_{CEO}	Collector-Emitter Voltage	V	5.5
I_C	Collector Current	mA	8
P_T	Power Dissipation[2] [3]	mW	100
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{jc} = 550°C/W$

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{Mounting\ Surface} = 25°C$.
3. Derate at 1.82 mW/°C for $T_C > 95°C$.

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	AT-30511			AT-30533		
				Min	Typ	Max	Min	Typ	Max
NF	Noise Figure $V_{CE} = 2.7$ V, $I_C = 1$ mA	f = 0.9 GHz	dB		1.1[1]	1.4[1]		1.1[2]	1.4[2]
G_A	Associated Gain $V_{CE} = 2.7$ V, $I_C = 1$ mA	f = 0.9 GHz	dB	14[1]	16[1]		11[2]	13[2]	
h_{FE}	Forward Current Transfer Ratio	$V_{CE} = 2.7$ V $I_C = 1$ mA	-	70		300	70		300
I_{CBO}	Collector Cutoff Current	$V_{CB} = 3$ V	µA		0.03	0.2		0.03	0.2
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 1$ V	µA		0.1	1.5		0.1	1.5

Notes:

1. Test circuit B, Figure 1. Numbers reflect device performance de-embedded from circuit losses. Input loss = 0.4 dB; output loss = 0.4 dB.
2. Test circuit A, Figure 1. Numbers reflect device performance de-embedded from circuit losses. Input loss = 0.4 dB; output loss = 0.4 dB.

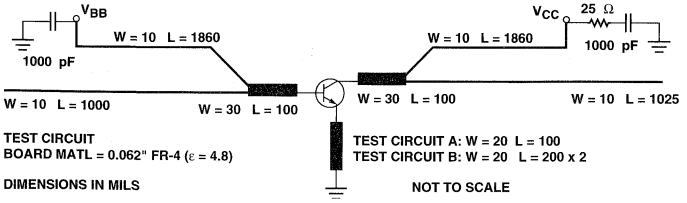


Figure 1. Test Circuit for Noise Figure and Associated Gain. This Circuit is a Compromise Match Between Best Noise Figure, Best Gain, Stability, a Practical, Synthesizable Match, and a Circuit Capable of Matching Both the AT-305 and AT-310 Geometries.

AT-30511, AT-30533 Characterization Information, T_A = 25°C

Symbol	Parameters and Test Conditions	Units	AT-30511 Typ	AT-30533 Typ
P_{1dB}	Power at 1 dB Gain Compression (opt tuning) V_{CE} = 2.7 V, I_C = 5 mA f = 0.9 GHz	dBm	7	7
G_{1dB}	Gain at 1 dB Gain Compression (opt tuning) V_{CE} = 2.7 V, I_C = 5 mA f = 0.9 GHz	dB	16.5	15
IP_3	Output Third Order Intercept Point, V_{CE} = 2.7 V, I_C = 5 mA (opt tuning) f = 0.9 GHz	dBm	17	17
$\|S_{21}\|_E^2$	Gain in 50 Ω System; V_{CE} = 2.7 V, I_C = 1 mA f = 0.9 GHz	dB	10	9
C_{CB}	Collector-Base Capacitance V_{CB} = 3V, f = 1 MHz	pF	0.04	0.04

Typical Performance

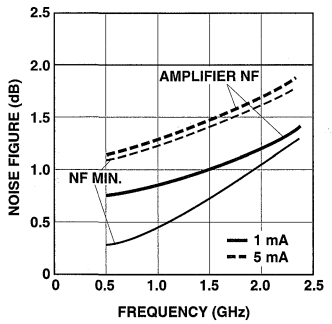


Figure 2. AT-30511 and AT-30533 Minimum Noise Figure and Amplifier NF[1] vs. Frequency and Current at V_{CE} = 2.7 V.

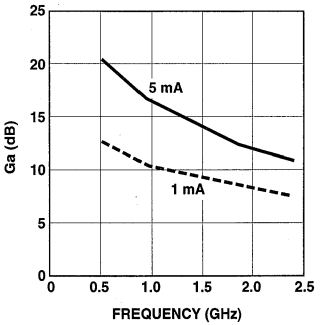


Figure 3. AT-30511 Associated Gain at Optimum Noise Match vs. Frequency and Current at V_{CE} = 2.7 V.

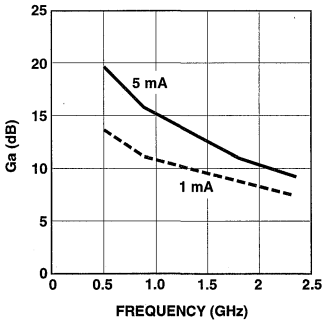


Figure 4. AT-30533 Associated Gain at Optimum Noise Match vs. Frequency and Current at V_{CE} = 2.7 V.

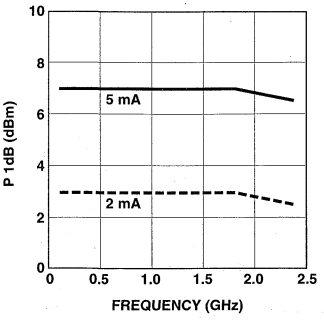


Figure 5. AT-30511 and AT-30533 Power at 1 dB Gain Compression vs. Frequency and Current at V_{CE} = 2.7 V.

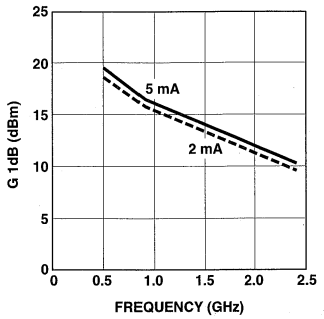


Figure 6. AT-30511 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 2.7 V.

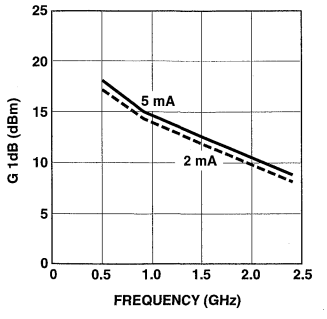


Figure 7. AT-30533 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 2.7 V.

Note:

1. Amplifier NF represents the noise figure which can be expected in a real circuit representing reasonable reflection coefficients and including circuit losses.

AT-30511, AT-30533 Typical Performance, continued

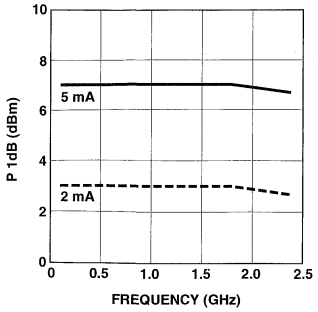


Figure 8. AT-30511 and AT-30533 Power at 1 dB Gain Compression vs. Frequency and Current at V_{CE} = 5 V.

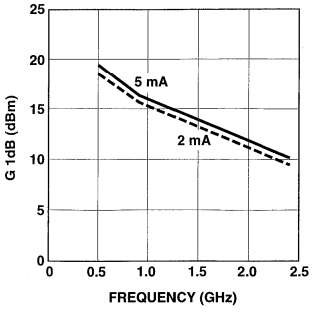


Figure 9. AT-30511 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 5 V.

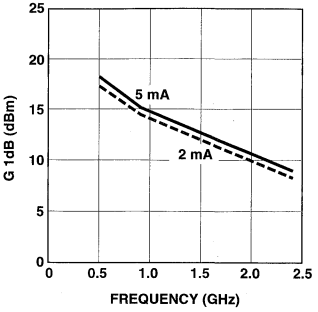


Figure 10. AT-30533 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 5 V.

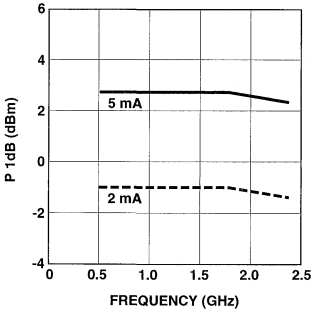


Figure 11. AT-30511 and AT-30533 Power at 1 dB Gain Compression vs. Frequency and Current at V_{CE} = 1 V.

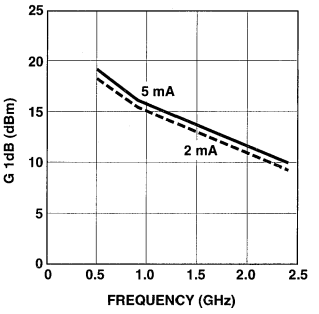


Figure 12. AT-30511 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 1 V.

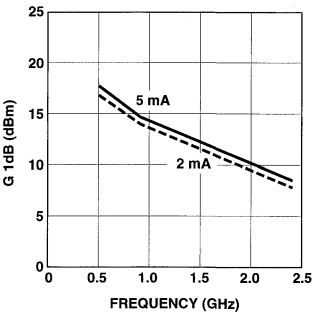


Figure 13. AT-30533 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 1 V.

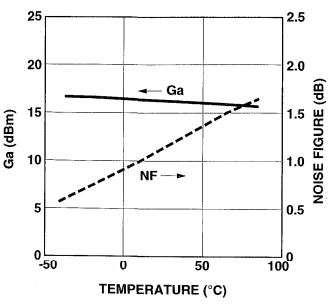


Figure 14. AT-30511 Noise Figure and Associated Gain at V_{CE} = 2.7 V, I_C = 1 mA vs. Temperature in Test Circuit, Figure 1. (Circuit Losses De-embedded)

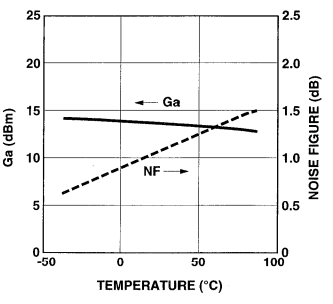


Figure 15. AT-30533 Noise Figure and Associated Gain at V_{CE} = 2.7 V, I_C = 1 mA vs. Temperature in Test Circuit, Figure 1. (Circuit Losses De-embedded)

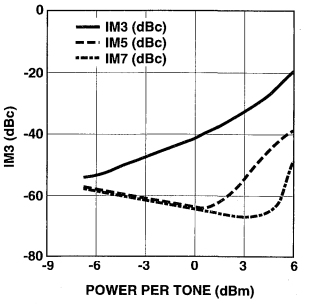


Figure 16. AT-30511 and AT-30533 Intermodulation Products vs. Output Power at V_{CE} = 2.7 V, I_C = 10 mA, 900 MHz with Optimal Tuning.

AT-30511 Typical Scattering Parameters, V_{CE} = 1 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.97	-5	10.84	3.48	175	-39.42	0.01	86	0.99	-2
0.5	0.95	-24	10.51	3.35	155	-25.87	0.05	72	0.95	-14
0.9	0.85	-42	9.96	3.15	137	-21.46	0.08	61	0.92	-24
1.0	0.83	-46	9.66	3.04	133	-20.71	0.09	58	0.91	-26
1.5	0.70	-67	8.71	2.73	113	-18.44	0.12	46	0.84	-36
1.8	0.63	-78	8.06	2.53	102	-17.69	0.13	41	0.80	-40
2.0	0.59	-85	7.75	2.44	96	-17.27	0.14	37	0.77	-43
2.4	0.50	-100	6.73	2.17	84	-16.79	0.14	32	0.73	-48
3.0	0.39	-122	5.58	1.90	67	-16.32	0.15	27	0.68	-53
4.0	0.29	-161	3.97	1.58	45	-15.87	0.16	20	0.63	-63
5.0	0.27	153	2.64	1.36	25	-15.47	0.17	20	0.61	-72

AT-30511 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 1 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.3	0.96	10	1.49
0.9	0.4	0.92	19	1.33
1.8	0.9	0.83	43	0.98
2.4	1.3	0.76	60	0.74

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{opt}|$ values unachievable in physical circuits. See Fig. 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

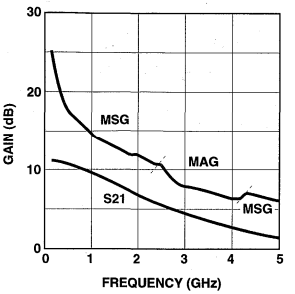


Figure 17. AT-30511 Gains vs. Frequency at V_{CE} = 1 V, I_C = 1 mA.

AT-30533 Typical Scattering Parameters, V_{CE} = 1 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.95	-5	10.90	3.51	174	-38.36	0.01	87	0.99	-3
0.5	0.91	-25	10.32	3.28	150	-25.08	0.06	73	0.95	-14
0.9	0.77	-41	9.44	2.97	128	-20.95	0.09	63	0.89	-24
1.0	0.73	-45	9.03	2.83	124	-20.21	0.10	61	0.88	-25
1.5	0.55	-62	7.75	2.44	102	-18.13	0.12	54	0.80	-33
1.8	0.46	-71	6.94	2.22	91	-17.33	0.14	51	0.77	-36
2.0	0.41	-76	6.51	2.12	85	-16.84	0.14	50	0.74	-38
2.4	0.30	-85	5.45	1.87	73	-16.05	0.16	49	0.71	-41
3.0	0.17	-95	4.26	1.63	57	-14.80	0.18	49	0.68	-46
4.0	0.02	-139	2.71	1.37	37	-12.58	0.24	48	0.65	-57
5.0	0.12	61	1.56	1.20	19	-10.14	0.31	45	0.62	-69

AT-30533 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 1 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.3	0.94	7	1.02
0.9	0.4	0.89	16	0.86
1.8	0.9	0.75	43	0.58
2.4	1.3	0.65	65	0.38

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{opt}|$ values unachievable in physical circuits. See Fig. 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

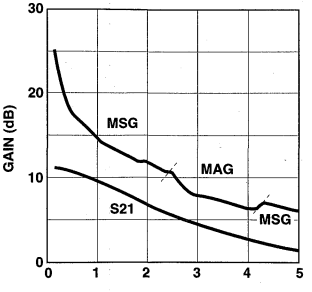


Figure 18. AT-30533 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 1 mA.

AT-30511 Typical Scattering Parameters, V_{CE} = 2.7 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.97	-5	10.88	3.50	175	-40.13	0.01	86	0.999	-2
0.5	0.95	-23	10.58	3.38	156	-26.71	0.05	74	0.96	-13
0.9	0.86	-39	10.09	3.20	139	-22.28	0.08	63	0.93	-23
1.0	0.84	-43	9.83	3.10	135	-21.51	0.08	60	0.92	-25
1.5	0.72	-63	8.94	2.80	115	-19.15	0.11	49	0.85	-34
1.8	0.65	-73	8.32	2.60	105	-18.28	0.12	43	0.82	-38
2.0	0.61	-80	8.06	2.53	99	-17.83	0.13	40	0.79	-41
2.4	0.52	-93	7.06	2.25	86	-17.29	0.14	35	0.75	-46
3.0	0.41	-114	5.92	1.98	70	-16.72	0.15	30	0.70	-51
4.0	0.30	-150	4.35	1.65	48	-16.13	0.16	23	0.66	-61
5.0	0.26	165	3.06	1.42	28	-15.65	0.16	22	0.63	-69

AT-30511 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 2.7 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.3	0.96	10	1.49
0.9	0.4	0.92	19	1.33
1.8	0.9	0.83	43	0.98
2.4	1.3	0.76	60	0.74

Notes:

1. Matching constraints may make F_{min} values associated with high $|\Gamma_{opt}|$ values unachievable in physical circuits. See Fig. 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

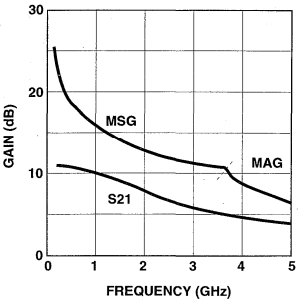


Figure 19. AT-30511 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 1 mA.

AT-30533 Typical Scattering Parameters, V_{CE} = 2.7 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.95	-5	10.76	3.45	174	-39.49	0.01	87	0.999	-2
0.5	0.92	-23	10.21	3.24	151	-26.05	0.05	74	0.95	-13
0.9	0.78	-39	9.42	2.96	130	-21.78	0.08	64	0.91	-22
1.0	0.75	-42	9.04	2.83	126	-21.05	0.09	63	0.90	-23
1.5	0.58	-59	7.83	2.46	105	-18.88	0.11	55	0.83	-31
1.8	0.49	-66	7.04	2.25	94	-18.08	0.12	53	0.79	-34
2.0	0.44	-71	6.64	2.15	88	-17.58	0.13	52	0.77	-36
2.4	0.33	-79	5.59	1.90	76	-16.77	0.15	51	0.74	-39
3.0	0.21	-87	4.40	1.66	60	-15.50	0.17	51	0.71	-44
4.0	0.05	-88	2.87	1.39	40	-13.20	0.22	52	0.68	-54
5.0	0.09	47	1.72	1.22	22	-10.67	0.29	49	0.66	-66

AT-30533 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 2.7 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.3	0.94	7	1.02
0.9	0.4	0.89	16	0.88
1.8	0.9	0.75	43	0.58
2.4	1.3	0.65	65	0.38

Notes:

1. Matching constraints may make F_{min} values associated with high $|\Gamma_{opt}|$ values unachievable in physical circuits. See Fig. 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

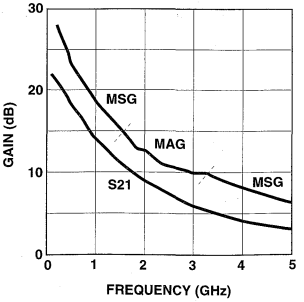


Figure 20. AT-30511- Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 1 mA.

AT-30511 Typical Scattering Parameters, V_{CE} = 2.7 V, I_C = 5 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.88	-11	22.49	13.32	169	-40.50	0.01	83	0.97	-5
0.5	0.70	-48	20.42	10.49	134	-28.45	0.04	64	0.82	-22
0.9	0.49	-72	17.77	7.73	111	-25.24	0.05	57	0.70	-30
1.0	0.46	-77	17.09	7.15	107	-24.70	0.06	55	0.69	-31
1.5	0.30	-100	14.44	5.27	89	-22.62	0.07	53	0.62	-35
1.8	0.24	-112	13.10	4.52	81	-21.65	0.08	52	0.59	-37
2.0	0.21	-120	12.31	4.13	76	-21.05	0.09	52	0.58	-39
2.4	0.16	-140	10.94	3.52	67	-20.01	0.10	50	0.57	-42
3.0	0.13	-172	9.18	2.88	55	-18.55	0.12	48	0.55	-46
4.0	0.15	137	7.03	2.25	38	-16.57	0.15	44	0.53	-55
5.0	0.21	106	5.44	1.87	22	-14.88	0.18	39	0.52	-64

AT-30511 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 2.7 V, I_C = 5 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT}		R_n
		Mag	Ang	
0.5[2]	1.1	0.77	9	1.10
0.9	1.2	0.71	18	0.96
1.8	1.5	0.60	45	0.66
2.4	1.8	0.51	65	0.47

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{opt}|$ values unachievable in physical circuits. See Fig. 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

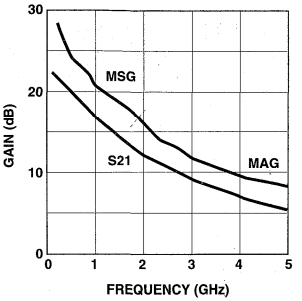


Figure 21. AT-30511 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 5 mA.

AT-30533 Typical Scattering Parameters, V_{CE} = 2.7 V, I_C = 5 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.84	-12	22.26	12.98	164	-39.96	0.01	82	0.98	-5
0.5	0.57	-39	18.54	8.46	121	-28.03	0.04	71	0.80	-18
0.9	0.37	-46	14.97	5.60	100	-24.09	0.06	70	0.73	-22
1.0	0.34	-46	14.20	5.13	96	-23.32	0.07	69	0.72	-22
1.5	0.23	-43	11.24	3.65	81	-20.30	0.10	68	0.69	-26
1.8	0.20	-38	9.85	3.11	73	-18.88	0.11	67	0.68	-28
2.0	0.19	-35	9.05	2.84	69	-18.02	0.13	66	0.68	-30
2.4	0.17	-27	7.70	2.43	61	-16.50	0.15	64	0.67	-33
3.0	0.15	-17	6.12	2.02	50	-14.57	0.19	61	0.66	-39
4.0	0.15	-2	4.30	1.64	34	-11.90	0.25	55	0.64	-49
5.0	0.17	11	3.07	1.42	19	-9.66	0.33	47	0.61	-61

AT-30533 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 2.7 V, I_C = 5 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT}		R_n
		Mag	Ang	
0.5[2]	1.1	0.71	8	0.78
0.9	1.2	0.61	16	0.66
1.8	1.5	0.42	39	0.41
2.4	1.8	0.28	57	0.25

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{opt}|$ values unachievable in physical circuits. See Fig. 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

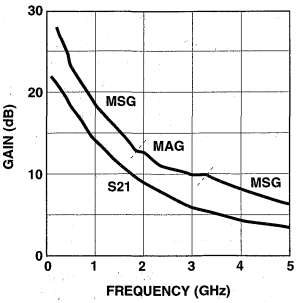


Figure 22. AT-30533 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 5 mA.

AT-30511 Typical Scattering Parameters, V_{CE} = 5 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.98	-5	10.56	3.37	175	-40.34	0.01	87	0.999	-2
0.5	0.96	-21	10.30	3.27	157	-26.99	0.04	74	0.96	-13
0.9	0.88	-37	9.83	3.10	139	-22.52	0.07	64	0.93	-22
1.0	0.85	-41	9.57	3.01	136	-21.75	0.08	62	0.92	-24
1.5	0.74	-59	8.71	2.73	116	-19.23	0.11	51	0.86	-33
1.8	0.67	-69	8.13	2.55	106	-18.34	0.12	45	0.82	-38
2.0	0.63	-75	7.88	2.48	100	-17.85	0.13	42	0.80	-41
2.4	0.55	-88	6.90	2.21	87	-17.23	0.14	37	0.77	-45
3.0	0.43	-106	5.79	1.95	71	-16.53	0.15	31	0.72	-50
4.0	0.31	-138	4.29	1.64	49	-15.83	0.16	23	0.67	-60
5.0	0.25	178	3.04	1.42	29	-15.38	0.17	20	0.64	-69

AT-30511 Typical Noise Parameters,
Common Emitter, Z_O = 50 Ω, 5 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.3	0.96	10	1.49
0.9	0.4	0.92	19	1.33
1.8	0.9	0.83	43	0.98
2.4	1.3	0.76	60	0.74

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{opt}|$ values unachievable in physical circuits. See Fig. 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

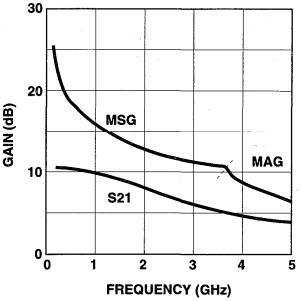


Figure 23. AT-30511 Gains vs. Frequency at V_{CE} = 5 V, I_C = 1 mA.

AT-30533 Typical Scattering Parameters, V_{CE} = 5 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.96	-5	10.59	3.38	174	-39.38	0.01	85	0.999	-2
0.5	0.92	-22	10.07	3.19	151	-26.22	0.05	74	0.95	-13
0.9	0.79	-37	9.32	2.92	131	-21.99	0.08	65	0.91	-21
1.0	0.77	-41	8.94	2.80	127	-21.21	0.09	63	0.90	-23
1.5	0.60	-57	7.76	2.44	106	-19.02	0.11	56	0.83	-30
1.8	0.51	-64	7.01	2.24	95	-18.16	0.12	54	0.80	-33
2.0	0.46	-69	6.61	2.14	89	-17.66	0.13	52	0.78	-35
2.4	0.35	-76	5.59	1.90	77	-16.85	0.14	51	0.75	-39
3.0	0.23	-83	4.43	1.66	61	-15.58	0.17	51	0.72	-43
4.0	0.07	-85	2.92	1.40	41	-13.34	0.22	52	0.69	-53
5.0	0.07	38	1.79	1.23	23	-10.85	0.29	49	0.67	-65

AT-30533 Typical Noise Parameters,
Common Emitter, Z_O = 50 Ω, 5 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.3	0.94	7	1.02
0.9	0.4	0.89	16	0.98
1.8	0.9	0.75	43	0.58
2.4	1.3	0.65	65	0.38

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unachievable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

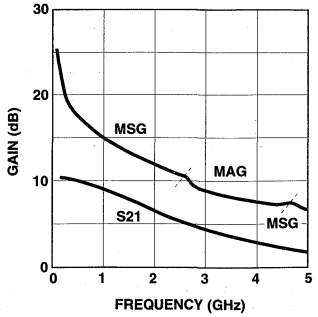


Figure 24. AT-30533 Gains vs. Frequency at V_{CE} = 5 V, I_C = 1 mA.

AT-30511 Typical Scattering Parameters, V_{CE} = 5 V, I_C = 5 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.90	-10	22.26	12.98	170	-40.75	0.01	82	0.97	-5
0.5	0.74	-43	20.41	10.49	136	-28.46	0.04	66	0.83	-22
0.9	0.53	-66	17.93	7.88	113	-25.18	0.06	58	0.72	-30
1.0	0.49	-70	17.28	7.31	109	-24.53	0.06	57	0.70	-31
1.5	0.33	-89	14.72	5.45	91	-22.46	0.08	54	0.63	-36
1.8	0.27	-99	13.41	4.68	83	-21.45	0.08	53	0.60	-38
2.0	0.24	-105	12.64	4.29	78	-20.87	0.09	52	0.59	-39
2.4	0.18	-120	11.27	3.66	69	-19.79	0.10	50	0.57	-42
3.0	0.12	-147	9.54	3.00	57	-18.34	0.12	48	0.55	-46
4.0	0.11	154	7.41	2.35	40	-16.45	0.15	43	0.53	-55
5.0	0.17	114	5.86	1.96	24	-14.84	0.18	38	0.52	-63

AT-30511 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 5 V, I_C = 5 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	1.1	0.77	9	1.10
0.9	1.2	0.71	18	0.96
1.8	1.5	0.60	45	0.66
2.4	1.8	0.51	65	0.47

Notes:

1. Matching constraints may make F_{min} values associated with high $|\Gamma_{opt}|$ values unachievable in physical circuits. See Fig. 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

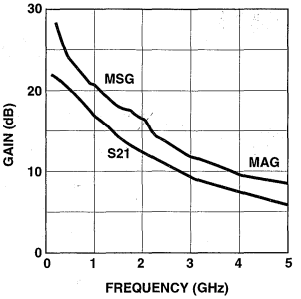


Figure 25. AT-30511 Gains vs. Frequency at V_{CE} = 5 V, I_C = 5 mA.

AT-30533 Typical Scattering Parameters, V_{CE} = 5 V, I_C = 5 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.86	-11	22.22	12.92	165	-40.16	0.01	83	0.98	-5
0.5	0.59	-37	18.69	8.60	122	-28.05	0.04	72	0.81	-18
0.9	0.40	-43	15.19	5.75	101	-24.14	0.06	70	0.74	-22
1.0	0.37	-43	14.43	5.27	97	-23.37	0.07	70	0.73	-22
1.5	0.27	-40	11.49	3.75	82	-20.30	0.10	68	0.70	-26
1.8	0.24	-37	10.11	3.20	75	-18.88	0.11	67	0.69	-28
2.0	0.23	-35	9.33	2.93	70	-18.05	0.13	66	0.68	-30
2.4	0.20	-30	7.97	2.50	62	-16.55	0.15	64	0.67	-33
3.0	0.18	-24	6.40	2.09	51	-14.64	0.19	61	0.66	-38
4.0	0.17	-14	4.58	1.70	36	-12.00	0.25	54	0.64	-49
5.0	0.16	-2	3.37	1.47	21	-9.83	0.32	46	0.61	-60

AT-30533 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 5 V, I_C = 5 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	1.1	0.71	8	0.78
0.9	1.2	0.61	16	0.66
1.8	1.5	0.42	39	0.41
2.4	1.8	0.28	57	0.25

Notes:

1. Matching constraints may make F_{min} values associated with high $|\Gamma_{opt}|$ values unachievable in physical circuits. See Fig. 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

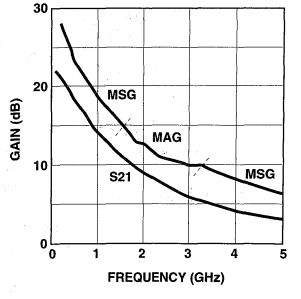


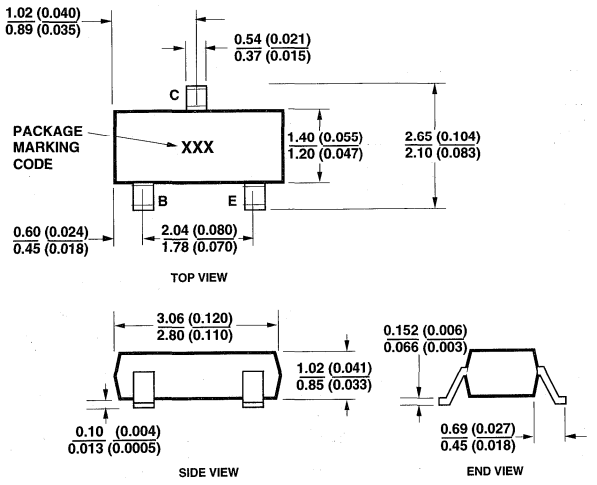
Figure 26. AT-30533 Gains vs. Frequency at V_{CE} = 5 V, I_C = 5 mA.

Ordering Information

Part Number	Increment	Comments
AT-30511-BLK	100	Bulk
AT-30511-TR1	3000	7" Reel
AT-30533-BLK	100	Bulk
AT-30533-TR1	3000	7" Reel

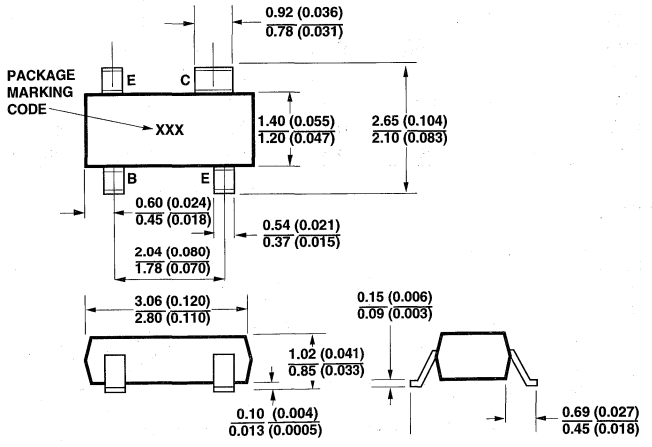
Package Dimensions

SOT-23 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

SOT-143 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Low Current, High Performance NPN Silicon Bipolar Transistor

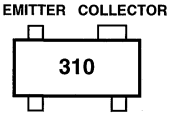
Technical Data

AT-31011
AT-31033

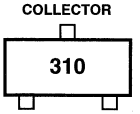
Features

- **High Performance Bipolar Transistor Optimized for Low Current, Low Voltage Operation**
- **900 MHz Performance:**
  AT-31011: 0.9 dB NF, 13 dB G_A
  AT-31033: 0.9 dB NF, 11 dB G_A
- **Characterized for End-Of-Life Battery Use (2.7 V)**
- **SOT-143 SMT Plastic Package**
- **Tape-And-Reel Packaging Option Available[1]**

Outline Drawing



SOT-143 (AT-31011)



SOT-23 (AT-31033)

Note:
1. Refer to "Tape-and-Reel Packaging for Semiconductor Devices"

Description

Hewlett-Packard's AT-31011 and AT-31033 are high performance NPN bipolar transistors that have been optimized for operation at low voltages, making them ideal for use in battery powered applications in wireless markets. The AT-31033 uses the 3 lead SOT-23, while the AT-31011 places the same die in the higher performance 4 lead SOT-143. Both packages are industry standards compatible with high volume surface mount assembly techniques.

The 3.2 micron emitter-to-emitter pitch and reduced parasitic design of these transistors yields extremely high performance products that can perform a multiplicity of tasks. The 10 emitter finger interdigitated geometry yields an extremely fast transistor with low operating currents and reasonable impedances.

Optimized performance at 2.7 V makes these devices ideal for use in 900 MHz, 1.9 GHz, and 2.4 GHz battery operated systems as an LNA, gain stage, buffer, oscillator, or active mixer. Applications include cellular and PCS handsets as well as Industrial-Scientific-Medical systems. Typical amplifier designs at 900 MHz yield 1.3 dB noise figures with 11 dB or more associated gain at a 2.7 V, 1 mA bias. Moderate output power capability (+9 dBm P_{1dB}) coupled with an excellent noise figure yields high dynamic range for a microcurrent device. High gain capability at 1 V, 1 mA makes these devices a good fit for 900 MHz pager applications.

The AT-3 series bipolar transistors are fabricated using an optimized version of Hewlett-Packard's 10 GHz f_T, 30 GHz f_{max} Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices.

5965-8919E

AT-31011, AT-31033 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	11
V_{CEO}	Collector-Emitter Voltage	V	5.5
I_C	Collector Current	mA	16
P_T	Power Dissipation[2,3]	mW	150
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{jc} = 550°C/W$

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{Mounting\ Surface} = 25°C$.
3. Derate at 1.82 mW/°C for $T_C > 67.5°C$.

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	AT-31011			AT-31033		
				Min	Typ	Max	Min	Typ	Max
NF	Noise Figure $V_{CE} = 2.7$ V, $I_C = 1$ mA	f = 0.9 GHz	dB		0.9[1]	1.2[1]		0.9[2]	1.2[2]
G_A	Associated Gain $V_{CE} = 2.7$ V, $I_C = 1$ mA	f = 0.9 GHz	dB	11[1]	13[1]		9[2]	11[2]	
h_{FE}	Forward Current Transfer Ratio	$V_{CE} = 2.7$ V $I_C = 1$ mA	-	70		300	70		300
I_{CBO}	Collector Cutoff Current	$V_{CB} = 3$ V	μA		0.05	0.2		0.05	0.2
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 1$ V	μA		0.1	1.5		0.1	1.5

Notes:
1. Test circuit B, Figure 1. Numbers reflect device performance de-embedded from circuit losses. Input loss = 0.4 dB; output loss = 0.4 dB.
2. Test circuit A, Figure 1. Numbers reflect device performance de-embedded from circuit losses. Input loss = 0.4 dB; output loss = 0.4 dB.

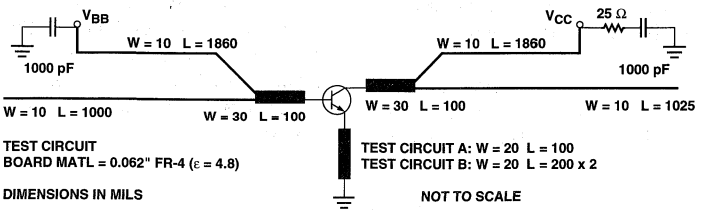


Figure 1. Test Circuit for Noise Figure and Associated Gain. This Circuit is a Compromise Match Between Best Noise Figure, Best Gain, Stability, a Practical, Synthesizable Match, and a Circuit Capable of Matching Both the AT-305 and AT-310 Geometries.

Characterization Information, T_A = 25° C

Symbol	Parameters and Test Conditions		Units	AT-31011 Typ	AT-31033 Typ
P_{1dB}	Power at 1 dB Gain Compression (opt tuning) V_{CE} = 2.7 V, I_C = 10 mA	f = 0.9 GHz	dBm	9	9
G_{1dB}	Gain at 1 dB Gain Compression (opt tuning) V_{CE} = 2.7 V, I_C = 10 mA	f = 0.9 GHz	dB	15	13
IP_3	Output Third Order Intercept Point, V_{CE} = 2.7 V, I_C = 10 mA (opt tuning)	f = 0.9 GHz	dBm	20	20
$\|S_{21}\|_E^2$	Gain in 50 Ω System; V_{CE} = 2.7 V, I_C = 1 mA	f = 0.9 GHz	dB	10	9
C_{CB}	Collector-Base Capacitance	V_{CB} = 3V, f = 1 MHz	pF	0.04	0.04

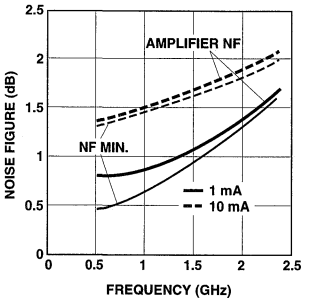


Figure 2. AT-31011 and AT-31033 Minimum Noise Figure and Amplifier NF[1] vs. Frequency and Current at V_{CE} = 2.7 V.

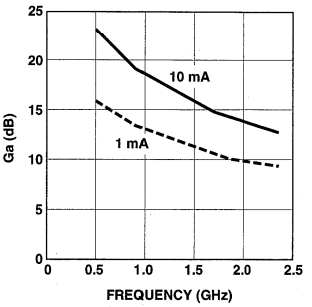


Figure 3. AT-31011 Associated Gain at Optimum Noise Match vs. Frequency and Current at V_{CE} = 2.7 V.

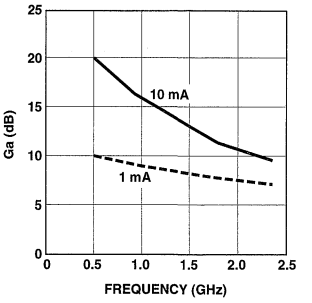


Figure 4. AT-33033 Associated Gain at Optimum Noise Match vs. Frequency and Current at V_{CE} = 2.7 V.

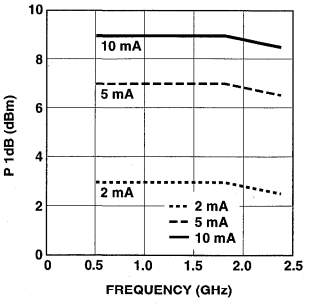


Figure 5. AT-31011 and AT-31033 Power at 1 dB Gain Compression vs. Frequency and Current at V_{CE} = 2.7 V.

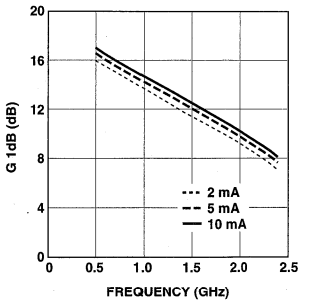


Figure 6. AT-31011 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 2.7 V.

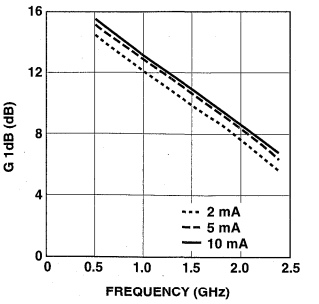


Figure 7. AT-33033 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 2.7 V.

Note:

1. Amplifier NF represents the noise figure which can be expected in a real circuit representing reasonable reflection coefficients and including circuit losses.

AT-31011, AT-31033 Typical Performance

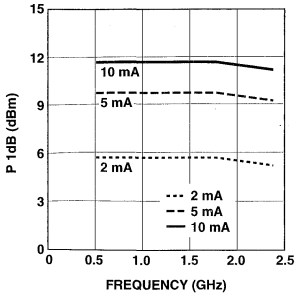


Figure 8. AT-31011 and AT-31033 Power at 1 dB Gain Compression vs. Frequency and Current at V_{CE} = 5 V.

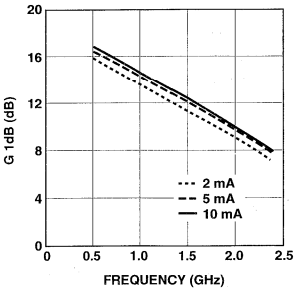


Figure 9. AT-31011 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 5 V.

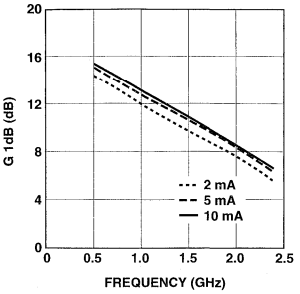


Figure 10. AT-31033 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 5 V.

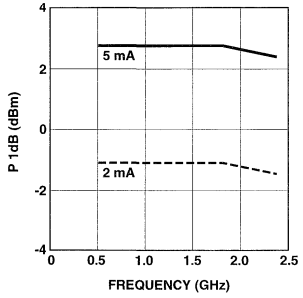


Figure 11. AT-31011 and AT-31033 Power at 1 dB Gain Compression vs. Frequency and Current at V_{CE} = 1 V.

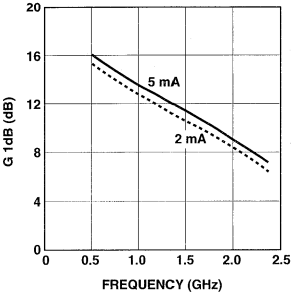


Figure 12. AT-31011 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 1 V.

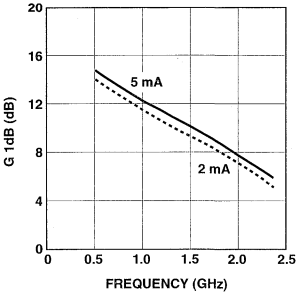


Figure 13. AT-33033 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 1 V.

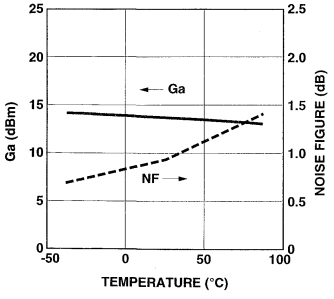


Figure 14. AT-31011 Noise Figure and Associated Gain at V_{CE} = 2.7 V, I_C = 1 mA vs. Temperature in Test Circuit, Figure 1. (Circuit Losses De-embedded)

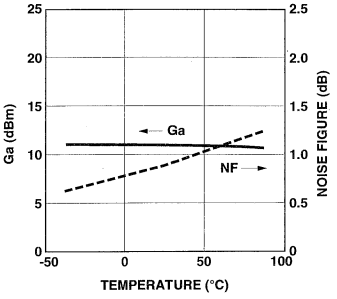


Figure 15. AT-31033 Noise Figure and Associated Gain at V_{CE} = 2.7 V, I_C = 1 mA vs. Temperature in Test Circuit, Figure 1. (Circuit Losses De-embedded)

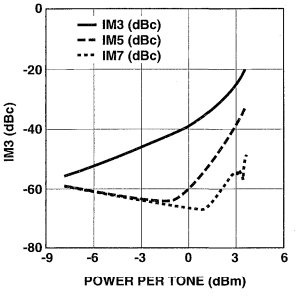


Figure 16. AT-31011 and AT-31033 Intermodulation Products vs. Output Power at V_{CE} = 2.7 V, I_C = 10 mA, 900 MHz with Optimal Tuning.

AT-31011 Typical Scattering Parameters, V_{CE} = 1 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.95	-8	11.12	3.60	174	-37.91	0.01	85	0.999	-3
0.5	0.92	-34	10.58	3.38	150	-24.67	0.06	68	0.94	-15
0.9	0.81	-60	9.74	3.07	130	-20.67	0.09	53	0.89	-25
1.0	0.79	-66	9.33	2.93	125	-20.03	0.10	50	0.88	-27
1.5	0.66	-94	8.02	2.52	104	-18.34	0.12	36	0.80	-36
1.8	0.60	-110	7.18	2.28	93	-17.95	0.13	30	0.76	-40
2.0	0.57	-119	6.76	2.18	87	-17.73	0.13	27	0.74	-42
2.4	0.51	-139	5.56	1.90	74	-17.69	0.13	22	0.71	-46
3.0	0.45	-167	4.22	1.63	57	-17.95	0.13	19	0.67	-51
4.0	0.45	153	2.30	1.30	36	-18.33	0.12	22	0.64	-62
5.0	0.49	120	0.73	1.09	17	-17.33	0.14	32	0.62	-72

AT-31011 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 1 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.5	0.90	13	0.85
0.9	0.6	0.85	29	0.73
1.8	1.1	0.68	67	0.46
2.4	1.6	0.55	98	0.28

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unachievable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

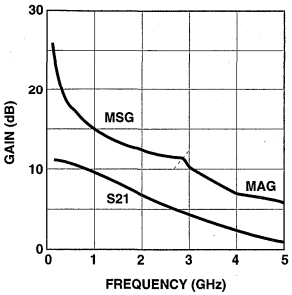


Figure 17. AT-31011 Gains vs. Frequency at V_{CE} = 1 V, I_C = 1 mA.

AT-31033 Typical Scattering Parameters, V_{CE} = 1 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.94	-7	11.16	3.61	173	-35.95	0.02	85	0.999	-3
0.5	0.87	-34	10.37	3.30	144	-22.84	0.07	68	0.92	-17
0.9	0.70	-58	9.17	2.87	121	-19.06	0.11	56	0.85	-27
1.0	0.66	-64	8.69	2.72	115	-18.49	0.12	53	0.83	-29
1.5	0.46	-90	7.11	2.27	92	-16.94	0.14	45	0.74	-37
1.8	0.36	-106	6.16	2.03	81	-16.40	0.15	43	0.70	-40
2.0	0.31	-117	5.66	1.92	74	-16.06	0.16	42	0.68	-42
2.4	0.22	-143	4.48	1.67	62	-15.50	0.17	42	0.66	-45
3.0	0.16	166	3.19	1.44	46	-14.34	0.19	44	0.63	-50
4.0	0.23	101	1.39	1.17	25	-11.85	0.26	46	0.60	-62
5.0	0.33	67	0.05	1.01	9	-9.11	0.35	41	0.56	-77

AT-31033 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 1 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.5	0.90	12	0.70
0.9	0.6	0.82	28	0.60
1.8	1.1	0.57	68	0.38
2.4	1.6	0.41	100	0.22

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unachievable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

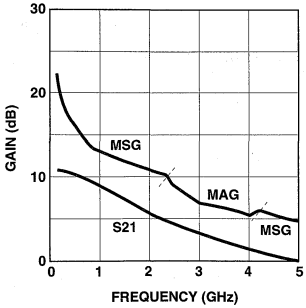


Figure 18. AT-31033 Gains vs. Frequency at V_{CE} = 1 V, I_C = 1 mA.

AT-31011 Typical Scattering Parameters, V_{CE} = 2.7 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.96	-7	11.11	3.59	174	-39.92	0.01	86	0.999	-2
0.5	0.93	-32	10.66	3.41	152	-26.43	0.05	69	0.95	-13
0.9	0.83	-56	9.90	3.13	132	-22.32	0.08	55	0.91	-22
1.0	0.81	-61	9.53	2.99	128	-21.66	0.08	53	0.90	-24
1.5	0.68	-89	8.32	2.61	107	-19.90	0.10	40	0.84	-32
1.8	0.62	-104	7.52	2.38	96	-19.46	0.11	34	0.80	-36
2.0	0.58	-113	7.15	2.28	90	-19.24	0.11	31	0.78	-38
2.4	0.52	-133	5.98	1.99	77	-19.15	0.11	27	0.75	-42
3.0	0.45	-160	4.65	1.71	61	-19.37	0.11	25	0.72	-46
4.0	0.43	158	2.75	1.37	39	-19.60	0.10	29	0.69	-56
5.0	0.46	123	1.16	1.14	20	-18.16	0.12	41	0.68	-66

AT-31011 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 2.7 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.5	0.92	13	0.85
0.9	0.6	0.85	29	0.73
1.8	1.1	0.68	67	0.46
2.4	1.6	0.55	98	0.28

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unachievable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

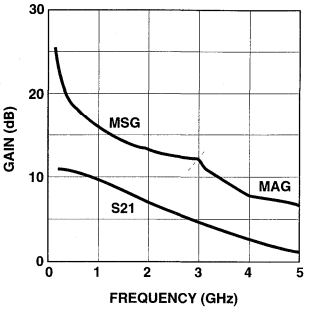


Figure 19. AT-31011 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 1 mA.

AT-31033 Typical Scattering Parameters, V_{CE} = 2.7 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.94	-7	11.07	3.58	173	-37.44	0.01	86	0.999	-3
0.5	0.89	-32	10.35	3.29	146	-24.11	0.06	70	0.94	-15
0.9	0.72	-54	9.27	2.91	123	-20.27	0.10	58	0.87	-25
1.0	0.69	-59	8.80	2.76	118	-19.65	0.10	56	0.86	-26
1.5	0.48	-83	7.32	2.32	95	-18.01	0.13	48	0.78	-33
1.8	0.38	-97	6.39	2.09	84	-17.43	0.13	46	0.74	-36
2.0	0.33	-107	5.91	1.97	77	-17.07	0.14	45	0.72	-38
2.4	0.23	-130	4.73	1.72	65	-16.46	0.15	46	0.70	-41
3.0	0.14	-178	3.43	1.48	49	-15.25	0.17	48	0.67	-46
4.0	0.19	103	1.62	1.21	28	-12.62	0.23	51	0.65	-57
5.0	0.30	67	0.25	1.03	12	-9.72	0.33	47	0.63	-71

AT-31033 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 2.7 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.5	0.90	12	0.70
0.9	0.6	0.82	28	0.60
1.8	1.1	0.57	68	0.38
2.4	1.6	0.41	100	0.22

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unachievable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

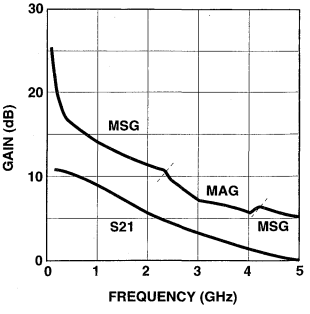


Figure 20. AT-31033 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 1 mA.

AT-31011 Typical Scattering Parameters, V_{CE} = 2.7 V, I_C = 10 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.74	-23	27.42	23.49	161	-41.00	0.01	77	0.95	-9
0.5	0.46	-85	22.65	13.57	116	-30.64	0.03	59	0.68	-24
0.9	0.32	-121	18.73	8.64	97	-27.55	0.04	59	0.59	-27
1.0	0.30	-128	17.91	7.86	93	-27.05	0.04	59	0.58	-27
1.5	0.25	-161	14.77	5.48	79	-24.48	0.06	61	0.55	-30
1.8	0.25	-177	13.29	4.62	72	-23.26	0.07	61	0.54	-32
2.0	0.24	174	12.42	4.18	68	-22.51	0.07	61	0.53	-33
2.4	0.25	157	10.97	3.54	60	-21.12	0.09	59	0.53	-36
3.0	0.27	138	9.11	2.86	49	-19.31	0.11	58	0.52	-40
4.0	0.31	113	6.86	2.20	33	-16.88	0.14	54	0.51	-50
5.0	0.37	94	5.19	1.82	17	-14.75	0.18	48	0.50	-59

AT-31011 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 2.7 V, I_C = 10 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	1.3	0.45	11	0.55
0.9	1.4	0.37	33	0.46
1.8	1.7	0.25	86	0.29
2.4	2.0	0.18	129	0.18

Notes:

1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unachievable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

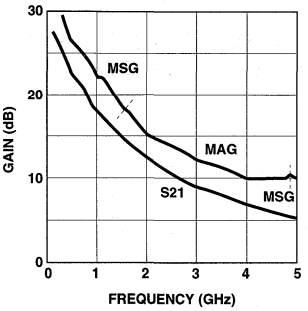


Figure 21. AT-31011 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 10 mA.

AT-31033 Typical Scattering Parameters, V_{CE} = 2.7 V, I_C = 10 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.72	-21	26.80	21.87	154	-38.46	0.01	80	0.92	-10
0.5	0.33	-49	19.93	9.92	106	-27.31	0.04	73	0.66	-20
0.9	0.19	-47	15.51	5.96	88	-22.90	0.07	72	0.61	-22
1.0	0.17	-46	14.66	5.41	85	-22.03	0.08	72	0.60	-23
1.5	0.11	-28	11.44	3.73	72	-18.74	0.12	69	0.59	-27
1.8	0.10	-14	9.99	3.16	66	-17.26	0.14	67	0.58	-30
2.0	0.10	-6	9.15	2.87	62	-16.40	0.15	65	0.58	-32
2.4	0.10	9	7.78	2.45	54	-14.88	0.18	62	0.57	-35
3.0	0.12	23	6.16	2.03	43	-12.99	0.22	57	0.55	-41
4.0	0.15	34	4.30	1.64	27	-10.49	0.30	48	0.52	-53
5.0	0.20	36	3.01	1.41	12	-8.53	0.37	38	0.48	-65

AT-31033 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 2.7 V, I_C = 10 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	1.3	0.42	10	0.38
0.9	1.4	0.31	30	0.34
1.8	1.7	0.16	80	0.23
2.4	2.0	0.08	118	0.17

Notes:

1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unachievable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

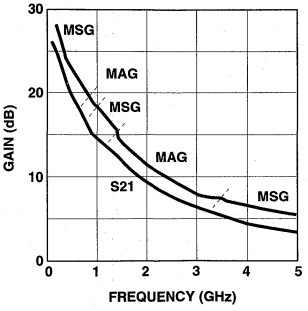


Figure 22. AT-31033 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 10 mA.

AT-31011 Typical Scattering Parameters, V_{CE} = 5 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.96	-7	11.10	3.59	174	-40.35	0.01	84	0.999	-2
0.5	0.94	-31	10.67	3.41	153	-26.95	0.04	69	0.96	-13
0.9	0.83	-54	9.93	3.14	133	-22.80	0.07	56	0.92	-22
1.0	0.81	-60	9.57	3.01	129	-22.18	0.08	53	0.91	-23
1.5	0.68	-86	8.41	2.63	108	-20.33	0.10	41	0.85	-31
1.8	0.62	-101	7.62	2.40	97	-19.85	0.10	35	0.81	-35
2.0	0.58	-110	7.27	2.31	91	-19.64	0.10	32	0.79	-37
2.4	0.52	-129	6.10	2.02	78	-19.50	0.11	28	0.76	-41
3.0	0.44	-157	4.78	1.73	62	-19.68	0.10	26	0.73	-45
4.0	0.42	161	2.90	1.40	40	-19.86	0.10	31	0.70	-55
5.0	0.45	125	1.33	1.17	21	-18.35	0.12	43	0.70	-65

AT-31011 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 5 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.5	0.92	13	0.85
0.9	0.6	0.85	29	0.73
1.8	1.1	0.68	67	0.46
2.4	1.6	0.55	98	0.28

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unachievable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

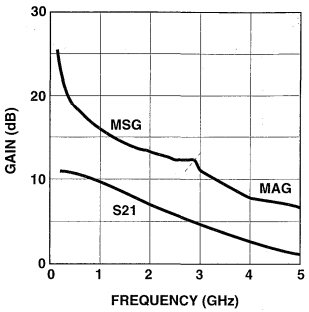


Figure 23. AT-31011 Gains vs. Frequency at V_{CE} = 5 V, I_C = 1 mA.

AT-31033 Typical Scattering Parameters, V_{CE} = 5 V, I_C = 1 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.95	-7	10.93	3.52	173	-37.78	0.01	85	0.999	-3
0.5	0.89	-31	10.24	3.25	147	-24.43	0.06	70	0.94	-15
0.9	0.73	-52	9.20	2.88	124	-20.49	0.09	59	0.88	-24
1.0	0.70	-57	8.75	2.74	119	-19.91	0.10	57	0.87	-26
1.5	0.49	-80	7.30	2.32	96	-18.15	0.12	49	0.79	-32
1.8	0.39	-93	6.41	2.09	85	-17.54	0.13	47	0.75	-36
2.0	0.34	-102	5.93	1.98	78	-17.19	0.14	46	0.73	-37
2.4	0.23	-122	4.77	1.73	66	-16.55	0.15	46	0.71	-40
3.0	0.13	-166	3.49	1.49	50	-15.35	0.17	49	0.68	-45
4.0	0.17	107	1.71	1.22	29	-12.83	0.23	51	0.66	-56
5.0	0.28	68	0.32	1.04	12	-9.96	0.32	48	0.64	-69

AT-31033 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 5 V, I_C = 1 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	0.5	0.90	12	0.70
0.9	0.6	0.82	28	0.60
1.8	1.1	0.57	68	0.38
2.4	1.6	0.41	100	0.22

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unachievable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

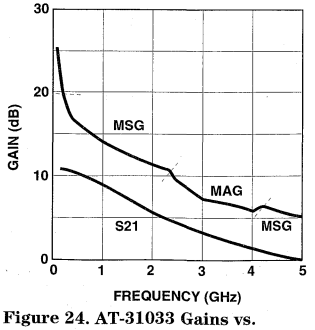


Figure 24. AT-31033 Gains vs. Frequency at V_{CE} = 5 V, I_C = 1 mA.

AT-31011 Typical Scattering Parameters, V_{CE} = 5 V, I_C = 10 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.77	-21	27.41	23.46	162	-41.49	0.01	80	0.95	-8
0.5	0.48	-77	22.97	14.07	118	-30.66	0.03	61	0.70	-24
0.9	0.32	-112	19.14	9.06	98	-27.77	0.04	59	0.61	-27
1.0	0.30	-119	18.34	8.26	95	-27.11	0.04	60	0.59	-27
1.5	0.23	-151	15.23	5.78	80	-24.56	0.06	60	0.56	-29
1.8	0.22	-168	13.75	4.87	73	-23.37	0.07	60	0.55	-31
2.0	0.21	-178	12.91	4.42	69	-22.62	0.07	60	0.55	-32
2.4	0.21	163	11.46	3.74	61	-21.25	0.09	59	0.54	-36
3.0	0.23	142	9.60	3.02	50	-19.45	0.11	58	0.53	-39
4.0	0.27	116	7.36	2.33	34	-17.08	0.14	54	0.52	-48
5.0	0.33	96	5.70	1.93	19	-14.97	0.18	48	0.51	-58

AT-31011 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 5 V, I_C = 10 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n
0.5[2]	1.3	0.45	11	0.55
0.9	1.4	0.37	33	0.46
1.8	1.7	0.25	86	0.29
2.4	2.0	0.18	129	0.18

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unachievable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

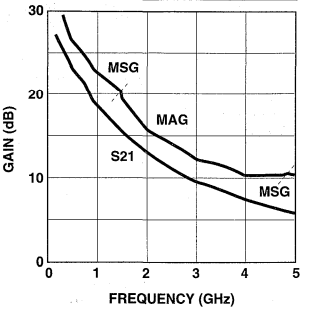


Figure 25. AT-31011 Gains vs. Frequency at V_{CE} = 5 V, I_C = 10 mA.

AT-31033 Typical Scattering Parameters, V_{CE} = 5 V, I_C = 10 mA, Common Emitter, Z_O = 50 Ω

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	0.75	-19	26.79	21.84	155	-38.82	0.01	79	0.92	-10
0.5	0.37	-45	20.17	10.20	107	-27.39	0.04	73	0.67	-20
0.9	0.23	-42	15.79	6.16	90	-23.00	0.07	72	0.62	-22
1.0	0.21	-42	14.94	5.58	86	-22.11	0.08	72	0.61	-23
1.5	0.15	-30	11.75	3.87	73	-18.86	0.11	69	0.60	-27
1.8	0.14	-21	10.30	3.27	67	-17.37	0.14	66	0.59	-29
2.0	0.13	-17	9.47	2.97	63	-16.51	0.15	65	0.58	-31
2.4	0.13	-7	8.08	2.54	55	-15.00	0.18	62	0.57	-35
3.0	0.13	3	6.47	2.11	45	-13.14	0.22	57	0.56	-41
4.0	0.14	19	4.61	1.7	29	-10.67	0.29	48	0.53	-52
5.0	0.18	28	3.33	1.47	14	-8.73	0.37	38	0.49	-64

AT-31033 Typical Noise Parameters,

Common Emitter, Z_O = 50 Ω, 5 V, I_C = 10 mA

Freq GHz	F_{min}[1] dB	Γ_{OPT} Mag	Γ_{OPT} Ang	R_n -
0.5[2]	1.3	0.42	10	0.38
0.9	1.4	0.31	30	0.34
1.8	1.7	0.16	80	0.23
2.4	2.0	0.08	118	0.17

Notes:
1. Matching constraints may make F_{min} values associated with high $|\Gamma_{OPT}|$ values unacheivable in physical circuits. See Figure 2 for expected performance.
2. 0.5 GHz noise parameter values are extrapolated, not measured.

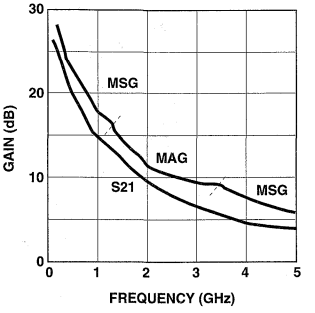


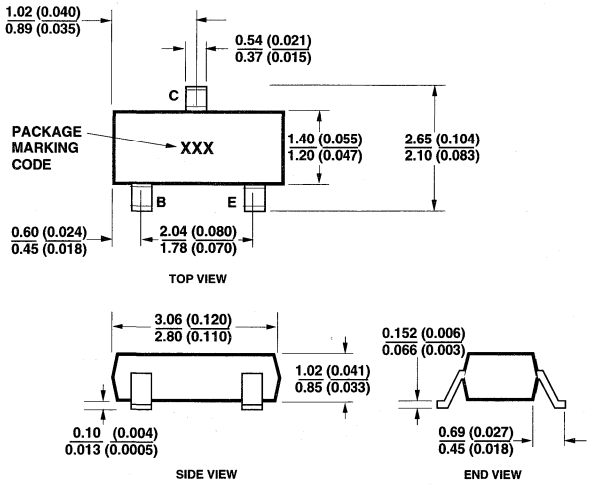
Figure 26. AT-31033 Gains vs. Frequency at V_{CE} = 5 V, I_C = 10 mA.

Ordering Information

Part Number	Increment	Comments
AT-31011-BLK	100	Bulk
AT-31011-TR1	3000	7" Reel
AT-31033-BLK	100	Bulk
AT-31033-TR1	3000	7" Reel

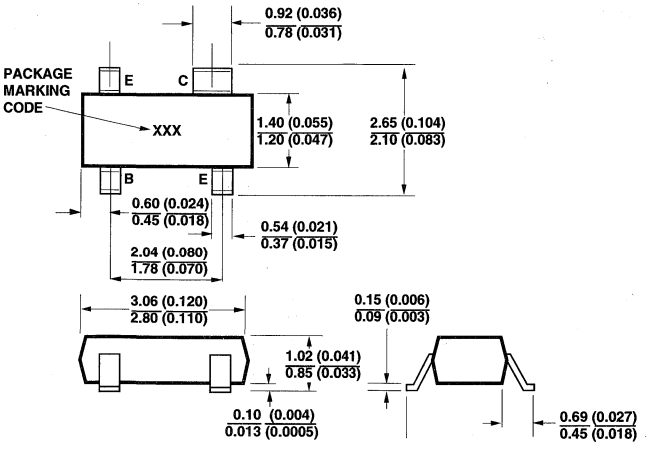
Package Dimensions

SOT-23 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

SOT-143 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

4.8 V NPN Common Emitter Medium Power Output Transistor

Technical Data

AT-31625

Features

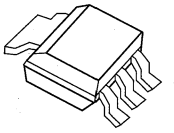
- **4.8 Volt Operation**
- **+28.0 dBm P_{out} @ 900 MHz, Typ.**
- **70% Collector Efficiency @ 900 MHz, Typ.**
- **9 dB Power Gain @ 900 MHz, Typ.**
- **-31 dBc IMD_3 @ P_{out} of 21 dBm per Tone, 900 MHz, Typ.**
- **50% Smaller than SOT-223 Package**

Applications

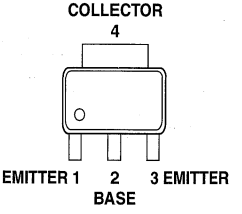
- **Medium Power Driver Device for Cellular/PCS, ISM 900, WLAN**
- **Output Power Device for ISM 900, Cordless, WLAN**

MSOP-3 Surface Mount Plastic Package

Outline 25



Pin Configuration



Description

Hewlett Packard's AT-31625 is a low cost, NPN medium power silicon bipolar junction transistor housed in a miniature, MSOP-3 surface mount plastic package. The AT-31625 can be used as a driver device or an output device, depending on the specific application. The AT-31625 features +28 dBm CW output power when operated at 4.8 volts. Excellent gain and superior efficiency make the AT-31625 ideal for use in battery powered systems.

The AT-31625 is fabricated with Hewlett Packard's 10 GHz F_t Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices.

5965-5911E

AT-31625 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.4
V_{CBO}	Collector-Base Voltage	V	16.0
V_{CEO}	Collector-Emitter Voltage	V	9.5
I_C	Collector Current	mA	320
P_T	Power Dissipation[2]	W	1.0
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[3]:
$\theta_{jc} = 65°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. Derate at 15.4 mW/°C for $T_c > 85°C$. T_c is defined to be the temperature of the collector pin 4, where the lead contacts the circuit board.
3. Using the liquid crystal technique, $V_{CE} = 4.8$ V, $I_c = 50$ mA, $T_j = 150°C$, 1-2 μm "hot-spot" resolution.

Electrical Specifications, $T_C = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
	Freq. = 900 MHz, $V_{CE} = 4.8$ V, $I_{CQ} = 5$ mA, CW operation, Test Circuit A, unless otherwise specified					
P_{out}	Output Power[1]	$P_{in} = +19$ dBm	dBm	+27.0	+28.0	
η_C	Collector Efficiency[1]	$P_{in} = +19$ dBm	%	55	70	
IMD_3	3rd Order Intermodulation Distortion, 2 Tone Test, P_{out} each Tone = +21 dBm[1]	F1 = 899 MHz F2 = 901 MHz	dBc		-31	
	Mismatch Tolerance, No Damage[1]	$P_{out} = +28$ dBm any phase, 2 sec duration				7:1
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = 0.2$ mA, open collector	V	1.4		
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = 1.0$ mA, open emitter	V	16.0		
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = 5.0$ mA, open base	V	9.5		
h_{FE}	Forward Current Transfer Ratio	$V_{CE} = 3$ V, $I_C = 180$ mA	—	80	150	330
I_{CEO}	Collector Leakage Current	$V_{CEO} = 5$ V	μA			15

Note:
1. With external matching on input and output, tested in a 50 ohm environment. Refer to Test Circuit A.

AT-31625 Typical Performance, T_C = 25°C

Frequency = 900 MHz, V_{CE} = 4.8 V, I_{CQ} = 5 mA, CW operation, Test Circuit A, unless otherwise specified.

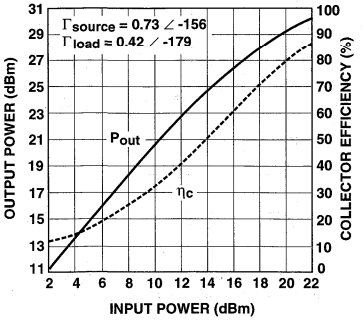


Figure 1. Output Power and Collector Efficiency vs. Input Power.

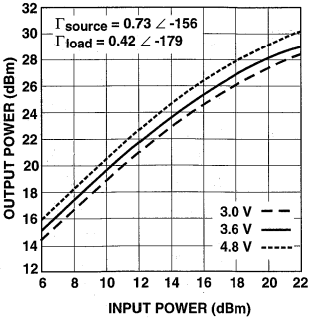


Figure 2. Output Power vs. Input Power Over Bias Voltage.

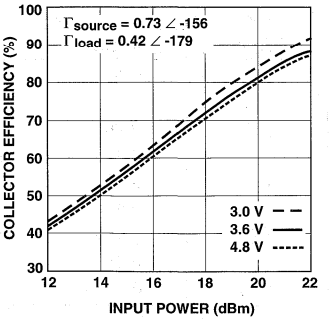


Figure 3. Collector Efficiency vs. Input Power Over Bias Voltage.

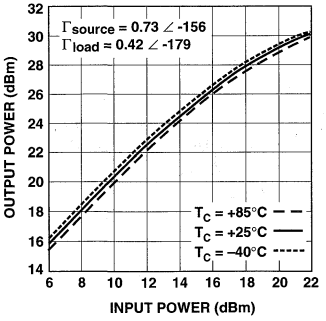


Figure 4. Output Power vs. Input Power Over Temperature.

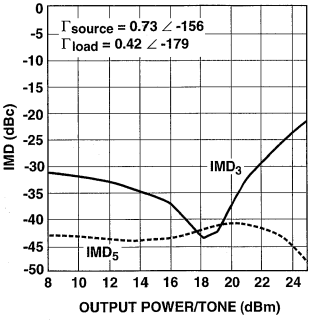


Figure 5. IMD_3, IMD_5 vs. Output Power Per Tone.

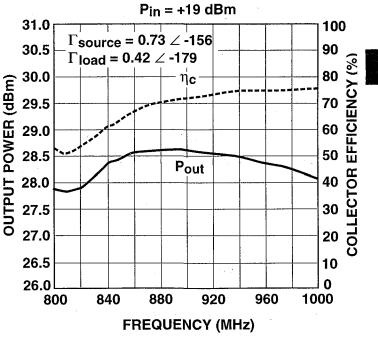


Figure 6. Output Power and Collector Efficiency vs. Frequency.
Note: Tuned at 900 MHz, then Swept over Frequency.

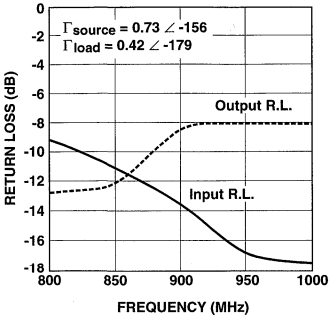


Figure 7. Input and Output Return Loss vs. Frequency.

AT-31625 Typical Large Signal Impedances

V_{CE} = 4.8 V, I_{CQ} = 5 mA, P_{out} = +28.0 dBm

Freq. MHz	Γ source		Γ load	
	Mag.	Ang.	Mag.	Ang.
800	0.661	-149.0	0.382	-171.3
825	0.679	-150.6	0.394	-172.8
850	0.697	-152.4	0.403	-174.6
875	0.712	-154.2	0.412	-176.5
900	0.727	-155.8	0.422	-179.0
925	0.740	-157.5	0.426	179.3
950	0.754	-159.0	0.432	177.2
975	0.767	-160.4	0.437	174.9
1000	0.777	-162.1	0.438	172.5

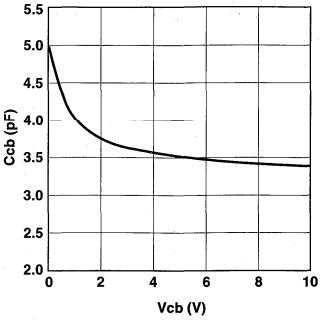
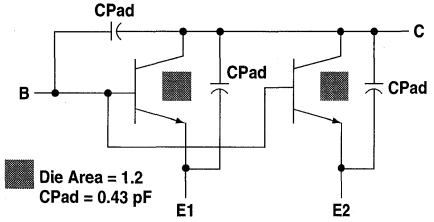


Figure 8. Collector-Base Capacitance vs. Collector-Base Voltage (DC Test).

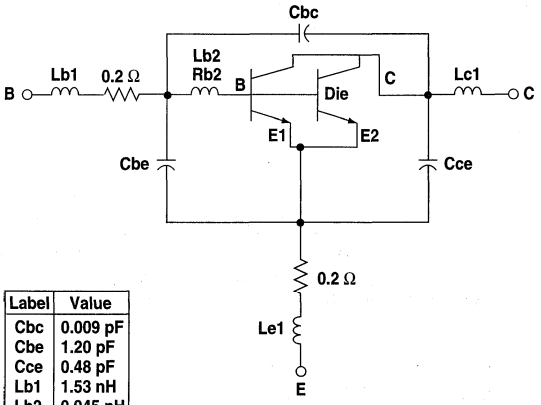
SPICE Model Parameters

Die Model



Label	Value	Label	Value
BF	150	TR	1E-9
IKF	299.9	EG	1.11
ISE	9.9E-11	IS	3.598E-15
NE	2.399	XTI	3
VAF	33.16	CJC	1.4E-12
NF	0.9935	VJC	0.4776
TF	1.6E-11	MJC	0.2508
XTF	0.006656	XCJC	0.001
VTF	0.02785	FC	0.999
ITF	0.001	CJE	5.06E-12
PTF	23	VJE	1.148
XTB	0	MJE	0.5965
BR	54.61	RB	0.752
IKR	81	IRB	0
ISC	8.7E-13	RBM	0.01
NC	1.587	RE	2.488
VAR	1.511	RC	1.288
NR	0.9886		

Packaged Model



Label	Value
Cbc	0.009 pF
Cbe	1.20 pF
Cce	0.48 pF
Lb1	1.53 nH
Lb2	0.045 nH
Rb2	0.1 Ω
Le1	0.38 nH
Lc1	0.47 nH

AT-31625 Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$

V_{CE} = 3.0 V, I_c = 200 mA, T_c = 25°C

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.05	0.72	-150	30.7	34.19	113	-34.0	0.02	40	0.56	-120
0.10	0.77	-166	25.3	18.43	99	-34.0	0.02	42	0.52	-148
0.25	0.79	179	17.5	7.54	86	-28.0	0.04	57	0.51	-169
0.50	0.79	169	11.6	3.81	74	-23.1	0.07	64	0.51	-178
0.75	0.79	161	8.2	2.58	65	-20.9	0.09	63	0.52	177
0.90	0.79	156	6.7	2.17	59	-19.2	0.11	62	0.52	175
1.00	0.79	153	5.9	1.97	56	-18.4	0.12	61	0.52	174
1.25	0.79	146	4.1	1.61	48	-16.5	0.15	58	0.53	170
1.50	0.79	140	2.7	1.37	40	-14.9	0.18	54	0.54	167
1.75	0.79	133	1.7	1.21	32	-13.6	0.21	49	0.54	164
2.00	0.79	126	0.7	1.09	26	-12.8	0.23	45	0.55	160
2.25	0.79	120	0.0	1.00	19	-11.7	0.26	41	0.55	156
2.50	0.79	114	-0.6	0.93	13	-11.1	0.28	36	0.56	152
V_{CE} = 3.6 V, I_c = 200 mA, T_c = 25°C										
0.05	0.71	-148	31.2	36.39	114	-34.0	0.02	41	0.56	-117
0.10	0.76	-165	25.9	19.69	100	-34.0	0.02	43	0.51	-146
0.25	0.78	180	18.1	8.06	86	-28.0	0.04	57	0.50	-168
0.50	0.78	169	12.2	4.07	75	-24.4	0.06	64	0.50	-177
0.75	0.78	161	8.8	2.75	65	-20.9	0.09	64	0.51	178
0.90	0.78	156	7.3	2.31	60	-19.2	0.11	62	0.51	176
1.00	0.78	153	6.4	2.10	56	-18.4	0.12	61	0.51	174
1.25	0.78	146	4.7	1.71	48	-16.5	0.15	58	0.52	171
1.50	0.78	140	3.3	1.46	40	-14.9	0.18	54	0.53	168
1.75	0.78	133	2.1	1.28	33	-14.0	0.20	50	0.54	164
2.00	0.78	127	1.3	1.16	26	-12.8	0.23	46	0.54	161
2.25	0.78	121	0.4	1.05	19	-11.7	0.26	41	0.55	157
2.50	0.78	115	-0.2	0.98	13	-11.1	0.28	37	0.55	153
V_{CE} = 4.8 V, I_c = 200 mA, T_c = 25°C										
0.05	0.70	-145	31.7	38.47	115	-34.0	0.02	41	0.56	-114
0.10	0.75	-164	26.4	20.90	100	-34.0	0.02	43	0.50	-144
0.25	0.77	-180	18.7	8.57	87	-28.0	0.04	57	0.49	-167
0.50	0.77	169	12.7	4.33	75	-24.4	0.06	64	0.49	-176
0.75	0.77	161	9.3	2.92	66	-20.9	0.09	64	0.49	179
0.90	0.77	157	7.8	2.45	60	-19.2	0.11	62	0.50	176
1.00	0.77	154	7.0	2.23	57	-18.4	0.12	61	0.50	175
1.25	0.77	147	5.2	1.81	48	-16.5	0.15	58	0.51	172
1.50	0.77	140	3.8	1.54	41	-14.9	0.18	54	0.51	168
1.75	0.77	134	2.6	1.35	33	-14.0	0.20	50	0.52	165
2.00	0.77	127	1.7	1.22	27	-12.8	0.23	46	0.53	162
2.25	0.77	121	0.9	1.11	20	-12.0	0.25	41	0.54	158
2.50	0.77	115	0.3	1.03	13	-11.1	0.28	37	0.54	154

Typical Performance

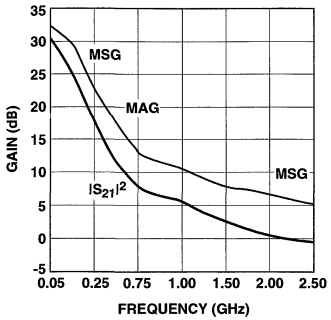


Figure 9. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{CE} = 3.0 V, I_c = 200 mA.

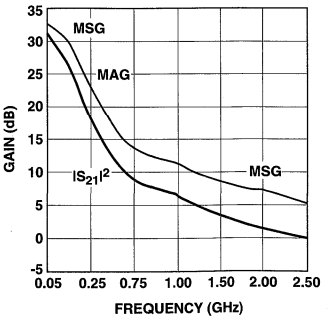


Figure 10. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{CE} = 3.6 V, I_c = 200 mA.

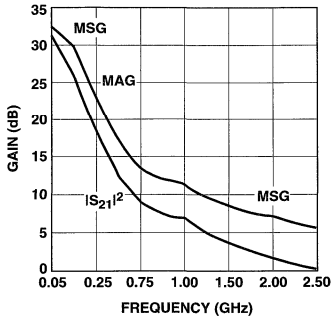


Figure 11. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{CE} = 4.8 V, I_c = 200 mA.

AT-31625 Typical Performance, T_C = 25°C

Frequency = 1800 MHz, V_{CE} = 4.8 V, I_{CQ} = 15 mA, CW operation, Test Circuit B, unless otherwise specified.

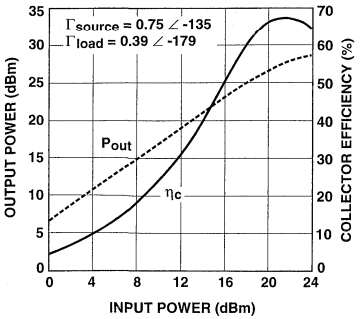


Figure 12. Output Power and Collector Efficiency vs. Input Power.

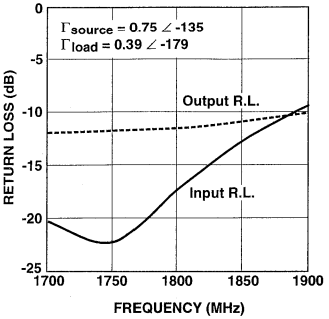


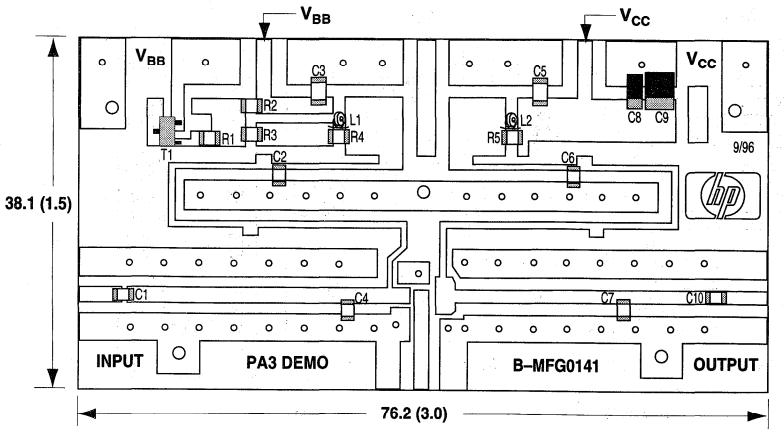
Figure 13. Input and Output Return Loss vs. Frequency.

AT-31625 Typical Large Signal Impedances

V_{CE} = 4.8 V, I_{CQ} = 15 mA, P_{out} = +25.0 dBm

Freq.	Γ source		Γ load	
MHz	Mag.	Ang.	Mag.	Ang.
1700	0.717	-131.8	0.373	-174.3
1725	0.724	-132.6	0.378	-175.6
1750	0.732	-133.4	0.381	-176.7
1775	0.743	-134.3	0.386	-177.9
1800	0.752	-135.4	0.390	-179.1
1825	0.763	-136.3	0.394	179.5
1850	0.773	-137.0	0.397	178.4
1875	0.780	-137.8	0.401	177.1
1900	0.788	-138.7	0.403	175.7

Test Circuit A: Test Circuit Board Layout @ 900 MHz

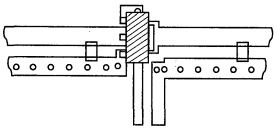


C1	100.0 pF
C2	100.0 pF
C3	100.0 nF
C4	6.8 pF
C5	100.0 nF
C6	100.0 pF
C7	2.7 pF
C8	1.5 µF
C9	10.0 µF
C10	100.0 pF
R1	2.2 Ω
R2	750.0 Ω
R3	2.2 Ω
R4	10.0 Ω
R5	10.0 Ω
T1	MBT 2222A
L1	18.0 µH
L2	18.0 µH

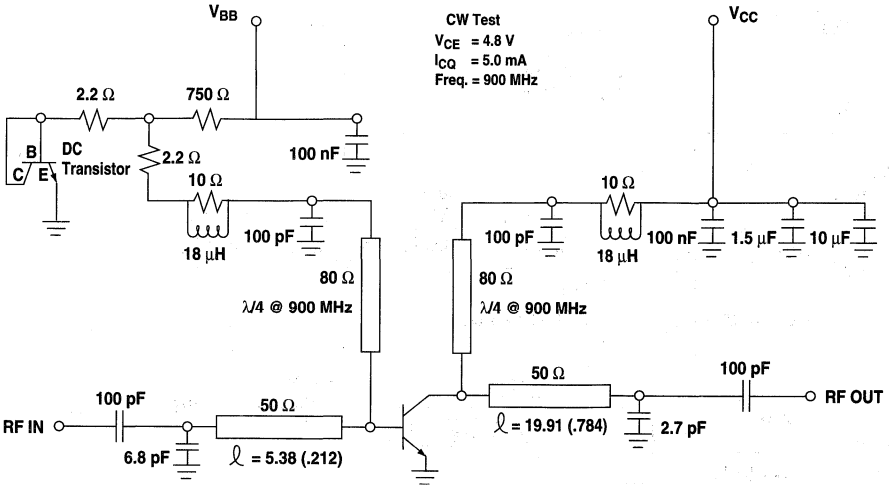
CW Test
V_{CE} = 4.8 V
I_{CQ} = 5.0 mA
Freq. = 900 MHz

Test Circuit:
FR-4 Microstrip, glass epoxy board
Dielectric Constant = 4.5
Thickness = 0.79 (.031)

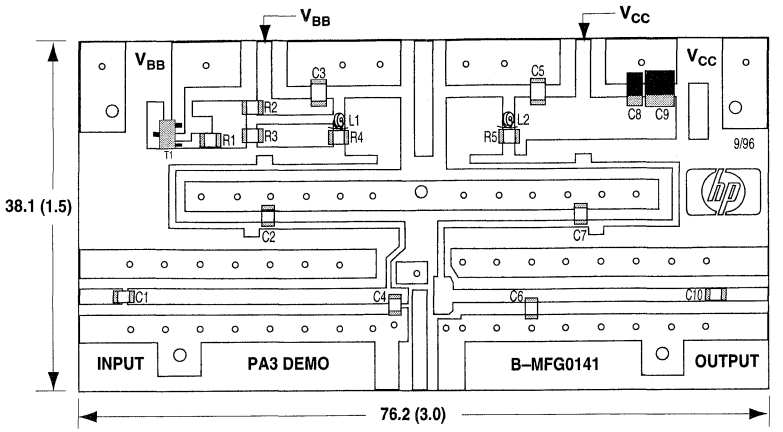
NOTE:
Dimensions are shown in millimeters (inches).



Test Circuit A: Test Circuit Schematic Diagram @ 900 MHz



Test Circuit B: Test Circuit Board Layout @ 1800 MHz

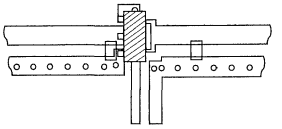


C1	100.0 pF
C2	100.0 pF
C3	100.0 nF
C4	3.0 pF
C5	100.0 nF
C6	1.4 pF
C7	100.0 pF
C8	1.5 µF
C9	10.0 µF
C10	100.0 pF
R1	2.2 Ω
R2	350.0 Ω
R3	2.2 Ω
R4	10.0 Ω
R5	10.0 Ω
T1	MBT 2222A
L1	18.0 µH
L2	18.0 µH

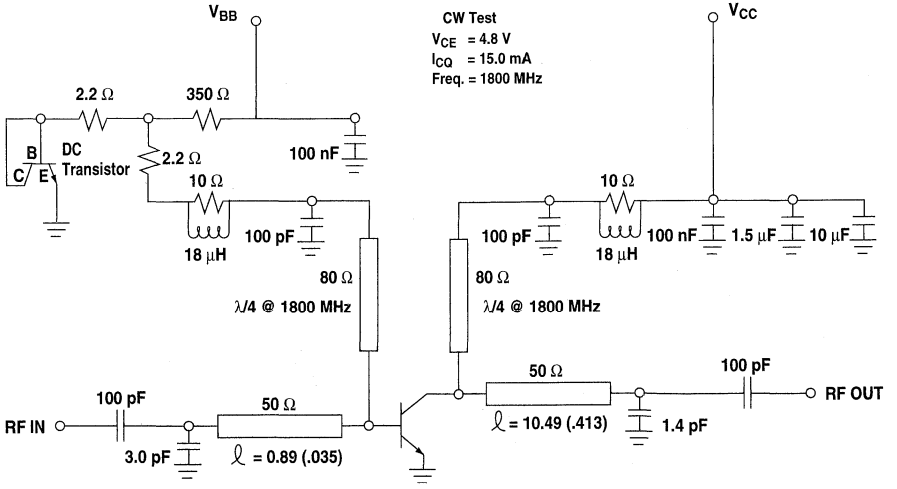
CW Test
V_{CE} = 4.8 V
I_{CQ} = 15.0 mA
Freq. = 1800 MHz

Test Circuit:
FR-4 Microstrip, glass epoxy board
Dielectric Constant = 4.5
Thickness = 0.79 (.031)

NOTE:
Dimensions are shown in millimeters (inches).



Test Circuit B: Test Circuit Schematic Diagram @ 1800 MHz

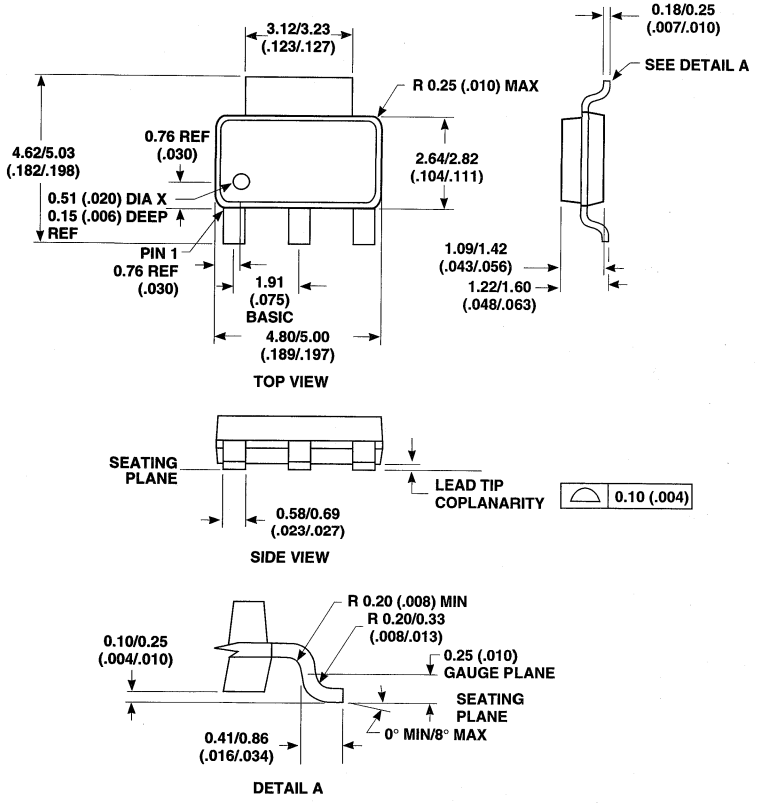


Part Number Ordering Information

Part Number	No. of Devices	Container
AT-31625-TR1	1000	7" Reel
AT-31625-BLK	25	Carrier Tape

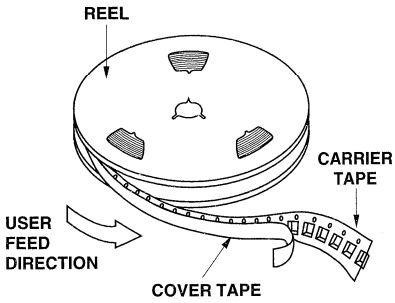
Package Dimensions

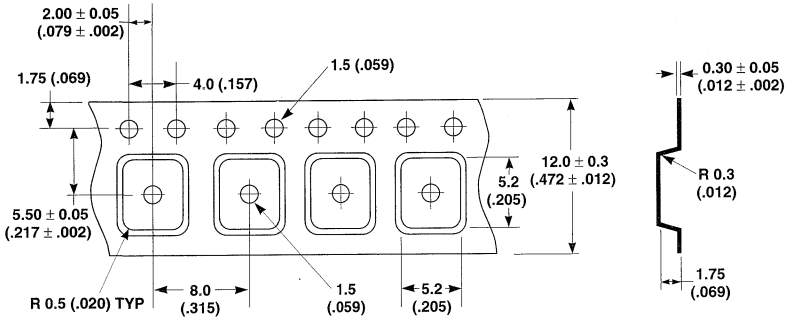
MSOP-3 Surface Mount Plastic Package



NOTE:
DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)

Tape Dimensions and Product Orientation for Package MSOP-3





NOTES:
1. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. TOLERANCES: .X ± 0.1 (.XXX ± .004)

HEWLETT® PACKARD

Low Current, High Performance NPN Silicon Bipolar Transistor

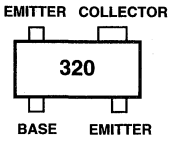
Technical Data

AT-32011
AT-32033

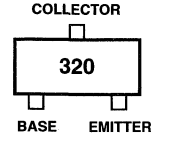
Features

- **High Performance Bipolar Transistor Optimized for Low Current, Low Voltage Operation**
- **900 MHz Performance:**
  AT-32011: 1 dB NF, 14 dB G_A
  AT-32033: 1 dB NF, 12.5 dB G_A
- **Characterized for End-Of-Life Battery Use (2.7 V)**
- **SOT-23 and SOT-143 SMT Plastic Packages**
- **Tape-And-Reel Packaging Option Available[1]**

Outline Drawing



SOT-143 (AT-32011)



SOT-23 (AT-32033)

Description

Hewlett Packard's AT-32011 and AT-32033 are high performance NPN bipolar transistors that have been optimized for maximum f_t at low voltage operation, making them ideal for use in battery powered applications in wireless markets. The AT-32033 uses the 3 lead SOT-23, while the AT-32011 places the same die in the higher performance 4 lead SOT-143. Both packages are industry standard, and compatible with high volume surface mount assembly techniques.

The 3.2 micron emitter-to-emitter pitch and reduced parasitic design of these transistors yields extremely high performance products that can perform a multiplicity of tasks. The 20 emitter finger interdigitated geometry yields an easy to match to and extremely fast transistor with moderate power, low noise resistance, and low operating currents.

Optimized performance at 2.7 V makes these devices ideal for use in 900 MHz, 1.8 GHz, and 2.4 GHz battery operated systems as an LNA, gain stage, buffer, oscillator, or active mixer. Typical amplifier designs at 900 MHz yield 1.2 dB noise figures with 12 dB or more associated gain at a 2.7 V, 2 mA bias, with noise performance being relatively insensitive to input match. High gain capability at 1 V, 1 mA makes these devices a good fit for 900 MHz pager applications. Voltage breakdowns are high enough for use at 5 volts.

The AT-3 series bipolar transistors are fabricated using an optimized version of Hewlett Packard's 10 GHz f_t, 30 GHz f_{MAX} Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices.

Note:
1. Refer to "Tape-and-Reel Packaging for Semiconductor Devices."

AT-32011, AT-32033 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	11
V_{CEO}	Collector-Emitter Voltage	V	5.5
I_C	Collector Current	mA	32
P_T	Power Dissipation[2, 3]	mW	200
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
θ_{jc} = 550 °C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{Mounting\ Surface}$ = 25°C.
3. Derate at 1.82 mW/°C for T_C > 40°C.

Electrical Specifications, T_A = 25°C

			AT-32011			AT-32033		
Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.	Min.	Typ.	Max.
NF	Noise Figure V_{CE} = 2.7 V, I_C = 2 mA f = 0.9 GHz	dB		1.0[1]	1.3[1]		1.0[2]	1.3[2]
G_A	Associated Gain V_{CE} = 2.7 V, I_C = 2 mA f = 0.9 GHz	dB	12.5[1]	14[1]		11[2]	12.5[2]	
h_{FE}	Forward Current Transfer Ratio V_{CE} = 2.7 V, I_C = 2 mA	–	70		300	70		300
I_{CBO}	Collector Cutoff Current V_{CB} = 3 V	µA			0.2			0.2
I_{EBO}	Emitter Cutoff Current V_{EB} = 1 V	µA			1.5			1.5

Notes:
1. Test circuit A, Figure 1. Numbers reflect device performance de-embedded from circuit losses. Input loss = 0.3 dB; output loss = 0.3 dB.
2. Test circuit B, Figure 1. Numbers reflect device performance de-embedded from circuit losses. Input loss = 0.3 dB; output loss = 0.3 dB.

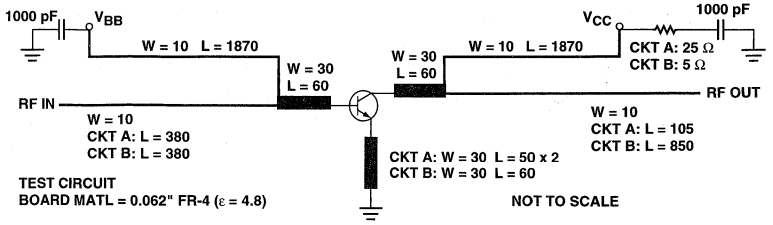


Figure 1. Test Circuit for Noise Figure and Associated Gain.
This circuit is a compromise match between best noise figure, best gain, stability, and a practical synthesizable match.

Characterization Information, T_A = 25°C

Symbol	Parameters and Test Conditions	Units	AT-32011 Typ.	AT-32033 Typ.
P_{1dB}	Power at 1 dB Gain Compression (opt tuning) V_{CE} = 2.7 V, I_C = 20 mA f = 0.9 GHz	dBm	13	13
G_{1dB}	Gain at 1 dB Gain Compression (opt tuning) V_{CE} = 2.7 V, I_C = 20 mA f = 0.9 GHz	dB	16.5	15
IP_3	Output Third Order Intercept Point (opt tuning) V_{CE} = 2.7 V, I_C = 20 mA f = 0.9 GHz	dBm	24	24
$\|S_{21}\|_E^2$	Gain in 50 Ω System V_{CE} = 2.7 V, I_C = 2 mA f = 0.9 GHz	dB	13	11.5

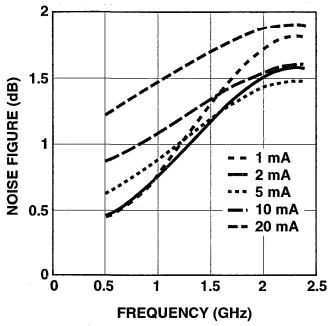


Figure 2. AT-32011 and AT-32033 Minimum Noise Figure vs. Frequency and Current at V_{CE} = 2.7 V.

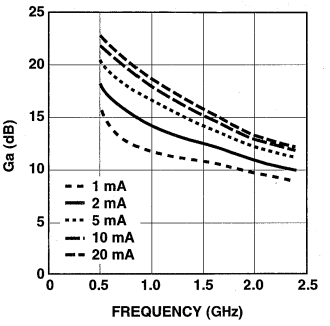


Figure 3. AT-32011 Associated Gain at Optimum Noise Match vs. Frequency and Current at V_{CE} = 2.7 V.

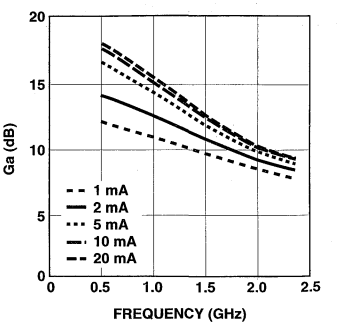


Figure 4. AT-32033 Associated Gain at Optimum Noise Match vs. Frequency and Current at V_{CE} = 2.7 V.

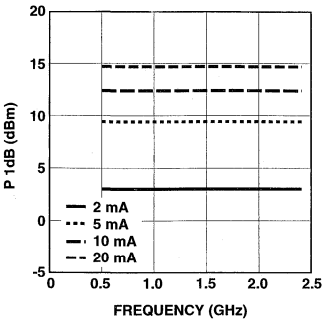


Figure 5. AT-32011 and AT-32033 Power at 1 dB Gain Compression vs. Frequency and Current at V_{CE} = 2.7 V.

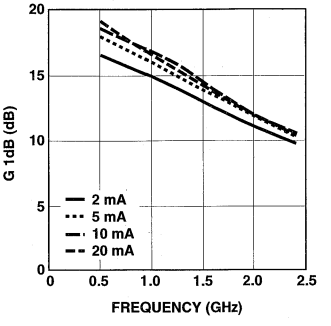


Figure 6. AT-32011 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 2.7 V.

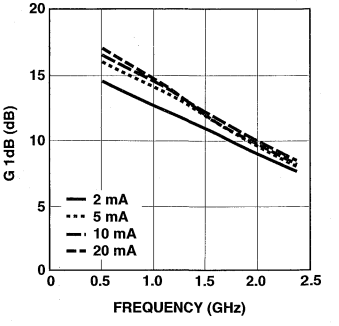


Figure 7. AT-32033 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 2.7 V.

AT-32011, AT-32033 Typical Performance

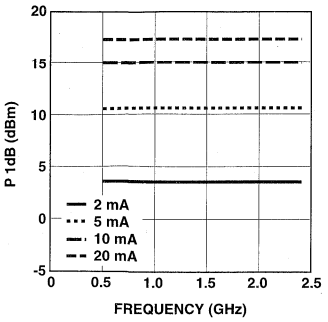


Figure 8. AT-32011 and AT-32033 Power at 1 dB Gain Compression vs. Frequency and Current at V_{CE} = 5 V.

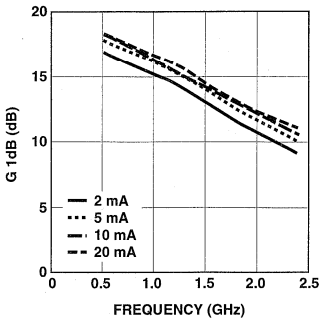


Figure 9. AT-32011 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 5 V.

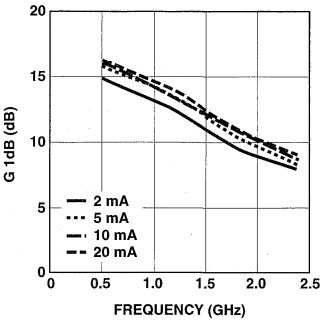


Figure 10. AT-32033 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 5 V.

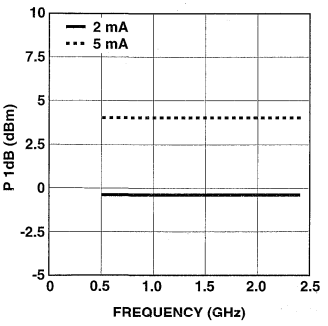


Figure 11. AT-32011 and AT-32033 Power at 1 dB Gain Compression vs. Frequency and Current at V_{CE} = 1 V.

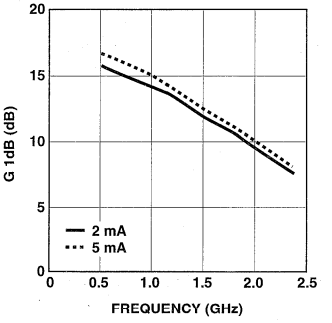


Figure 12. AT-32011 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 1 V.

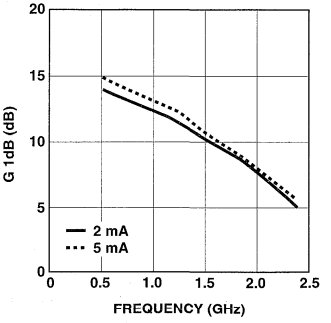


Figure 13. AT-32033 1 dB Compressed Gain vs. Frequency and Current at V_{CE} = 1 V.

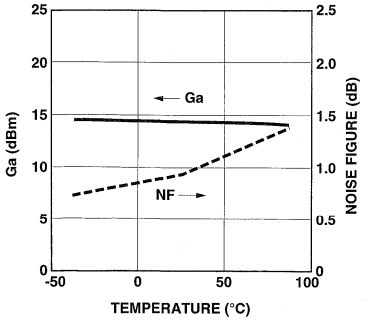


Figure 14. AT-32011 Noise Figure and Associated Gain at V_{CE} = 2.7 V, I_C = 2 mA vs. Temperature in Test Circuit, Figure 1. (Circuit Losses De-embedded).

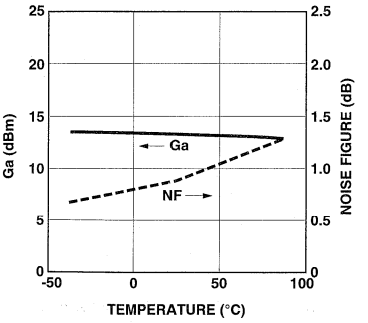


Figure 15. AT-32033 Noise Figure and Associated Gain at V_{CE} = 2.7 V, I_C = 2 mA vs. Temperature in Test Circuit, Figure 1. (Circuit Losses De-embedded).

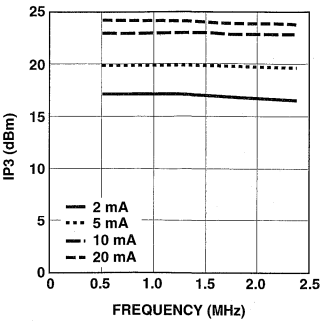


Figure 16. AT-32011 and AT-32033 Third Order Intercept vs. Frequency and Bias at V_{CE} = 2.7 V, with Optimal Tuning.

AT-32011 Typical Scattering Parameters, Common Emitter, Zo = 50 Ω V_{CE} = 1 V, I_C = 1 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.97	-11	11.09	3.59	172	-33.55	0.021	83	0.99	-5
0.5	0.88	-52	10.13	3.21	141	-20.85	0.091	59	0.92	-21
0.9	0.78	-86	8.67	2.71	117	-17.62	0.132	41	0.82	-32
1.0	0.75	-94	8.35	2.62	112	-17.27	0.137	37	0.79	-35
1.5	0.67	-127	6.35	2.08	89	-16.30	0.153	23	0.71	-45
1.8	0.63	-144	5.25	1.83	77	-16.28	0.154	16	0.67	-50
2.0	0.61	-155	4.75	1.73	70	-16.42	0.151	13	0.65	-53
2.4	0.59	-175	3.48	1.49	57	-16.86	0.144	9	0.62	-59
3.0	0.59	157	1.77	1.23	40	-17.89	0.128	8	0.61	-68
4.0	0.63	120	-0.39	0.96	18	-18.40	0.120	23	0.59	-84
5.0	0.69	94	-2.39	0.76	0	-15.60	0.166	35	0.59	-104

AT-32011 Typical Noise Parameters,

Common Emitter, Zo = 50 Ω, 1 V, I_C = 1 mA

Freq.	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	–
0.5[1]	0.42	0.79	26	0.44
0.9	0.71	0.70	54	0.35
1.8	1.37	0.53	119	0.18
2.4	1.80	0.55	158	0.08

Note:
1. 0.5 GHz noise parameter values are extrapolated, not measured.

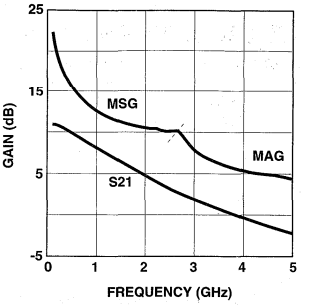


Figure 17. AT-32011 Gains vs. Frequency at V_{CE} = 1 V, I_C = 1 mA.

AT-32033 Typical Scattering Parameters, Common Emitter, Zo = 50 Ω V_{CE} = 1 V, I_C = 1 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.97	-11	11.09	3.58	170	-32.75	0.023	83	0.99	-5
0.5	0.81	-52	9.88	3.12	134	-20.30	0.097	60	0.90	-22
0.9	0.61	-87	8.07	2.53	107	-17.57	0.132	46	0.78	-33
1.0	0.56	-95	7.65	2.41	101	-17.24	0.137	44	0.76	-35
1.5	0.41	-136	5.43	1.87	77	-16.61	0.148	39	0.68	-42
1.8	0.36	-160	4.30	1.64	66	-16.36	0.152	41	0.65	-46
2.0	0.34	-177	3.74	1.54	59	-16.05	0.158	44	0.63	-49
2.4	0.34	154	2.49	1.33	47	-15.10	0.176	49	0.61	-55
3.0	0.38	119	0.96	1.12	32	-12.77	0.230	55	0.59	-65
4.0	0.46	81	-0.84	0.91	15	-8.68	0.368	50	0.56	-87
5.0	0.51	56	-1.90	0.80	5	-5.68	0.520	37	0.51	-114

AT-32033 Typical Noise Parameters,

Common Emitter, Zo = 50 Ω, 1 V, I_C = 1 mA

Freq.	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	–
0.5[1]	0.42	0.87	25	0.48
0.9	0.71	0.73	55	0.34
1.8	1.37	0.42	143	0.11
2.4	1.80	0.50	-162	0.07

Note:
1. 0.5 GHz noise parameter values are extrapolated, not measured.

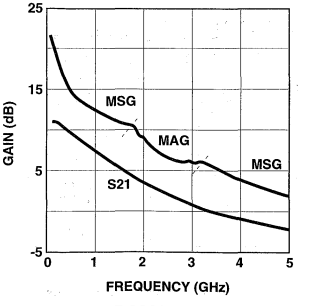


Figure 18. AT-32033 Gains vs. Frequency at V_{CE} = 1 V, I_C = 1 mA.

AT-32011 Typical Scattering Parameters, Common Emitter, Zo = 50 Ω V_{CE} = 2.7 V, I_C = 2 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.94	-13	16.67	6.81	170	-35.25	0.017	82	0.99	-6
0.5	0.80	-60	15.10	5.69	136	-23.07	0.070	57	0.86	-24
0.9	0.67	-97	12.97	4.45	112	-20.34	0.096	41	0.73	-35
1.0	0.64	-104	12.48	4.21	107	-20.05	0.099	39	0.70	-37
1.5	0.55	-137	10.04	3.18	86	-19.21	0.110	30	0.61	-45
1.8	0.51	-154	8.77	2.75	76	-19.04	0.112	28	0.58	-49
2.0	0.50	-165	8.13	2.55	70	-18.99	0.112	27	0.56	-52
2.4	0.48	176	6.75	2.18	58	-18.84	0.114	27	0.54	-57
3.0	0.49	150	4.97	1.77	43	-18.52	0.119	30	0.52	-64
4.0	0.54	116	2.73	1.37	22	-16.98	0.142	36	0.50	-77
5.0	0.61	92	0.83	1.10	4	-14.50	0.188	37	0.50	-95

AT-32011 Typical Noise Parameters,

Common Emitter, Zo = 50 Ω, 2.7 V, I_C = 2 mA

Freq.	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	–
0.5[1]	0.57	0.69	22	0.30
0.9	0.78	0.60	51	0.25
1.8	1.25	0.42	117	0.14
2.4	1.57	0.44	159	0.08

Note:
1. 0.5 GHz noise parameter values are extrapolated, not measured.

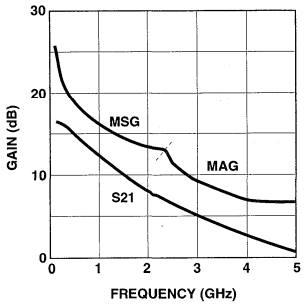


Figure 19. AT-32011 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 2 mA.

AT-32033 Typical Scattering Parameters, Common Emitter, Zo = 50 Ω V_{CE} = 2.7 V, I_C = 2 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.93	-13	16.61	6.77	167	-34.89	0.018	82	0.99	-6
0.5	0.68	-56	14.29	5.18	127	-23.10	0.070	61	0.83	-22
0.9	0.44	-86	11.48	3.75	101	-20.35	0.096	55	0.71	-30
1.0	0.39	-93	10.88	3.50	96	-19.91	0.101	54	0.70	-31
1.5	0.23	-129	8.16	2.56	76	-17.99	0.126	55	0.64	-36
1.8	0.18	-156	6.89	2.21	66	-16.89	0.143	57	0.62	-39
2.0	0.16	-176	6.19	2.04	60	-16.14	0.156	57	0.61	-42
2.4	0.17	146	4.91	1.76	50	-14.70	0.184	58	0.60	-47
3.0	0.22	108	3.35	1.47	36	-12.51	0.237	57	0.58	-56
4.0	0.32	76	1.51	1.19	18	-9.19	0.347	51	0.55	-73
5.0	0.40	56	0.17	1.02	4	-6.54	0.471	40	0.51	-95

AT-32033 Typical Noise Parameters,

Common Emitter, Zo = 50 Ω, 2.7 V, I_C = 2 mA

Freq.	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	–
0.5[1]	0.57	0.77	15	0.36
0.9	0.78	0.63	49	0.28
1.8	1.25	0.32	136	0.10
2.4	1.57	0.40	-159	0.08

Note:
1. 0.5 GHz noise parameter values are extrapolated, not measured.

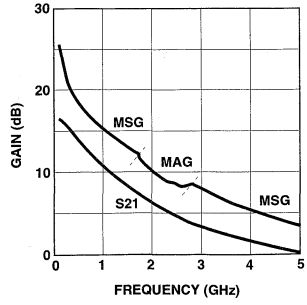


Figure 20. AT-32033 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 2 mA.

AT-32011 Typical Scattering Parameters, Common Emitter, Zo = 50 Ω V_{CE} = 2.7 V, I_C = 20 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.52	-49	31.08	35.79	149	-37.78	0.013	72	0.83	-22
0.5	0.36	-138	22.96	14.06	102	-28.93	0.036	62	0.40	-42
0.9	0.34	-168	18.33	8.25	86	-25.15	0.055	64	0.31	-42
1.0	0.34	-174	17.46	7.47	83	-24.41	0.060	64	0.30	-42
1.5	0.34	165	14.13	5.09	71	-21.35	0.086	63	0.28	-45
1.8	0.34	155	12.61	4.27	64	-19.92	0.101	61	0.28	-49
2.0	0.35	148	11.74	3.86	60	-19.08	0.111	60	0.27	-52
2.4	0.36	136	10.23	3.25	52	-17.60	0.132	57	0.27	-58
3.0	0.39	120	8.38	2.62	40	-15.86	0.161	51	0.26	-67
4.0	0.45	98	6.00	2.00	23	-13.68	0.207	42	0.24	-84
5.0	0.52	82	4.25	1.63	7	-11.93	0.253	32	0.23	-106

AT-32011 Typical Noise Parameters,
Common Emitter, Zo = 50 Ω, 2.7 V, I_C = 20 mA

Freq.	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	–
0.5[1]	1.39	0.15	65	0.16
0.9	1.51	0.14	105	0.13
1.8	1.78	0.28	-164	0.12
2.4	1.96	0.40	-142	0.13

Note:
1. 0.5 GHz noise parameter values are extrapolated, not measured.

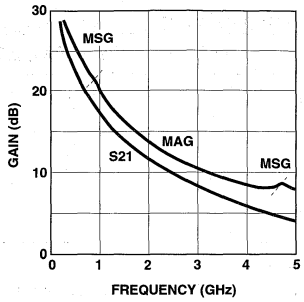


Figure 21. AT-32011 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 20 mA.

AT-32033 Typical Scattering Parameters, Common Emitter, Zo = 50 Ω V_{CE} = 2.7 V, I_C = 20 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.50	-35	29.84	31.03	137	-37.08	0.014	77	0.79	-18
0.5	0.16	-52	19.58	9.53	94	-25.35	0.054	77	0.53	-20
0.9	0.08	-36	14.81	5.50	81	-20.63	0.093	75	0.50	-24
1.0	0.07	-31	13.96	4.99	78	-19.66	0.104	74	0.50	-25
1.5	0.06	12	10.71	3.43	66	-16.31	0.153	69	0.49	-31
1.8	0.07	31	9.31	2.92	60	-14.75	0.183	66	0.48	-35
2.0	0.08	40	8.50	2.66	56	-13.85	0.203	63	0.47	-38
2.4	0.11	48	7.16	2.28	48	-12.32	0.242	59	0.46	-44
3.0	0.15	53	5.62	1.91	37	-10.49	0.299	52	0.43	-54
4.0	0.21	52	3.86	1.56	20	-8.11	0.393	41	0.39	-71
5.0	0.26	48	2.61	1.35	6	-6.34	0.482	29	0.33	-91

AT-32033 Typical Noise Parameters,
Common Emitter, Zo = 50 Ω, 2.7 V, I_C = 20 mA

Freq.	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	–
0.5[1]	1.39	0.15	45	0.28
0.9	1.51	0.12	100	0.22
1.8	1.78	0.28	-135	0.14
2.4	1.96	0.46	-107	0.22

Note:
1. 0.5 GHz noise parameter values are extrapolated, not measured.

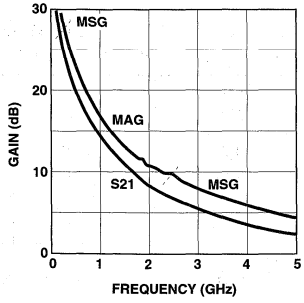


Figure 22. AT-32033 Gains vs. Frequency at V_{CE} = 2.7 V, I_C = 20 mA.

AT-32011 Typical Scattering Parameters, Common Emitter, Zo = 50 Ω V_{CE} = 5 V, I_C = 2 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.95	-13	16.65	6.80	170	-35.84	0.016	82	0.99	-6
0.5	0.81	-57	15.18	5.74	137	-23.56	0.066	58	0.87	-23
0.9	0.68	-93	13.16	4.55	113	-20.72	0.092	43	0.74	-34
1.0	0.64	-100	12.69	4.31	109	-20.42	0.095	40	0.72	-36
1.5	0.55	-133	10.31	3.28	88	-19.49	0.106	32	0.63	-43
1.8	0.51	-150	9.05	2.84	78	-19.29	0.109	29	0.60	-47
2.0	0.49	-161	8.43	2.64	71	-19.22	0.109	28	0.58	-50
2.4	0.47	180	7.06	2.25	60	-19.03	0.112	29	0.55	-55
3.0	0.47	153	5.29	1.84	45	-18.72	0.116	31	0.54	-62
4.0	0.52	118	3.07	1.42	24	-17.19	0.138	37	0.52	-75
5.0	0.59	94	1.17	1.14	6	-14.73	0.183	38	0.51	-92

AT-32011 Typical Noise Parameters,

Common Emitter, Zo = 50 Ω, 2.7 V, I_C = 2 mA

Freq.	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	–
0.5[1]	0.52	0.73	20	0.34
0.9	0.75	0.63	49	0.28
1.8	1.26	0.44	111	0.16
2.4	1.60	0.45	153	0.09

Note:
1. 0.5 GHz noise parameter values are extrapolated, not measured.

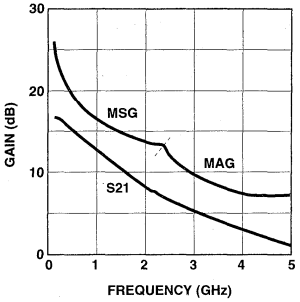


Figure 23. AT-32011 Gains vs. Frequency at V_{CE} = 5 V, I_C = 2 mA.

AT-32033 Typical Scattering Parameters, Common Emitter, Zo = 50 Ω V_{CE} = 5 V, I_C = 2 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.94	-13	16.56	6.73	167	-35.39	0.017	82	0.99	-5
0.5	0.69	-54	14.34	5.21	128	-23.74	0.065	62	0.85	-21
0.9	0.45	-82	11.62	3.81	102	-20.92	0.090	56	0.73	-28
1.0	0.40	-89	11.03	3.56	98	-20.35	0.096	55	0.72	-30
1.5	0.23	-121	8.33	2.61	77	-18.49	0.119	56	0.66	-35
1.8	0.17	-147	7.04	2.25	68	-17.39	0.135	58	0.65	-37
2.0	0.15	-167	6.36	2.08	62	-16.59	0.148	59	0.63	-40
2.4	0.14	151	5.06	1.79	51	-15.14	0.175	60	0.62	-44
3.0	0.20	109	3.52	1.50	37	-12.92	0.226	59	0.61	-53
4.0	0.31	76	1.66	1.21	19	-9.55	0.333	53	0.59	-70
5.0	0.38	55	0.26	1.03	5	-6.80	0.457	42	0.55	-90

AT-32033 Typical Noise Parameters,

Common Emitter, Zo = 50 Ω, 5 V, I_C = 2 mA

Freq.	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	–
0.5[1]	0.52	0.79	15	0.42
0.9	0.75	0.65	48	0.30
1.8	1.26	0.33	127	0.11
2.4	1.60	0.39	-166	0.07

Note:
1. 0.5 GHz noise parameter values are extrapolated, not measured.

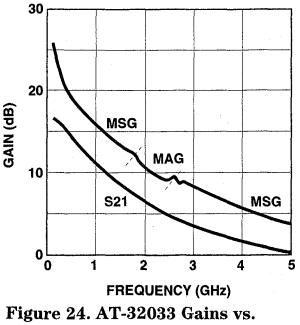


Figure 24. AT-32033 Gains vs. Frequency at V_{CE} = 5 V, I_C = 2 mA.

AT-32011 Typical Scattering Parameters, Common Emitter, Zo = 50 Ω V_{CE} = 5 V, I_C = 20 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.58	-43	31.28	36.64	151	-38.13	0.012	72	0.83	-21
0.5	0.35	-128	23.51	14.99	103	-29.05	0.035	62	0.42	-40
0.9	0.31	-161	18.93	8.84	87	-25.30	0.054	64	0.33	-40
1.0	0.30	-167	18.06	8.00	84	-24.57	0.059	64	0.32	-40
1.5	0.29	170	14.74	5.46	72	-21.50	0.084	63	0.30	-44
1.8	0.30	158	13.22	4.58	65	-20.06	0.099	61	0.29	-47
2.0	0.30	151	12.35	4.15	61	-19.23	0.109	60	0.29	-50
2.4	0.32	138	10.85	3.49	53	-17.77	0.129	57	0.28	-56
3.0	0.35	121	8.99	2.82	42	-16.03	0.158	52	0.27	-64
4.0	0.41	98	6.64	2.15	25	-13.85	0.203	42	0.25	-80
5.0	0.48	83	4.90	1.76	9	-12.12	0.248	33	0.24	-100

AT-32011 Typical Noise Parameters,
Common Emitter, Zo = 50 Ω, 5 V, I_C = 20 mA

Freq.	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	–
0.5[1]	1.38	0.18	50	0.20
0.9	1.50	0.15	88	0.16
1.8	1.78	0.23	176	0.13
2.4	1.96	0.34	-156	0.12

Note:
1. 0.5 GHz noise parameter values are extrapolated, not measured.

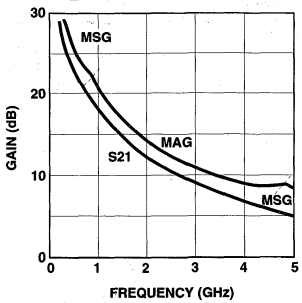


Figure 25. AT-32011 Gains vs. Frequency at V_{CE} = 5 V, I_C = 20 mA.

AT-32033 Typical Scattering Parameters, Common Emitter, Zo = 50 Ω V_{CE} = 5 V, I_C = 20 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.55	-31	30.00	31.61	138	-37.72	0.013	78	0.81	-16
0.5	0.20	-44	19.91	9.90	95	-25.85	0.051	77	0.56	-19
0.9	0.13	-31	15.15	5.72	82	-21.01	0.089	75	0.53	-22
1.0	0.12	-28	14.30	5.19	79	-20.18	0.098	74	0.53	-23
1.5	0.10	-7	11.03	3.56	68	-16.77	0.145	69	0.52	-30
1.8	0.09	5	9.63	3.03	61	-15.19	0.174	66	0.51	-33
2.0	0.10	13	8.82	2.76	57	-14.33	0.192	64	0.50	-36
2.4	0.11	25	7.49	2.37	50	-12.77	0.230	60	0.49	-42
3.0	0.13	36	5.93	1.98	39	-10.90	0.285	54	0.47	-51
4.0	0.18	42	4.19	1.62	23	-8.50	0.376	43	0.42	-67
5.0	0.22	43	2.98	1.41	8	-6.65	0.465	31	0.37	-86

AT-32033 Typical Noise Parameters,
Common Emitter, Zo = 50 Ω, 5 V, I_C = 20 mA

Freq.	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	–
0.5[1]	1.38	0.25	35	0.30
0.9	1.50	0.19	85	0.23
1.8	1.78	0.21	-150	0.14
2.4	1.96	0.39	-114	0.19

Note:
1. 0.5 GHz noise parameter values are extrapolated, not measured.

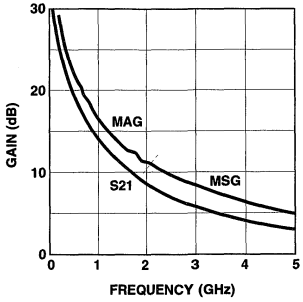


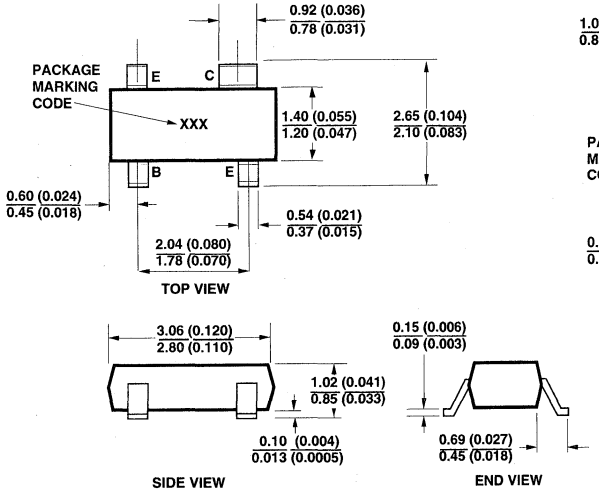
Figure 26. AT-32033 Gains vs. Frequency at V_{CE} = 5 V, I_C = 20 mA.

Ordering Information

Part Number	Increment	Comments
AT-32011-BLK	100	Bulk
AT-32011-TR1	3000	7" Reel
AT-32033-BLK	100	Bulk
AT-32033-TR1	3000	7" Reel

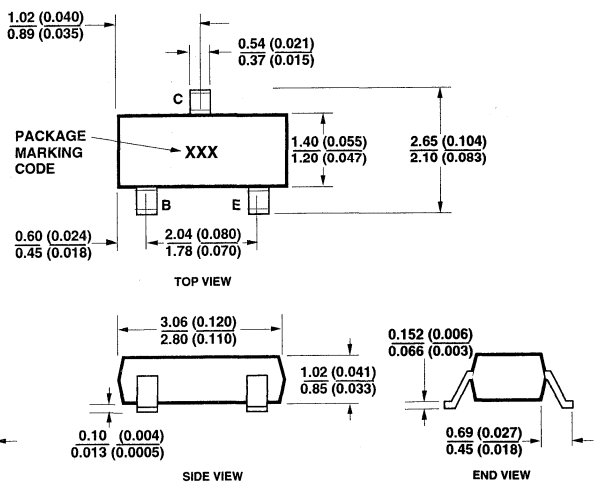
Package Dimensions

SOT-143 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

SOT-23 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Low Current, High Performance NPN Silicon Bipolar Transistor

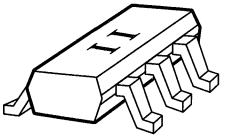
Technical Data

AT-32063

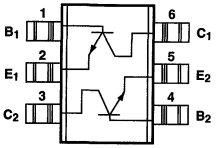
Features

- **High Performance Bipolar Transistor Optimized for Low Current, Low Voltage Operation**
- **900 MHz Performance: 1.1 dB NF, 14.5 dB G_A**
- **Characterized for End-of-Life Battery Use (2.7 V)**
- **SOT-363 (SC-70) Plastic Package**
- **Tape-and-Reel Packaging Option Available [1]**

Surface Mount Package SOT-363 (SC-70)



Pin Connections and Package Marking



Description

The AT-32063 contains two high performance NPN bipolar transistors in a single SOT-363 package. The devices are unconnected, allowing flexibility in design. The pin-out is convenient for cascode amplifier designs. The SOT-363 package is an industry standard plastic surface mount package.

The 3.2 micron emitter-to-emitter pitch and reduced parasitic design of the transistor yields extremely high performance products that can perform a multiplicity of tasks. The 20 emitter finger interdigitated geometry yields a transistor that is easy to match to and extremely fast, with moderate power, low noise resistance, and low operating currents.

Optimized performance at 2.7 V makes this device ideal for use in 900 MHz, 1.8 GHz, and 2.4 GHz battery operated systems as an LNA, gain stage, buffer, oscillator, or active mixer. Typical amplifier designs at 900 MHz yield 1.3 dB noise figures with 12 dB or more associated gain at a 2.7 V, 5 mA bias, with noise performance being relatively insensitive to input match. High gain capability at 1 V, 1 mA makes this device a good fit for 900 MHz pager applications. Voltage breakdowns are high enough for use at 5 volts.

The AT-3 series bipolar transistors are fabricated using an optimized version of Hewlett-Packard's 10 GHz f_t, 30 GHz f_{max} Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

5965-8921E

AT-32063 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	11
V_{CEO}	Collector-Emitter Voltage	V	5.5
I_C	Collector Current	mA	32
P_T	Power Dissipation[2,3]	mW	150
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

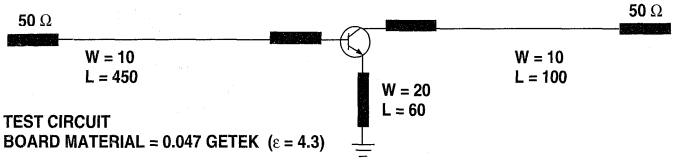
Thermal Resistance[2]:
$\theta_{jc} = 370°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface} = 25°C$.
3. Derate at 2.7 mW/°C for $T_C > 94.5°C$.
4. 150 mW per device.

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF	Noise Figure; $V_{CE} = 2.7$ V, $I_C = 5$ mA	f = 0.9 GHz	dB		1.1[2]	1.4[2]
G_A	Associated Gain; $V_{CE} = 2.7$ V, $I_C = 5$ mA	f = 0.9 GHz	dB	12.5[2]	14.5[2]	
h_{FE}	Forward Current Transfer Ratio; $V_{CE} = 2.7$ V, $I_C = 5$ mA		—	50		270
I_{CBO}	Collector Cutoff Current; $V_{CB} = 3$ V		μA			0.2
I_{EBO}	Noise Figure; $V_{EB} = 1$ V		μA			1.5

Notes:
1. All data is per individual transistor.
2. Test circuit, Figure 1. Numbers reflect device performance de-embedded from circuit losses. Input loss = 0.2 dB; output loss = 0.3 dB.



DIMENSIONS IN MILS
NOT TO SCALE

Figure 1. Test circuit for Noise Figure and Associated Gain. This circuit is a compromise match between best noise figure, best gain, stability, and a practical synthesizable match.

AT-32063 Characterization Information, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Typ.
$P_{1\,dB}$	Power at 1 dB Gain Compression (opt tuning); V_{CE} = 2.7 V, I_C = 20 mA	f = 0.9 GHz	dBm	12
$G_{1\,dB}$	Gain at 1 dB Gain Compression (opt tuning); V_{CE} = 2.7 V, I_C = 20 mA	f = 0.9 GHz	dB	16
IP_3	Output Third Order Intercept Point (opt tuning); V_{CE} = 2.7 V, I_C = 20 mA	f = 0.9 GHz	dBm	24

Typical Performance, T_A = 25°C

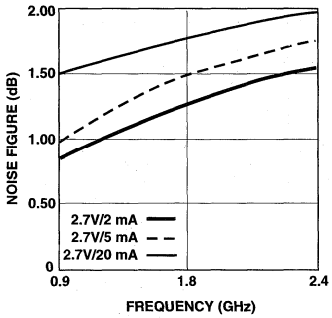


Figure 2. Minimum Noise Figure vs. Frequency and Current at V_{CE} = 2.7 V.

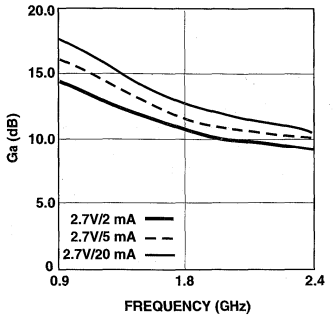


Figure 3. Associated Gain at Optimum Noise Match vs. Frequency and Current at V_{CE} = 2.7 V.

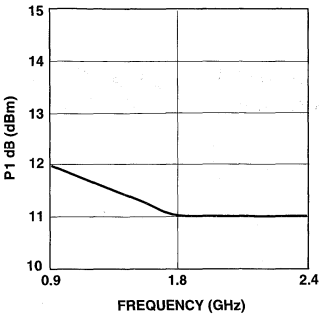


Figure 4. Power at 1 dB Gain Compression vs. Frequency at V_{CE} = 2.7 V and I_C = 20 mA.

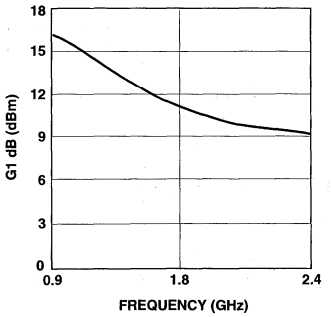


Figure 5. 1 dB Compressed Gain vs. Frequency at V_{CE} = 2.7 V and I_C = 20 mA.

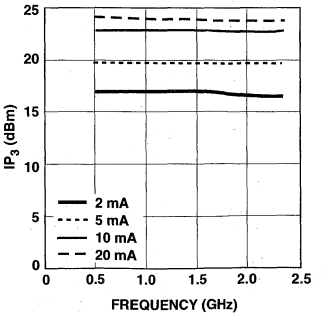


Figure 6. Third Order Intercept vs. Frequency and Bias at V_{CE} = 2.7 V, with Optimal Tuning.

AT-32063 Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, V_{CE} = 1 V, I_C = 1 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.98	-11	11.36	3.7	171	-34.77	0.02	83	0.99	-4
0.5	0.86	-50	10.14	3.21	138	-22.02	0.08	59	0.91	-20
0.9	0.72	-82	8.39	2.63	113	-18.97	0.11	43	0.82	-31
1.0	0.69	-88	7.87	2.48	108	-18.61	0.12	41	0.8	-32
1.5	0.58	-119	5.87	1.97	85	-17.8	0.13	31	0.73	-41
1.8	0.52	-134	4.83	1.74	74	-17.72	0.13	28	0.7	-45
2.0	0.49	-145	4.3	1.64	67	-17.69	0.13	28	0.68	-48
2.4	0.45	-165	3.16	1.44	55	-17.68	0.13	30	0.67	-54
3.0	0.41	166	1.84	1.24	39	-16.99	0.14	37	0.64	-63
4.0	0.42	124	0.17	1.02	16	-13.67	0.21	45	0.6	-81
5.0	0.47	93	-1.15	0.88	-2	-9.84	0.32	38	0.54	-107

AT-32063 Typical Noise Parameters

Common Emitter, Z_O = 50 Ω, V_{CE} = 1 V, I_C = 1 mA

Freq. GHz	F_{min} dB	G_A dB	G_{opt} Mag.	Ang.	R_n —
0.9	0.71	10.4	0.76	50	0.44
1.8	1.37	8.3	0.60	112	0.24
2.4	1.80	7.2	0.50	155	0.10

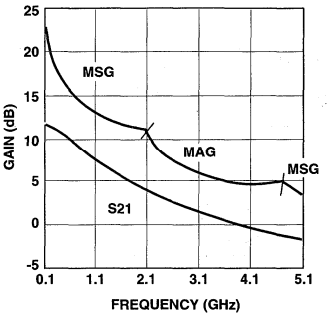


Figure 7. Gain vs. Frequency at V_{CE} = 1 V, I_C = 1 mA.

AT-32063 Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, V_{CE} = 2.7 V, I_C = 2 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.96	-12	16.46	6.66	169	-37.32	0.014	82	0.98	-5
0.5	0.77	-55	14.73	5.45	132	-25.13	0.055	59	0.87	-21
0.9	0.59	-87	12.37	4.15	107	-22.42	0.076	48	0.76	-29
1.0	0.55	-93	11.74	3.86	103	-22.07	0.079	47	0.74	-30
1.5	0.42	-121	9.26	2.90	83	-20.79	0.091	44	0.69	-36
1.8	0.37	-135	8.01	2.52	73	-20.13	0.099	45	0.67	-39
2.0	0.34	-145	7.35	2.33	67	-19.67	0.104	46	0.66	-41
2.4	0.29	-164	6.05	2.01	56	-18.68	0.116	48	0.65	-46
3.0	0.26	167	4.54	1.69	41	-16.95	0.142	50	0.64	-53
4.0	0.28	124	2.73	1.37	20	-13.75	0.205	48	0.61	-68
5.0	0.33	94	1.36	1.17	1	-10.70	0.292	41	0.57	-89

AT-32063 Typical Noise Parameters

Common Emitter, Z_O = 50 Ω, V_{CE} = 2.7 V, I_C = 2 mA

Freq. GHz	F_{min} dB	G_A dB	G_{opt} Mag.	Ang.	R_n —
0.9	0.78	14.3	0.65	50	0.31
1.8	1.25	10.7	0.45	105	0.20
2.4	1.57	9.1	0.35	145	0.13

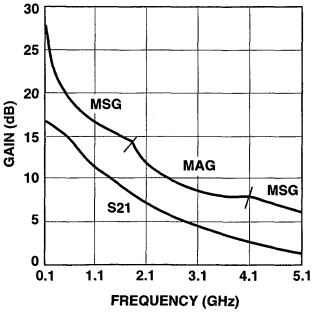


Figure 8. Gain vs. Frequency at V_{CE} = 2.7 V, I_C = 2 mA.

AT-32063 Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, V_{CE} = 2.7 V, I_C = 5 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.87	-19	23.36	14.72	162	-37.77	0.013	80	0.96	-9
0.5	0.52	-72	19.21	9.13	116	-27.03	0.045	60	0.72	-25
0.9	0.34	-101	15.40	5.89	94	-24.01	0.063	58	0.62	-28
1.0	0.31	-106	14.60	5.37	90	-23.41	0.067	58	0.61	-29
1.5	0.22	-129	11.54	3.77	74	-20.85	0.091	58	0.58	-33
1.8	0.19	-141	10.12	3.21	66	-19.52	0.106	58	0.57	-36
2.0	0.17	-150	9.33	2.93	61	-18.72	0.116	57	0.57	-38
2.4	0.14	-169	7.95	2.50	52	-17.22	0.138	56	0.57	-42
3.0	0.12	160	6.34	2.08	39	-15.25	0.173	52	0.56	-49
4.0	0.16	117	4.46	1.67	20	-12.40	0.240	44	0.53	-63
5.0	0.22	93	3.15	1.44	2	-10.03	0.315	33	0.48	-82

AT-32063 Typical Noise Parameters

Common Emitter, Z_O = 50 Ω, V_{CE} = 2.7 V, I_C = 5 mA

Freq. GHz	F_{min} dB	G_A dB	G_{opt} Mag.	Ang.	R_n —
0.9	0.98	16.4	0.45	51	0.23
1.8	1.50	11.6	0.29	100	0.16
2.4	1.77	10.1	0.33	153	0.11

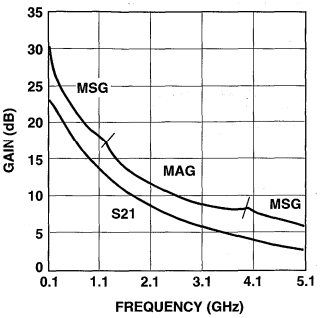


Figure 9. Gain vs. Frequency at V_{CE} = 2.7 V, I_C = 5 mA.

AT-32063 Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, V_{CE} = 2.7 V, I_C = 20 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.55	-41	30.48	33.40	143	-39.81	0.010	74	0.83	-15
0.5	0.20	-107	21.24	11.53	97	-29.18	0.035	72	0.56	-20
0.9	0.13	-137	16.48	6.66	82	-24.63	0.059	72	0.53	-22
1.0	0.13	-141	15.60	6.02	79	-23.79	0.065	71	0.53	-22
1.5	0.10	-164	12.26	4.10	67	-20.43	0.095	68	0.52	-27
1.8	0.09	-178	10.78	3.46	60	-18.88	0.114	66	0.53	-31
2.0	0.09	172	9.93	3.14	56	-17.98	0.126	64	0.53	-34
2.4	0.08	152	8.52	2.67	48	-16.39	0.151	60	0.53	-39
3.0	0.10	127	6.85	2.20	36	-14.4	0.191	54	0.52	-47
4.0	0.15	101	4.92	1.76	18	-11.68	0.261	43	0.48	-61
5.0	0.21	86	3.59	1.51	0	-9.52	0.334	31	0.44	-79

AT-32063 Typical Noise Parameters

Common Emitter, Z_O = 50 Ω, V_{CE} = 2.7 V, I_C = 20 mA

Freq. GHz	F_{min} dB	G_A dB	G_{opt} Mag.	Ang.	R_n —
0.9	1.51	17.9	0.13	88	0.20
1.8	1.78	12.7	0.20	178	0.13
2.4	1.96	10.6	0.28	235	0.08

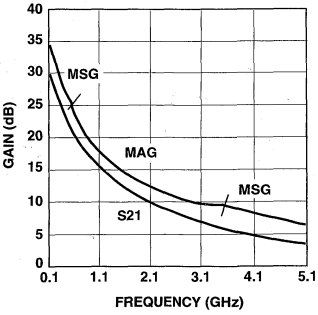


Figure 10. Gain vs. Frequency at V_{CE} = 2.7 V, I_C = 20 mA.

AT-32063 Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, V_{CE} = 5 V, I_C = 2 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.96	-12	16.50	6.69	169	-38.44	0.012	82	0.98	-5
0.5	0.78	-53	14.84	5.52	133	-26.20	0.049	60	0.88	-19
0.9	0.59	-84	12.5	4.23	108	-23.4	0.068	50	0.79	-27
1.0	0.56	-90	11.92	3.94	104	-23.04	0.070	49	0.77	-28
1.5	0.42	-117	9.46	2.97	84	-21.71	0.082	46	0.72	-33
1.8	0.36	-131	8.21	2.57	74	-21.04	0.089	47	0.70	-36
2.0	0.33	-140	7.55	2.38	68	-20.56	0.094	48	0.69	-39
2.4	0.28	-159	6.24	2.05	57	-19.54	0.105	50	0.69	-43
3.0	0.24	171	4.72	1.72	43	-17.76	0.129	53	0.68	-50
4.0	0.25	126	2.88	1.39	21	-14.47	0.189	52	0.66	-64
5.0	0.31	95	1.49	1.19	3	-11.32	0.272	45	0.63	-83

AT-32063 Typical Noise Parameters

Common Emitter, Z_O = 50 Ω, V_{CE} = 5 V, I_C = 2 mA

Freq. GHz	F_{min} dB	G_A dB	G_{opt} Mag.	Ang.	R_n —
0.9	0.75	13.7	0.74	47	0.37
1.8	1.26	10.8	0.55	101	0.22
2.4	1.60	9.6	0.45	139	0.13

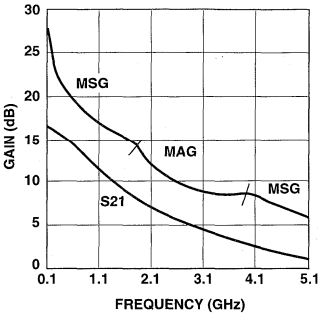


Figure 11. Gain vs. Frequency at V_{CE} = 5 V, I_C = 2 mA.

AT-32063 Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, V_{CE} = 5 V, I_C = 20 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.61	-36	30.56	33.74	145	-40.46	0.01	75	0.86	-14
0.5	0.22	-91	21.75	12.23	98	-29.90	0.03	72	0.6	-19
0.9	0.13	-115	17.02	7.10	83	-25.40	0.05	72	0.57	-21
1.0	0.12	-118	16.14	6.41	81	-24.56	0.06	71	0.57	-21
1.5	0.08	-137	12.80	4.36	68	-21.23	0.09	69	0.57	-26
1.8	0.06	-148	11.31	3.68	62	-19.69	0.10	66	0.57	-30
2.0	0.06	-159	10.46	3.33	58	-18.79	0.12	65	0.57	-32
2.4	0.04	175	9.02	2.83	50	-17.21	0.14	61	0.57	-37
3.0	0.05	131	7.35	2.33	39	-15.22	0.17	56	0.56	-45
4.0	0.10	99	5.39	1.86	21	-12.48	0.24	46	0.54	-58
5.0	0.16	86	4.05	1.6	3	-10.27	0.31	34	0.50	-75

AT-32063 Typical Noise Parameters

Common Emitter, Z_O = 50 Ω, V_{CE} = 5 V, I_C = 20 mA

Freq. GHz	F_{min} dB	G_A dB	G_{opt} Mag.	Ang.	R_n —
0.9	1.50	18.6	0.18	74	0.20
1.8	1.78	13.3	0.19	147	0.16
2.4	1.96	11.3	0.24	198	0.14

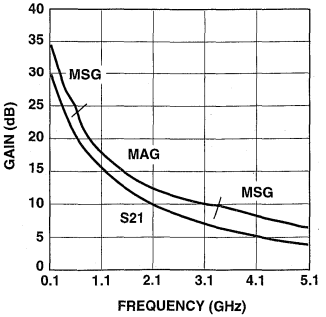
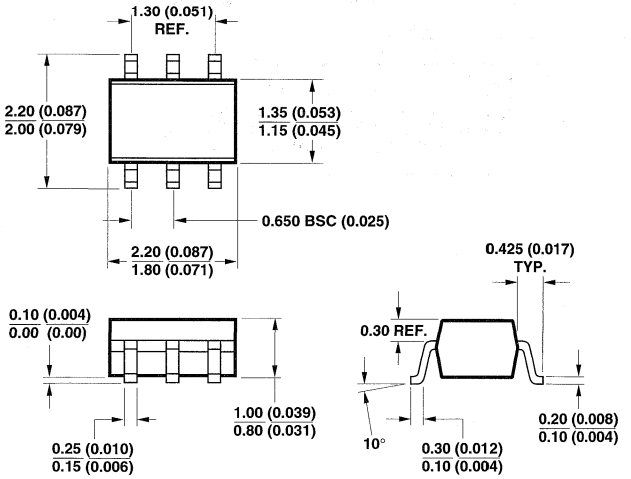


Figure 12. Gain vs. Frequency at V_{CE} = 5 V, I_C = 20 mA.

Package Dimensions

Outline 63 (SOT-363/SC-70)

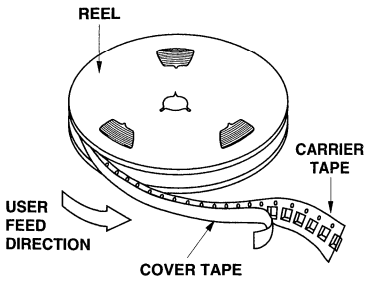


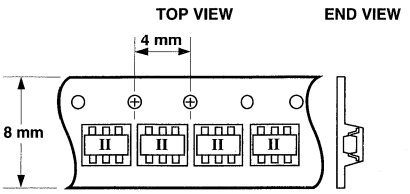
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Part Number Ordering Information

Part Number	No. of Devices	Container
AT-32063-TR1	3000	7" Reel
AT-32063-BLK	100	antistatic bag

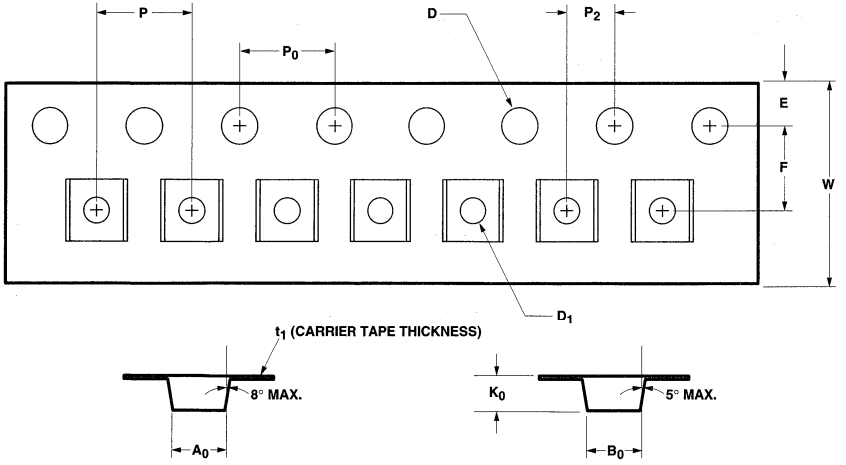
Device Orientation





Tape Dimensions

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

4.8 V NPN Common Emitter Output Power Transistor for AMPS, ETACS Phones

Technical Data

AT-33225

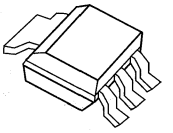
Features

- **4.8 Volt Operation**
- **+31.0 dBm P_{out} @ 900 MHz, Typ.**
- **70% Collector Efficiency @ 900 MHz, Typ.**
- **9 dB Power Gain @ 900 MHz, Typ.**
- **-29 dBc IMD_3 @ P_{out} of 24 dBm per tone, 900 MHz, Typ.**
- **Internal Input Pre-Matching Facilitates Cascading**
- **50% Smaller than SOT-223 Package**

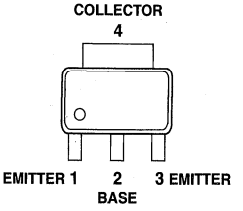
Applications

- **Output Power Device for AMPS and ETACS Handsets**
- **900 MHz ISM**

MSOP-3 Surface Mount Plastic Package Outline 25



Pin Configuration



Description

Hewlett Packard's AT-33225 is a low cost, NPN power silicon bipolar junction transistor housed in a miniature MSOP-3 surface mount plastic package. This device is designed for use as an output device for AMPS and ETACS mobile phones. The AT-33225 features over 1 watt CW output power when operated at 4.8 volts. Excellent gain and superior efficiency make the AT-33225 ideal for use in battery powered systems.

The AT-33225 is fabricated with Hewlett Packard's 10 GHz F_t Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices.

5965-5910E

AT-33225 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.4
V_{CBO}	Collector-Base Voltage	V	16.0
V_{CEO}	Collector-Emitter Voltage	V	9.5
I_C	Collector Current	mA	640
P_T	Power Dissipation[2]	W	1.6
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[3]:
$\theta_{jc} = 40°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. Derate at 25 mW/°C for $T_C > 85°C$. T_c is defined to be the temperature of the collector pin 4, where the lead contacts the circuit board.
3. Using the liquid crystal technique, $V_{CE} = 4.5$ V, $I_c = 100$ mA, $T_j = 150°C$, 1-2 µm "hot-spot" resolution.

Electrical Specifications, $T_C = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
	Freq. = 900 MHz, $V_{CE} = 4.8$ V, $I_{CQ} = 6$ mA, CW operation, Test Circuit A, unless otherwise specified					
P_{out}	Output Power[1]	$P_{in} = +22$ dBm	dBm	+30.0	+31.0	
η_C	Collector Efficiency[1]	$P_{in} = +22$ dBm	%	60	70	
IMD_3	3rd Order Intermodulation Distortion, 2 Tone Test, P_{out} each Tone = +24 dBm[1]	F1 = 899 MHz F2 = 901 MHz	dBc		-29	
	Mismatch Tolerance, No Damage[1]	$P_{out} = +31$ dBm any phase, 2 sec duration				7:1
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = 0.4$ mA, open collector	V	1.4		
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = 2.0$ mA, open emitter	V	16.0		
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = 10.0$ mA, open base	V	9.5		
h_{FE}	Forward Current Transfer Ratio	$V_{CE} = 3$ V, $I_C = 180$ mA	—	80	150	330
I_{CEO}	Collector Leakage Current	$V_{CEO} = 5$ V	µA			30

Note:
1. With external matching on input and output, tested in a 50 ohm environment. Refer to Test Circuit A (ETACS/ISM).

AT-33225 Typical Performance, T_C = 25°C

Frequency = 900 MHz, V_{CE} = 4.8 V, I_{CQ} = 6 mA, CW operation, Test Circuit A (ETACS/ISM), unless otherwise specified.

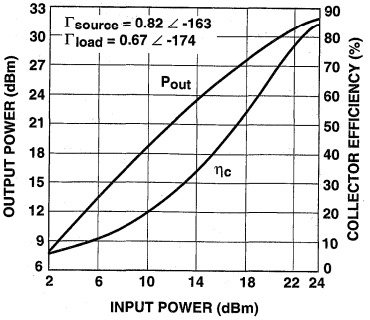


Figure 1. Output Power and Collector Efficiency vs. Input Power.

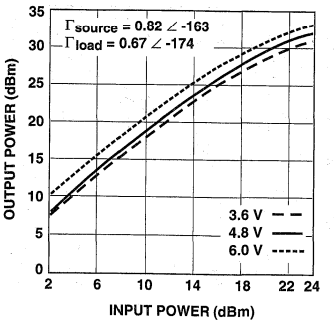


Figure 2. Output Power vs. Input Power Over Bias Voltage.

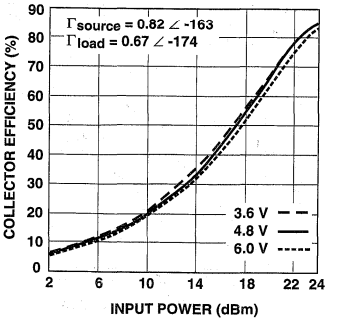


Figure 3. Collector Efficiency vs. Input Power Over Bias Voltage.

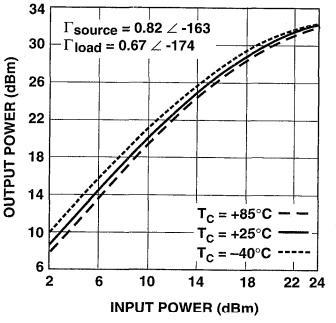


Figure 4. Output Power vs. Input Power Over Temperature.

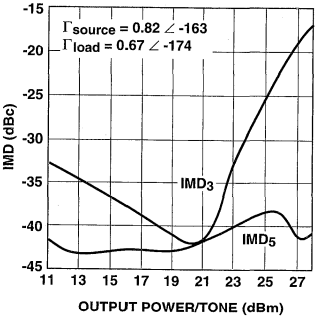


Figure 5. IMD_3, IMD_5 vs. Output Power Per Tone.

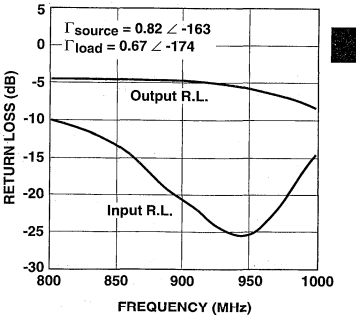


Figure 6. Input and Output Return Loss vs. Frequency.

AT-33225 Typical Performance, T_C = 25°C

Frequency = 836.5 MHz, V_{CE} = 4.8 V, I_{CQ} = 6 mA, CW operation, Test Circuit B (AMPS), unless otherwise specified.

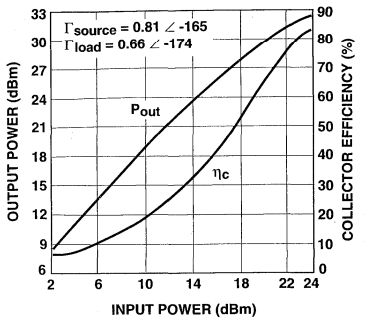


Figure 7. Output Power and Collector Efficiency vs. Input Power.

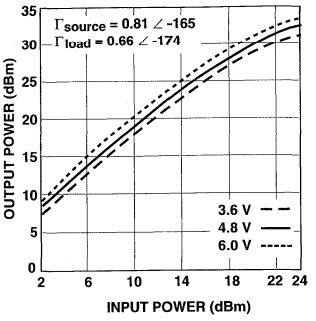


Figure 8. Output Power vs. Input Power Over Bias Voltage.

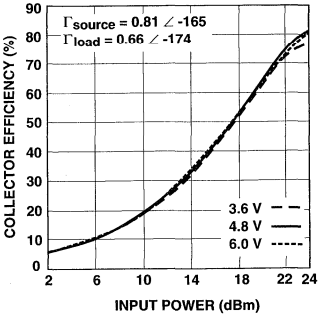


Figure 9. Collector Efficiency vs. Input Power Over Bias Voltage.

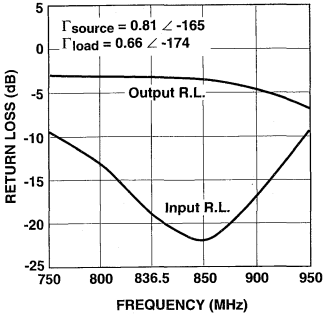


Figure 10. Input and Output Return Loss vs. Frequency.

AT-33225 Typical Large Signal Impedances

V_{CE} = 4.8 V, I_{CQ} = 6 mA, P_{out} = +31.0 dBm

Freq. MHz	Γ source		Γ load	
	Mag.	Ang.	Mag.	Ang.
750	0.77	-162	0.64	-174
800	0.80	-169	0.67	-173
850	0.82	-164	0.64	-175
900	0.82	-163	0.67	-174
950	0.83	-166	0.74	-175

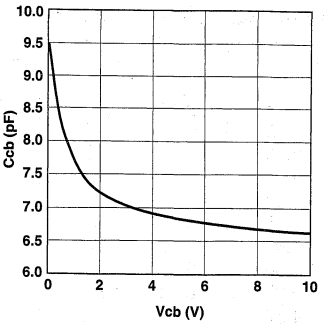
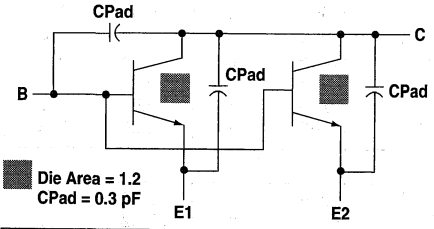


Figure 11. Collector-Base Capacitance vs. Collector-Base Voltage (DC Test).

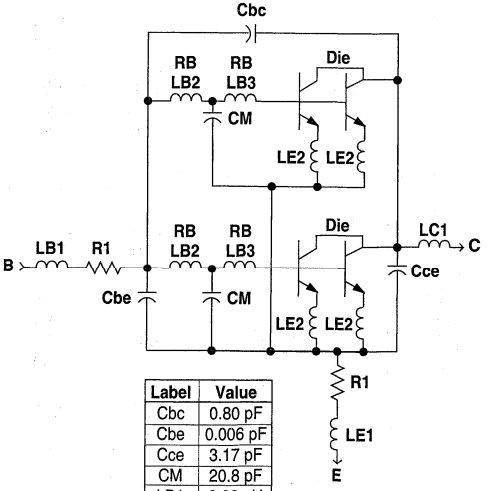
SPICE Model Parameters

Die Model



Label	Value	Label	Value
BF	280	TR	1E-9
IKF	299.9	EG	1.11
ISE	9.9E-11	IS	3.598E-15
NE	2.399	XTI	3
VAF	33.16	CJC	0.8E-12
NF	0.9935	VJC	0.4831
TF	1.6E-11	MJC	0.2508
XTF	0.006656	XCJC	0.001
VTF	0.02785	FC	0.999
ITF	0.001	CJE	6.16E-12
PTF	23	VJE	1.186
XTB	0	MJE	0.5965
BR	54.61	RB	0.752
IKR	81	IRB	0
ISC	8.7E-13	RBM	0.01
NC	1.587	RE	1.27
VAR	1.511	RC	0.107
NR	0.9886		

Packaged Model



Label	Value
Cbc	0.80 pF
Cbe	0.006 pF
Cce	3.17 pF
CM	20.8 pF
LB1	0.63 nH
LB2	0.10 nH
LB3	0.87 nH
LE1	0.35 nH
LE2	0.78 nH
LC1	0.74 nH
RB	0.1 Ω
R1	0.2 Ω

AT-33225 Typical Scattering Parameters, Common Emitter, $Z_o = 50\ \Omega$

V_{CE} = 3.6 V, I_C = 200 mA, T_C = 25°C

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.05	0.88	-164	27.0	22.26	99	-34.9	0.018	26	0.58	-153
0.10	0.89	-174	21.2	11.42	91	-34.0	0.020	32	0.57	-168
0.25	0.88	178	13.6	4.80	79	-30.5	0.030	47	0.56	-179
0.50	0.85	172	9.1	2.85	62	-25.8	0.051	51	0.49	175
0.75	0.77	168	8.2	2.58	38	-23.2	0.069	40	0.34	-177
0.90	0.70	171	8.5	2.67	13	-23.4	0.068	25	0.36	-142
1.00	0.71	178	8.2	2.57	-10	-26.0	0.050	14	0.59	-133
1.25	0.93	178	2.3	1.30	-68	-26.6	0.047	93	0.98	-162
1.50	0.98	169	-5.5	0.53	-97	-20.5	0.094	86	0.97	180
1.75	0.98	163	-13.6	0.21	-119	-18.1	0.125	78	0.93	170
2.00	0.98	159	-23.2	0.07	-163	-16.4	0.151	72	0.90	164
V_{CE} = 4.8 V, I_C = 150 mA, T_C = 25°C										
0.05	0.87	-162	27.1	22.76	100	-34.4	0.019	25	0.55	-149
0.10	0.88	-172	21.4	11.69	91	-33.6	0.021	30	0.53	-166
0.25	0.88	179	13.8	4.91	78	-30.2	0.031	44	0.52	-178
0.50	0.85	172	9.2	2.89	61	-26.0	0.050	49	0.45	177
0.75	0.78	169	8.2	2.58	37	-23.6	0.066	39	0.33	-171
0.90	0.72	172	8.4	2.62	13	-24.0	0.063	26	0.38	-138
1.00	0.72	178	8.1	2.53	-9	-26.4	0.048	17	0.59	-132
1.25	0.93	177	2.6	1.35	-66	-26.7	0.046	93	0.98	-161
1.50	0.98	169	-5.1	0.56	-97	-20.5	0.094	86	0.97	-179
1.75	0.98	163	-13.0	0.22	-119	-18.1	0.125	78	0.92	171
2.00	0.98	159	-22.2	0.08	-159	-16.5	0.150	72	0.90	165
V_{CE} = 6.0 V, I_C = 150 mA, T_C = 25°C										
0.05	0.87	-161	27.3	23.07	100	-34.4	0.019	25	0.54	-149
0.10	0.88	-172	21.5	11.86	91	-33.6	0.021	30	0.52	-166
0.25	0.88	179	13.9	4.97	78	-30.5	0.030	44	0.51	-178
0.50	0.85	173	9.3	2.93	61	-26.2	0.049	49	0.44	177
0.75	0.78	169	8.3	2.59	37	-23.7	0.065	39	0.32	-169
0.90	0.72	172	8.4	2.63	13	-24.2	0.062	26	0.38	-137
1.00	0.73	177	8.1	2.53	-9	-26.6	0.047	18	0.60	-131
1.25	0.92	177	2.7	1.37	-65	-26.7	0.046	94	0.98	-160
1.50	0.98	169	-5.0	0.57	-96	-20.5	0.094	86	0.97	-179
1.75	0.98	163	-12.7	0.23	-119	-18.1	0.125	78	0.92	171
2.00	0.98	158	-21.7	0.08	-158	-16.5	0.150	72	0.90	165

Typical Performance

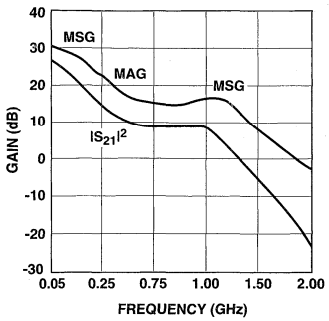


Figure 12. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency, V_{CE} = 3.6 V, I_C = 200 mA.

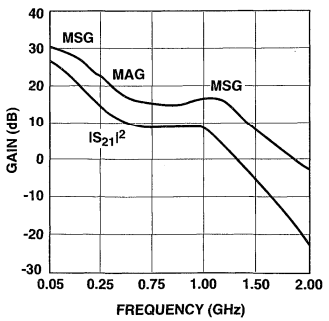


Figure 13. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency, V_{CE} = 4.8 V, I_C = 150 mA.

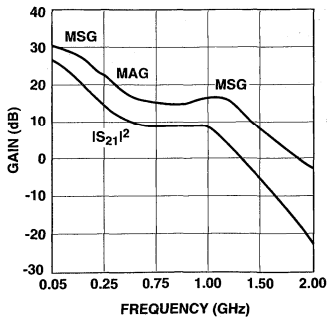
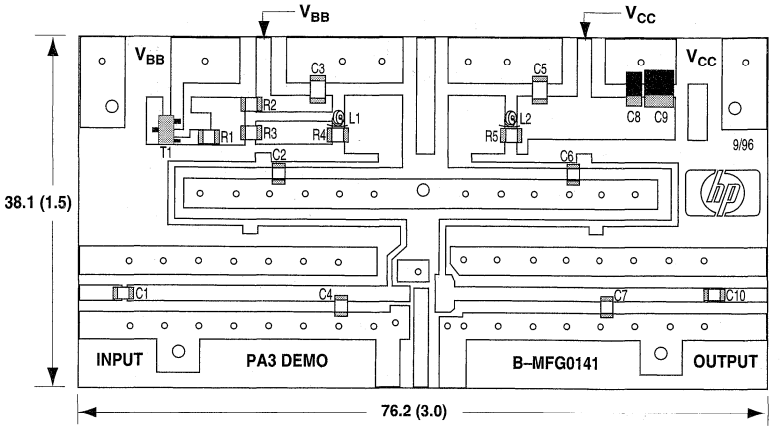


Figure 14. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency, V_{CE} = 6.0 V, I_C = 150 mA.

Test Circuit A: Test Circuit Board Layout @ 900 MHz (ETACS/ISM)

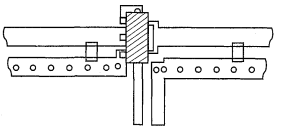


C1	100.0 pF
C2	100.0 pF
C3	100.0 nF
C4	7.5 pF
C5	100.0 nF
C6	100.0 pF
C7	5.1 pF
C8	1.5 µF
C9	10.0 µF
C10	100.0 pF
R1	2.2 Ω
R2	750.0 Ω
R3	2.2 Ω
R4	10.0 Ω
R5	10.0 Ω
T1	MBT 2222A
L1	18.0 µH
L2	18.0 µH

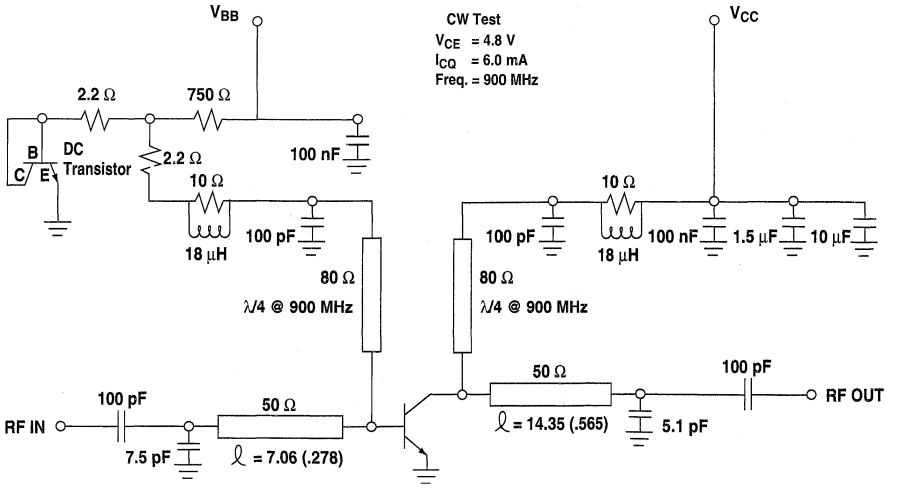
CW Test
V_{CE} = 4.8 V
I_{CQ} = 6.0 mA
Freq. = 900 MHz

Test Circuit:
FR-4 Microstrip, glass epoxy board
Dielectric Constant = 4.5
Thickness = 0.79 (.031)

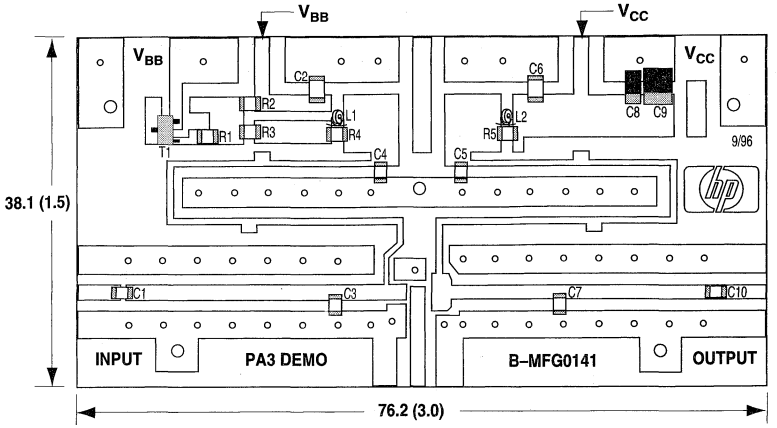
NOTE:
Dimensions are shown in millimeters (inches).



Test Circuit A: Test Circuit Schematic Diagram @ 900 MHz (ETACS/ISM)



Test Circuit B: Test Circuit Board Layout @ 836.5 MHz (AMPS)

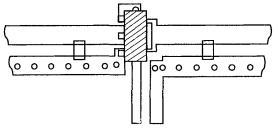


C1	100.0 pF
C2	100.0 nF
C3	9.5 pF
C4	100.0 pF
C5	100.0 pF
C6	100.0 nF
C7	6.8 pF
C8	1.5 µF
C9	10.0 µF
C10	100.0 pF
R1	2.2 Ω
R2	750.0 Ω
R3	2.2 Ω
R4	10.0 Ω
R5	10.0 Ω
T1	MBT 2222A
L1	18.0 µH
L2	18.0 µH

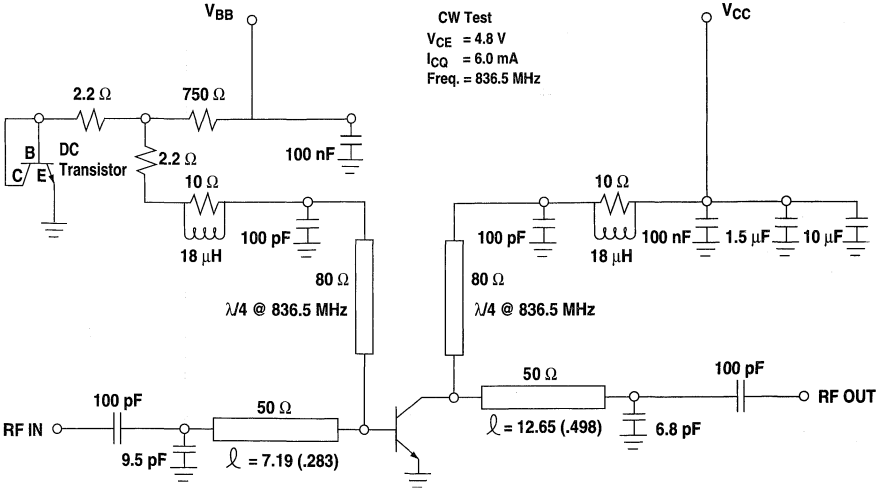
CW Test
V_{CE} = 4.8 V
I_{CQ} = 6.0 mA
Freq. = 836.5 MHz

Test Circuit:
FR-4 Microstrip, glass epoxy board
Dielectric Constant = 4.5
Thickness = 0.79 (.031)

NOTE:
Dimensions are shown in millimeters (inches).



Test Circuit B: Test Circuit Schematic Diagram @ 836.5 MHz (AMPS)

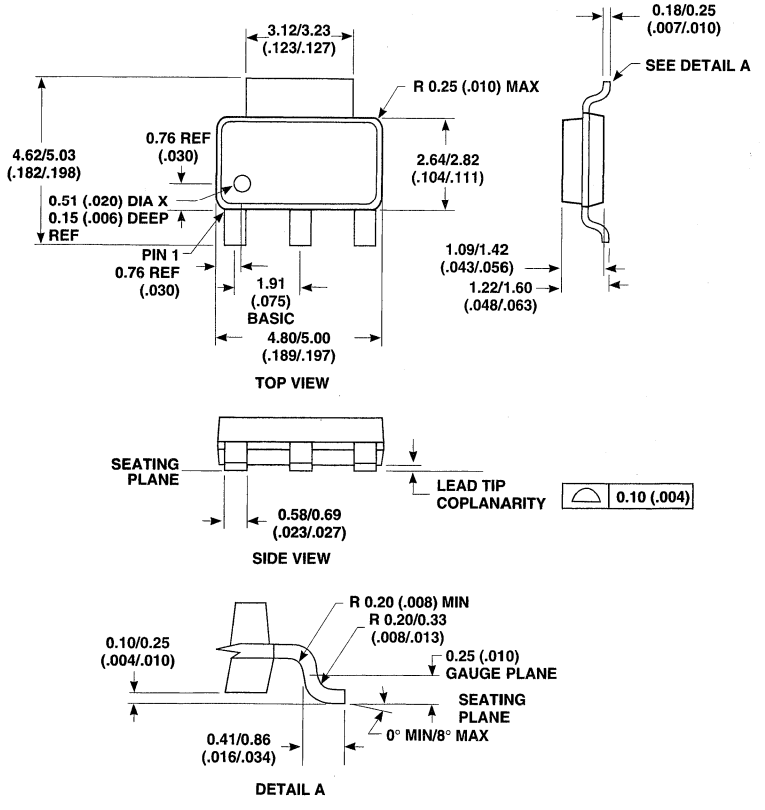


Part Number Ordering Information

Part Number	No. of Devices	Container
AT-33225-TR1	1000	7" Reel
AT-33225-BLK	25	Carrier Tape

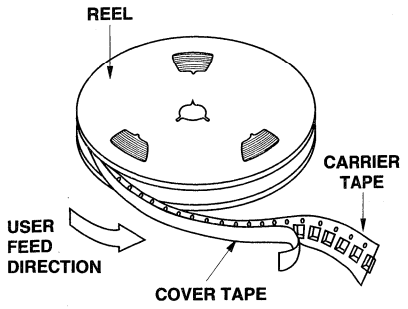
Package Dimensions

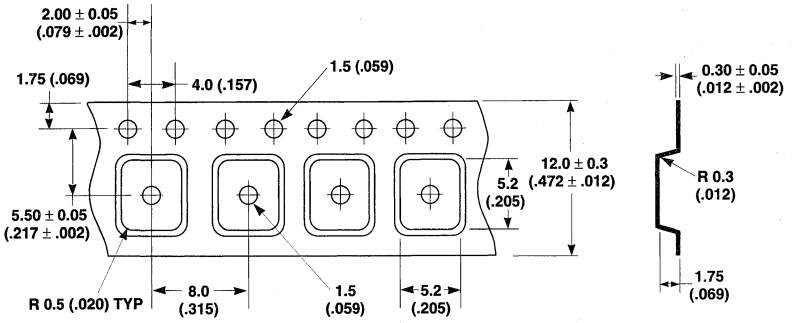
MSOP-3 Surface Mount Plastic Package



NOTE:
DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)

Tape Dimensions and Product Orientation for Package MSOP-3





NOTES:
1. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. TOLERANCES: .X ± 0.1 (.XXX ± .004)

HEWLETT® PACKARD

4.8 V NPN Common Emitter Output Power Transistor for GSM Class IV Phones

Technical Data

AT-36408

Features

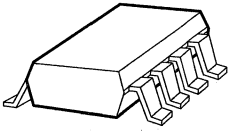
- **4.8 Volt Pulsed Operation (pulse width = 577 μsec, duty cycle = 12.5%)**
- **+35.0 dBm P_{out} @ 900 MHz, Typ.**
- **65% Collector Efficiency @ 900 MHz, Typ.**
- **9 dB Power Gain @ 900 MHz, Typ.**
- **Internal Input Pre-Matching Facilitates Cascading**

Applications

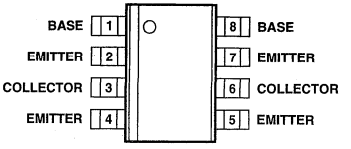
- **Output Power Device for GSM Class IV Handsets**

SOIC-8 Surface Mount Plastic Package

Outline P8



Pin Configuration



Description

Hewlett Packard's AT-36408 combines internal input pre-matching with low cost, NPN power silicon bipolar junction transistors in a SOIC-8 surface mount plastic package. This device is designed for use as the output device for GSM Class IV handsets. At 4.8 volts, the device features +35 dBm pulsed output power, superior power added efficiency, and excellent gain, making the AT-36408 an excellent choice for battery powered systems.

The AT-36408 is fabricated with Hewlett Packard's 10 GHz F_t Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices.

AT-36408 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.4
V_{CBO}	Collector-Base Voltage	V	16.0
V_{CEO}	Collector-Emitter Voltage	V	9.5
I_C	Collector Current[2]	A	1.7
P_T	Peak Power Dissipation[2, 3]	W	8.6
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[4]:
$\theta_{jc} = 60°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. Pulsed operation, pulse width = 577 µsec, duty cycle = 12.5%.
3. Derate at 133.3 mW/°C for $T_C > 85°C$. T_C is defined to be the temperature of the collector pins 3 and 6, where the lead contacts the circuit board.
4. Using the liquid crystal technique, $V_{CE} = 4.5$ V, $I_c = 100$ mA, $T_j = 150°C$, 1-2 µm "hot-spot" resolution.

Electrical Specifications, $T_C = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
	Freq. = 900 MHz, $V_{CE} = 4.8$ V, $I_{CQ} = 50$ mA, pulsed operation, pulse width = 577 µsec, duty cycle = 12.5%, Test Circuit A,unless otherwise specified					
P_{out}	Output Power[1]	$P_{in} = +26$ dBm	dBm	+34.0	+35.0	
η_C	Collector Efficiency[1]	$P_{in} = +26$ dBm	%	55	65	
H2	2nd Harmonic[1]	$F_0 = 900$ MHz	dBc		-50	
H3	3rd Harmonic[1]	$F_0 = 900$ MHz	dBc		-40	
	Mismatch Tolerance, No Damage[1]	$P_{out} = +35$ dBm any phase, 2 sec duration				7:1
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = 0.8$ mA, open collector	V	1.4		
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = 4.0$ mA, open emitter	V	16.0		
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = 20.0$ mA, open base	V	9.5		
h_{FE}	Forward Current Transfer Ratio	$V_{CE} = 3$ V, $I_C = 180$ mA	—	80	150	330
I_{CEO}	Collector Leakage Current	$V_{CEO} = 5$ V	µA			50

Note:
1. With external matching on input and output, tested in a 50 ohm environment. Refer to Test Circuit A (GSM).

AT-36408 Typical Performance, T_C = 25°C

Frequency = 900 MHz, V_{CE} = 4.8 V, I_{CQ} = 50 mA, pulsed operation, pulse width = 577 µsec, duty cycle = 12.5%, Test Circuit A (GSM), unless otherwise specified.

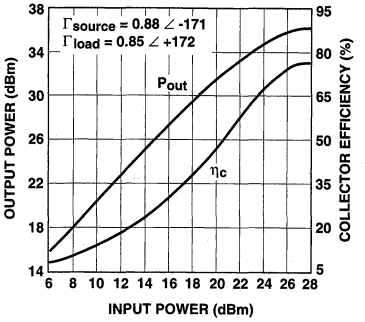


Figure 1. Output Power and Collector Efficiency vs. Input Power.

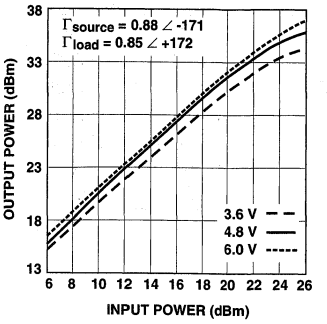


Figure 2. Output Power vs. Input Power Over Bias Voltage.

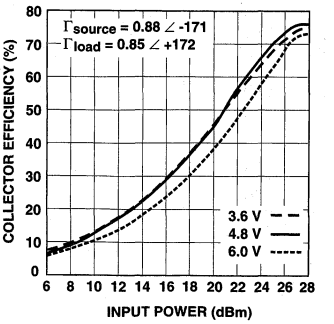


Figure 3. Collector Efficiency vs. Input Power Over Bias Voltage.

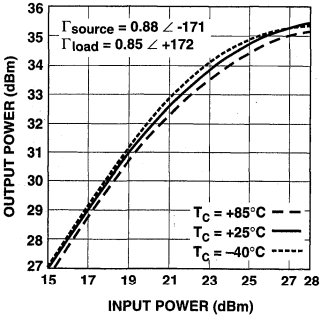


Figure 4. Output Power vs. Input Power Over Temperature.

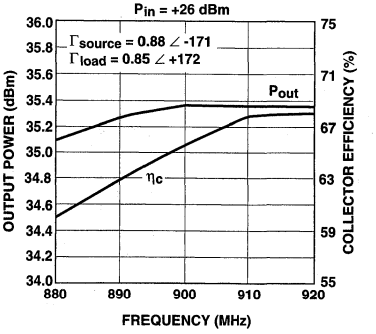


Figure 5. Output Power and Collector Efficiency vs. Frequency.

Note: Tuned at 900 MHz, then swept over frequency.

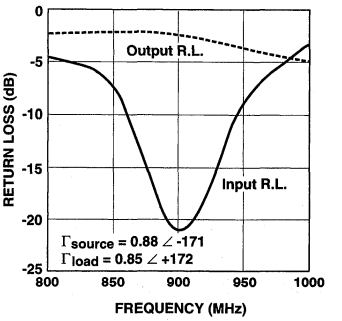


Figure 6. Input and Output Return Loss vs. Frequency.

AT-36408 Typical Large Signal Impedances

V_{CE} = 4.8 V, I_{CQ} = 50 mA, Pulsed Operation, P_{out} = +35.0 dBm

Freq. MHz	Γ source		Γ load	
	Mag.	Ang.	Mag.	Ang.
880	0.882	-170.0	0.847	172.7
890	0.885	-170.5	0.849	172.2
900	0.887	-171.1	0.851	171.6
910	0.890	-171.4	0.853	171.1
915	0.891	-169.0	0.854	168.4
920	0.893	-168.4	0.855	168.2

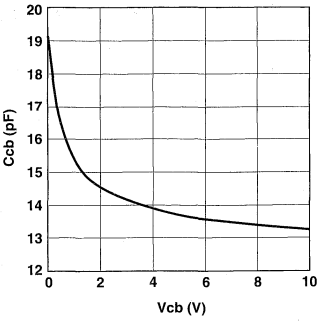
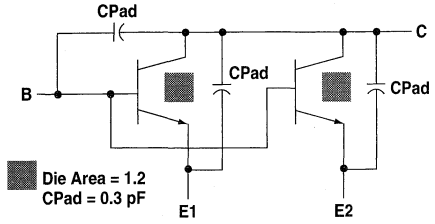


Figure 7. Collector-Base Capacitance vs. Collector-Base Voltage (DC Test).

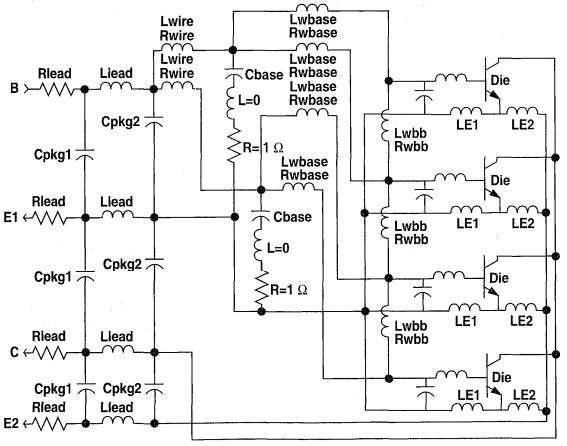
SPICE Model Parameters

Die Model



Label	Value	Label	Value
BF	280	TR	1E-9
IKF	299.9	EG	1.11
ISE	9.9E-11	IS	3.598E-15
NE	2.399	XTI	3
VAF	33.16	CJC	0.8E-12
NF	0.9935	VJC	0.4831
TF	1.6E-11	MJC	0.2508
XTF	0.006656	XCJC	0.001
VTF	0.02785	FC	0.999
ITF	0.001	CJE	6.16E-12
PTF	23	VJE	1.186
XTB	0	MJE	0.5965
BR	54.61	RB	0.752
IKR	81	IRB	0
ISC	8.7E-13	RBM	0.01
NC	1.587	RE	1.27
VAR	1.511	RC	0.107
NR	0.9886		

Packaged Model



Label	Value	Label	Value
Rlead	0.63 Ω	LE2	0.00064 nH
Llead	1.45 nH	Cbase	46.0 pF
Rwire	1.3 Ω	Rwbase	0.2 Ω
Lwire	0.52 nH	Lwbase	1.19 nH
Cpkg1	0.4 pF	Rwbb	0.1 Ω
Cpkg2	1.2 pF	Lwbb	0.1 nH
LE1	0.3 nH		

AT-36408 Typical Scattering Parameters, Common Emitter, $Z_0 = 50\ \Omega$

V_{CE} = 3.6 V, I_c = 200 mA, T_c = 25°C

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.05	0.96	-175	22.3	13.08	93	-38.4	0.012	11	0.74	-169
0.10	0.96	-178	16.4	6.61	88	-37.7	0.013	13	0.74	-174
0.25	0.96	177	8.8	2.76	80	-36.5	0.015	24	0.75	-177
0.50	0.94	173	4.2	1.63	66	-34.4	0.019	33	0.73	-177
0.75	0.90	169	3.4	1.49	46	-32.0	0.025	27	0.71	-172
0.90	0.84	168	4.2	1.63	24	-32.0	0.025	10	0.72	-165
1.00	0.79	170	4.6	1.70	0	-34.0	0.020	-14	0.81	-160
1.25	0.92	175	-1.2	0.87	-68	-37.1	0.014	126	1.01	-172
1.50	0.97	169	-9.6	0.33	-98	-30.2	0.031	97	0.96	-177
V_{CE} = 4.8 V, I_c = 200 mA, T_c = 25°C										
0.05	0.96	-174	22.6	13.42	93	-37.7	0.013	11	0.74	-169
0.10	0.96	-178	16.6	6.79	88	-37.7	0.013	13	0.73	-174
0.25	0.96	178	9.0	2.83	80	-36.5	0.015	23	0.74	-177
0.50	0.94	173	4.4	1.66	66	-34.4	0.019	32	0.72	-176
0.75	0.90	169	3.6	1.51	46	-32.4	0.024	26	0.70	-172
0.90	0.84	168	4.3	1.64	24	-32.0	0.025	9	0.72	-164
1.00	0.80	170	4.6	1.71	0	-34.0	0.020	-14	0.81	-160
1.25	0.92	175	-1.0	0.89	-67	-37.1	0.014	126	1.01	-171
1.50	0.97	169	-9.4	0.34	-97	-30.2	0.031	97	0.96	-177
V_{CE} = 6.0 V, I_c = 200 mA, T_c = 25°C										
0.05	0.96	-174	22.7	13.60	93	-37.7	0.013	12	0.73	-169
0.10	0.96	-178	16.7	6.88	88	-37.1	0.014	14	0.72	-174
0.25	0.96	178	9.2	2.87	79	-35.9	0.016	23	0.73	-177
0.50	0.94	173	4.5	1.68	65	-34.0	0.020	30	0.71	-176
0.75	0.90	169	3.7	1.52	45	-32.0	0.025	24	0.69	-171
0.90	0.85	168	4.3	1.64	23	-32.0	0.025	8	0.72	-164
1.00	0.80	170	4.6	1.70	0	-34.0	0.020	-14	0.81	-159
1.25	0.92	175	-1.0	0.90	-67	-37.7	0.013	125	1.01	-171
1.50	0.97	169	-9.2	0.35	-97	-30.2	0.031	96	0.95	-177

Typical Performance

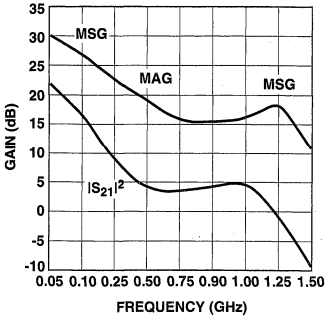


Figure 8. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{CE} = 3.6 V, I_c = 200 mA.

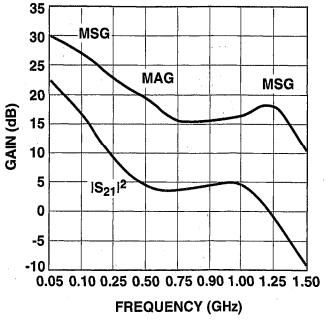


Figure 9. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{CE} = 4.8 V, I_c = 200 mA.

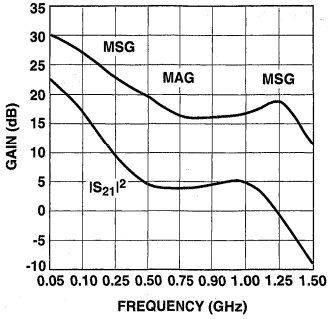
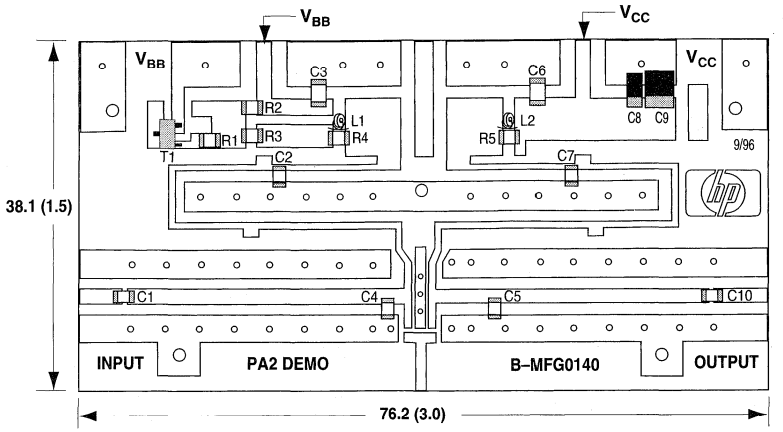


Figure 10. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{CE} = 6.0 V, I_c = 200 mA.

Test Circuit A: Test Circuit Board Layout @ 900 MHz (GSM)

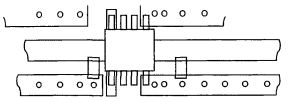


C1	39.0 pF
C2	39.0 pF
C3	100.0 nF
C4	12.5 pF
C5	11.5 pF
C6	100.0 nF
C7	39.0 pF
C8	1.5 µF
C9	10.0 µF
C10	39.0 pF
R1	2.2 Ω
R2	619.0 Ω
R3	2.2 Ω
R4	10.0 Ω
R5	10.0 Ω
T1	MBT 2222A
L1	18.0 µH
L2	18.0 µH

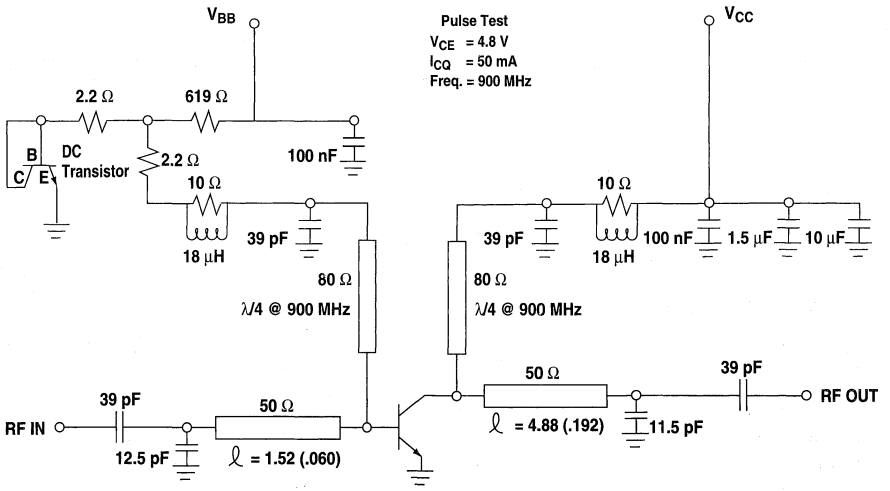
Pulse Test
V_{CE} = 4.8 V
I_{CQ} = 50 mA
Freq. = 900 MHz

Test Circuit:
FR-4 Microstrip, glass epoxy board
Dielectric Constant = 4.5
Thickness = 0.79 (.031)

NOTE:
Dimensions are shown in millimeters (inches).



Test Circuit A: Test Circuit Schematic Diagram @ 900 MHz (GSM)

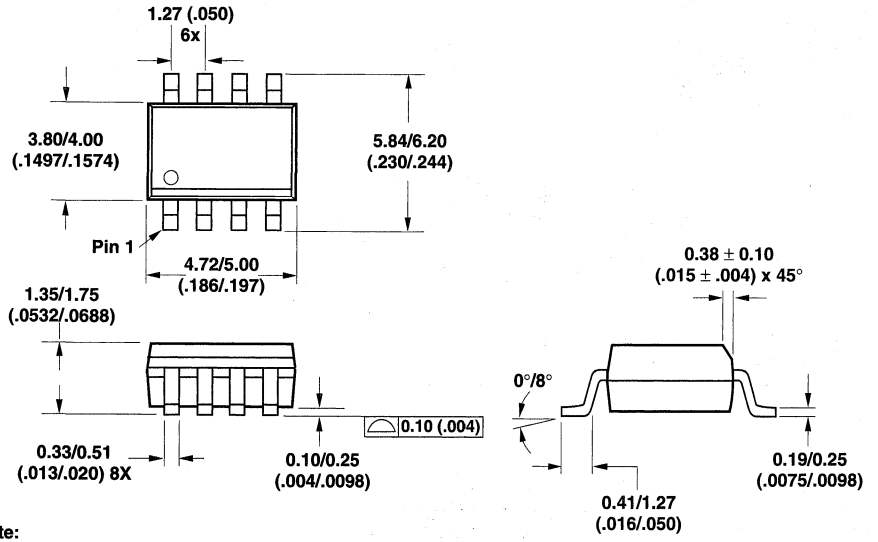


Part Number Ordering Information

Part Number	No. of Devices	Container
AT-36408-TR1	1000	7" Reel
AT-36408-BLK	25	Carrier Tape

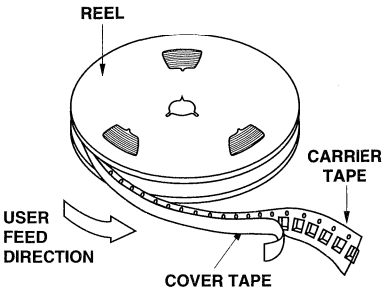
Package Dimensions

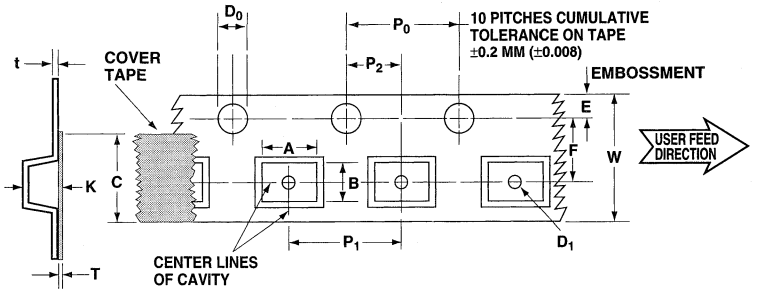
SOIC-8 Surface Mount Plastic Package



Note:
1. Dimensions are shown in millimeters (inches).

Tape Dimensions and Product Orientation For Package SOIC-8





DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A	6.45 ± 0.10	0.254 ± 0.004
	WIDTH	B	5.13 ± 0.10	0.202 ± 0.004
	DEPTH	K	2.11 ± 0.10	0.083 ± 0.004
	PITCH	P_1	8.00 ± 0.10	0.315 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.50 min.	0.059 min.
PERFORATION	DIAMETER	D_0	1.50 + 0.10/-0	0.059 + 0.004/-0
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t	0.255 ± 0.013	0.0100 ± 0.0005
COVER TAPE	WIDTH	C	9.19 ± 0.10	0.362 ± 0.004
	TAPE THICKNESS	T	0.051 ± 0.010	0.0020 ± 0.0004
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	5.51 ± 0.05	0.217 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

4.8 V NPN Silicon Bipolar Common Emitter Transistor

Technical Data

AT-38086

Features

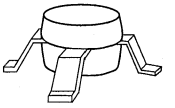
- **4.8 Volt Pulsed (pulse width = 577 μsec, duty cycle = 12.5%)/CW Operation**
- **+28 dBm Pulsed P_{out} @ 900 MHz, Typ.**
- **+23.5 dBm CW P_{out} @ 836.5 MHz, Typ.**
- **60% Pulsed Collector Efficiency @ 900 MHz, Typ.**
- **11 dB Pulsed Power Gain @ 900 MHz, Typ.**
- **-35 dBc IMD_3 @ P_{out} of 17 dBm per tone, 900 MHz, Typ.**

Applications

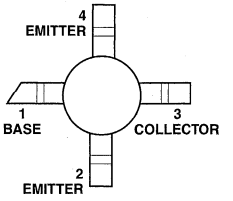
- **Driver Amplifier for GSM and AMPS/ETACS/ 900 MHz NMT Cellular Phones**
- **900 MHz ISM and Special Mobile Radio**

85 mil Plastic Surface Mount Package

Outline 86



Pin Configuration



Description

Hewlett Packard's AT-38086 is a low cost, NPN silicon bipolar junction transistor housed in a surface mount plastic package. This device is designed for use as a pre-driver or driver device in applications for cellular and wireless communications markets. At 4.8 volts, the AT-38086 features +28 dBm pulsed output power, Class AB operation, and +23.5 dBm CW. Superior efficiency and gain makes the AT-38086 an excellent choice for battery powered systems.

The AT-38086 is fabricated with Hewlett Packard's 10 GHz F_t Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices.

AT-38086 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.4
V_{CBO}	Collector-Base Voltage	V	16.0
V_{CEO}	Collector-Emitter Voltage	V	9.5
I_C	Collector Current[2]	mA	250
I_C	Collector Current[3]	mA	160
P_T	Peak Power Dissipation[2, 4]	W	3.7
P_T	CW Power Dissipation[3, 5]	mW	460
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[6]:
$\theta_{jc} = 140°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. Pulsed operation, pulse width = 577 µsec, duty cycle = 12.5%.
3. CW operation.
4. Derate at 57.1 mW/°C for $T_C > 85°C$. T_C is defined to be the temperature of the collector pin 3, where the lead contacts the circuit board.
5. Derate at 7.1 mW/°C for $T_C > 85°C$. T_C is defined to be the temperature of the collector pin 3, where the lead contacts the circuit board.
6. Using the liquid crystal technique, $V_{CE} = 4.5$ V, $I_C = 50$ mA, $T_j = 150°C$, 1-2 µm "hot-spot" resolution.

Electrical Specifications, $T_C = 25°C$

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
	Freq. = 900 MHz, $V_{CE} = 4.8$ V, $I_{CQ} = 20$ mA, Pulse width = 577 µsec, duty cycle = 12.5%, unless otherwise specified				
P_{out}	Output Power, Pulsed Operation[1] — Test Circuit A, $P_{in} = +17$ dBm	dBm	+26.5	+28.0	
η_C	Collector Efficiency, Pulsed Operation[1] — Test Circuit A, $P_{in} = +17$ dBm	%	50	60	
	Mismatch Tolerance, No Damage, Pulsed[1] — Test Circuit A, $P_{out} = +28$ dBm, any phase, 2 sec duration				7:1
P_{out}	Output Power, CW Operation[2] — F = 836.5 MHz, $I_{CQ} = 15$ mA, Test Circuit B, $P_{in} = +10$ dBm	dBm	+22.0	+23.5	
IMD_3	3rd Order Intermodulation Distortion, 2-Tone Test, P_{out} each tone = +17 dBm, CW[2,3] — F1 = 899 MHz, F2 = 901 MHz, $I_{CQ} = 15$ mA, Test Circuit B	dBc		-35	
	Mismatch Tolerance, No Damage, CW[2] — F = 836.5 MHz, $I_{CQ} = 15$ mA, Test Circuit B, $P_{out} = +23.5$ dBm, any phase, 2 sec duration				7:1
BV_{EBO}	Emitter-Base Breakdown Voltage — $I_E = 0.2$ mA, open collector	V	1.4		
BV_{CBO}	Collector-Base Breakdown Voltage — $I_C = 1.0$ mA, open emitter	V	16.0		
BV_{CEO}	Collector-Emitter Breakdown Voltage — $I_C = 3.0$ mA, open base	V	9.5		
h_{FE}	Forward Current Transfer Ratio — $V_{CE} = 3$ V, $I_C = 160$ mA	—	40	150	330
I_{CEO}	Collector Leakage Current — $V_{CEO} = 5$ V	µA			15

Notes:
1. With external matching on input and output, tested in a 50 ohm environment. Refer to Test Circuit A (GSM).
2. With external matching on input and output, tested in a 50 ohm environment. Refer to Test Circuit B (AMPS).
3. Test circuit B re-tuned at 900 MHz.

AT-38086 Typical Performance, T_C = 25°C

Frequency = 900 MHz, V_{CE} = 4.8 V, I_{CQ} = 20 mA, pulsed operation, pulse width = 577 µsec, duty cycle = 12.5%, Test Circuit A (GSM), unless otherwise specified

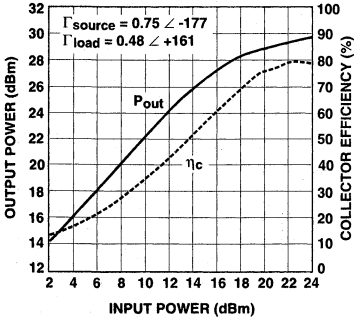


Figure 1. Output Power and Collector Efficiency vs. Input Power.

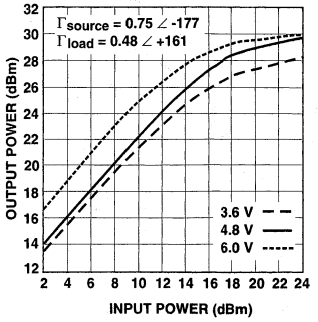


Figure 2. Output Power vs. Input Power Over Bias Voltage.

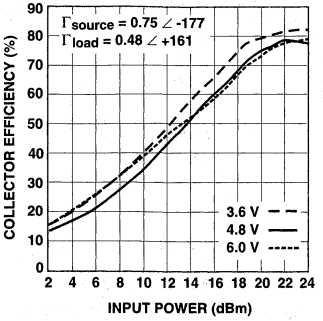


Figure 3. Collector Efficiency vs. Input Power Over Bias Voltage.

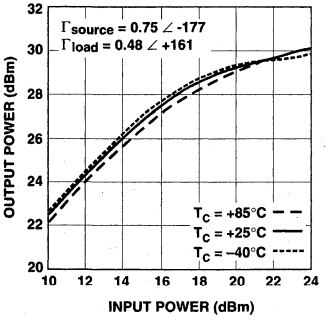


Figure 4. Output Power vs. Input Power Over Temperature.

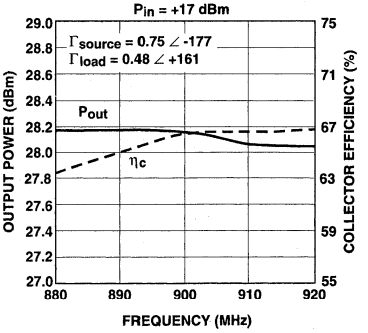


Figure 5. Output Power and Collector Efficiency vs. Frequency.
Note: Tuned at 900 MHz, then Swept over Frequency.

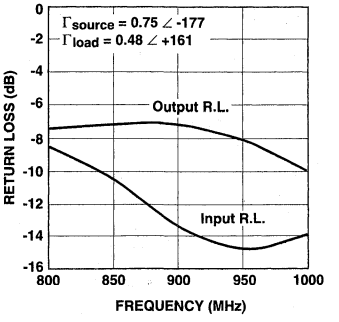


Figure 6. Input and Output Return Loss vs. Frequency.

AT-38086 Typical Performance, T_C = 25°C

Freq. = 836.5 MHz, V_{CE} = 4.8 V, I_{CQ} = 15 mA, CW operation, Test Circuit B (AMPS), unless otherwise specified

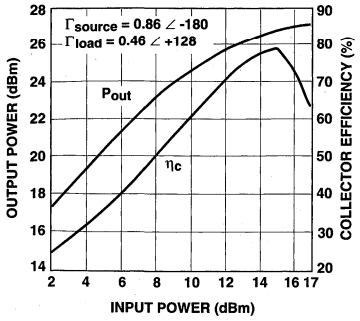


Figure 7. Output Power and Collector Efficiency vs. Input Power.

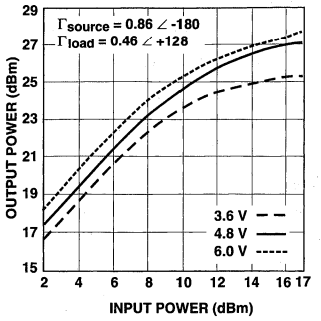


Figure 8. Output Power vs. Input Power Over Bias Voltage.

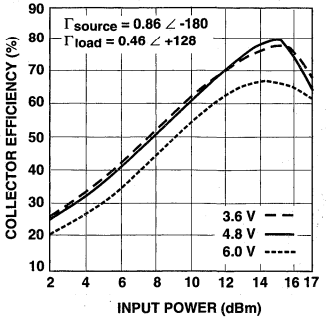


Figure 9. Collector Efficiency vs. Input Power Over Bias Voltage.

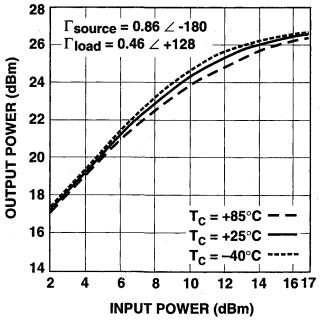


Figure 10. Output Power vs. Input Power Over Temperature.

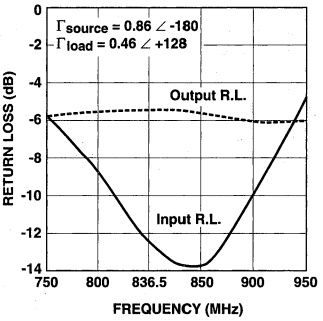


Figure 11. Input and Output Return Loss vs. Frequency.

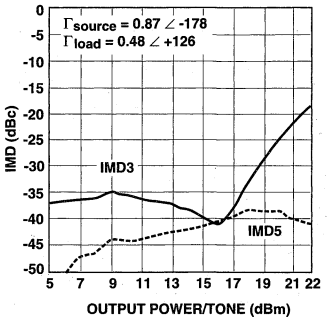


Figure 12. IMD3, IMD5 vs. Output Power Per Tone.

Note: Test circuit B (AMPS) used and re-tuned at 900 MHz.

AT-38086 Typical Large Signal Impedances (GSM)

Freq. = 900 MHz, V_{CE} = 4.8 V, I_{CQ} = 20 mA, Pulsed Operation, P_{out} = +28.0 dBm

Freq. MHz	Γ source		Γ load	
	Mag.	Ang.	Mag.	Ang.
880	0.743	-175.6	0.474	162.0
890	0.741	-176.4	0.476	161.5
900	0.747	-177.3	0.478	161.2
910	0.751	-178.1	0.481	160.0
915	0.752	-178.6	0.482	159.6
920	0.754	-179.1	0.483	158.9

AT-38086 Typical Large Signal Impedances (AMPS)

Freq. = 836.5 MHz, V_{CE} = 4.8 V, I_{CQ} = 15 mA, CW Operation, P_{out} = +23.5 dBm

Freq. MHz	Γ source		Γ load	
	Mag.	Ang.	Mag.	Ang.
824	0.856	-178.9	0.455	129.1
836.5	0.864	-179.9	0.459	128.2
849	0.870	-179.1	0.464	127.3

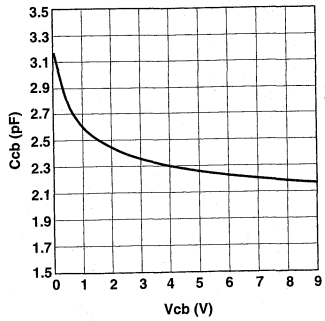
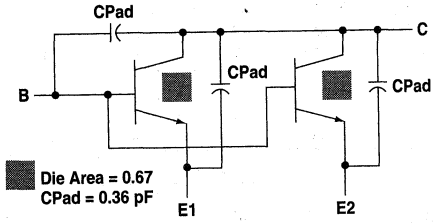


Figure 13. Collector-Base Capacitance vs. Collector-Base Voltage (DC Test).

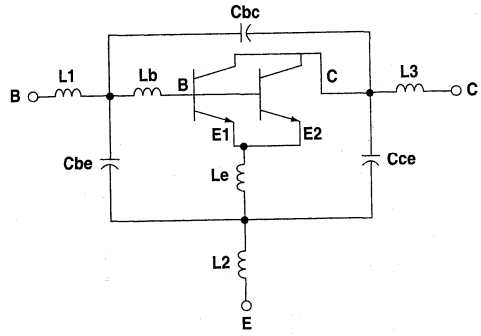
SPICE Model Parameters

Die Model



Label	Value	Label	Value
BF	280	NR	0.9886
IKF	299.9	TR	1E-9
ISE	9.9E-11	EG	1.11
NE	2.399	IS	3.598E-15
VAF	33.16	XTI	3
NF	0.9935	CJC	1.02 pF
TF	1.6E-11	VJC	0.4276
XTF	0.006656	MJC	0.2508
VTF	0.02785	XCJC	0.001
ITF	0.001	FC	0.999
PTF	23	CJE	0.98 pF
XTB	0	VJE	0.811
BR	54.61	MJE	0.596
IKR	81	RB	5.435
ISC	8.7E-13	RE	1.30
NC	1.587	RC	0.01
VAR	1.511		

Packaged Model



Label	Value
Cbe	0.032 pF
Cbc	0.036 pF
Cce	0.122 pF
L1	0.46 nH
L2	0.46 nH
L3	0.46 nH
Lb	0.47 nH
Le	0.14 nH

AT-38086 Typical Scattering Parameters, Common Emitter, Z_0 = 50 Ω

V_{CE} = 3.6 V, I_c = 50 mA, T_c = 25°C

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.05	0.71	-85	31.7	38.52	138	-31.7	0.026	54	0.75	-57
0.10	0.73	-124	28.2	25.72	118	-29.1	0.035	39	0.56	-90
0.25	0.75	-160	21.3	11.66	84	-27.3	0.043	35	0.39	-133
0.50	0.76	-176	15.5	5.95	76	-25.5	0.053	43	0.36	-155
0.75	0.76	175	12.0	3.98	72	-23.6	0.066	50	0.36	-165
0.90	0.77	171	10.4	3.32	69	-22.6	0.074	52	0.36	-168
1.00	0.77	169	9.5	2.99	63	-22.0	0.079	54	0.37	-170
1.25	0.78	164	7.6	2.39	57	-20.5	0.094	56	0.38	-174
1.50	0.78	160	6.0	1.99	51	-19.3	0.108	57	0.40	-176
1.75	0.79	156	4.7	1.71	46	-18.3	0.122	57	0.41	-179
2.00	0.80	152	3.5	1.49	41	-17.3	0.137	57	0.43	179
2.25	0.80	148	2.5	1.33	37	-16.4	0.151	57	0.45	176
2.50	0.81	145	1.5	1.19	32	-15.7	0.164	56	0.47	174
2.75	0.81	142	0.7	1.08	28	-15.0	0.178	55	0.49	172
3.00	0.82	139	-0.1	0.99	25	-14.4	0.191	54	0.51	169
V_{CE} = 4.8 V, I_c = 50 mA, T_c = 25°C										
0.05	0.72	-82	31.8	39.02	139	-31.7	0.026	54	0.76	-55
0.10	0.73	-121	28.4	26.32	119	-29.1	0.035	40	0.56	-87
0.25	0.75	-158	21.6	12.00	97	-27.3	0.043	35	0.38	-130
0.50	0.75	-176	15.8	6.14	85	-25.5	0.053	43	0.35	-154
0.75	0.76	176	12.3	4.10	76	-23.7	0.065	49	0.35	-163
0.90	0.76	172	10.7	3.42	72	-22.7	0.073	52	0.35	-167
1.00	0.76	169	9.8	3.08	69	-22.0	0.079	53	0.36	-169
1.25	0.77	164	7.8	2.46	63	-20.6	0.093	56	0.37	-172
1.50	0.78	160	6.2	2.05	57	-19.4	0.107	57	0.38	-175
1.75	0.78	156	4.9	1.76	51	-18.3	0.121	58	0.40	-178
2.00	0.79	152	3.8	1.54	46	-17.4	0.135	57	0.42	180
2.25	0.80	149	2.7	1.37	41	-16.5	0.150	57	0.44	177
2.50	0.80	145	1.8	1.23	37	-15.8	0.163	56	0.46	175
2.75	0.81	142	1.0	1.12	32	-15.0	0.177	55	0.48	173
3.00	0.82	139	0.2	1.02	28	-14.4	0.190	55	0.50	170
V_{CE} = 6.0 V, I_c = 50 mA, T_c = 25°C										
0.05	0.73	-79	31.8	39.07	140	-32.0	0.025	55	0.76	-54
0.10	0.74	-119	28.5	26.60	120	-29.1	0.035	40	0.56	-85
0.25	0.74	-157	21.7	12.21	98	-27.3	0.043	35	0.38	-128
0.50	0.75	-175	15.9	6.25	85	-25.5	0.053	42	0.34	-152
0.75	0.75	176	12.4	4.18	76	-23.7	0.065	49	0.34	-162
0.90	0.76	172	10.8	3.48	72	-22.7	0.073	52	0.34	-166
1.00	0.76	170	9.9	3.13	69	-22.2	0.078	53	0.34	-167
1.25	0.77	165	8.0	2.51	63	-20.7	0.092	56	0.36	-171
1.50	0.77	160	6.4	2.09	57	-19.5	0.106	57	0.37	-174
1.75	0.78	156	5.1	1.79	51	-18.4	0.120	57	0.39	-177
2.00	0.79	152	3.9	1.56	46	-17.5	0.134	58	0.41	-179
2.25	0.79	149	2.9	1.39	41	-16.6	0.148	57	0.43	178
2.50	0.80	146	1.9	1.25	37	-15.8	0.162	56	0.45	176
2.75	0.81	142	1.1	1.13	32	-15.1	0.175	56	0.47	174
3.00	0.81	139	0.3	1.03	28	-14.5	0.188	55	0.49	171

Typical Performance

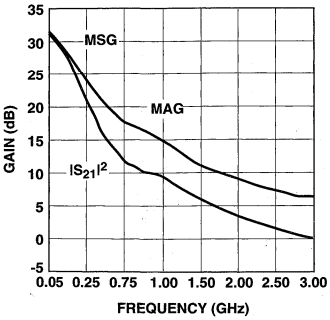


Figure 14. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{CE} = 3.6 V, I_C = 50 mA.

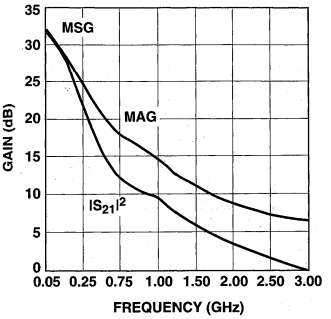


Figure 15. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{CE} = 4.8 V, I_C = 50 mA.

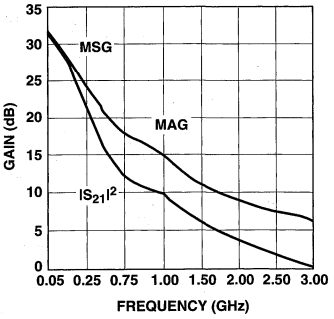


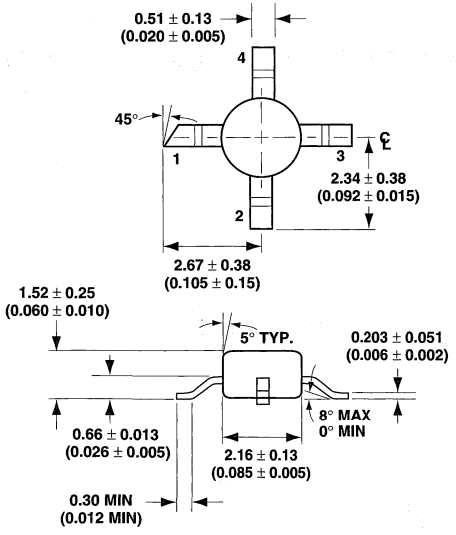
Figure 16. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{CE} = 6.0 V, I_C = 50 mA.

Part Number Ordering Information

Part Number	No. of Devices	Container
AT-38086-TR1	1000	7" Reel
AT-38086-BLK	100	Antistatic Bag

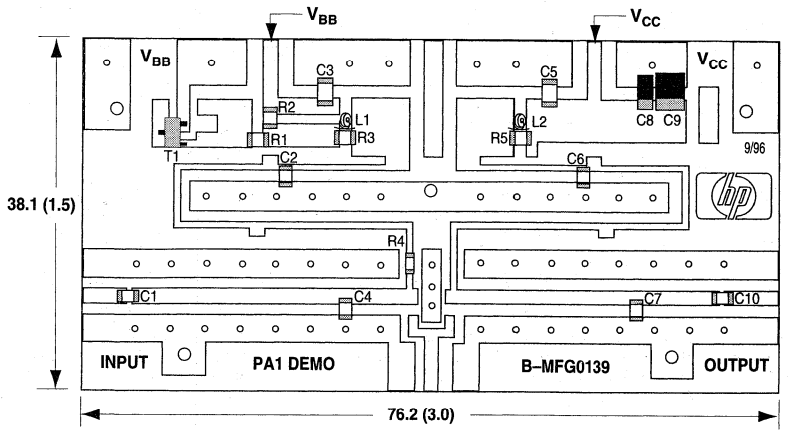
Package Dimensions

Outline 86



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Test Circuit A: Test Circuit Board Layout @ 900 MHz for Pulsed Operation (GSM)

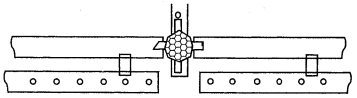


C1	100.0 pF
C2	100.0 pF
C3	100.0 nF
C4	8.2 pF
C5	100.0 nF
C6	100.0 pF
C7	3.6 pF
C8	1.5 µF
C9	10.0 µF
C10	100.0 pF
R1	10.0 Ω
R2	619.0 Ω
R3	10.0 Ω
R4	40.0 Ω
R5	10.0 Ω
T1	MBT 2222A
L1	18.0 µH
L2	18.0 µH

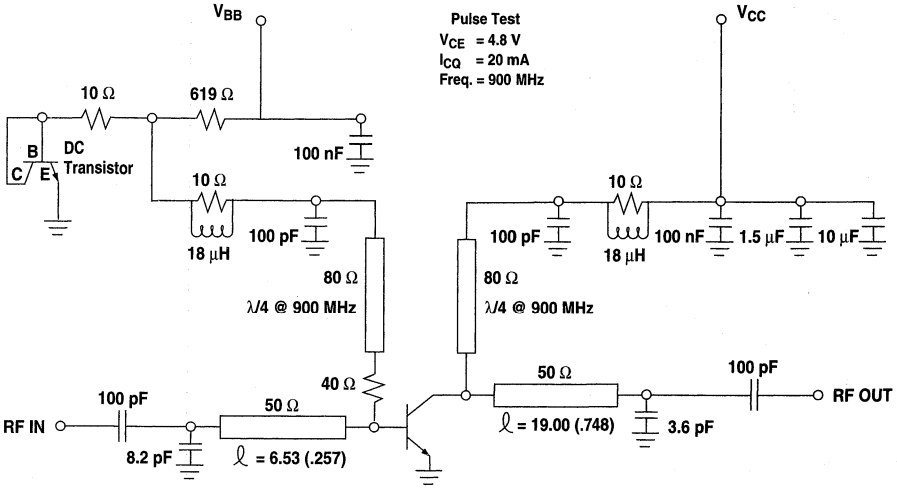
Pulse Test
V_{CE} = 4.8 V
I_{CQ} = 20 mA
Freq. = 900 MHz

Test Circuit:
FR-4 Microstrip, glass epoxy board
Dielectric Constant = 4.5
Thickness = 0.79 (.031)

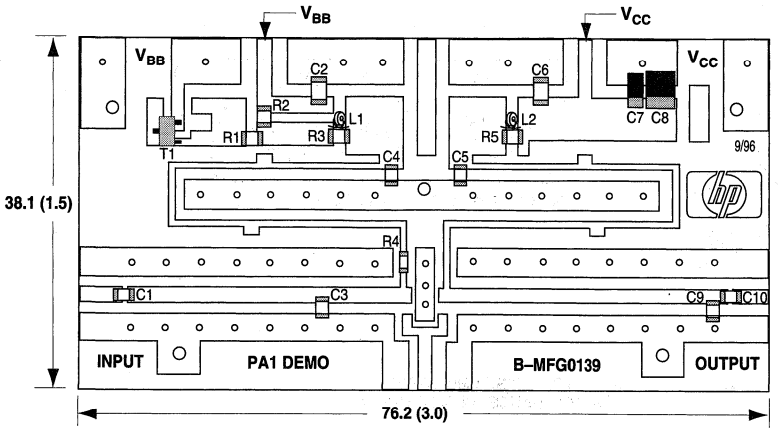
NOTE:
Dimensions are shown in millimeters (inches).



Test Circuit A: Test Circuit Schematic Diagram @ 900 MHz for Pulsed Operation (GSM)



Test Circuit B: Test Circuit Board Layout @ 836.5 MHz for CW Operation (AMPS)

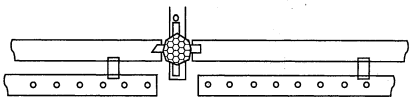


C1	100.0 pF
C2	100.0 nF
C3	11.0 pF
C4	100.0 pF
C5	100.0 pF
C6	100.0 nF
C7	1.5 µF
C8	10.0 µF
C9	4.7 pF
C10	100.0 pF
R1	10.0 Ω
R2	619.0 Ω
R3	10.0 Ω
R4	40.0 Ω
R5	10.0 Ω
T1	MBT 2222A
L1	18.0 µH
L2	18.0 µH

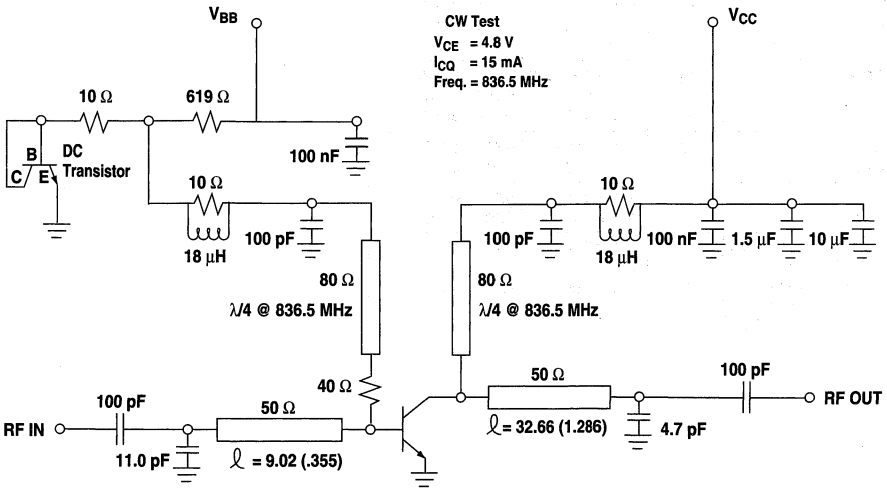
CW Test
V_{CE} = 4.8 V
I_{CQ} = 15 mA
Freq. = 836.5 MHz

Test Circuit:
FR-4 Microstrip, glass epoxy board
Dielectric Constant = 4.5
Thickness = 0.79 (.031)

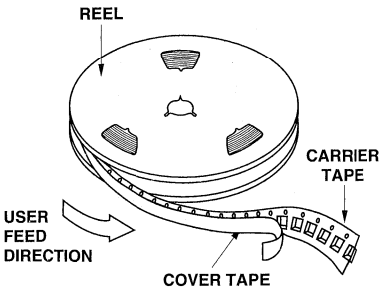
NOTE:
Dimensions are shown in millimeters (inches).

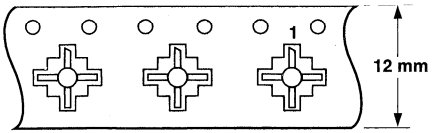


Test Circuit B: Test Circuit Schematic Diagram @ 836.5 MHz for CW Operation (AMPS)

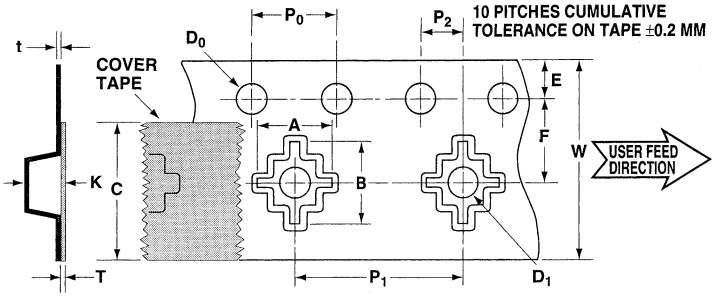


Tape Dimensions and Product Orientation for Outline 86





NOTE: 1 INDICATES PIN 1 ORIENTATION



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A	5.77 ± 0.10	0.227 ± 0.004
	WIDTH	B	6.10 ± 0.10	0.240 ± 0.004
	DEPTH	K	1.70 ± 0.10	0.067 ± 0.004
	PITCH	P_1	8.00 ± 0.10	0.314 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.50 min.	0.059 min.
PERFORATION	DIAMETER	D_0	1.50 + 0.10/-0.05	0.059 + 0.004/-0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	12.00 ± 0.20	0.472 ± 0.008
	THICKNESS	t	0.30 ± 0.05	0.012 ± 0.002
COVER TAPE	WIDTH	C	9.30 ± 0.10	0.366 ± 0.004
	TAPE THICKNESS	T	0.065 ± 0.010	0.0026 ± 0.0004
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	5.50 ± 0.05	0.217 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

Up to 6 GHz Low Noise Silicon Bipolar Transistor Chip

Technical Data

AT-41400

Features

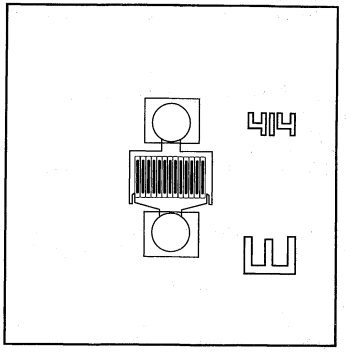
- **Low Noise Figure:**
  1.6 dB Typical at 2.0 GHz
  3.0 dB Typical at 4.0 GHz
- **High Associated Gain:**
  14.5 dB Typical at 2.0 GHz
  10.5 dB Typical at 4.0 GHz
- **High Gain-Bandwidth Product:**
  9.0 GHz Typical f_T

Description

Hewlett-Packard's AT-41400 is a general purpose NPN bipolar transistor chip that offers excellent high frequency performance. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 14 emitter finger interdigitated geometry yields an intermediate sized transistor with impedances that are easy to match for low noise and moderate power applications. This device is designed for use in low noise, wideband amplifier, mixer and oscillator applications in the VHF, UHF, and microwave frequencies. An optimum noise match near 50 Ω at 1 GHz , makes this device easy to use as a low noise amplifier.

The AT-41400 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

Chip Outline



5965-8922E

AT-41400 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	60
P_T	Power Dissipation[2,3]	mW	500
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to 200

Thermal Resistance[2,4]:
$\theta_{jc} = 95°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE} = 25°C$.
3. Derate at 10.5 mW/°C for $T_{MOUNTING\ SURFACE} > 153°C$.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

Part Number	Devices Per Tray
AT-41400-GP4	100

Note: For more information, see "Tape and Reel Packaging for Semiconductor Devices".

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; $V_{CE} = 8$ V, $I_C = 25$ mA	f = 2.0 GHz f = 4.0 GHz	dB		12.0 6.5	
$P_{1\ dB}$	Power Output @ 1 dB Gain Compression $V_{CE} = 8$ V, $I_C = 25$ mA	f = 2.0 GHz f= 4.0 GHz	dBm		19.0 18.5	
$G_{1\ dB}$	1 dB Compressed Gain; $V_{CE} = 8$ V, $I_C = 25$ mA	f = 2.0 GHz f = 4.0 GHz	dB		15.0 10.5	
NF_O	Optimum Noise Figure: $V_{CE} = 8$ V, $I_C = 10$ mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.3 1.6 3.0	
G_A	Gain @ NF_O; $V_{CE} = 8$ V, $I_C = 10$ mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		18.5 14.5 10.5	
f_T	Gain Bandwidth Product: $V_{CE} = 8$ V, $I_C = 25$ mA		GHz		9.0	
h_{FE}	Forward Current Transfer Ratio; $V_{CE} = 8$ V, $I_C = 10$ mA		—	30	150	300
I_{CBO}	Collector Cutoff Current; $V_{CB} = 8$ V		μA			0.2
I_{EBO}	Emitter Cutoff Current; $V_{EB} = 1$ V		μA			1.0
C_{CB}	Collector Base Capacitance[2]: $V_{CB} = 8$ V, f = 1 MHz		pF		0.17	

Notes:
1. RF performance is determined by packaging and testing 10 devices per wafer.
2. For this test, the emitter is grounded.

AT-41400 Typical Performance, T_A = 25°C

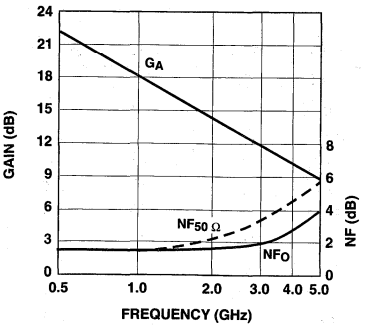


Figure 1. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

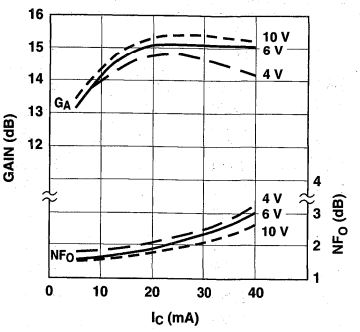


Figure 2. Optimum Noise Figure and Associated Gain vs. Collector Current and Collector Voltage. f = 2.0 GHz.

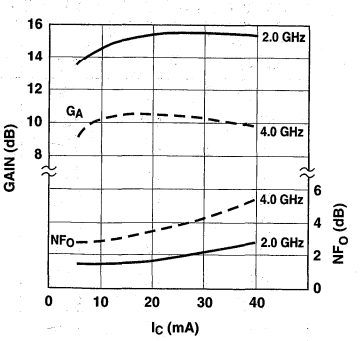


Figure 3. Optimum Noise Figure and Associated Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

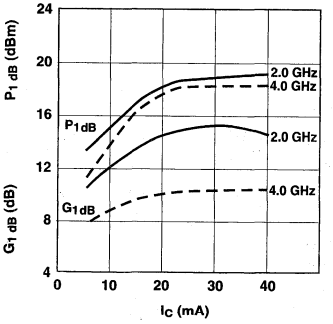


Figure 4. Output Power and 1 dB Compressed Gain vs. Collector Current. V_{CE} = 8 V.

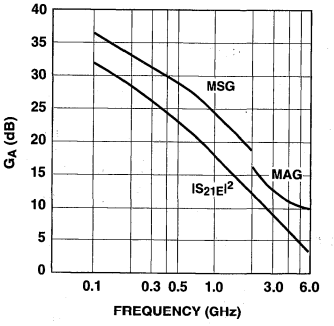


Figure 5. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 25 mA.

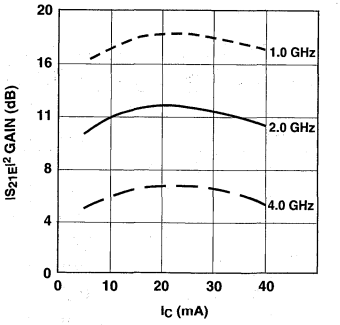


Figure 6. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

AT-41400 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.73	-39	28.3	25.84	159	-39.2	.011	75	.94	-12
0.5	.60	-121	22.2	12.91	113	-30.2	.031	48	.61	-28
1.0	.57	-156	17.2	7.27	94	-28.0	.040	51	.50	-25
1.5	.56	-172	13.7	4.84	84	-26.4	.048	59	.47	-25
2.0	.57	176	11.4	3.71	77	-24.9	.057	66	.46	-24
2.5	.57	170	9.5	2.97	71	-23.6	.066	69	.46	-26
3.0	.60	164	8.0	2.52	64	-22.3	.077	72	.45	-28
3.5	.60	157	6.8	2.18	61	-20.9	.090	77	.47	-29
4.0	.61	152	5.5	1.89	55	-20.1	.099	79	.47	-30
4.5	.63	147	4.7	1.72	51	-18.7	.116	81	.47	-36
5.0	.63	144	3.7	1.53	46	-17.8	.129	80	.48	-40
5.5	.65	139	3.1	1.42	42	-17.0	.141	82	.49	-44
6.0	66	136	2.1	1.28	38	-16.1	.156	83	.50	-47

AT-41400 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 25 mA

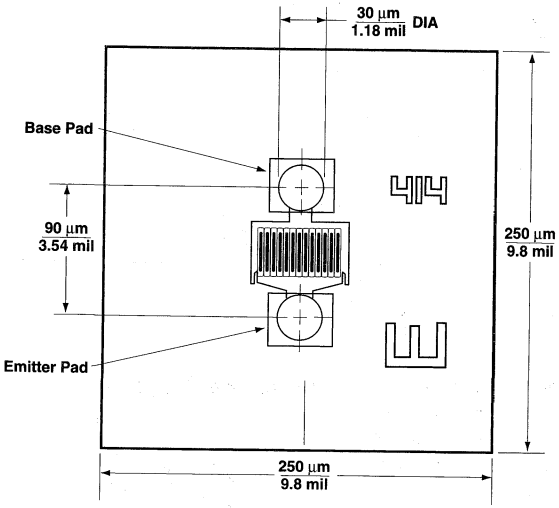
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.56	-60	31.8	39.07	152	-40.9	.009	69	.87	-18
0.5	.54	-145	23.5	15.00	104	-32.8	.023	56	.49	-28
1.0	.54	-170	18.1	8.03	90	-29.6	.033	65	.42	-23
1.5	.55	179	14.5	5.30	82	-26.9	.045	72	.41	-22
2.0	.56	170	12.1	4.04	76	-24.7	.058	75	.41	-23
2.5	.56	165	10.2	3.24	72	-23.1	.070	78	.40	-23
3.0	.58	159	8.8	2.75	65	-21.6	.083	79	.40	-25
3.5	.59	154	7.5	2.37	62	-20.4	.096	82	.41	-26
4.0	.60	149	6.3	2.06	57	-19.3	.108	83	.42	-28
4.5	.61	145	5.4	1.87	53	-18.1	.124	84	.42	-33
5.0	.62	142	4.5	1.67	49	-17.3	.136	83	.43	-36
5.5	.64	137	3.8	1.54	44	-16.5	.150	85	.42	-40
6.0	.65	134	2.9	1.40	41	-15.7	.165	84	.44	-45

A model for this device is available in the DEVICE MODELS section.

AT-41400 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.2	.12	3	0.17
0.5	1.2	.10	15	0.17
1.0	1.3	.06	27	0.16
2.0	1.6	.24	163	0.16
4.0	3.0	.52	-153	0.18

AT-41400 Chip Dimensions



Note: Die thickness is 5 to 6 mil.

HEWLETT® PACKARD

Up to 6 GHz Low Noise Silicon Bipolar Transistor

Technical Data

AT-41410

Features

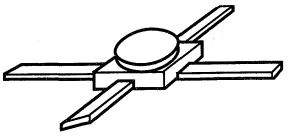
- **Low Noise Figure:**
  1.6 dB Typical at 2.0 GHz
  3.0 dB Typical at 4.0 GHz
- **High Associated Gain:**
  14.0 dB Typical at 2.0 GHz
  10.0 dB Typical at 4.0 GHz
- **High Gain-Bandwidth Product:** 8.0 GHz Typical f_T
- **Hermetic, Gold-ceramic Microstrip Package**

Description

Hewlett-Packard's AT-41410 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-41410 is housed in a hermetic, high reliability 100 mil ceramic package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 14 emitter finger interdigitated geometry yields an intermediate sized transistor with impedances that are easy to match for low noise and moderate power applications. This device is designed for use in low noise, wideband amplifier, mixer and oscillator applications in the VHF, UHF, and microwave frequencies. An optimum noise match near 50 Ω at 1 GHz , makes this device easy to use as a low noise amplifier.

The AT-41410 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

100 mil Package



AT-41410 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	60
P_T	Power Dissipation[2,3]	mW	500
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to 200

Thermal Resistance[2,4]:
θ_{jc} = 170°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 5.9 mW/°C for T_C > 115°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz	dB		12.0	
		f = 4.0 GHz			6.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression	f = 2.0 GHz	dBm		19.0	
	V_{CE} = 8 V, I_C = 25 mA	f= 4.0 GHz			18.5	
$G_{1\,dB}$	1 dB Compressed Gain; V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz	dB		14.0	
		f = 4.0 GHz			9.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz	dB		1.3	
		f = 2.0 GHz			1.6	1.9
		f = 4.0 GHz			3.0	
G_A	Gain @ NF_O; V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz	dB		18.5	
		f = 2.0 GHz		13.0	14.0	
		f = 4.0 GHz			10.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 25 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; V_{CE} = 8 V, I_C = 10 mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current; V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.2	

Notes:
1. For this test, the emitter is grounded.

AT-41410 Typical Performance, T_A = 25°C

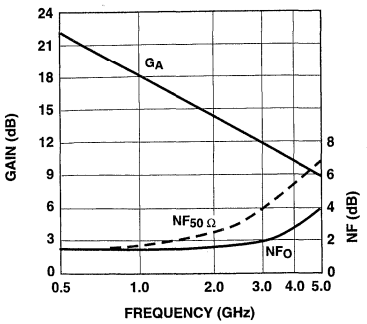


Figure 1. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

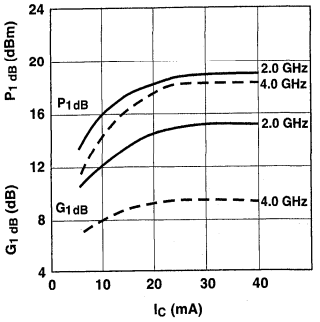


Figure 2. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

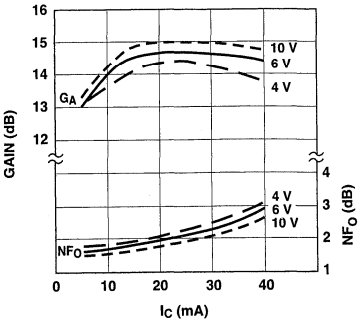


Figure 3. Optimum Noise Figure and Associated Gain vs. Collector Current and Collector Voltage. f = 2.0 GHz.

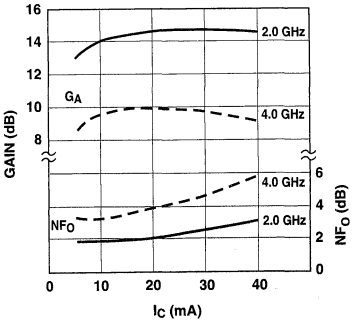


Figure 4. Optimum Noise Figure and Associated Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

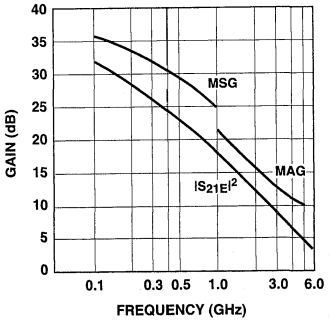


Figure 5. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 25 mA.

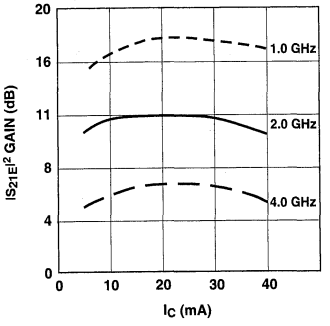


Figure 6. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

AT-41410 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.61	-40	27.7	24.38	159	-40.0	.010	75	.94	-13
0.5	.60	-127	22.2	12.83	110	-30.4	.030	40	.62	-33
1.0	.60	-163	17.1	7.12	86	-28.2	.039	35	.50	-38
1.5	.60	179	13.8	4.89	71	-27.5	.042	45	.46	-42
2.0	.61	165	11.4	3.72	59	-26.0	.050	42	.45	-48
2.5	.61	157	9.7	3.04	52	-24.7	.058	46	.44	-52
3.0	.62	149	8.2	2.56	42	-23.9	.064	50	.44	-58
3.5	.63	140	7.0	2.23	31	-22.3	.077	48	.46	-68
4.0	.62	130	5.9	1.96	20	-21.3	.086	44	.48	-78
4.5	.61	120	4.9	1.76	10	-20.4	.095	41	.50	-85
5.0	.61	106	4.0	1.59	-1	-18.9	.113	38	.52	-91
5.5	.62	94	3.2	1.45	-11	-18.3	.121	33	.52	-97
6.0	.66	82	2.4	1.31	-22	-17.5	.133	30	.51	-105

AT-41410 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 25 mA

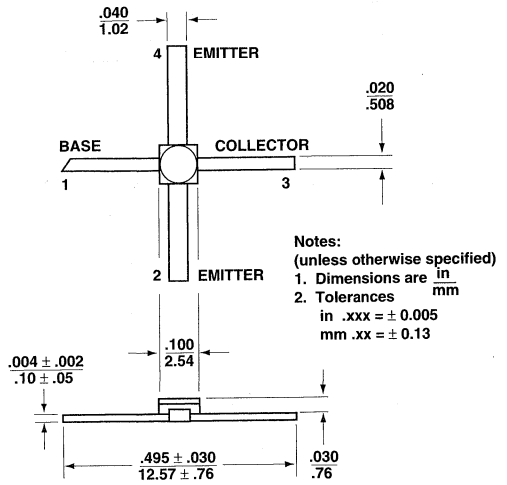
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.45	-69	31.4	37.17	150	-39.2	.011	64	.87	-18
0.5	.58	-153	23.3	14.63	101	-33.6	.021	43	.49	-33
1.0	.59	-178	17.7	7.68	81	-30.4	.030	53	.43	-35
1.5	.60	169	14.3	5.21	68	-28.2	.039	58	.41	-40
2.0	.60	157	11.9	3.94	56	-25.8	.051	55	.41	-45
2.5	.61	151	10.1	3.20	50	-24.4	.060	55	.40	-49
3.0	.62	144	8.6	2.70	40	-23.1	.070	58	.40	-56
3.5	.63	135	7.4	2.35	30	-21.9	.080	54	.42	-66
4.0	.62	126	6.3	2.07	19	-20.5	.094	53	.44	-76
4.5	.61	116	5.3	1.85	9	-19.3	.108	45	.46	-84
5.0	.61	103	4.5	1.67	-2	-18.5	.119	41	.49	-90
5.5	.63	91	3.6	1.52	-12	-17.6	.131	34	.49	-96
6.0	.67	80	2.8	1.37	-22	-16.8	.144	29	.47	-104

A model for this device is available in the DEVICE MODELS section.

AT-41410 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.2	.12	4	0.17
0.5	1.2	.10	23	0.17
1.0	1.3	.06	49	0.16
2.0	1.6	.26	172	0.16
4.0	3.0	.46	-133	0.26

100 mil Package Dimensions



HEWLETT® PACKARD

Surface Mount Low Noise Silicon Bipolar Transistor Chip

Technical Data

AT-41411

Features

- **Low Noise Figure:**
  1.4 dB Typical at 1.0 GHz
  1.8 dB Typical at 2.0 GHz
- **High Associated Gain:**
  18.0 dB Typical at 1.0 GHz
  13.0 dB Typical at 2.0 GHz
- **High Gain-Bandwidth Product:** 7.0 GHz Typical f_T
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

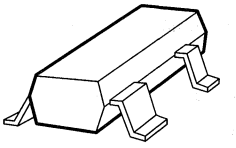
Description

Hewlett-Packard's AT-41411 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-41411 is housed in a low cost low parasitic 4 lead SOT-143 surface mount package. The SOT-143 is an industry standard and is compatible with high volume surface mount assembly techniques. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 14 emitter finger interdigitated geometry yields an intermediate sized transistor with impedances that are easy to match for low noise and moderate power applications. This device is designed for use in low noise, wideband amplifier, mixer and oscillator applications in the VHF, UHF, and microwave frequencies. An optimum noise match near 50 Ω in the 1 to 2 GHz frequency range, makes this device easy to use as a low noise amplifier.

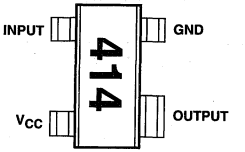
The AT-41411 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

Note:
1. Refer to "Tape-and-Reel Packaging for Semiconductor Devices".

SOT-143 Plastic



Pin Connections



5965-8924E

AT-41411 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	50
P_T	Power Dissipation[2,3]	mW	225
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2,4]:
$\theta_{jc} = 550°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 1.8 mW/°C for $T_C > 26°C$.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

Part Number	Increment	Comments
AT-41411-TR1	3000	Reel
AT-41411-BLK	100	Bulk

Note: For more information, see "Tape and Reel Packaging for Semiconductor Devices".

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; $V_{CE} = 8$ V, $I_C = 20$ mA	f = 1.0 GHz f = 2.0 GHz	dB	14.5	16.5 11.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression $V_{CE} = 8$ V, $I_C = 20$ mA	f = 2.0 GHz	dBm		17.0	
$G_{1\,dB}$	1 dB Compressed Gain; $V_{CE} = 8$ V, $I_C = 20$ mA	f = 2.0 GHz	dB		13.0	
NF_O	Optimum Noise Figure: $V_{CE} = 8$ V, $I_C = 10$ mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.8 3.5	
G_A	Gain @ NF_O; $V_{CE} = 8$ V, $I_C = 10$ mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		18.0 13.0 9.0	
f_T	Gain Bandwidth Product: $V_{CE} = 8$ V, $I_C = 20$ mA		GHz		7.0	
h_{FE}	Forward Current Transfer Ratio; $V_{CE} = 8$ V, $I_C = 10$ mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; $V_{CB} = 8$ V		μA			0.2
I_{EBO}	Emitter Cutoff Current; $V_{EB} = 1$ V		μA			1.0

Notes:
1. Refer to PACKAGING Section, "Tape-and-Reel Packaging for Semiconductor Devices."

AT-41411 Typical Performance, T_A = 25°C

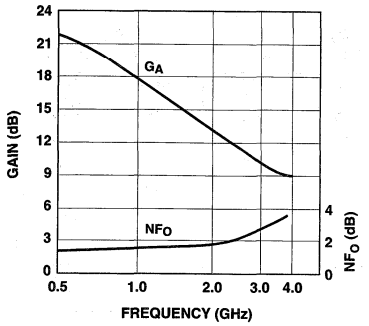


Figure 1. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

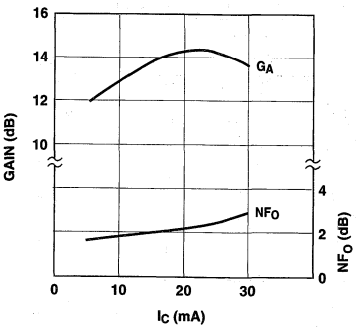


Figure 2. Optimum Noise Figure and Associated Gain vs. Collector Current and Frequency. V_{CE} = 8 V, f = 2.0 GHz.

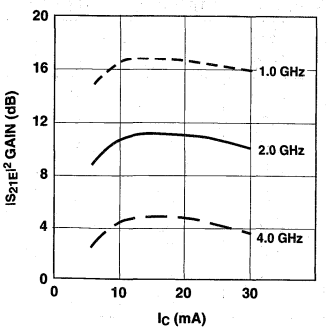


Figure 3. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

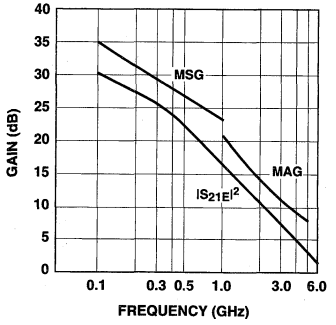


Figure 4. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 20 mA.

AT-41411 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.85	-30	27.3	23.20	158	-37.7	.013	64	.93	-11
0.5	.58	-112	21.7	12.18	109	-29.1	.035	44	.62	-30
1.0	.49	-156	16.5	6.70	85	-27.2	.044	43	.50	-33
1.5	.49	178	13.2	4.58	71	-25.0	.056	47	.46	-36
2.0	.50	160	10.8	3.45	59	-23.4	.068	47	.45	-41
2.5	.53	153	9.0	2.82	53	-22.5	.075	56	.43	-43
3.0	.55	142	7.5	2.37	43	-21.0	.089	54	.43	-53
3.5	.56	133	6.1	2.02	33	-19.8	.102	52	.44	-63
4.0	.56	121	4.9	1.76	23	-18.8	.115	49	.46	-73

AT-41411 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 20 mA

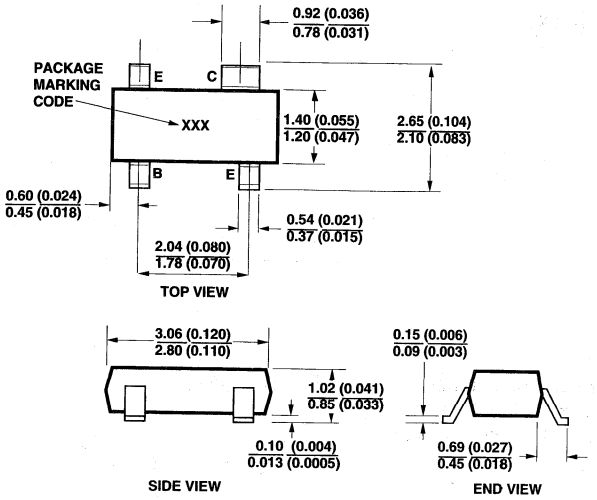
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.65	-46	30.4	33.07	150	-40.0	.010	59	.89	-15
0.5	.46	-137	22.4	13.21	100	-32.0	.025	56	.57	-26
1.0	.43	-175	16.7	6.85	80	-28.4	.038	58	.52	-29
1.5	.44	163	13.3	4.63	67	-26.4	.048	61	.51	-32
2.0	.47	148	10.8	3.47	56	-24.2	.062	61	.50	-37
2.5	.50	140	9.0	2.82	50	-22.9	.071	60	.47	-39
3.0	.53	132	7.5	2.36	40	-20.7	.092	61	.46	-48
3.5	.55	122	6.1	2.02	30	-19.6	.105	57	.45	-60
4.0	.56	112	4.8	1.74	19	-18.3	.122	53	.45	-73

A model for this device is available in the DEVICE MODELS section.

AT-41411 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.3	.12	4	0.17
0.5	1.3	.10	23	0.17
1.0	1.4	.07	57	0.16
2.0	1.8	.09	-158	0.16
4.0	3.5	.31	-87	0.38

SOT-143 Plastic Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Up to 6 GHz Low Noise Silicon Bipolar Transistor

Technical Data

AT-41435

Features

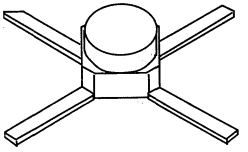
- **Low Noise Figure:**
  1.7 dB Typical at 2.0 GHz
  3.0 dB Typical at 4.0 GHz
- **High Associated Gain:**
  14.0 dB Typical at 2.0 GHz
  10.0 dB Typical at 4.0 GHz
- **High Gain-Bandwidth Product:** 8.0 GHz Typical f_T
- **Cost Effective Ceramic Microstrip Package**

Description

Hewlett-Packard's AT-41435 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-41435 is housed in a cost effective surface mount 100 mil micro-X package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 14 emitter finger interdigitated geometry yields an intermediate sized transistor with impedances that are easy to match for low noise and moderate power applications. This device is designed for use in low noise, wideband amplifier, mixer and oscillator applications in the VHF, UHF, and microwave frequencies. An optimum noise match near 50 Ω at 1 GHz, makes this device easy to use as a low noise amplifier.

The AT-41435 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

35 micro-X Package



AT-41435 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	60
P_T	Power Dissipation[2,3]	mW	500
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature[4]	°C	-65 to 200

Thermal Resistance[2,5]:
θ_{jc} = 200°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 5 mW/°C for T_C > 100°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 200°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz	dB		11.5	
		f = 4.0 GHz			6.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression	f = 2.0 GHz	dBm		19.0	
	V_{CE} = 8 V, I_C = 25 mA	f = 4.0 GHz			18.5	
$G_{1\,dB}$	1 dB Compressed Gain; V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz	dB		14.0	
		f = 4.0 GHz			9.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz	dB		1.3	
		f = 2.0 GHz			1.7	2.0
		f = 4.0 GHz			3.0	
G_A	Gain @ NF_O; V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz	dB		18.5	
		f = 2.0 GHz		13.0	14.0	
		f = 4.0 GHz			10.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 25 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; V_{CE} = 8 V, I_C = 10 mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current; V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.2	

Note:
1. For this test, the emitter is grounded.

AT-41435 Typical Performance, T_A = 25°C

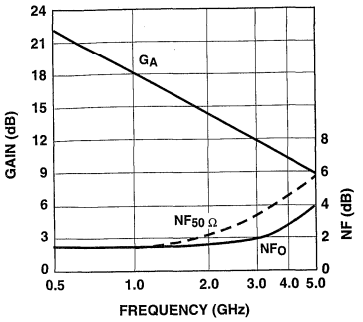


Figure 1. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

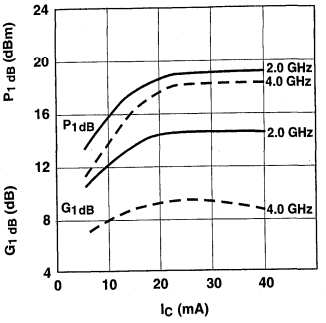


Figure 2. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

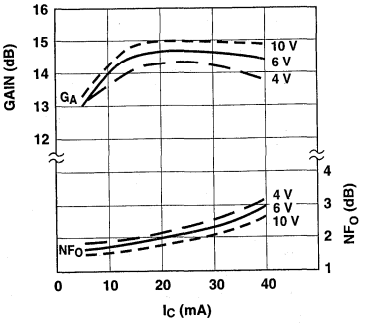


Figure 3. Optimum Noise Figure and Associated Gain vs. Collector Current and Collector Voltage. f = 2.0 GHz.

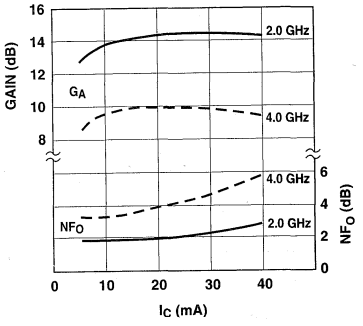


Figure 4. Optimum Noise Figure and Associated Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

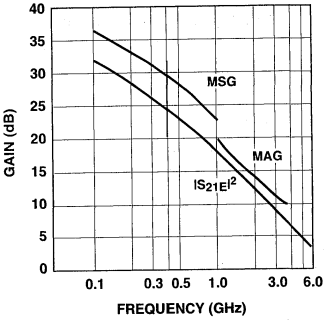


Figure 5. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 25 mA.

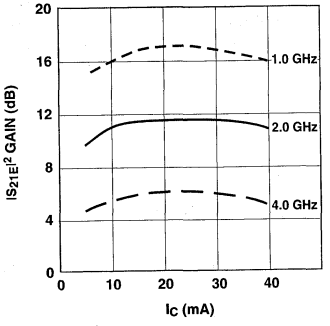


Figure 6. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

AT-41435 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.80	-32	28.0	24.99	157	-39.2	.011	82	.93	-12
0.5	.50	-110	21.8	12.30	108	-29.6	.033	52	.61	-28
1.0	.40	-152	16.6	6.73	85	-26.2	.049	56	.51	-30
1.5	.38	-176	13.3	4.63	71	-24.0	.063	59	.48	-32
2.0	.39	166	11.0	3.54	60	-21.9	.080	58	.46	-37
2.5	.41	156	9.3	2.91	53	-20.4	.095	61	.44	-40
3.0	.44	145	7.9	2.47	43	-18.8	.115	61	.43	-48
3.5	.46	137	6.7	2.15	33	-17.5	.133	58	.43	-58
4.0	.46	127	5.6	1.91	23	-16.0	.153	53	.45	-68
4.5	.47	116	4.7	1.72	13	-15.0	.178	50	.46	-75
5.0	.49	104	4.0	1.58	3	-13.9	.201	47	.48	-82
5.5	.52	91	3.3	1.45	-7	-13.0	.224	40	.47	-89
6.0	.59	81	2.5	1.34	-17	-12.1	.247	36	.43	-101

AT-41435 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 25 mA

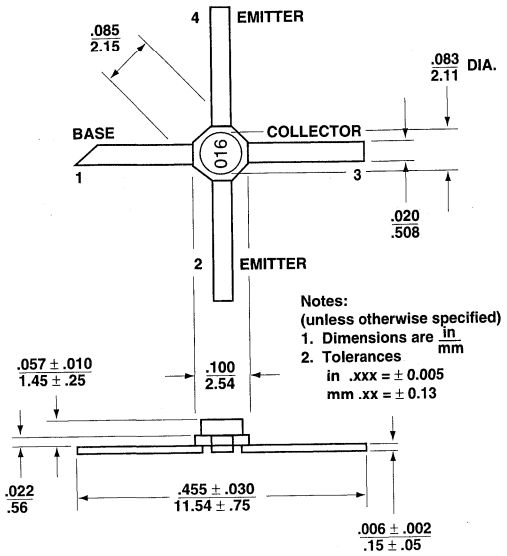
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.63	-50	31.8	39.08	146	-40.0	.010	83	.84	-18
0.5	.39	-137	22.9	13.97	99	-31.4	.027	60	.50	-26
1.0	.36	-171	17.2	7.28	80	-27.1	.044	67	.45	-26
1.5	.36	171	13.9	4.94	68	-23.5	.067	66	.43	-30
2.0	.38	156	11.5	3.76	58	-21.6	.083	63	.41	-34
2.5	.40	149	9.8	3.08	52	-19.6	.105	63	.39	-38
3.0	.43	140	8.3	2.61	43	-18.3	.122	64	.38	-47
3.5	.45	132	7.2	2.28	33	-16.8	.144	59	.39	-57
4.0	.46	122	6.1	2.02	23	-15.6	.165	55	.40	-67
4.5	.46	112	5.2	1.82	14	-14.6	.185	50	.42	-75
5.0	.47	101	4.4	1.66	4	-13.7	.207	45	.43	-81
5.5	.51	89	3.7	1.54	-5	-12.6	.233	39	.42	-89
6.0	.58	79	3.0	1.41	-15	-11.8	.257	33	.37	-101

A model for this device is available in the DEVICE MODELS section.

AT-41435 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.2	.12	3	0.17
0.5	1.2	.10	14	0.17
1.0	1.3	.05	28	0.17
2.0	1.7	.30	-154	0.16
4.0	3.0	.54	-118	0.35

35 micro-X Package Dimensions



HEWLETT® PACKARD

Up to 6 GHz Low Noise Silicon Bipolar Transistor

Technical Data

AT-41470

Features

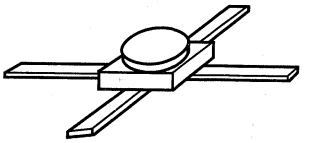
- **Low Noise Figure:**
  1.6 dB Typical at 2.0 GHz
  3.0 dB Typical at 4.0 GHz
- **High Associated Gain:**
  14.5 dB Typical at 2.0 GHz
  10.5 dB Typical at 4.0 GHz
- **High Gain-Bandwidth Product:** 8.0 GHz Typical f_T
- **Hermetic, Gold-ceramic Microstrip Package**

Description

Hewlett-Packard's AT-41470 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-41470 is housed in a hermetic, high reliability gold-ceramic 70 mil microstrip package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 14 emitter finger interdigitated geometry yields an intermediate sized transistor with impedances that are easy to match for low noise and moderate power applications. This device is designed for use in low noise, wideband amplifier, mixer and oscillator applications in the VHF, UHF, and microwave frequencies. An optimum noise match near 50 Ω at 1 GHz , makes this device easy to use as a low noise amplifier.

The AT-41470 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

70 mil Package



5965-8927E

AT-41470 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	60
P_T	Power Dissipation[2,3]	mW	500
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to 200

Thermal Resistance[2,4]:
θ_{jc} = 175°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 5.7 mW/°C for T_C > 113°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz	dB		12.0	
		f = 4.0 GHz			6.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression	f = 2.0 GHz	dBm		19.0	
	V_{CE} = 8 V, I_C = 25 mA	f = 4.0 GHz			18.5	
$G_{1\,dB}$	1 dB Compressed Gain; V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz	dB		15.0	
		f = 4.0 GHz			10.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz	dB		1.3	
		f = 2.0 GHz			1.6	1.9
		f = 4.0 GHz			3.0	
G_A	Gain @ NF_O; V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz	dB		18.5	
		f = 2.0 GHz		13.0	14.5	
		f = 4.0 GHz			10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 25 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; V_{CE} = 8 V, I_C = 10 mA		—	30	150	300
I_{CBO}	Collector Cutoff Current; V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current; V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.2	

Note:
1. For this test, the emitter is grounded.

AT-41470 Typical Performance, T_A = 25°C

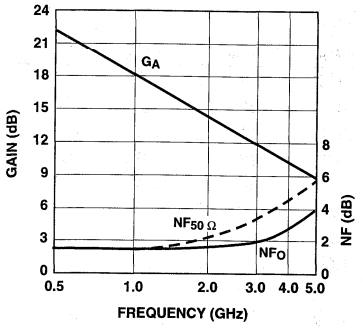


Figure 1. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

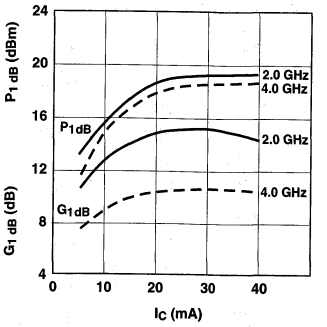


Figure 2. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

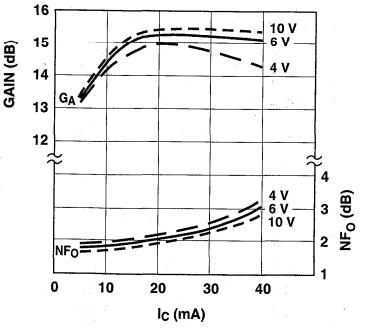


Figure 3. Optimum Noise Figure and Associated Gain vs. Collector Current and Collector Voltage. f = 2.0 GHz.

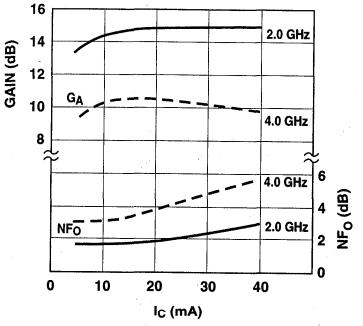


Figure 4. Optimum Noise Figure and Associated Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

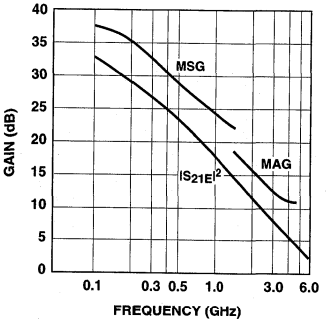


Figure 5. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 25 mA.

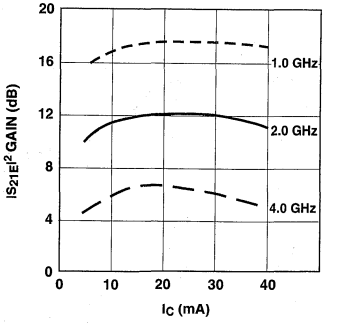


Figure 6. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

AT-41470 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.79	-37	28.4	26.27	157	-39.2	.011	57	.94	-13
0.5	.65	-120	22.3	13.05	110	-30.8	.029	40	.62	-30
1.0	.61	-155	17.1	7.17	88	-28.9	.036	41	.52	-32
1.5	.60	-172	13.9	4.93	76	-27.5	.042	46	.50	-36
2.0	.60	176	11.5	3.75	65	-26.4	.048	46	.50	-40
2.5	.61	169	9.7	3.06	59	-26.0	.050	58	.48	-41
3.0	.62	161	8.3	2.59	51	-24.7	.058	61	.49	-48
3.5	.61	154	7.0	2.24	42	-23.2	.069	63	.51	-56
4.0	.60	146	5.9	1.97	32	-21.4	.085	62	.52	-63
4.5	.60	137	4.9	1.77	24	-20.1	.099	59	.55	-69
5.0	.60	127	4.1	1.61	15	-19.5	.106	59	.57	-75
5.5	.61	115	3.4	1.47	6	-18.3	.121	56	.58	-80
6.0	.64	104	2.6	1.34	-4	-17.4	.135	53	.57	-87

AT-41470 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 25 mA

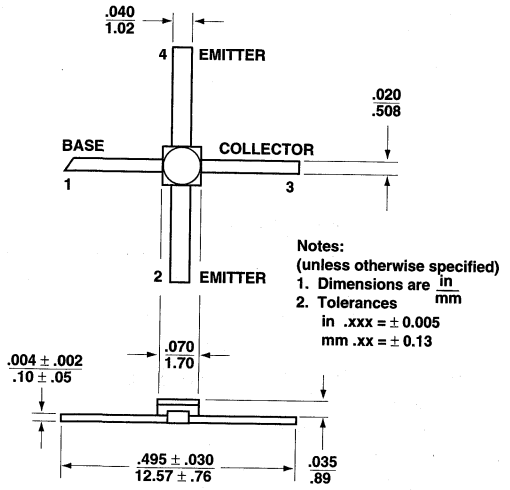
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.64	-62	32.5	42.11	147	-40.9	.009	75	.85	-19
0.5	.61	-146	23.7	15.31	100	-34.4	.019	47	.50	-30
1.0	.61	-170	18.1	8.00	83	-30.2	.031	53	.44	-31
1.5	.60	177	14.7	5.42	72	-29.1	.035	62	.44	-34
2.0	.61	167	12.3	4.10	62	-27.1	.044	60	.44	-39
2.5	.61	163	10.4	3.32	58	-25.7	.052	67	.43	-39
3.0	.62	156	9.0	2.81	50	-23.6	.066	67	.44	-46
3.5	.62	150	7.7	2.44	41	-22.6	.074	67	.46	-55
4.0	.62	142	6.6	2.13	32	-21.7	.082	63	.48	-62
4.5	.61	134	5.6	1.91	24	-20.1	.099	62	.50	-68
5.0	.60	123	4.8	1.73	15	-18.9	.113	59	.52	-73
5.5	.61	112	4.0	1.59	6	-18.1	.124	54	.54	-78
6.0	.64	102	3.2	1.45	-3	-17.3	.136	50	.53	-85

A model for this device is available in the DEVICE MODELS section.

AT-41470 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.2	.12	5	0.17
0.5	1.2	.11	17	0.17
1.0	1.3	.06	35	0.17
2.0	1.6	.21	160	0.16
4.0	3.0	.45	-150	0.20

70 mil Package Dimensions



Package marking is "414"

HEWLETT® PACKARD

Up to 6 GHz Low Noise Silicon Bipolar Transistor

Technical Data

AT-41485

Features

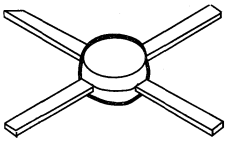
- **Low Noise Figure:**
  1.4 dB Typical at 1.0 GHz
  1.7 dB Typical at 2.0 GHz
- **High Associated Gain:**
  18.5 dB Typical at 1.0 GHz
  13.5 dB Typical at 2.0 GHz
- **High Gain-Bandwidth Product:** 8.0 GHz Typical f_T

Description

Hewlett-Packard's AT-41485 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-41485 is housed in a low cost .085" diameter plastic package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 14 emitter finger interdigitated geometry yields an intermediate sized transistor with impedances that are easy to match for low noise and moderate power applications. Applications include use in wireless systems as an LNA, gain stage, buffer, oscillator, and mixer. An optimum noise match near 50 Ω at 900 MHz, makes this device easy to use as a low noise amplifier.

The AT-41485 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

85 Plastic Package



AT-41485 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	60
P_T	Power Dissipation[2,3]	mW	500
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2,4]:
θ_{jc} = 155°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.5 mW/°C for T_C > 73°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; V_{CE} = 8 V, I_C = 25 mA	f = 1.0 GHz	dB		17.5	
		f = 2.0 GHz			11.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz	dBm		18.5	
$G_{1\,dB}$	1 dB Compressed Gain; V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz	dB		14.0	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz	dB		1.4	1.8
		f = 2.0 GHz			1.7	
		f = 4.0 GHz			3.0	
G_A	Gain @ NF_O; V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz	dB	17.5	18.5	
		f = 2.0 GHz			13.5	
		f = 4.0 GHz			9.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 25 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; V_{CE} = 8 V, I_C = 10 mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current; V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.25	

Notes:
1. For this test, the emitter is grounded.

AT-41485 Typical Performance, T_A = 25°C

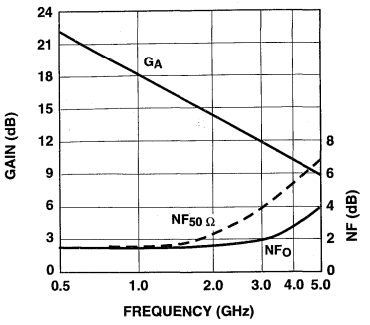


Figure 1. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

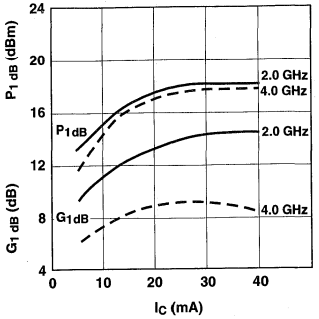


Figure 2. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

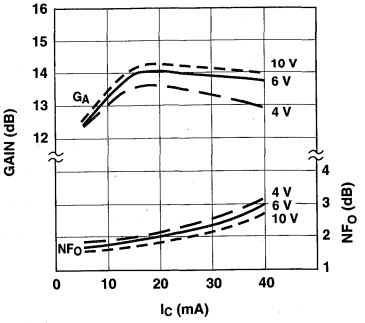


Figure 3. Optimum Noise Figure and Associated Gain vs. Collector Current and Collector Voltage. f = 2.0 GHz.

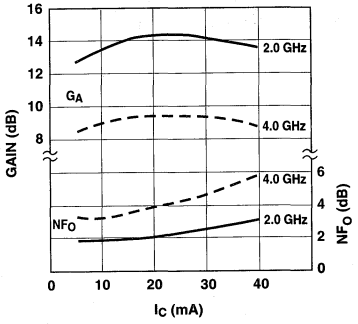


Figure 4. Optimum Noise Figure and Associated Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

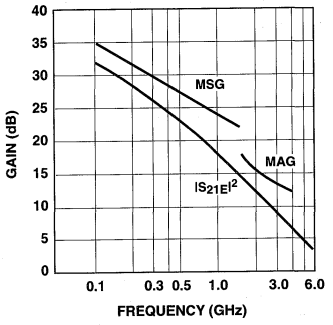


Figure 5. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 25 mA.

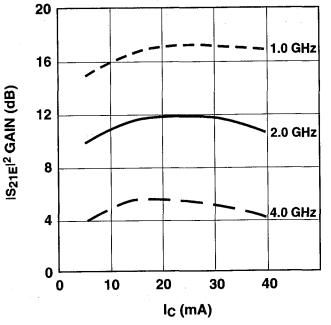


Figure 6. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

AT-41485 Typical Scattering Parameters, Common Emitter,

Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.74	-40	28.2	25.80	156	-35.6	.017	81	.93	-14
0.5	.61	-126	21.9	12.46	108	-29.2	.035	44	.57	-31
1.0	.57	-161	16.6	6.80	87	-27.9	.040	38	.46	-33
1.5	.57	-180	13.4	4.67	75	-25.7	.052	47	.43	-34
2.0	.58	166	11.0	3.55	64	-24.5	.060	54	.41	-38
2.5	.59	160	9.3	2.92	59	-23.3	.068	58	.40	-39
3.0	.61	150	7.7	2.42	50	-21.9	.080	63	.39	-46
3.5	.62	142	6.4	2.09	41	-20.8	.091	61	.41	-54
4.0	.62	134	5.3	1.84	32	-19.5	.106	59	.42	-62
4.5	.62	125	4.3	1.65	24	-18.4	.120	57	.43	-67
5.0	.63	115	3.5	1.50	15	-17.2	.138	54	.44	-73
5.5	.65	103	2.7	1.37	6	-16.1	.157	49	.43	-78
6.0	.69	92	1.8	1.24	-4	-15.3	.172	46	.40	-86

AT-41485 Typical Scattering Parameters, Common Emitter,

Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 25 mA

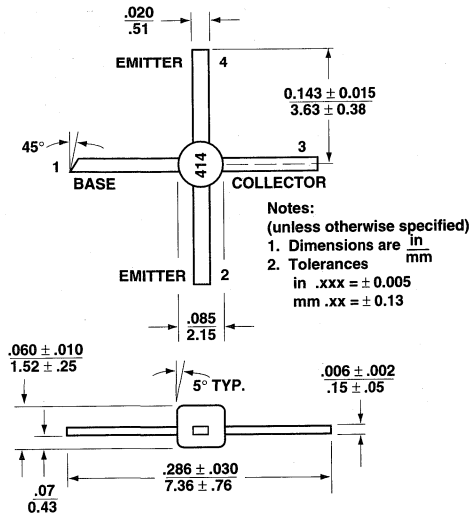
Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.55	-68	32.0	40.01	146	-40.9	.009	57	.85	-19
0.5	.58	-153	23.1	14.20	99	-32.7	.023	52	.47	-29
1.0	.58	-177	17.4	7.39	82	-29.8	.032	63	.41	-28
1.5	.58	169	14.0	5.01	71	-27.3	.043	60	.39	-30
2.0	.60	158	11.6	3.78	61	-24.6	.059	64	.38	-36
2.5	.60	153	9.8	3.09	58	-23.7	.065	71	.36	-39
3.0	.63	147	8.1	2.55	48	-21.7	.082	68	.35	-47
3.5	.64	140	6.9	2.21	39	-20.7	.092	67	.37	-56
4.0	.64	133	5.8	1.94	31	-19.4	.107	65	.39	-64
4.5	.64	125	4.8	1.74	23	-18.1	.125	63	.40	-71
5.0	.64	115	4.0	1.58	14	-17.1	.140	56	.41	-78
5.5	.66	105	3.2	1.45	5	-15.9	.160	50	.40	-82
6.0	.70	94	2.4	1.32	-5	-15.1	.175	47	.37	-91

A model for this device is available in the DEVICE MODELS section.

AT-41485 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Γ_{opt}		$R_N/50$
		Mag	Ang	
0.1	1.3	.12	5	0.17
0.5	1.3	.10	25	0.17
1.0	1.4	.06	50	0.16
2.0	1.7	.25	172	0.16
4.0	3.0	.48	-131	0.24

85 Plastic Package Dimensions



HEWLETT® PACKARD

Up to 6 GHz Low Noise Silicon Bipolar Transistor

Technical Data

AT-41486

Features

- **Low Noise Figure:**
  1.4 dB Typical at 1.0 GHz
  1.7 dB Typical at 2.0 GHz
- **High Associated Gain:**
  18.0 dB Typical at 1.0 GHz
  13.0 dB Typical at 2.0 GHz
- **High Gain-Bandwidth Product:** 8.0 GHz Typical f_T
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

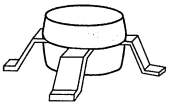
Note:
1. Refer to "Tape-and-Reel Packaging for Semiconductor Devices".

Description

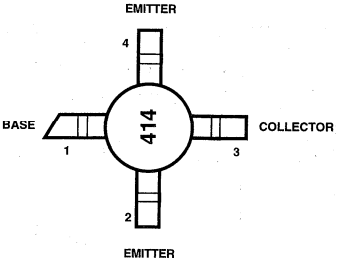
Hewlett-Packard's AT-41486 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-41486 is housed in a low cost surface mount .085" diameter plastic package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 14 emitter finger interdigitated geometry yields an intermediate sized transistor with impedances that are easy to match for low noise and moderate power applications. Applications include use in wireless systems as an LNA, gain stage, buffer, oscillator, and mixer. An optimum noise match near 50 Ω at 900 MHz, makes this device easy to use as a low noise amplifier.

The AT-41486 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

86 Plastic Package



Pin Connections



5965-8928E

AT-41486 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	60
P_T	Power Dissipation[2,3]	mW	500
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2,4]:
$\theta_{jc} = 165°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 6 mW/°C for $T_C > 68°C$.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

Part Number	Increment	Comments
AT-41486-TR1	1000	Reel
AT-41486-BLK	100	Bulk

Note: For more information, see "Tape and Reel Packaging for Semiconductor Devices".

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; $V_{CE} = 8$ V, $I_C = 25$ mA	f = 2.0 GHz f = 4.0 GHz	dB		17.5 11.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression $V_{CE} = 8$ V, $I_C = 25$ mA	f = 2.0 GHz	dBm		18.0	
$G_{1\,dB}$	1 dB Compressed Gain; $V_{CE} = 8$ V, $I_C = 25$ mA	f = 2.0 GHz	dB		13.5	
NF_O	Optimum Noise Figure: $V_{CE} = 8$ V, $I_C = 10$ mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.7 3.0	1.8
G_A	Gain @ NF_O; $V_{CE} = 8$ V, $I_C = 10$ mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	17.0	18.0 13.0 9.0	
f_T	Gain Bandwidth Product: $V_{CE} = 8$ V, $I_C = 25$ mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; $V_{CE} = 8$ V, $I_C = 10$ mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; $V_{CB} = 8$ V		μA			0.2
I_{EBO}	Emitter Cutoff Current; $V_{EB} = 1$ V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: $V_{CB} = 8$ V, f = 1 MHz		pF		0.25	

Note:
1. For this test, the emitter is grounded.

AT-41486 Typical Performance, T_A = 25°C

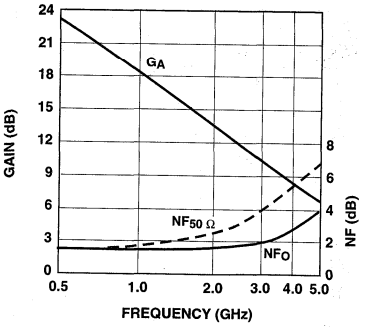


Figure 1. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

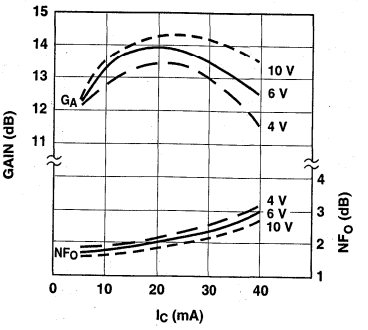


Figure 2. Optimum Noise Figure and Associated Gain vs. Collector Current and Collector Voltage. f = 2.0 GHz.

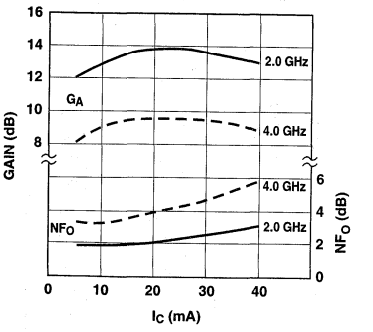


Figure 3. Optimum Noise Figure and Associated Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

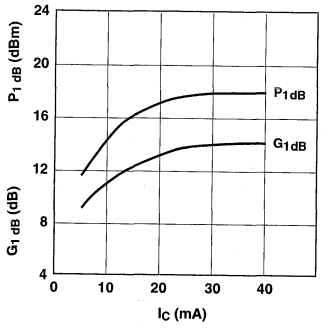


Figure 4. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V, f = 2.0 GHz.

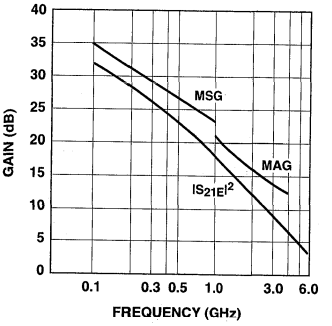


Figure 5. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 25 mA.

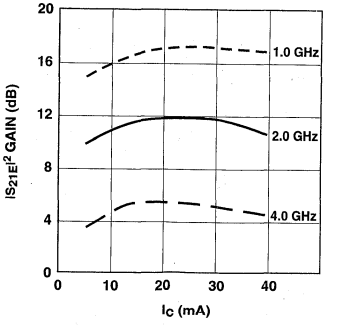


Figure 6. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

AT-41486 Typical Scattering Parameters, Common Emitter,

Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.74	-38	28.1	25.46	157	-39.6	.011	68	.94	-12
0.5	.59	-127	22.0	12.63	107	-30.2	.031	47	.60	-29
1.0	.56	-168	16.8	6.92	84	-27.7	.041	46	.49	-29
1.5	.57	169	13.5	4.72	69	-26.2	.049	49	.45	-32
2.0	.62	152	11.1	3.61	56	-24.8	.058	43	.42	-39
2.5	.63	142	9.3	2.91	47	-23.4	.068	52	.40	-42
3.0	.64	130	7.6	2.41	37	-22.2	.078	52	.39	-50
3.5	.68	122	6.3	2.06	26	-20.6	.093	51	.37	-60
4.0	.71	113	5.1	1.80	16	-19.5	.106	48	.35	-70
4.5	.74	105	4.0	1.59	7	-18.0	.125	48	.35	-84
5.0	.77	99	3.1	1.42	-4	-17.2	.139	43	.35	-98
5.5	.79	93	2.0	1.27	-13	-16.3	.153	38	.35	-114
6.0	.81	87	1.1	1.13	-22	-15.4	.170	34	.35	-131

AT-41486 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 25 mA

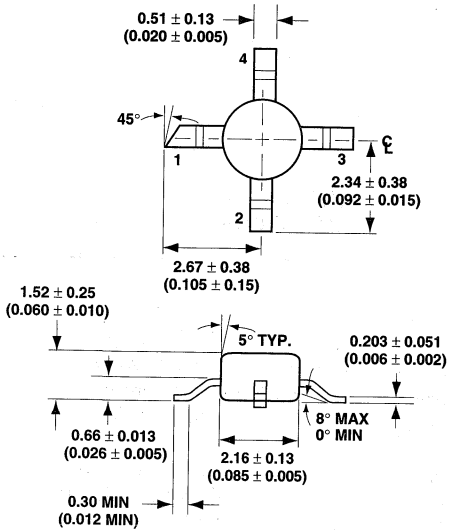
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.50	-75	32.0	40.01	142	-41.3	.009	54	.85	-17
0.5	.55	-158	23.2	14.38	97	-34.1	.020	48	.51	-24
1.0	.57	177	17.5	7.50	78	-29.9	.032	61	.46	-24
1.5	.57	161	14.1	5.07	65	-27.3	.043	62	.44	-28
2.0	.59	148	11.5	3.75	53	-24.8	.058	59	.43	-35
2.5	.61	139	9.6	3.02	45	-22.9	.072	58	.40	-41
3.0	.65	128	8.0	2.52	34	-21.6	.083	57	.38	-49
3.5	.70	121	6.7	2.17	24	-20.1	.099	56	.36	-59
4.0	.74	113	5.7	1.92	14	-18.8	.115	52	.34	-72
4.5	.78	107	4.7	1.72	3	-17.6	.132	47	.32	-87
5.0	.78	102	3.7	1.53	-8	-16.6	.149	42	.31	-106
5.5	.78	96	2.7	1.36	-19	-15.4	.169	36	.31	-125
6.0	.76	91	1.6	1.21	-29	-14.5	.188	31	.33	-144

A model for this device is available in the DEVICE MODELS section.

AT-41486 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.3	.12	3	0.17
0.5	1.3	.10	16	0.17
1.0	1.4	.04	43	0.16
2.0	1.7	.12	-145	0.16
4.0	3.0	.44	-99	0.40

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

General Purpose, Low Noise NPN Silicon Bipolar Transistor

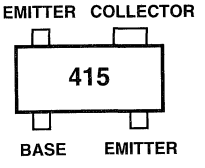
Technical Data

AT-41511
AT-41533

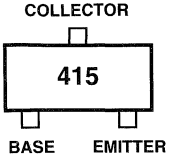
Features

- **General Purpose NPN Bipolar Transistor**
- **900 MHz Performance:**
  AT-41511: 1 dB NF, 15.5 dB G_A
  AT-41533: 1 dB NF, 14.5 dB G_A
- **Characterized for 3, 5, and 8 Volt Use**
- **SOT-23 and SOT-143 SMT Plastic Packages**
- **Tape-and-Reel Packaging Option Available[1]**

Outline Drawing



SOT 143 (AT-41511)



SOT 23 (AT-41533)

1. Refer to "Tape-and-Reel Packaging for Semiconductor Devices."

Description

Hewlett-Packard's AT-41511 and AT-41533 are general purpose NPN bipolar transistors that offer excellent high frequency performance at an economical price. The AT-41533 uses the 3 lead SOT-23, while the AT-41511 places the same die in the lower parasitic 4 lead SOT-143. Both packages are industry standard, and compatible with high volume surface mount assembly techniques.

The 4 micron emitter-to-emitter pitch of these transistors yields high performance products that can perform a multiplicity of tasks. The 14 emitter finger interdigitated geometry yields an intermediate-sized transistor with easy to match to impedances, low noise figure, and moderate power.

Optimized for best performace from a 5 to 8 volt bias supply, these transistors are also good performers at 2.7 V. Applications include use in wireless systems as an LNA, gain stage, buffer, oscillator, or active mixer.

An optimum noise match near 50 ohms at 900 MHz makes these devices particularly easy to use as LNAs. Typical amplifier designs at 900 MHz yield 1 dB noise figures with 15 dB or more associated gain at a 5 V, 5 mA bias, with good gain and noise figure obtainable at biases as low as 2 mA.

The AT-415 series bipolar transistors are fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices.

AT-41511, AT-41533 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	50
P_T	Power Dissipation[2,3]	mW	225
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance:[2]
θ_{jc} =550°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{Mounting\ Surface}$ = 25°C.
3. Derate at 1.82 mW/°C for T_C > 26°C.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	AT-41511			AT-41533		
				Min	Typ	Max	Min	Typ	Max
h_{FE}	Forward Current Transfer Ratio	V_{CE} = 5 V I_C = 5 mA	-	30	150	270	30	150	270
I_{CBO}	Collector Cutoff Current	V_{CB} = 3 V	μA			0.2			0.2
I_{EBO}	Emitter Cutoff Current	V_{EB} = 1 V	μA			1.0			1.0

Characterization Information, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	AT-41511		AT-41533	
				Min	Typ	Min	Typ
NF	Noise Figure V_{CE} = 5 V, I_C = 5 mA	f = 0.9 GHz f = 2.4 GHz	dB		1.0 1.7		1.0 1.6
G_A	Associated Gain V_{CE} = 5 V, I_C = 5 mA	f = 0.9 GHz f = 2.4 GHz	dB		15.5 11		14.5 9
P_{1dB}	Power at 1 dB Gain Compression (opt tuning) V_{CE} = 5 V, I_C = 25 mA	f = 0.9 GHz	dBm		14.5		14.5
G_{1dB}	Gain at 1 dB Gain Compression (opt tuning) V_{CE} = 5 V, I_C = 25 mA	f = 0.9 GHz	dB		17.5		14.5
IP_3	Output Third Order Intercept Point, V_{CE} = 5 V, I_C =25 mA (opt tuning)	f = 0.9 GHz	dBm		25		25
$\|S_{21E}\|^2$	Gain in 50 Ω system; V_{CE} = 5 V, I_C = 5 mA	f = 0.9 GHz f = 2.4 GHz	dB	13.5	15.5 7.9	10.8	12.8 5.2

Ordering Information

Part Number	Increment	Comments
AT-41511-BLK	100	Bulk
AT-41511-TR1	3000	7" Reel
AT-41533-BLK	100	Bulk
AT-41533-TR1	3000	7" Reel

AT-41511, AT-41533 Typical Performance

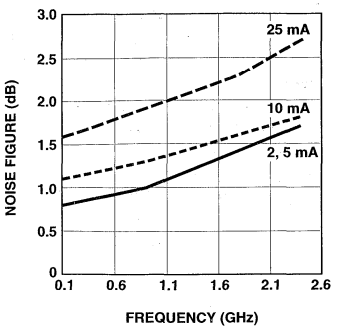


Figure 1. AT-41511 and AT-41533 Minimum Noise Figure vs. Frequency and Current at V_{CE} = 2.7 V.

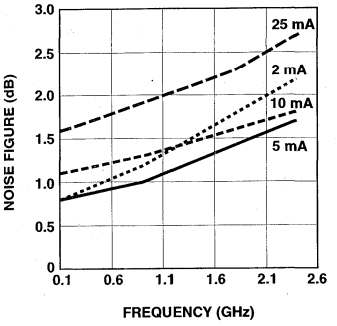


Figure 2. AT-41511 and AT-41533 Minimum Noise Figure vs. Frequency and Current at V_{CE} = 5 V.

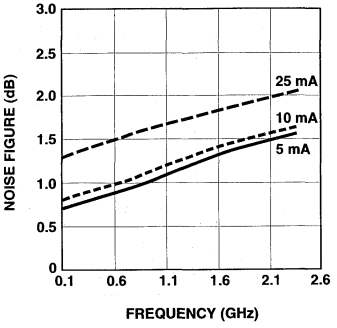


Figure 3. AT-41511 and AT-41533 Minimum Noise Figure vs. Frequency and Current at V_{CE} = 8 V.

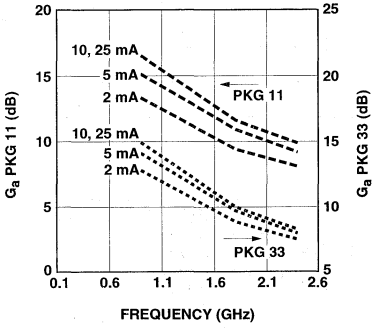


Figure 4. AT-41511 and AT-41533 Associated Gain vs. Frequency and Current at V_{CE} = 2.7 V.

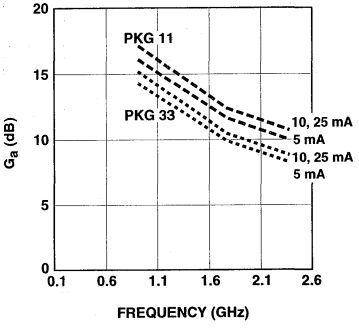


Figure 5. AT-41511 and AT-41533 Associated Gain vs. Frequency and Current at V_{CE} = 5 V.

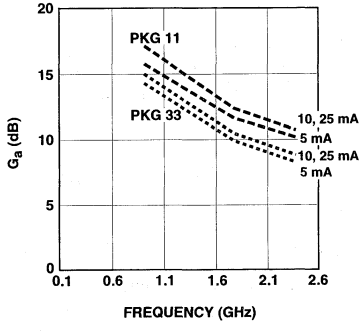


Figure 6. AT-41511 and AT-41533 Associated Gain vs. Frequency and Current at V_{CE} = 8 V.

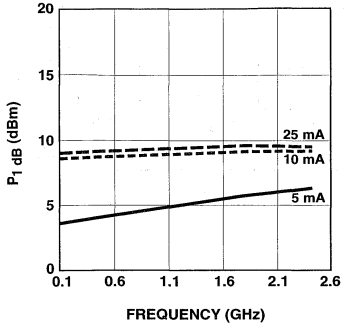


Figure 7. AT-41511 and AT-41533 P_{1dB} vs. Frequency and Bias at V_{CE} = 2.7 V, with Optimal Tuning.

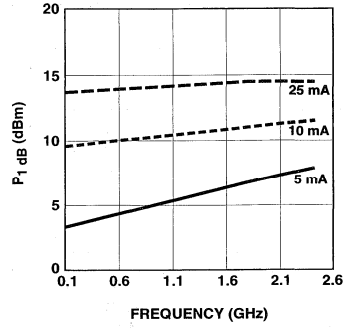


Figure 8. AT-41511 and AT-41533 P_{1dB} vs. Frequency and Bias at V_{CE} = 5 V, with Optimal Tuning.

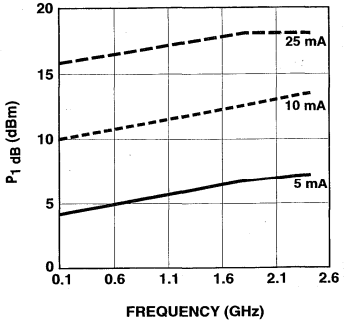


Figure 9. AT-41511 and AT-41533 P_{1dB} vs. Frequency and Bias at V_{CE} = 8 V, with Optimal Tuning.

AT-41511 Typical Scattering Parameters, Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 2.7\,V$, $I_C = 5\,mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.84	-27	23.44	14.854	161	-34.89	0.018	76	0.95	-11
0.5	0.59	-102	19.01	8.924	115	-24.88	0.057	48	0.65	-34
0.9	0.49	-141	15.09	5.684	93	-22.97	0.071	43	0.51	-39
1.0	0.48	-149	14.30	5.189	89	-22.73	0.073	43	0.49	-39
1.5	0.46	-176	11.15	3.61	72	-21.21	0.087	44	0.44	-43
1.8	0.46	170	9.69	3.051	64	-20.26	0.097	45	0.43	-45
2.0	0.46	162	8.86	2.774	59	-19.74	0.103	45	0.42	-47
2.4	0.47	148	7.37	2.337	50	-18.64	0.117	46	0.42	-51
3.0	0.5	130	5.58	1.901	36	-17.14	0.139	45	0.41	-59
4.0	0.56	106	3.25	1.454	17	-14.89	0.18	42	0.4	-73
5.0	0.61	87	1.36	1.17	0	-12.96	0.225	37	0.4	-91

AT-41511 Typical Noise Parameters,
Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 2.7\,V$, $I_C = 5\,mA$

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	0.8	0.45	6	0.25
0.9	1.0	0.39	63	0.19
1.8	1.4	0.32	137	0.12
2.4	1.7	0.40	177	0.09

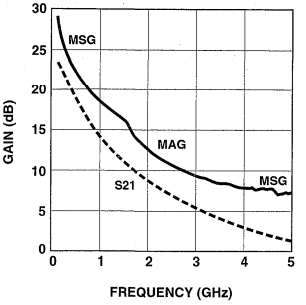


Figure 10. AT-41511 Gains vs. Frequency at $V_{CE} = 2.7\,V$, $I_C = 5\,mA$.

AT-41533 Typical Scattering Parameters, Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 2.7\,V$, $I_C = 5\,mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.78	-30	23.43	14.834	155	-33.98	0.020	75	0.94	-12
0.5	0.35	-99	16.91	7.004	103	-24.58	0.059	60	0.62	-28
0.9	0.23	-144	12.50	4.219	84	-21.21	0.087	62	0.55	-30
1.0	0.21	-154	11.65	3.826	80	-20.54	0.094	63	0.54	-31
1.5	0.20	162	8.50	2.661	64	-17.46	0.134	64	0.52	-36
1.8	0.22	144	7.09	2.261	56	-15.97	0.159	63	0.51	-40
2.0	0.23	134	6.30	2.065	51	-15.09	0.176	63	0.51	-42
2.4	0.26	118	4.97	1.773	42	-13.39	0.214	61	0.50	-48
3.0	0.30	101	3.45	1.488	30	-11.21	0.275	56	0.48	-58
4.0	0.37	80	1.66	1.211	13	-8.20	0.389	46	0.45	-80
5.0	0.44	62	0.35	1.041	-1	-5.90	0.507	33	0.42	-104

AT-41533 Typical Noise Parameters,
Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 2.7\,V$, $I_C = 5\,mA$

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	0.7	0.45	8	0.20
0.9	1.0	0.25	94	0.13
1.8	1.4	0.38	-159	0.08
2.4	1.6	0.54	-122	0.16

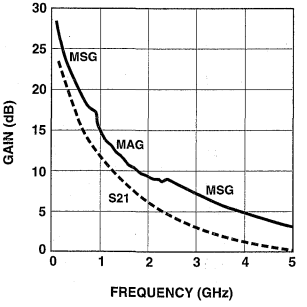


Figure 11. AT-41533 Gains vs. Frequency at $V_{CE} = 2.7\,V$, $I_C = 5\,mA$.

AT-41511 Typical Scattering Parameters, Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 2.7$ V, $I_C = 25$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.49	-91	29.26	29.048	136	-37.72	0.013	62	0.73	-22
0.5	0.53	-168	18.55	8.459	92	-30.46	0.030	61	0.45	-23
0.9	0.53	172	13.62	4.798	79	-26.56	0.047	66	0.42	-26
1.0	0.53	169	12.73	4.330	76	-25.68	0.052	67	0.42	-27
1.5	0.54	153	9.34	2.932	63	-22.50	0.075	67	0.42	-34
1.8	0.55	145	7.86	2.473	57	-21.01	0.089	66	0.42	-38
2.0	0.56	140	6.97	2.232	52	-20.09	0.099	66	0.42	-41
2.4	0.57	129	5.47	1.877	44	-18.49	0.119	64	0.42	-48
3.0	0.60	116	3.67	1.525	32	-16.54	0.149	59	0.41	-58
4.0	0.64	95	1.30	1.162	14	-13.98	0.200	51	0.40	-75
5.0	0.67	79	-0.58	0.935	-1	-11.90	0.254	43	0.39	-96

AT-41511 Typical Noise Parameters,
Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 2.7$ V, $I_C = 25$ mA

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	1.6	0.13	18	0.16
0.9	1.9	0.24	-162	0.13
1.8	2.3	0.40	-137	0.23
2.4	2.7	0.50	-122	0.35

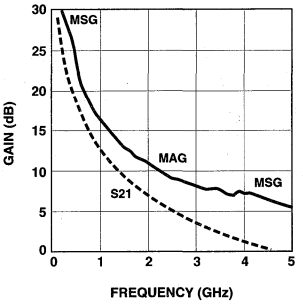


Figure 12. AT-41511 Gains vs. Frequency at $V_{CE} = 2.7$ V, $I_C = 25$ mA.

AT-41533 Typical Scattering Parameters, Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 2.7$ V, $I_C = 25$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.34	-75	29.37	29.404	127	-37.08	0.014	72	0.71	-21
0.5	0.19	-168	17.63	7.614	88	-25.68	0.052	76	0.47	-20
0.9	0.20	161	12.73	4.329	74	-20.82	0.091	74	0.46	-24
1.0	0.20	154	11.84	3.909	71	-19.91	0.101	74	0.45	-26
1.5	0.24	132	8.56	2.679	59	-16.42	0.151	70	0.45	-33
1.8	0.25	121	7.12	2.271	52	-14.85	0.181	67	0.44	-38
2.0	0.27	115	6.32	2.071	47	-13.94	0.201	65	0.44	-41
2.4	0.29	105	4.99	1.777	39	-12.32	0.242	61	0.43	-48
3.0	0.33	93	3.46	1.489	27	-10.31	0.305	54	0.41	-59
4.0	0.39	76	1.69	1.215	11	-7.66	0.414	42	0.37	-81
5.0	0.45	60	0.40	1.047	-3	-5.73	0.517	29	0.33	-106

AT-41533 Typical Noise Parameters,
Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 2.7$ V, $I_C = 25$ mA

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	1.3	0.10	24	0.12
0.9	1.6	0.25	-158	0.11
1.8	1.9	0.48	-122	0.19
2.4	2.1	0.59	-101	0.37

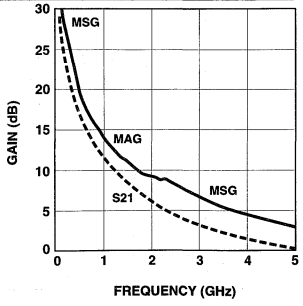


Figure 13. AT-41533 Gains vs. Frequency at $V_{CE} = 2.7$ V, $I_C = 25$ mA.

AT-41511 Typical Scattering Parameters, Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 5\ V$, $I_C = 5\ mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.88	-25	23.47	14.918	162	-34.89	0.018	77	0.95	-11
0.5	0.61	-96	19.31	9.234	116	-25.04	0.056	49	0.66	-33
0.9	0.50	-135	15.49	5.948	94	-23.22	0.069	44	0.52	-38
1.0	0.48	-142	14.70	5.433	90	-22.85	0.072	43	0.50	-39
1.5	0.45	-170	11.59	3.796	74	-21.31	0.086	44	0.45	-42
1.8	0.45	176	10.13	3.210	66	-20.45	0.095	45	0.44	-44
2.0	0.45	168	9.31	2.921	61	-19.91	0.101	46	0.43	-46
2.4	0.45	154	7.85	2.469	52	-18.86	0.114	46	0.42	-51
3.0	0.48	136	6.06	2.009	39	-17.33	0.136	46	0.42	-58
4.0	0.53	111	3.77	1.544	19	-15.09	0.176	43	0.40	-72
5.0	0.58	92	1.91	1.246	2	-13.07	0.222	39	0.40	-90

AT-41511 Typical Noise Parameters,
Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 5\ V$, $I_C = 5\ mA$

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	0.8	0.46	5	0.30
0.9	1.0	0.39	60	0.22
1.8	1.4	0.34	130	0.13
2.4	1.7	0.39	173	0.09

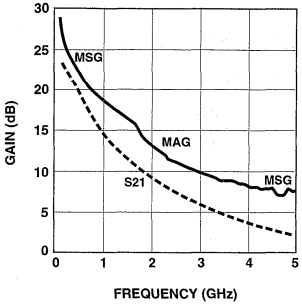


Figure 14. AT-41511 Gains vs. Frequency at $V_{CE} = 5\ V$, $I_C = 5\ mA$.

AT-41533 Typical Scattering Parameters, Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 5\ V$, $I_C = 5\ mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.79	-28	23.48	14.932	155	-34.89	0.018	76	0.95	-11
0.5	0.36	-94	17.15	7.200	104	-25.35	0.054	61	0.65	-25
0.9	0.22	-137	12.77	4.349	84	-21.94	0.080	63	0.58	-27
1.0	0.20	-148	11.93	3.948	81	-21.21	0.087	64	0.57	-29
1.5	0.18	165	8.77	2.746	65	-18.20	0.123	65	0.56	-34
1.8	0.19	145	7.34	2.328	58	-16.65	0.147	65	0.55	-37
2.0	0.21	134	6.56	2.128	53	-15.70	0.164	65	0.55	-39
2.4	0.24	118	5.22	1.823	44	-14.02	0.199	63	0.54	-45
3.0	0.28	100	3.68	1.527	32	-11.77	0.258	59	0.53	-55
4.0	0.35	80	1.87	1.240	14	-8.61	0.371	50	0.50	-74
5.0	0.42	61	0.52	1.062	0	-6.18	0.491	37	0.47	-97

AT-41533 Typical Noise Parameters,
Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 5\ V$, $I_C = 5\ mA$

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	0.7	0.46	7	0.21
0.9	1.0	0.29	86	0.13
1.8	1.4	0.36	-163	0.07
2.4	1.6	0.53	-126	0.15

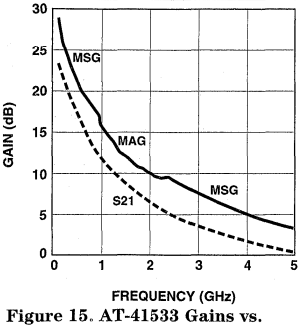


Figure 15. AT-41533 Gains vs. Frequency at $V_{CE} = 5\ V$, $I_C = 5\ mA$.

AT-41511 Typical Scattering Parameters, Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 5\,V$, $I_C = 25\,mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.51	-74	30	32.792	140	-39	0.011	65	0.80	-19
0.5	0.46	-161	20	10.259	95	-31	0.028	62	0.51	-21
0.9	0.47	177	15	5.830	80	-27	0.043	66	0.48	-23
1.0	0.47	173	14	5.257	78	-27	0.047	67	0.48	-24
1.5	0.48	157	11	3.553	65	-23	0.068	68	0.47	-30
1.8	0.49	148	9	2.983	58	-22	0.081	68	0.48	-34
2.0	0.49	142	9	2.692	54	-21	0.090	67	0.48	-36
2.4	0.51	132	7	2.254	46	-19	0.108	65	0.48	-42
3.0	0.54	118	5	1.825	34	-17	0.135	61	0.47	-51
4.0	0.59	97	3	1.386	16	-15	0.183	54	0.46	-66
5.0	0.63	81	1	1.113	0	-13	0.234	47	0.46	-84

AT-41511 Typical Noise Parameters,
Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 5\,V$, $I_C = 25\,mA$

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	1.6	0.08	14	0.18
0.9	1.9	0.11	165	0.16
1.8	2.3	0.28	-153	0.18
2.4	2.7	0.39	-134	0.22

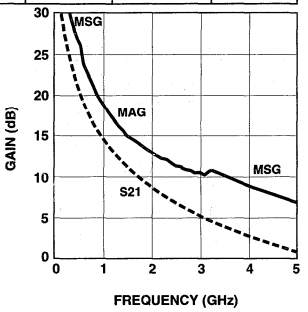


Figure 16. AT-41511 Gains vs. Frequency at $V_{CE} = 5\,V$, $I_C = 25\,mA$.

AT-41533 Typical Scattering Parameters, Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 5\,V$, $I_C = 25\,mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.37	-62	30.00	31.606	129	-37.72	0.013	73	0.74	-19
0.5	0.13	-153	18.46	8.375	89	-26.20	0.049	76	0.51	-19
0.9	0.13	163	13.56	4.764	76	-21.31	0.086	75	0.49	-23
1.0	0.13	154	12.68	4.305	73	-20.45	0.095	74	0.49	-25
1.5	0.17	128	9.38	2.945	61	-16.95	0.142	71	0.48	-31
1.8	0.19	117	7.93	2.493	54	-15.39	0.170	68	0.48	-35
2.0	0.20	111	7.14	2.274	50	-14.47	0.189	66	0.48	-38
2.4	0.23	102	5.80	1.949	42	-12.84	0.228	62	0.47	-44
3.0	0.27	90	4.25	1.632	31	-10.84	0.287	56	0.45	-54
4.0	0.33	76	2.48	1.331	14	-8.13	0.392	45	0.42	-74
5.0	0.39	60	1.19	1.147	-1	-6.09	0.496	32	0.38	-97

AT-41533 Typical Noise Parameters,
Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 5\,V$, $I_C = 25\,mA$

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	1.3	0.08	13	0.12
0.9	1.6	0.19	-170	0.10
1.8	1.9	0.42	-126	0.16
2.4	2.1	0.55	-105	0.32

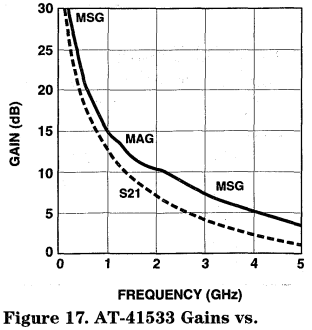


Figure 17. AT-41533 Gains vs. Frequency at $V_{CE} = 5\,V$, $I_C = 25\,mA$.

AT-41511 Typical Scattering Parameters, Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 8\,V$, $I_C = 10\,mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.75	-36	27.71	24.305	155	-37.72	0.013	73	0.92	-13
0.5	0.47	-119	21.24	11.535	106	-28.87	0.036	53	0.60	-27
0.9	0.41	-155	16.80	6.921	88	-26.20	0.049	55	0.51	-28
1.0	0.40	-161	15.96	6.281	84	-25.68	0.052	56	0.50	-29
1.5	0.39	174	12.66	4.294	70	-23.10	0.070	58	0.48	-32
1.8	0.40	162	11.16	3.615	63	-21.83	0.081	59	0.48	-35
2.0	0.40	155	10.29	3.269	59	-21.11	0.088	58	0.48	-37
2.4	0.42	143	8.77	2.745	50	-19.66	0.104	58	0.48	-41
3.0	0.44	126	6.95	2.226	38	-17.86	0.128	55	0.47	-48
4.0	0.51	104	4.60	1.698	19	-15.44	0.169	50	0.46	-61
5.0	0.56	87	2.73	1.370	3	-13.39	0.214	45	0.46	-76

AT-41511 Typical Noise Parameters,
Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 8\,V$, $I_C = 10\,mA$

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	1.1	0.40	7	0.27
0.9	1.3	0.33	62	0.20
1.8	1.6	0.27	135	0.13
2.4	1.8	0.35	178	0.10

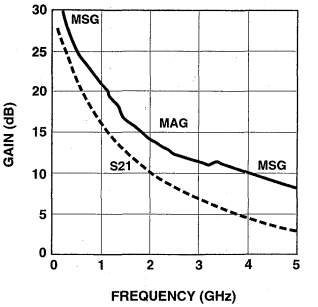


Figure 18. AT-41511 Gains vs. Frequency at $V_{CE} = 8\,V$, $I_C = 10\,mA$.

AT-41533 Typical Scattering Parameters, Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 8\,V$, $I_C = 10\,mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.65	-37	27.45	23.576	145	-35.92	0.016	73	0.88	-15
0.5	0.20	-100	18.60	8.509	97	-26.20	0.049	69	0.57	-23
0.9	0.11	-146	13.89	4.947	81	-21.83	0.081	71	0.54	-25
1.0	0.09	-161	13.03	4.482	78	-20.92	0.090	70	0.53	-26
1.5	0.11	144	9.77	3.081	64	-17.59	0.132	69	0.52	-32
1.8	0.13	125	8.34	2.611	58	-16.03	0.158	67	0.51	-35
2.0	0.14	116	7.53	2.379	53	-15.09	0.176	65	0.51	-38
2.4	0.17	104	6.20	2.041	45	-13.47	0.212	62	0.50	-43
3.0	0.22	91	4.66	1.710	33	-11.40	0.269	57	0.49	-52
4.0	0.28	77	2.90	1.396	16	-8.61	0.371	47	0.46	-71
5.0	0.35	62	1.61	1.204	1	-6.45	0.476	35	0.43	-92

AT-41533 Typical Noise Parameters,
Common Emitter, $Z_o = 50\,\Omega$, $V_{CE} = 8\,V$, $I_C = 10\,mA$

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	0.8	0.40	13	0.18
0.9	1.1	0.20	93	0.12
1.8	1.5	0.32	-154	0.09
2.4	1.7	0.49	-121	0.17

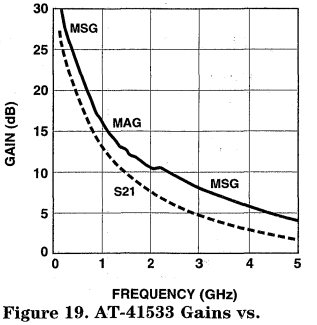


Figure 19. AT-41533 Gains vs. Frequency at $V_{CE} = 8\,V$, $I_C = 10\,mA$.

AT-41511 Typical Scattering Parameters, Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 8$ V, $I_C = 25$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.55	-65	30.44	33.264	142	-39.17	0.011	66	0.82	-17
0.5	0.44	-155	20.69	10.832	96	-31.37	0.027	61	0.54	-21
0.9	0.44	-179	15.83	6.190	81	-27.54	0.042	66	0.50	-22
1.0	0.44	176	14.95	5.588	78	-26.74	0.046	67	0.50	-23
1.5	0.45	159	11.55	3.779	66	-23.61	0.066	67	0.49	-29
1.8	0.46	150	10.03	3.173	59	-22.16	0.078	67	0.50	-32
2.0	0.46	144	9.14	2.865	55	-21.31	0.086	66	0.50	-35
2.4	0.48	133	7.61	2.401	46	-19.66	0.104	65	0.50	-40
3.0	0.51	119	5.78	1.945	35	-17.72	0.130	61	0.49	-48
4.0	0.57	99	3.39	1.477	17	-15.09	0.176	55	0.49	-63
5.0	0.61	83	1.49	1.187	1	-12.92	0.226	48	0.48	-80

AT-41511 Typical Noise Parameters,
Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 8$ V, $I_C = 25$ mA

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	1.6	0.08	10	0.20
0.9	1.9	0.10	100	0.19
1.8	2.3	0.22	-170	0.18
2.4	2.7	0.32	-147	0.18

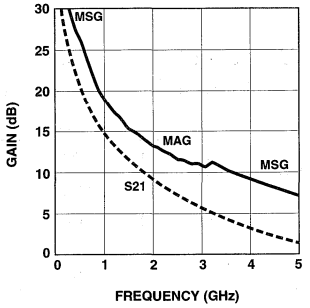


Figure 20. AT-41511 Gains vs. Frequency at $V_{CE} = 8$ V, $I_C = 25$ mA.

AT-41533 Typical Scattering Parameters, Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 8$ V, $I_C = 25$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	0.41	-57	30.11	32.026	130	-37.72	0.013	73	0.76	-18
0.5	0.11	-138	18.75	8.664	90	-26.38	0.048	76	0.52	-19
0.9	0.10	168	13.87	4.938	77	-21.51	0.084	75	0.50	-22
1.0	0.10	156	12.99	4.460	74	-20.63	0.093	74	0.50	-24
1.5	0.14	126	9.70	3.054	62	-17.14	0.139	71	0.49	-31
1.8	0.16	115	8.25	2.585	55	-15.60	0.166	68	0.49	-34
2.0	0.17	108	7.45	2.359	51	-14.66	0.185	66	0.49	-37
2.4	0.20	99	6.11	2.020	43	-13.03	0.223	62	0.48	-43
3.0	0.24	89	4.56	1.691	32	-11.03	0.281	56	0.46	-53
4.0	0.30	75	2.80	1.380	15	-8.31	0.384	45	0.43	-72
5.0	0.37	61	1.51	1.190	0	-6.25	0.487	33	0.39	-94

AT-41533 Typical Noise Parameters,
Common Emitter, $Z_o = 50\ \Omega$, $V_{CE} = 8$ V, $I_C = 25$ mA

Freq	F_{min}	Γ_{opt}		R_n
GHz	dB	Mag	Ang	-
0.1	1.3	0.07	18	0.16
0.9	1.6	0.12	164	0.12
1.8	1.9	0.36	-134	0.15
2.4	2.1	0.51	-109	0.28

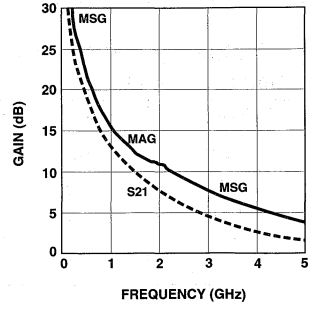
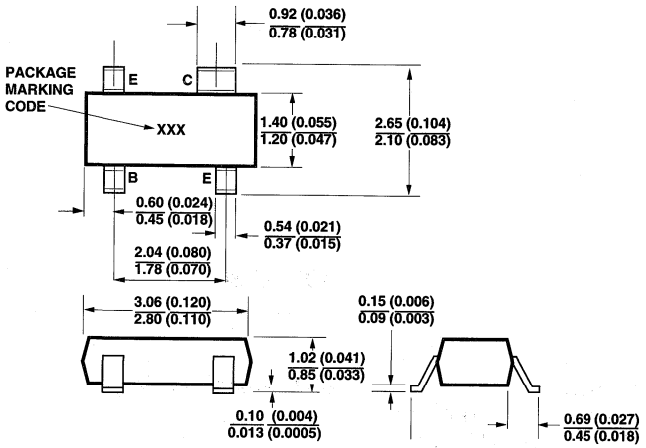


Figure 21. AT-41533 Gains vs. Frequency at $V_{CE} = 8$ V, $I_C = 25$ mA.

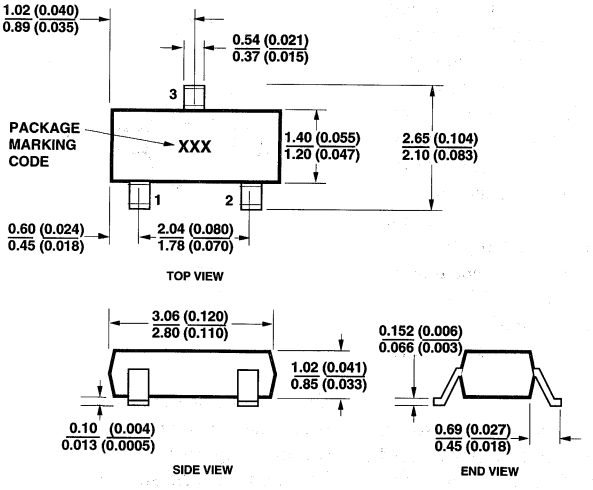
Package Dimensions

SOT-143 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

SOT-23 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Low Cost General Purpose Transistors

Technical Data

AT-41586

Features

- **Low Noise Figure**
  1.4 dB Typical at 1 GHz
  1.7 dB Typical at 2 GHz
- **High Associated Gain**
  17.0 dB Typical at 1 GHz
  12.5 dB Typical at 2 GHz
- **Low Cost Surface Mount Package**
- **Tape and Reel Option Available**

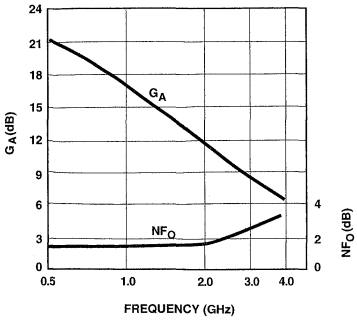


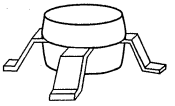
Figure 1. AT-41586 Noise Figure and Associated Gain vs. Frequency at V_{CE} = 8 V, I_C = 10 mA.

Description

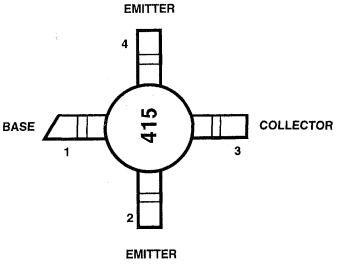
Hewlett-Packard's AT-41586 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-41586 is housed in a low cost surface mount .085" diameter plastic package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 14 emitter finger interdigitated geometry yields an intermediate sized transistor with impedances that are easy to match for low noise and moderate power applications. Applications include use in wireless systems as an LNA, gain stage, buffer, oscillator, and mixer. An optimum noise match near 50 Ω in the 1 to 2 GHz frequency range, makes this device easy to use as a low noise amplifier.

The AT-41586 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection.

86 Plastic Package



Pin Connections



Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

AT-41586 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	60
P_T	Power Dissipation[2]	mW	500
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance:[3]
θ_{jc} = 165°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. See MEASUREMENTS section, "Thermal Resistance," for more information.

Electrical Specifications, T_A = 25°C, V_{CE} = 8 V

Symbol	Parameters and Test Conditions		Unit	Min.	Typ.	Max.
NF_o	Optimum Noise Figure: I_C = 10 mA	f = 1.0 GHz	dB		1.4	
		f = 2.0 GHz			1.7	
		f = 4.0 GHz			3.0	
G_A	Gain @ NF_0: I_C = 10 mA	f = 1.0 GHz	dB		17.0	
		f = 2.0 GHz			12.5	
		f = 4.0 GHz			8.0	
$\|S_{21E}\|^2$	Insertion Power Gain: I_C = 25 mA	f = 1.0 GHz	dB		17.0	
		f = 2.0 GHz			11.0	
P_{1dB}	Power Output @ 1 dB Gain Compression: I_C = 25 mA	f = 2.0 GHz	dBm		18.0	
G_{1dB}	1 dB Compressed Gain: I_C = 25 mA	f = 2.0 GHz	dB		13.0	
f_T	Gain Bandwidth Product: I_C = 25 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: I_C = 10 mA			30	150	270
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0

Note:
1. For more information on outlines 86, refer to "Tape and Reel Packaging for Surface Mount Devices."

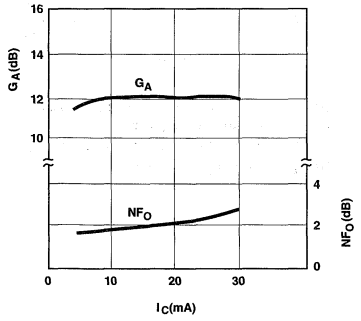


Figure 2. AT-41586 Optimum Noise Figure and Associated Gain vs. Collector Current at V_{CE} = 8 V, f = 2.0 GHz.

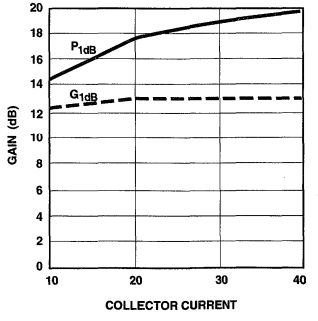


Figure 3. AT-41586 P_{1dB} and G_{1dB} vs. Collector Current at V_{CE} = 8 V, f = 2.0 GHz.

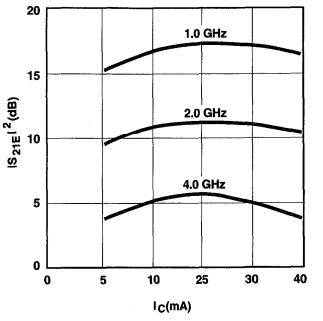


Figure 4. AT-41586 Insertion Power Gain vs. Collector Current and Frequency at 25°C, V_{CE} = 8 V.

AT-41586 Typical Scattering Parameters at T_A = 25°C

V_{CE} = 8 V, I_C = 10 mA, Z_o = 50 Ω

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.100	0.78	-39	28.4	26.3	154	-36.4	0.015	71	0.91	-16
0.200	0.71	-71	26.9	22.1	134	-31.7	0.026	59	0.79	-27
0.300	0.65	-95	25.2	18.1	122	-29.8	0.032	50	0.67	-34
0.400	0.61	-113	23.5	15.0	119	-28.8	0.036	44	0.58	-38
0.500	0.59	-127	22.0	12.6	114	-28.1	0.039	43	0.52	-40
0.600	0.57	-137	20.7	10.8	100	-27.5	0.042	43	0.47	-40
0.700	0.56	-146	19.6	9.5	95	-27.1	0.044	43	0.44	-41
0.800	0.56	-154	18.5	8.4	91	-26.5	0.047	43	0.42	-41
0.900	0.55	-160	17.6	7.6	86	-26.1	0.049	44	0.40	-42
1.000	0.55	-166	16.8	6.9	83	-25.8	0.051	47	0.38	-42
1.500	0.55	173	13.4	4.7	70	-23.8	0.064	49	0.34	-45
2.000	0.57	157	10.9	3.5	57	-22.0	0.079	49	0.32	-52
2.500	0.59	144	9.2	2.9	44	-20.6	0.093	48	0.31	-61
3.000	0.62	133	7.6	2.4	34	-19.3	0.108	47	0.30	-71
3.500	0.64	123	6.0	2.0	25	-18.1	0.124	45	0.30	-83
4.000	0.67	114	5.1	1.8	16	-17.0	0.141	42	0.31	-95
4.500	0.70	106	4.1	1.6	5	-15.9	0.159	39	0.32	-108
5.000	0.73	99	2.9	1.4	-3	-15.0	0.176	35	0.32	-121
5.500	0.76	93	1.6	1.2	-8	-14.2	0.193	31	0.34	-135
6.000	0.78	88	0.8	1.1	-18	-13.5	0.209	31	0.36	-150

AT-41586 Typical Noise Parameters at T_C = 25°C,

Z_O = 50 Ω, I_C = 10 mA, V_{CE} = 8 V

Frequency (GHz)	NF_O (dB)	Γ_{opt} Mag.	Ang.	$R_N/50\ \Omega$
0.1	1.3	0.12	3	0.17
0.5	1.3	0.10	16	0.17
1.0	1.4	0.04	43	0.16
2.0	1.7	0.12	-145	0.16

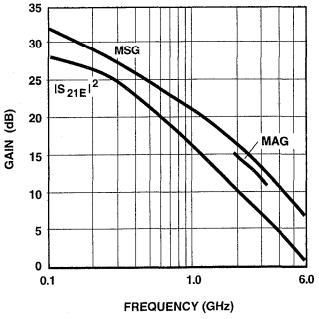


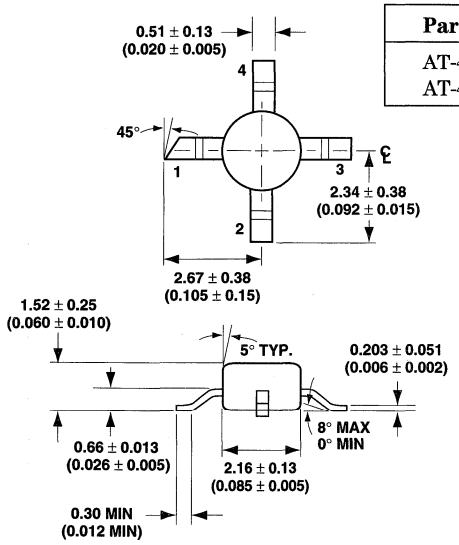
Figure 5. AT-41586 Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency at V_{CE} = 8 V, I_C = 10 mA.

AT-41586 Typical Scattering Parameters at T_A = 25°C

V_{CE} = 8 V, I_C = 25 mA, Z_o = 50 Ω

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.100	0.64	-61	31.9	39.4	154	-37.0	0.014	64	0.82	-24
0.200	0.59	-101	29.2	28.7	169	-33.1	0.022	53	0.64	-35
0.300	0.56	-125	26.6	21.4	124	-31.7	0.026	49	0.53	-38
0.400	0.55	-140	24.6	17.0	111	-30.4	0.030	49	0.47	-39
0.500	0.54	-151	22.9	14.0	104	-29.6	0.033	50	0.43	-38
0.600	0.54	-159	21.4	11.7	97	-28.8	0.036	52	0.40	-38
0.700	0.54	-166	20.1	10.1	91	-28.1	0.039	53	0.40	-37
0.800	0.54	-171	19.0	8.9	86	-27.5	0.042	55	0.38	-37
0.900	0.54	-176	18.0	7.9	81	-26.9	0.045	56	0.37	-37
1.000	0.55	177	17.1	7.2	77	-26.3	0.048	57	0.36	-37
1.500	0.57	164	13.6	4.8	64	-23.8	0.064	59	0.34	-42
2.000	0.57	152	11.1	3.6	55	-21.9	0.080	57	0.32	-49
2.500	0.60	141	9.2	2.9	44	-20.0	0.100	55	0.31	-58
3.000	0.62	132	7.6	2.4	34	-18.4	0.120	52	0.31	-68
3.500	0.64	124	6.4	2.1	24	-17.0	0.140	49	0.31	-80
4.000	0.67	116	5.6	1.9	18	-14.8	0.180	45	0.32	-94
4.500	0.70	109	4.1	1.6	9	-15.9	0.160	45	0.30	-109
5.000	0.73	102	3.5	1.5	1	-15.3	0.170	42	0.30	-123
5.500	0.77	96	2.3	1.3	-7	-14.4	0.190	38	0.32	-138
6.000	0.76	90	1.6	1.2	-14	-13.9	0.200	33	0.35	-152

Outline 86 Dimensions

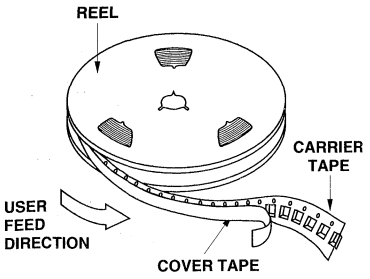


DIMENSIONS ARE IN MILLIMETERS (INCHES)

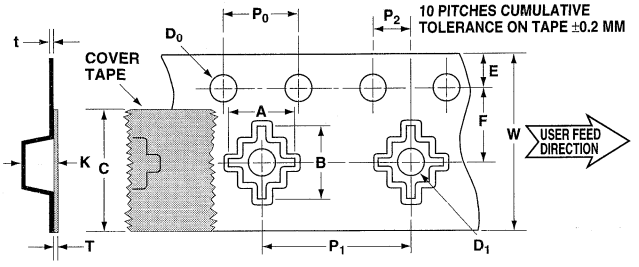
AT-41586 Ordering Information

Part Number	Increment	Comments
AT-41586-BLK	100	Bulk
AT-41586-TR1	1000	7" Reel

Device Orientation



Tape Dimensions and Product Orientation



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	6.45 ± 0.10	0.254 ± 0.004
	WIDTH	B_0	5.13 ± 0.10	0.202 ± 0.004
	DEPTH	K_0	2.11 ± 0.10	0.083 ± 0.004
	PITCH	P_1	8.00 ± 0.10	0.315 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.50 min.	0.059 min.
PERFORATION	DIAMETER	D_0	1.50 + 0.10/-0	0.059 + 0.004/-0
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t	0.255 ± 0.013	0.0100 ± 0.0005
COVER TAPE	WIDTH	C	9.19 ± 0.10	0.362 ± 0.004
	TAPE THICKNESS	T_t	0.051 ± 0.010	0.0020 ± 0.0004
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	5.51 ± 0.05	0.217 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

Up to 6 GHz Medium Power Silicon Bipolar Transistor Chip

Technical Data

AT-42000

Features

- **High Output Power:** 21.0 dBm Typical $P_{1\,dB}$ at 2.0 GHz 20.5 dBm Typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:** 15.0 dB Typical $G_{1\,dB}$ at 2.0 GHz 10.0 dB Typical $G_{1\,dB}$ at 4.0 GHz
- **Low Noise Figure:** 1.9 dB Typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:** 9.0 GHz Typical f_T

Description

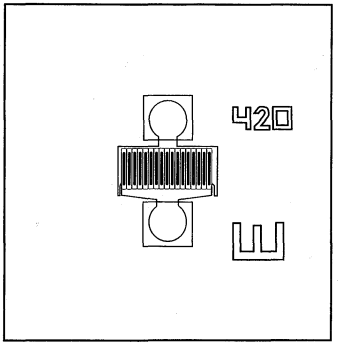
Hewlett-Packard's AT-42000 is a general purpose NPN bipolar transistor chip that offers excellent high frequency performance. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 20 emitter finger interdigitated geometry yields a medium sized transistor with impedances that are easy to match for low noise and medium power applications.

This device is designed for use in low noise, wideband amplifier, mixer and oscillator applications in the VHF, UHF, and microwave frequencies. An optimum noise match near 50 Ω up to 1 GHz , makes this device easy to use as a low noise amplifier.

The AT-42000 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See APPLICATIONS section, "Chip Use".

Chip Outline



AT-42000 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	80
P_T	Power Dissipation[2,3]	mW	600
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to 200

Thermal Resistance[2,4]:
θ_{jc} = 70°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ = 25°C.
3. Derate at 14.3 mW/°C for $T_{Mounting\ Surface}$ > 158°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

Part Number	Devices Per Tray
AT-42000-GP4	100

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		11.5 5.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f= 4.0 GHz	dBm		21.0 20.5	
$G_{1\,dB}$	1 dB Compressed Gain; V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		15.0 10.0	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		1.9 3.0	
G_A	Gain @ NF_O; V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		9.0	
h_{FE}	Forward Current Transfer Ratio; V_{CE} = 8 V, I_C = 35 mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current; V_{EB} = 1 V		μA			2.0
C_{CB}	Collector Base Capacitance[2]: V_{CB} = 8 V, f = 1 MHz		pF		0.23	

Notes:
1. RF performance is determined by packaging and testing 10 devices per wafer.
2. For this test, the emitter is grounded.

AT-42000 Typical Performance, T_A = 25°C

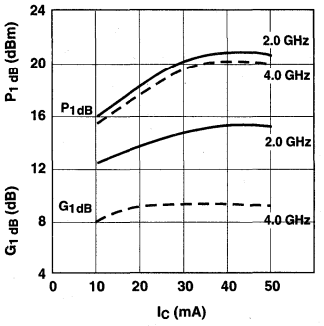


Figure 1. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

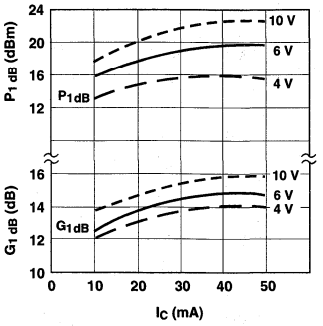


Figure 2. Output Power and 1 dB Compressed Gain vs. Collector Current and Voltage. f = 2.0 GHz.

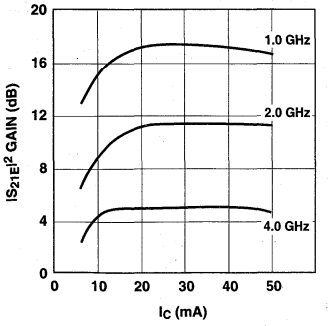


Figure 3. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

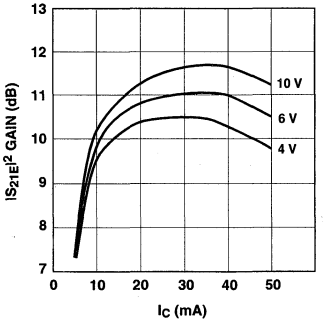


Figure 4. Insertion Power Gain vs. Collector Current and Voltage. f = 2.0 GHz.

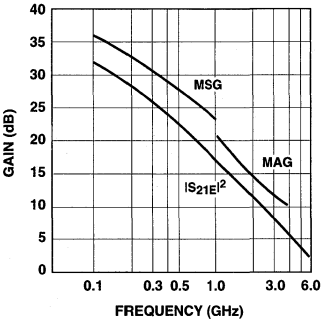


Figure 5. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 35 mA.

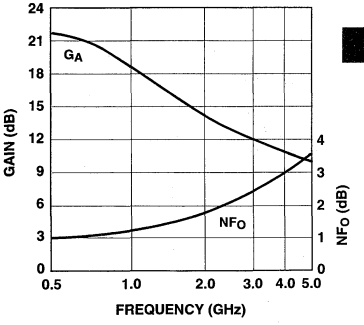


Figure 6. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

AT-42000 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.70	-50	28.0	25.19	155	-37.7	.013	71	.92	-14
0.5	.67	-136	20.9	11.04	108	-30.5	.030	43	.57	-27
1.0	.66	-166	15.7	6.08	90	-28.9	.036	47	.50	-24
1.5	.66	-173	12.1	4.02	86	-28.2	.039	52	.48	-23
2.0	.66	179	9.8	3.09	82	-27.5	.042	57	.47	-23
2.5	.67	170	7.8	2.46	74	-26.0	.050	66	.47	-23
3.0	.67	165	6.3	2.08	68	-24.7	.058	72	.47	-26
3.5	.70	157	5.1	1.80	61	-23.4	.068	77	.47	-28
4.0	.70	151	3.9	1.56	57	-21.8	.081	82	.48	-30
4.5	.71	145	2.9	1.40	51	-20.7	.092	86	.50	-34
5.0	.73	138	1.9	1.24	41	-19.3	.109	87	.51	-38
5.5	.74	132	1.2	1.15	36	-17.2	.138	88	.51	-50
6.0	.76	129	0.2	1.02	32	-16.3	.154	87	.53	-56

AT-42000 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 35 mA

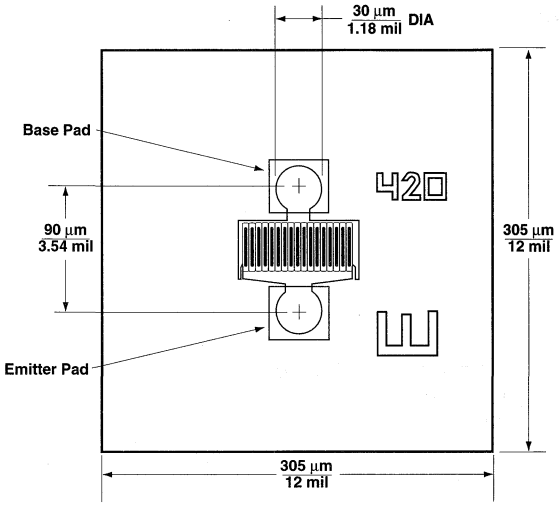
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.49	-96	33.0	44.61	143	-40.9	.009	65	.79	-24
0.5	.62	-163	22.8	13.87	98	-34.4	.019	58	.42	-26
1.0	.63	179	17.2	7.25	86	-30.5	.030	70	.38	-22
1.5	.63	171	13.5	4.74	78	-27.7	.041	76	.38	-23
2.0	.65	163	11.2	3.62	72	-25.4	.054	79	.38	-25
2.5	.65	159	9.3	2.90	67	-23.6	.066	82	.38	-27
3.0	.68	154	7.8	2.44	60	-22.1	.079	82	.38	-29
3.5	.67	148	6.5	2.12	57	-20.6	.093	84	.39	-32
4.0	.69	144	5.3	1.83	51	-19.7	.104	86	.40	-34
4.5	.70	139	4.4	1.65	47	-18.3	.121	86	.41	-40
5.0	.70	137	3.3	1.46	43	-17.5	.133	85	.42	-44
5.5	.72	131	2.7	1.36	38	-16.5	.149	86	.41	-48
6.0	.74	128	1.7	1.22	34	-15.7	.164	85	.44	-55

A model for this device is available in the DEVICE MODELS section.

AT-42000 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.0	.04	13	0.13
0.5	1.1	.05	69	0.13
1.0	1.5	.09	127	0.12
2.0	1.9	.23	171	0.11
4.0	3.0	.47	-154	0.14

AT-42000 Chip Dimensions



Note: Die thickness is 5 to 6 mil.

HEWLETT® PACKARD

Up to 6 GHz Medium Power Silicon Bipolar Transistor

Technical Data

AT-42010

Features

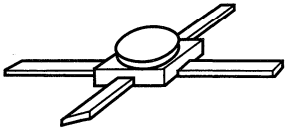
- **High Output Power:** 12.0 dBm Typical $P_{1\,dB}$ at 2.0 GHz 20.5 dBm Typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:** 14.0 dB Typical $G_{1\,dB}$ at 2.0 GHz 9.5 dB Typical $G_{1\,dB}$ at 4.0 GHz
- **Low Noise Figure:** 1.9 dB Typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:** 8.0 GHz Typical f_T
- **Hermetic Gold-ceramic Microstrip Package**

Description

Hewlett-Packard's AT-42010 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-42010 is housed in a hermetic, high reliability 100 mil ceramic package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 20 emitter finger interdigitated geometry yields a medium sized transistor with impedances that are easy to match for low noise and medium power applications. This device is designed for use in low noise, wideband amplifier, mixer and oscillator applications in the VHF, UHF, and microwave frequencies. An optimum noise match near 50 Ω up to 1 GHz , makes this device easy to use as a low noise amplifier.

The AT-42010 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

100 mil Package



AT-42010 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	80
P_T	Power Dissipation[2,3]	mW	600
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to 200

Thermal Resistance[2,4]:
$\theta_{jc} = 150°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 6.7 mW/°C for $T_C > 110°C$.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; $V_{CE} = 8$ V, $I_C = 35$ mA	f = 2.0 GHz f = 4.0 GHz	dB	10.5	11.5 5.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression $V_{CE} = 8$ V, $I_C = 35$ mA	f = 2.0 GHz f= 4.0 GHz	dBm		21.0 20.5	
$G_{1\,dB}$	1 dB Compressed Gain; $V_{CE} = 8$ V, $I_C = 35$ mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 9.5	
NF_O	Optimum Noise Figure: $V_{CE} = 8$ V, $I_C = 10$ mA	f = 2.0 GHz f = 4.0 GHz	dB		1.9 3.0	
G_A	Gain @ NF_O; $V_{CE} = 8$ V, $I_C = 10$ mA	f = 2.0 GHz f = 4.0 GHz	dB		13.5 10.0	
f_T	Gain Bandwidth Product: $V_{CE} = 8$ V, $I_C = 35$ mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; $V_{CE} = 8$ V, $I_C = 35$ mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; $V_{CB} = 8$ V		μA			0.2
I_{EBO}	Emitter Cutoff Current; $V_{EB} = 1$ V		μA			2.0
C_{CB}	Collector Base Capacitance[1]: $V_{CB} = 8$ V, f = 1 MHz		pF		0.28	

Notes:
1. For this test, the emitter is grounded.

AT-42010 Typical Performance, T_A = 25°C

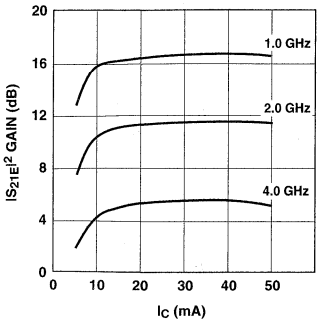


Figure 1. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

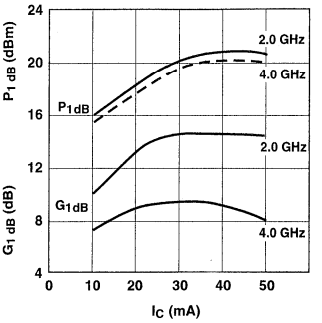


Figure 2. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

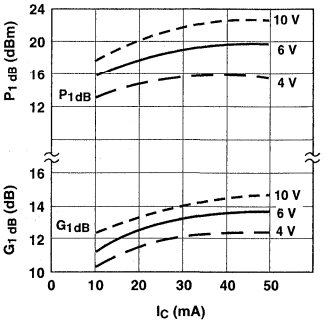


Figure 3. Output Power and 1 dB Compressed Gain vs. Collector Current and Voltage. f = 2.0 GHz.

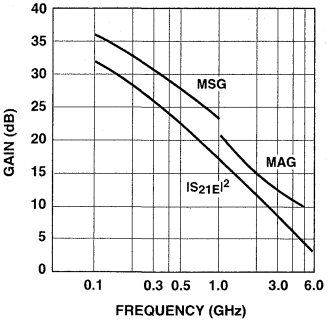


Figure 4. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 35 mA.

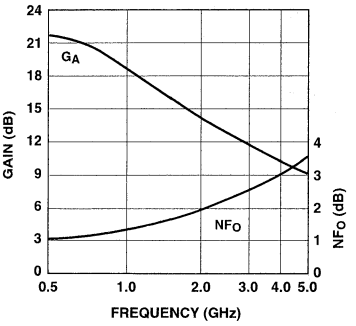


Figure 5. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

AT-42010 Typical Scattering Parameters, Common Emitter,

Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.74	-47	28.5	26.65	153	-36.4	.015	72	.91	-18
0.5	.65	-136	21.4	11.71	103	-29.4	.034	38	.51	-39
1.0	.63	-168	15.9	6.24	82	-27.2	.044	36	.40	-42
1.5	.63	174	12.6	4.26	69	-26.0	.050	42	.38	-45
2.0	.63	161	10.1	3.23	57	-24.6	.059	43	.38	-49
2.5	.64	154	8.4	2.64	51	-23.0	.070	52	.38	-51
3.0	.65	145	6.9	2.22	41	-22.0	.080	54	.37	-56
3.5	.66	136	5.8	1.94	31	-21.0	.090	51	.38	-65
4.0	.66	126	4.7	1.72	21	-19.7	.104	50	.39	-74
4.5	.66	115	3.8	1.55	11	-18.0	.126	45	.40	-82
5.0	.66	103	3.0	1.41	1	-17.3	.136	41	.40	-89
5.5	.68	90	2.1	1.28	-9	-16.1	.156	36	.40	-98
6.0	.72	81	1.3	1.16	-19	-15.4	.170	31	.37	-110

AT-42010 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 35 mA

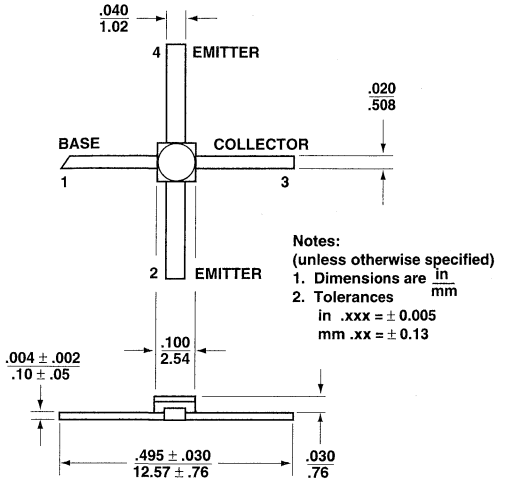
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.54	-90	33.3	45.97	138	-39.2	.011	54	.76	-29
0.5	.62	-163	22.8	13.83	94	-33.2	.022	52	.34	-40
1.0	.62	177	17.0	7.10	78	-28.8	.036	59	.30	-40
1.5	.62	166	13.6	4.82	67	-26.2	.049	61	.29	-42
2.0	.62	155	11.3	3.65	56	-23.8	.065	57	.29	-47
2.5	.63	150	9.5	2.99	51	-21.8	.081	62	.29	-50
3.0	.64	142	8.0	2.52	42	-21.0	.090	63	.30	-57
3.5	.65	133	6.8	2.19	32	-19.7	.103	59	.30	-67
4.0	.65	124	5.7	1.93	22	-18.4	.120	54	.31	-76
4.5	.65	113	4.7	1.72	13	-17.2	.138	49	.33	-85
5.0	.66	102	3.9	1.56	3	-16.6	.148	45	.34	-92
5.5	.69	91	3.0	1.41	-6	-15.6	.166	39	.33	-100
6.0	.73	83	2.1	1.27	-16	-14.9	.180	32	.30	-110

A model for this device is available in the DEVICE MODELS section.

AT-42010 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.0	.04	15	0.13
0.5	1.1	.05	76	0.12
1.0	1.5	.10	132	0.12
2.0	1.9	.23	-177	0.11
4.0	3.0	.45	-125	0.26

100 mil Package Dimensions



HEWLETT® PACKARD

Up to 6 GHz Medium Power Silicon Bipolar Transistor

Technical Data

AT-42035

Features

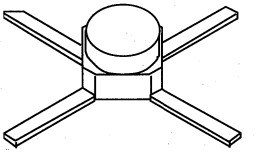
- **High Output Power:**
  21.0 dBm Typical $P_{1\,dB}$ at 2.0 GHz
  20.5 dBm Typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:**
  14.0 dB Typical $G_{1\,dB}$ at 2.0 GHz
  9.5 dB Typical $G_{1\,dB}$ at 4.0 GHz
- **Low Noise Figure:**
  1.9 dB Typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:** 8.0 GHz Typical f_T
- **Cost Effective Ceramic Microstrip Package**

Description

Hewlett-Packard's AT-42035 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-42035 is housed in a cost effective surface mount 100 mil micro-X package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 20 emitter finger interdigitated geometry yields a medium sized transistor with impedances that are easy to match for low noise and medium power applications. This device is designed for use in low noise, wideband amplifier, mixer and oscillator applications in the VHF, UHF, and microwave frequencies. An optimum noise match near 50 Ω up to 1 GHz, makes this device easy to use as a low noise amplifier.

The AT-42035 bipolar transistor is fabricated using Hewlett- Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

35 micro-X Package



5965-8911E

AT-42035 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	80
P_T	Power Dissipation[2,3]	mW	600
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature[4]	°C	-65 to 200

Thermal Resistance[2,5]:
$\theta_{jc} = 175°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 5.7 mW/°C for $T_C > 95°C$.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 200°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; $V_{CE} = 8$ V, $I_C = 35$ mA	f = 2.0 GHz f = 4.0 GHz	dB	10.0	11.0 5.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression $V_{CE} = 8$ V, $I_C = 35$ mA	f = 2.0 GHz f= 4.0 GHz	dBm		21.0 20.5	
$G_{1\,dB}$	1 dB Compressed Gain; $V_{CE} = 8$ V, $I_C = 35$ mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 9.5	
NF_O	Optimum Noise Figure: $V_{CE} = 8$ V, $I_C = 10$ mA	f = 2.0 GHz f = 4.0 GHz	dB		2.0 3.0	
G_A	Gain @ NF_O; $V_{CE} = 8$ V, $I_C = 10$ mA	f = 2.0 GHz f = 4.0 GHz	dB		13.5 10.0	
f_T	Gain Bandwidth Product: $V_{CE} = 8$ V, $I_C = 35$ mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; $V_{CE} = 8$ V, $I_C = 35$ mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; $V_{CB} = 8$ V		μA			0.2
I_{EBO}	Emitter Cutoff Current; $V_{EB} = 1$ V		μA			2.0
C_{CB}	Collector Base Capacitance[1]: $V_{CB} = 8$ V, f = 1 MHz		pF		0.28	

Notes:
1. For this test, the emitter is grounded.

AT-42035 Typical Performance, T_A = 25°C

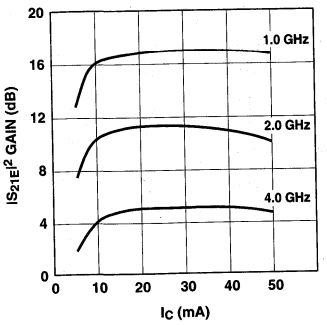


Figure 1. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

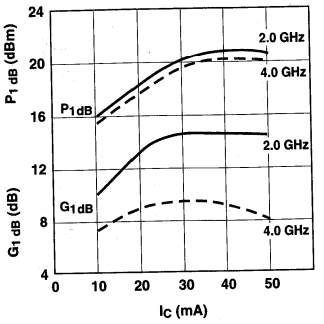


Figure 2. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

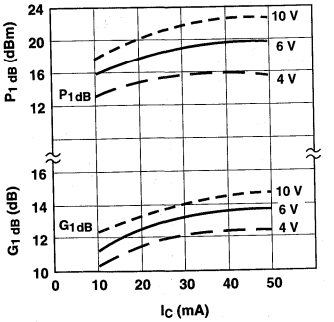


Figure 3. Output Power and 1 dB Compressed Gain vs. Collector Current and Voltage. f = 2.0 GHz.

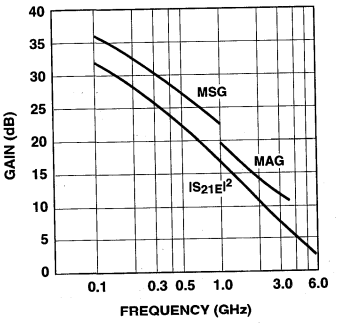


Figure 4. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 35 mA.

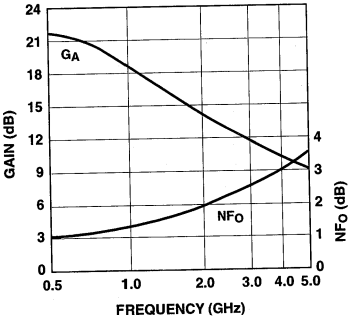


Figure 5. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

AT-42035 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.72	-46	28.3	26.09	152	-37.0	.014	73	.92	-14
0.5	.59	-137	20.9	11.13	102	-31.0	.028	44	.58	-27
1.0	.56	-171	15.4	5.91	80	-28.2	.039	47	.51	-29
1.5	.56	169	12.1	4.03	67	-26.6	.047	52	.50	-33
2.0	.58	155	9.7	3.06	55	-24.2	.062	55	.48	-38
2.5	.59	147	8.0	2.50	48	-22.6	.074	61	.47	-42
3.0	.61	137	6.5	2.10	38	-20.8	.092	65	.46	-51
3.5	.63	128	5.2	1.82	27	-19.6	.105	62	.47	-63
4.0	.63	117	4.0	1.60	17	-18.0	.126	57	.49	-72
4.5	.63	106	3.1	1.43	7	-16.5	.149	53	.51	-80
5.0	.64	93	2.3	1.30	-3	-15.4	.169	48	.52	-87
5.5	.67	79	1.5	1.19	-13	-14.3	.193	41	.51	-94
6.0	.72	70	0.6	1.07	-23	-13.4	.215	35	.46	-105

AT-42035 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 35 mA

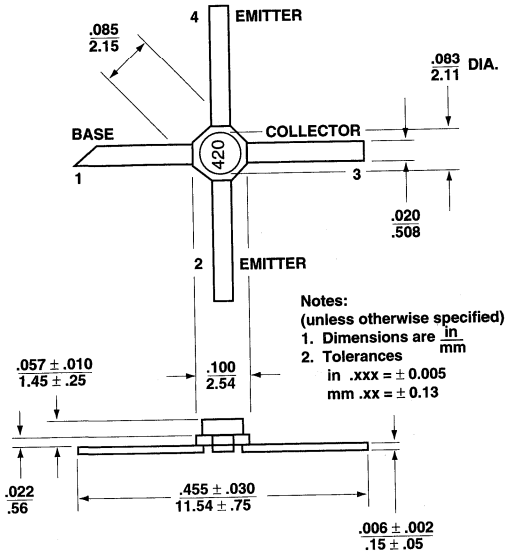
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.50	-88	33.2	45.64	135	-42.0	.008	68	.77	-22
0.5	.52	-164	22.4	13.24	92	-32.8	.023	57	.45	-25
1.0	.53	174	16.6	6.75	76	-28.2	.039	63	.42	-26
1.5	.53	160	13.1	4.55	64	-25.6	.053	66	.41	-30
2.0	.55	148	10.8	3.45	53	-23.2	.069	65	.41	-36
2.5	.57	142	9.0	2.81	47	-21.6	.084	67	.39	-40
3.0	.59	134	7.5	2.37	37	-20.0	.101	64	.38	-49
3.5	.60	125	6.3	2.06	27	-18.4	.120	61	.39	-61
4.0	.60	116	5.2	1.81	17	-17.0	.141	57	.41	-71
4.5	.60	104	4.2	1.62	7	-16.0	.158	50	.43	-78
5.0	.61	92	3.4	1.47	-2	-14.9	.179	45	.44	-84
5.5	.64	79	2.6	1.35	-13	-14.1	.198	37	.43	-91
6.0	.69	70	1.7	1.21	-23	-13.2	.219	30	.38	-102

A model for this device is available in the DEVICE MODELS section.

AT-42035 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.0	.04	10	0.13
0.5	1.1	.04	66	0.12
1.0	1.3	.07	150	0.12
2.0	2.0	.20	-178	0.12
4.0	3.0	.51	-110	0.36

35 micro-X Package Dimensions



HEWLETT® PACKARD

Up to 6 GHz Medium Power Silicon Bipolar Transistor

Technical Data

AT-42070

Features

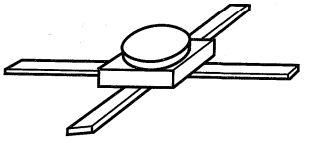
- **High Output Power:**
  21.0 dBm Typical $P_{1\,dB}$ at 2.0 GHz
  20.5 dBm Typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:**
  15.0 dB Typical $G_{1\,dB}$ at 2.0 GHz
  10.0 dB Typical $G_{1\,dB}$ at 4.0 GHz
- **Low Noise Figure:**
  1.9 dB Typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:** 8.0 GHz Typical f_T
- **Hermetic Gold-ceramic Microstrip Package**

Description

Hewlett-Packard's AT-42070 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-42070 is housed in a hermetic, high reliability gold-ceramic 70 mil microstrip package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 20 emitter finger interdigitated geometry yields a medium sized transistor with impedances that are easy to match for low noise and medium power applications. This device is designed for use in low noise, wideband amplifier, mixer and oscillator applications in the VHF, UHF, and microwave frequencies. An optimum noise match near 50 Ω up to 1 GHz, makes this device easy to use as a low noise amplifier.

The AT-42070 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

70 mil Package



AT-42070 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	80
P_T	Power Dissipation[2,3]	mW	600
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to 200

Thermal Resistance[2,4]:
θ_{jc} = 150°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.7 mW/°C for T_C > 110°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB	10.5	11.5 5.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f= 4.0 GHz	dBm		21.0 20.5	
$G_{1\,dB}$	1 dB Compressed Gain; V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		15.0 10.0	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		1.9 3.0	
G_A	Gain @ NF_O; V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; V_{CE} = 8 V, I_C = 35 mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current; V_{EB} = 1 V		μA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.28	

Note:
1. For this test, the emitter is grounded.

AT-42070 Typical Performance, T_A = 25°C

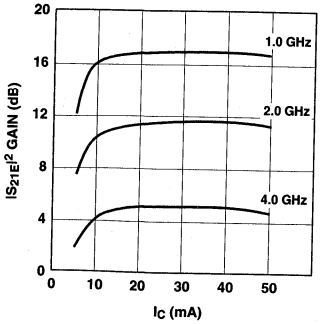


Figure 1. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

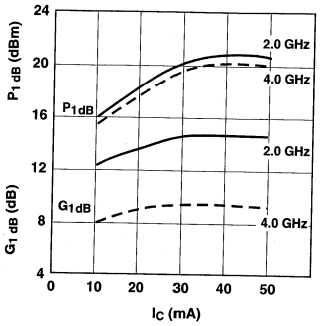


Figure 2. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

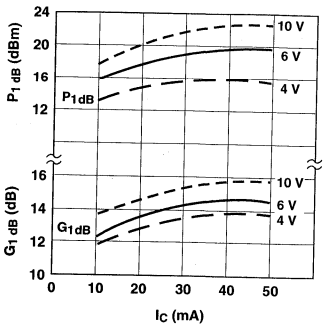


Figure 3. Output Power and 1 dB Compressed Gain vs. Collector Current and Voltage. f = 2.0 GHz.

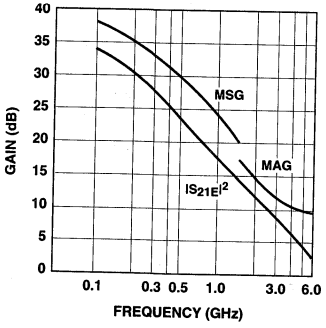


Figure 4. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 35 mA.

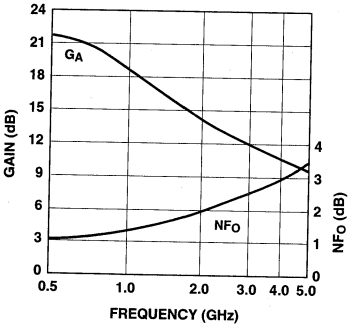


Figure 5. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

AT-42070 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.70	-49	28.5	26.56	154	-36.0	.016	77	.91	-18
0.5	.69	-137	21.5	11.85	105	-29.6	.033	34	.50	-41
1.0	.69	-165	16.0	6.34	85	-27.2	.044	29	.40	-44
1.5	.68	-179	12.7	4.33	72	-27.4	.043	37	.38	-48
2.0	.69	169	10.3	3.26	62	-25.6	.052	42	.37	-54
2.5	.69	164	8.5	2.64	56	-25.4	.054	46	.37	-55
3.0	.70	157	6.9	2.22	48	-23.8	.065	52	.39	-63
3.5	.70	151	5.6	1.91	39	-22.4	.076	51	.41	-71
4.0	.69	144	4.5	1.68	30	-21.4	.085	55	.43	-77
4.5	.68	137	3.5	1.50	22	-20.4	.096	49	.46	-83
5.0	.68	128	2.7	1.37	14	-19.4	.107	50	.48	-87
5.5	.68	117	2.0	1.26	5	-18.3	.121	45	.48	-91
6.0	.70	107	1.2	1.15	-3	-17.6	.132	44	.48	-98

AT-42070 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 35 mA

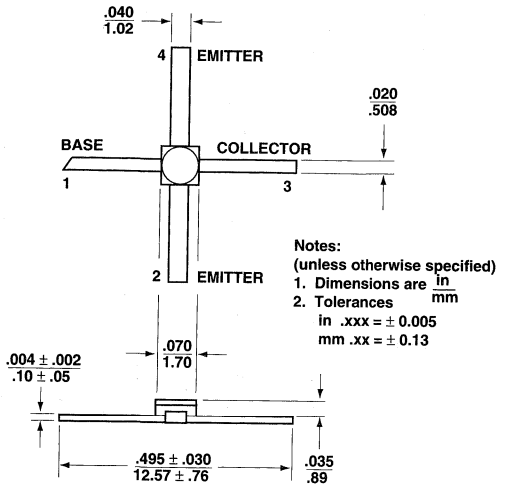
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.52	-95	33.4	46.52	139	-40.0	.010	50	.77	-29
0.5	.66	-163	23.1	14.33	95	-34.4	.019	46	.34	-42
1.0	.67	179	17.3	7.36	80	-29.6	.033	51	.28	-41
1.5	.67	169	13.9	4.97	69	-28.0	.040	59	.27	-44
2.0	.68	160	11.4	3.74	60	-27.3	.053	59	.27	-51
2.5	.69	157	9.6	3.04	55	-23.8	.065	65	.28	-53
3.0	.69	151	8.1	2.55	47	-22.8	.072	65	.28	-62
3.5	.69	145	6.8	2.20	39	-21.4	.086	59	.30	-72
4.0	.68	139	5.7	1.93	20	-20.2	.097	60	.33	-80
4.5	.67	132	4.7	1.74	22	-19.3	.109	54	.36	-85
5.0	.67	123	4.0	1.59	13	-18.0	.126	50	.38	-90
5.5	.67	113	3.2	1.46	5	-17.2	.138	46	.39	-94
6.0	.69	103	2.5	1.34	-4	-16.4	.152	40	.38	-102

A model for this device is available in the DEVICE MODELS section.

AT-42070 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.0	.05	15	0.13
0.5	1.1	.06	75	0.13
1.0	1.5	.10	126	0.12
2.0	1.9	.23	172	0.11
4.0	3.0	.45	-145	0.17

70 mil Package Dimensions



HEWLETT® PACKARD

Up to 6 GHz Medium Power Silicon Bipolar Transistor

Technical Data

AT-42085

Features

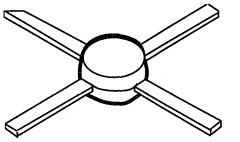
- **High Output Power:** 20.5 dBm Typical $P_{1\,dB}$ at 2.0 GHz
- **High Gain at 1 dB Compression:** 14.0 dB Typical $G_{1\,dB}$ at 2.0 GHz
- **Low Noise Figure:** 2.0 dB Typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:** 8.0 GHz Typical f_T
- **Low Cost Plastic Package**

Description

Hewlett-Packard's AT-42085 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-42085 is housed in a low cost .085" diameter plastic package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 20 emitter finger interdigitated geometry yields a medium sized transistor with impedances that are easy to match for low noise and medium power applications. Applications include use in wireless systems as an LNA, gain stage, buffer, oscillator, and mixer. An optimum noise match near 50 Ω up to 1 GHz, makes this device easy to use as a low noise amplifier.

The AT-42085 bipolar transistor is fabricated using Hewlett-Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

85 Plastic Package



5965-8913E

AT-42085 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	80
P_T	Power Dissipation[2,3]	mW	500
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2,4]:
θ_{jc} = 130°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.7 mW/°C for T_C > 85°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; V_{CE} = 8 V, I_C = 35 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	15.5	17.0 11.0 5.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f= 4.0 GHz	dBm		20.5 20.0	
$G_{1\,dB}$	1 dB Compressed Gain; V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 9.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		2.0 3.5	
G_A	Gain @ NF_O; V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		13.5 9.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; V_{CE} = 8 V, I_C = 35 mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current; V_{EB} = 1 V		μA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.32	

Note:
1. For this test, the emitter is grounded.

AT-42085 Typical Performance, T_A = 25°C

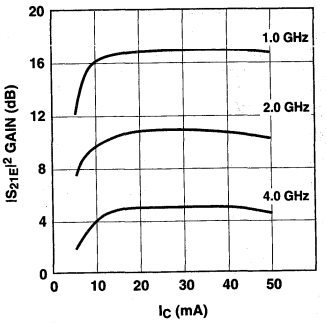


Figure 1. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

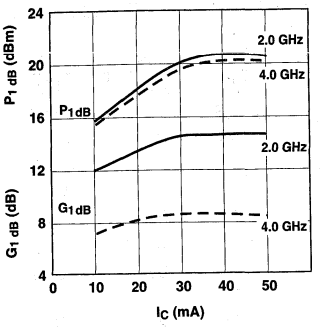


Figure 2. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

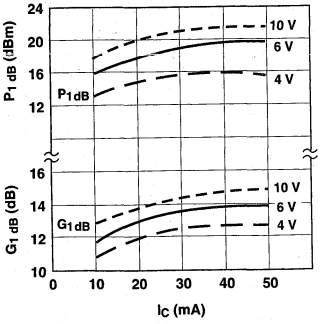


Figure 3. Output Power and 1 dB Compressed Gain vs. Collector Current and Voltage. f = 2.0 GHz.

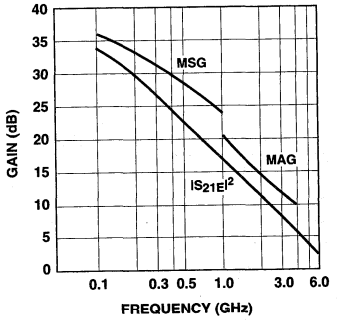


Figure 4. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 35 mA.

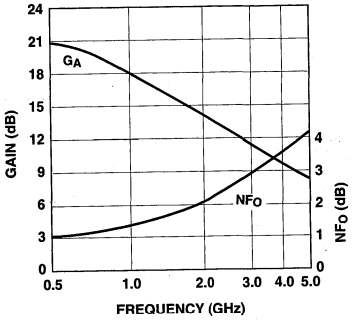


Figure 5. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

AT-42085 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.72	-50	28.5	26.52	152	-37.0	.014	73	.90	-16
0.5	.66	-139	21.0	11.23	103	-29.2	.035	36	.53	-32
1.0	.65	-168	15.5	5.96	84	-28.6	.037	39	.45	-33
1.5	.65	175	12.2	4.06	71	-27.0	.045	46	.43	-36
2.0	.65	163	9.7	3.06	60	-25.3	.054	51	.42	-41
2.5	.66	157	8.0	2.51	55	-24.0	.063	60	.42	-42
3.0	.68	149	6.3	2.07	46	-22.8	.072	65	.41	-48
3.5	.68	141	5.1	1.79	38	-21.4	.085	64	.43	-55
4.0	.69	133	3.9	1.57	29	-19.7	.104	64	.45	-61
4.5	.69	125	3.0	1.41	21	-18.5	.119	63	.46	-66
5.0	.69	114	2.2	1.28	12	-17.1	.139	58	.47	-71
5.5	.71	103	1.4	1.17	3	-15.9	.161	55	.44	-76
6.0	.75	91	0.6	1.07	-6	-15.1	.177	49	.40	-85

AT-42085 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 35 mA

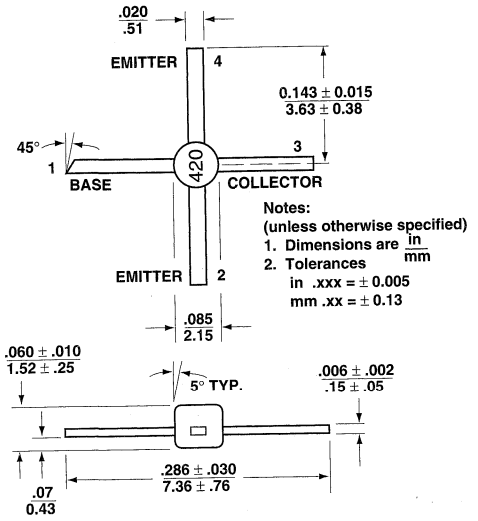
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.54	-90	33.1	45.38	137	-40.1	.010	66	.76	-26
0.5	.61	-163	22.6	13.45	95	-32.8	.023	52	.38	-30
1.0	.61	178	16.8	6.90	79	-29.5	.034	61	.34	-28
1.5	.62	167	13.4	4.67	68	-26.4	.048	68	.32	-31
2.0	.63	156	10.9	3.52	59	-23.9	.064	66	.31	-36
2.5	.64	152	9.2	2.89	54	-22.5	.075	68	.31	-40
3.0	.66	146	7.6	2.39	45	-21.2	.088	69	.30	-48
3.5	.67	139	6.3	2.07	37	-19.8	.102	67	.31	-58
4.0	.68	131	5.2	1.81	28	-18.6	.117	65	.33	-67
4.5	.68	123	4.2	1.62	19	-17.2	.138	60	.35	-73
5.0	.68	114	3.4	1.48	10	-16.4	.152	56	.35	-79
5.5	.71	103	2.5	1.34	1	-15.3	.171	50	.34	-85
6.0	.74	93	1.7	1.21	-8	-14.5	.188	46	.31	-96

A model for this device is available in the DEVICE MODELS section.

AT-42085 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.1	.05	16	0.13
0.5	1.2	.06	77	0.13
1.0	1.3	.10	131	0.12
2.0	2.0	.24	-179	0.11
4.0	3.5	.46	-128	0.25

85 Plastic Package Dimensions



HEWLETT® PACKARD

Up to 6 GHz Medium Power Silicon Bipolar Transistor

Technical Data

AT-42086

Features

- **High Output Power:** 20.5 dBm Typical $P_{1\,dB}$ at 2.0 GHz
- **High Gain at 1 dB Compression:** 13.5 dB Typical $G_{1\,dB}$ at 2.0 GHz
- **Low Noise Figure:** 1.9 dB Typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:** 8.0 GHz Typical f_T
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

Description

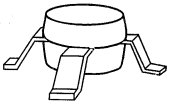
Hewlett-Packard's AT-42086 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-42086 is housed in a low cost surface mount .085" diameter plastic package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 20 emitter finger interdigitated geometry yields a medium sized transistor with impedances that are easy to match for low noise and medium power applications. Applications include use in wireless systems as an LNA, gain stage, buffer, oscillator, and mixer. An optimum noise match near 50 Ω up to 1 GHz, makes this device easy to use as a low noise amplifier.

The AT-42086 bipolar transistor is fabricated using Hewlett- Packard's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

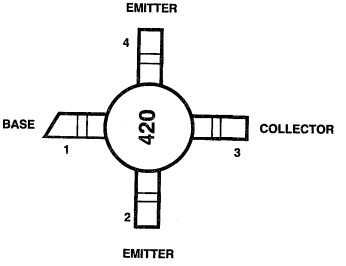
Note:

1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."

86 Plastic Package



Pin Connections



AT-42086 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	80
P_T	Power Dissipation[2,3]	mW	500
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2,4]:
θ_{jc} = 140°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.1 mW/°C for T_C > 80°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

Part Number	Increment	Comments
AT-42086-BLK	100	Bulk
AT-42086-TR1	1000	Reel

Note: For more information, see "Tape and Reel Packaging for Semiconductor Devices".

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; V_{CE} = 8 V, I_C = 35 mA	f = 1.0 GHz	dB	15.0	16.5	
		f = 2.0 GHz			10.5	
		f = 4.0 GHz			4.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression	f = 2.0 GHz	dBm		20.5	
	V_{CE} = 8 V, I_C = 35 mA	f= 4.0 GHz			20.0	
$G_{1\,dB}$	1 dB Compressed Gain; V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz	dB		13.5	
		f = 4.0 GHz			9.0	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dB		1.9	
		f = 4.0 GHz			3.5	
G_A	Gain @ NF_O; V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dB		13.0	
		f = 4.0 GHz			9.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; V_{CE} = 8 V, I_C = 35 mA		—	30	150	270
I_{CBO}	Collector Cutoff Current; V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current; V_{EB} = 1 V		μA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.32	

Note:
1. For this test, the emitter is grounded.

AT-42086 Typical Performance, T_A = 25°C

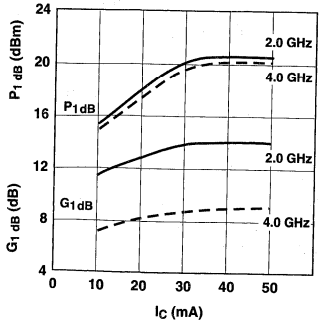


Figure 1. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

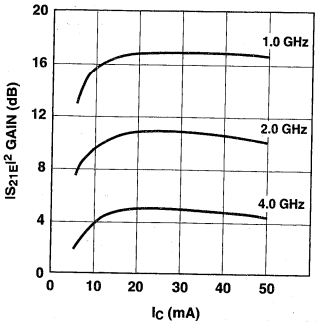


Figure 2. Insertion Power Gain vs. Collector Current and Frequency. V_{CE} = 8 V.

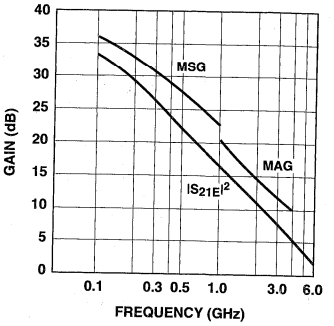


Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 8 V, I_C = 35 mA.

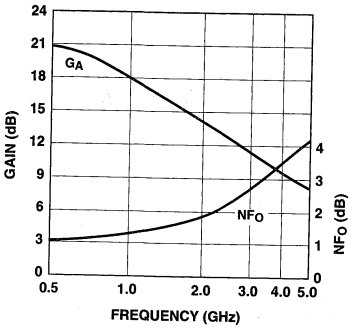


Figure 4. Noise Figure and Associated Gain vs. Frequency. V_{CE} = 8 V, I_C = 10 mA.

AT-42086 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.68	-48	28.0	25.12	153	-36.0	.016	65	.91	-15
0.5	.63	-141	20.9	11.07	102	-29.9	.032	42	.54	-30
1.0	.63	-176	15.4	5.87	80	-27.4	.043	43	.43	-30
1.5	.65	164	12.0	3.98	65	-26.0	.050	46	.40	-34
2.0	.66	151	9.5	2.99	53	-23.9	.064	52	.38	-40
2.5	.69	142	7.8	2.44	45	-23.1	.070	53	.36	-46
3.0	.71	132	6.2	2.04	34	-21.6	.084	54	.34	-54
3.5	.73	123	4.8	1.74	24	-19.7	.104	53	.33	-67
4.0	.75	115	3.6	1.51	14	-18.3	.122	51	.30	-80
4.5	.78	108	2.6	1.34	5	-17.2	.138	50	.31	-94
5.0	.80	101	1.6	1.20	-4	-16.0	.159	46	.31	-110
5.5	.82	95	0.6	1.08	-12	-14.8	.182	40	.32	-129
6.0	.85	89	-0.2	0.97	-21	-14.0	.200	35	.34	-148

AT-42086 Typical Scattering Parameters,

Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 8 V, I_C = 35 mA

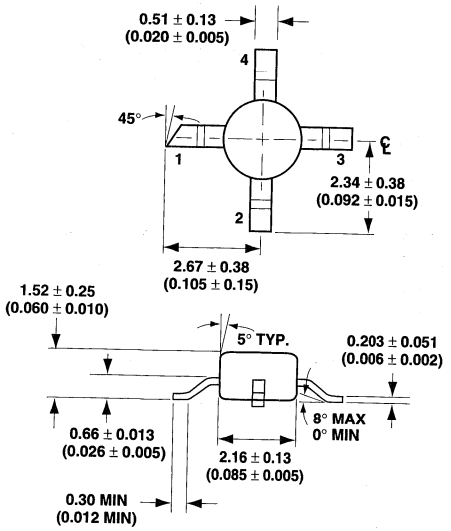
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.48	-94	32.8	43.62	137	-37.7	.013	65	.77	-25
0.5	.57	-168	22.4	13.21	92	-32.6	.023	57	.39	-28
1.0	.59	168	16.5	6.69	75	-28.7	.037	62	.33	-27
1.5	.61	154	13.0	4.48	62	-24.8	.057	64	.31	-31
2.0	.63	143	10.5	3.36	51	-23.0	.071	61	.29	-37
2.5	.68	137	8.7	2.72	43	-21.0	.089	56	.26	-45
3.0	.68	127	7.0	2.25	33	-19.7	.104	58	.25	-53
3.5	.71	118	5.7	1.92	24	-18.4	.121	55	.24	-65
4.0	.73	111	4.5	1.69	14	-17.3	.136	49	.20	-80
4.5	.76	104	3.5	1.49	5	-15.9	.161	46	.21	-95
5.0	.78	98	2.4	1.32	-3	-15.2	.174	43	.21	-115
5.5	.81	91	1.6	1.20	-12	-14.3	.193	36	.22	-136
6.0	.84	85	0.7	1.08	-20	-13.4	.213	31	.25	-156

A model for this device is available in the DEVICE MODELS section.

AT-42086 Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq.	NF_O	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.0	.04	8	0.13
0.5	1.1	.03	62	0.12
1.0	1.5	.06	168	0.12
2.0	1.9	.25	-146	0.12
4.0	3.5	.58	-100	0.52

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Up to 4 GHz Linear Power Silicon Bipolar Transistor

Technical Data

AT-64020

Features

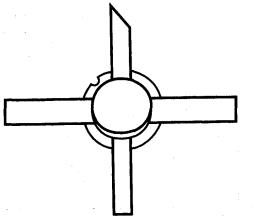
- **High Output Power:**
  27.5 dBm Typical $P_{1\,dB}$ at 2.0 GHz
  26.5 dBm Typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:**
  10.0 dB Typical $G_{1\,dB}$ at 2.0 GHz
  6.5 dB Typical $G_{1\,dB}$ at 4.0 GHz
- **35% Total Efficiency**
- **Emitter Ballast Resistors**
- **Hermetic, Metal/Beryllia Package**

Description

The AT-64020 is a high performance NPN silicon bipolar transistor housed in a hermetic BeO disk package for good thermal characteristics. This device is designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices. The use of ion-implanted ballast resistors ensures uniform current distribution through the multiple emitter fingers.

200 mil BeO Package



5965-8915E

AT-64020 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	2
V_{CBO}	Collector-Base Voltage	V	40
V_{CEO}	Collector-Emitter Voltage	V	20
I_C	Collector Current	mA	200
P_T	Power Dissipation[2,3]	W	3
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to 200

Thermal Resistance[2,4]:
$\theta_{jc} = 40°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 25 mW/°C for $T_C > 80°C$.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; $V_{CE} = 16$ V, $I_C = 110$ mA	f = 2.0 GHz f = 4.0 GHz	dB		7.0 2.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression $V_{CE} = 16$ V, $I_C = 110$ mA	f = 2.0 GHz f= 4.0 GHz	dBm	26.5	27.5 26.5	
$G_{1\,dB}$	1 dB Compressed Gain; $V_{CE} = 16$ V, $I_C = 110$ mA	f = 2.0 GHz f = 4.0 GHz	dB	8.5	10.0 6.5	
η_T	Total Efficiency at 1 dB Compression: $V_{CE} = 16$ V, $I_C = 110$ mA	f = 4.0 GHz	%		35.0	
h_{FE}	Forward Current Transfer Ratio; $V_{CE} = 8$ V, $I_C = 110$ mA		—	20	50	200
I_{CBO}	Collector Cutoff Current; $V_{CB} = 16$ V		μA			100
I_{EBO}	Emitter Cutoff Current; $V_{EB} = 1$ V		μA			5.0

Note:
1. $\eta_T = (\text{RF Output Power})/(\text{RF Input Power} + V_{CE}I_C)$.

AT-64020 Typical Performance, T_A = 25°C

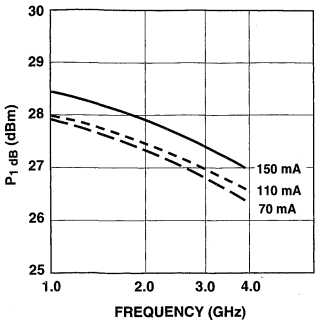


Figure 1. Power Output @ 1 dB Gain Compression vs. Frequency and Collector Current. V_{CE} = 16 V.

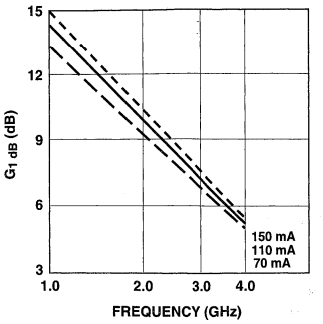


Figure 2. 1 dB Compressed Gain vs. Frequency and Collector Current. V_{CE} = 16 V.

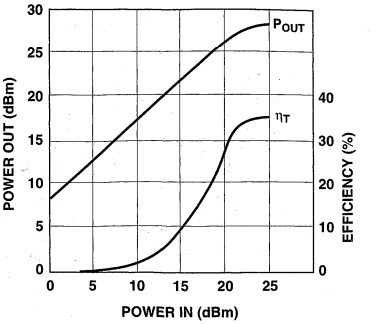


Figure 3. Output Power and Efficiency vs. Input Power. V_{CE} = 16 V, I_C = 110 mA, f = 4.0 GHz.

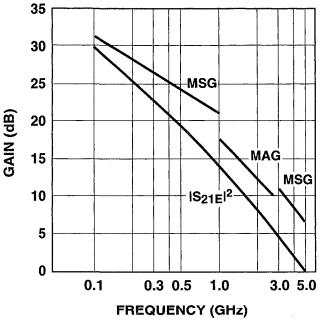


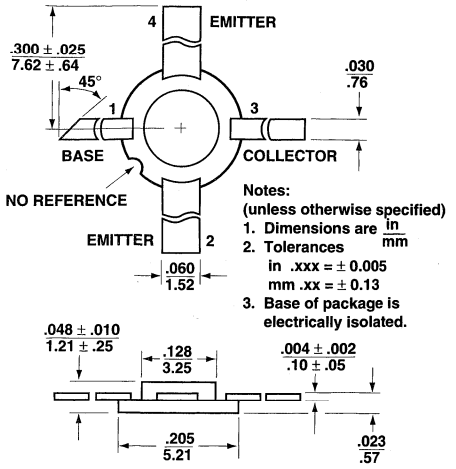
Figure 4. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 16 V, I_C = 110 mA.

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 16 V, I_C = 110 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.61	-116	30.0	31.51	130	-33.1	.022	57	.67	-48
0.5	.75	-173	18.4	8.27	86	-28.8	.036	41	.23	-88
1.0	.75	171	12.5	4.23	66	-27.4	.043	49	.20	-100
1.5	.74	159	9.2	2.90	50	-23.5	.067	48	.21	-110
2.0	.74	148	7.0	2.23	35	-21.6	.083	46	.25	-120
2.5	.73	141	5.2	1.82	26	-19.8	.103	47	.27	-127
3.0	.73	130	3.8	1.56	12	-17.5	.133	41	.32	-135
3.5	.74	119	2.7	1.37	-2	-16.1	.157	35	.35	-146
4.0	.73	107	1.8	1.23	-16	-14.7	.186	26	.38	-158
4.5	.72	93	0.9	1.11	-30	-13.3	.217	18	.41	-168
5.0	.71	79	0.1	1.01	-43	-11.8	.256	8	.42	179

A model for this device is available in the DEVICE MODELS section.

200 mil BeO Package Dimensions



HEWLETT® PACKARD

Up to 4 GHz Linear Power Silicon Bipolar Transistor

Technical Data

AT-64023

Features

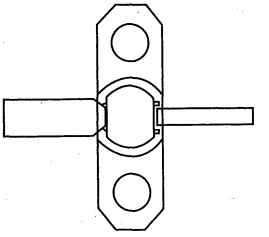
- **High Output Power:**
  27.5 dBm Typical $P_{1\,dB}$ at 2.0 GHz
  26.5 dBm Typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:**
  12.5 dB Typical $G_{1\,dB}$ at 2.0 GHz
  9.5 dB Typical $G_{1\,dB}$ at 4.0 GHz
- **35% Total Efficiency**
- **Emitter Ballast Resistors**
- **Hermetic, Metal/Beryllia Stripline Package**

Description

The AT-64023 is a high performance NPN silicon bipolar transistor housed in a hermetic BeO flange package for good thermal characteristics. This device is designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices. The use of ion-implanted ballast resistors ensures uniform current distribution through the multiple emitter fingers.

230 mil BeO Package



5965-8916E

AT-64023 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	2.2
V_{CBO}	Collector-Base Voltage	V	40
V_{CEO}	Collector-Emitter Voltage	V	20
I_C	Collector Current	mA	200
P_T	Power Dissipation[2,3]	W	3
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to 200

Thermal Resistance[2,4]:
$\theta_{jc} = 40°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 25 mW/°C for $T_C > 80°C$.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; $V_{CE} = 16$ V, $I_C = 110$ mA	f = 2.0 GHz f = 4.0 GHz	dB		6.5 2.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression $V_{CE} = 16$ V, $I_C = 110$ mA	f = 2.0 GHz f= 4.0 GHz	dBm	 25.5	27.5 26.5	
$G_{1\,dB}$	1 dB Compressed Gain; $V_{CE} = 16$ V, $I_C = 110$ mA	f = 2.0 GHz f = 4.0 GHz	dB	 7.0	12.5 9.5	
η_T	Total Efficiency[1] at 1 dB Compression: $V_{CE} = 16$ V, $I_C = 110$ mA	f = 4.0 GHz	%		35.0	
h_{FE}	Forward Current Transfer Ratio; $V_{CE} = 8$ V, $I_C = 110$ mA		—	20	50	200
I_{CBO}	Collector Cutoff Current; $V_{CB} = 16$ V		μA			100
I_{EBO}	Emitter Cutoff Current; $V_{EB} = 1$ V		μA			5.0

Note:
1. η_T = (RF Output Power)/(RF Input Power + $V_{CE}I_C$).

AT-64023 Typical Performance, T_A = 25°C

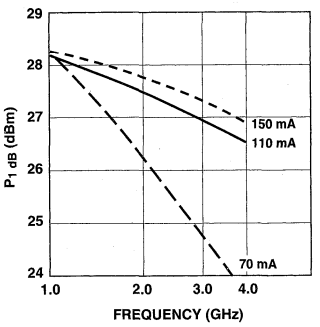


Figure 1. Power Output @ 1 dB Gain Compression vs. Frequency and Collector Current. V_{CE} = 16 V.

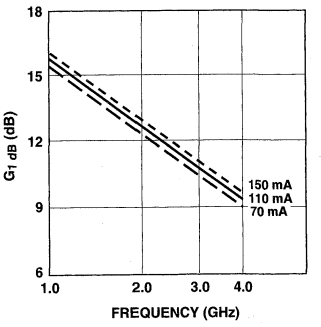


Figure 2. 1 dB Compressed Gain vs. Frequency and Collector Current. V_{CE} = 16 V.

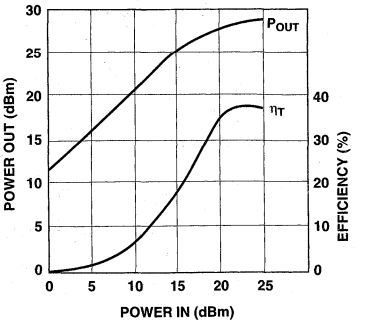


Figure 3. Output Power and Efficiency vs. Input Power. V_{CE} = 16 V, I_C = 110 mA, f = 4.0 GHz.

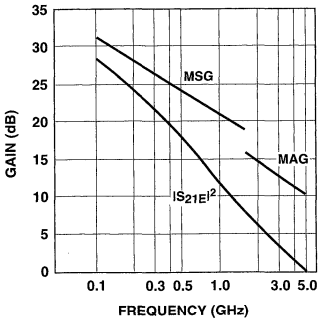


Figure 4. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{CE} = 16 V, I_C = 110 mA.

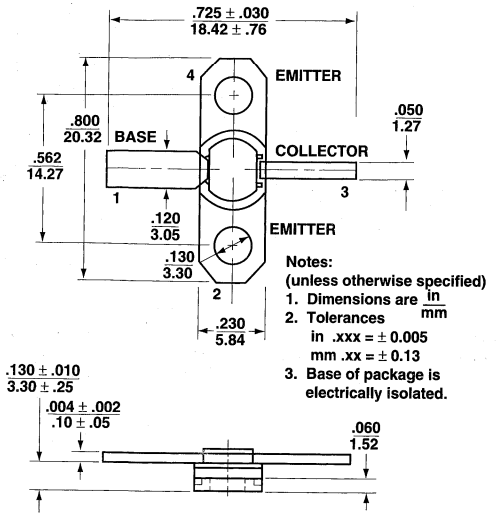
Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{CE} = 16 V, I_C = 110 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.54	-124	28.2	25.71	135	-33.3	.022	42	.72	-51
0.5	.80	-178	17.6	7.57	78	-29.5	.034	18	.33	-119
1.0	.80	162	11.9	3.92	47	-28.6	.037	10	.33	-142
1.5	.80	147	8.6	2.70	21	-27.9	.040	12	.40	-156
2.0	.78	133	6.3	2.07	-4	-27.6	.042	1	.48	-169
2.5	.77	127	5.1	1.80	-24	-25.5	.053	-5	.58	-178
3.0	.73	116	3.8	1.56	-51	-25.0	.056	-20	.67	170
3.5	.66	106	2.9	1.40	-79	-25.8	.051	-28	.78	156
4.0	.60	99	2.2	1.28	-109	-27.2	.044	-49	.86	142
4.5	.55	98	1.4	1.18	-141	-31.2	.028	-70	.93	127
5.0	.54	99	0.6	1.07	-175	-40.9	.009	-144	.93	112

A model for this device is available in the DEVICE MODELS section.

S-parameters at other bias conditions are available on the Hewlett-Packard Design Pak disk.

230 mil BeO Package Dimensions



HEWLETT® PACKARD

NPN Silicon Bipolar Transistor

Reliability Data

AT-3XXXX Series

Description

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-883. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Hewlett-Packard Communications Components Designer's Catalog.

1. Life Test

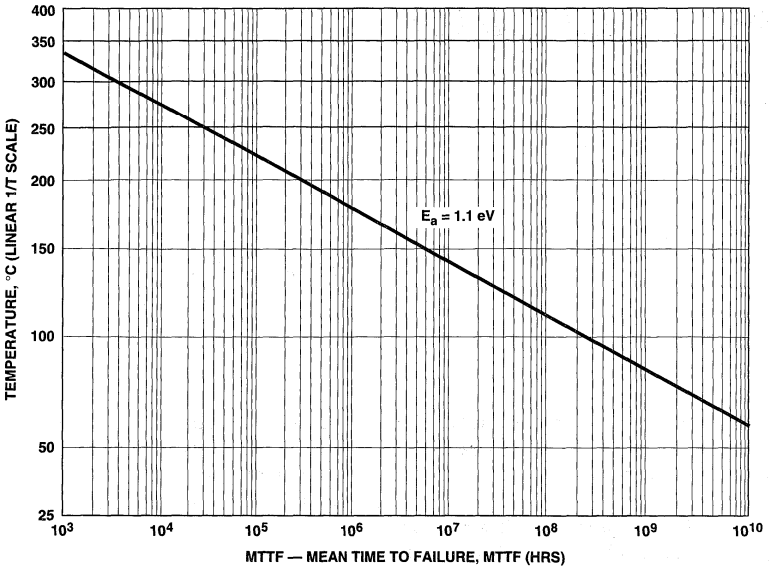
A. Demonstrated Performance

Test Name	Test Condition	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temperature Operating Life (HTOL)	$T_j = 150°C$	140	140,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1 eV, and is listed in the following table.

Junction Temp. T_j (°C)	Point[1]		90% Confidence Level[2]	
	MTTF* (Hours)	MTTF FIT[3]	MTTF (Hours)	FIT[3]
175	1.3×10^5	7692	5.65×10^4	17692
150	6.94×10^5	1440	3.02×10^5	3314
125	4.57×10^6	218.8	1.68×10^7	503.3
100	3.87×10^7	25.8	1.99×10^6	59.4
55	4.13×10^9	0.242	1.79×10^9	0.56



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

(25.8 x 10^{-9}) x (25%) x (8760 hrs/yr) = 5.65 x 10^{-3}% per year

Likewise, the 90% confidence level failure rate per year is:

(59.4 x 10^{-9}/hrs.) x (25%) x (8760 hrs/yr) = 1.3 x 10^{-2}% per year

2. Environmental Tests

Test Name	MIL-STD-750 Reference	Test Conditions	Units Tested	Units Failed
Thermal Shock	1056	-65°C to 150°C, 5 min. dwell 200 cycles	154	0
Temperature Cycle	1051	-65°C to 150°C, 10 min. dwell 200 cycles	152	0
HTRB	HPGSS-12-107	VCB = 16 V, 121°C, 1,000 hours	154	0
Autoclave	HPGSS 12-109	121°C, 15 PSIG, 96 hours	148	0

3. Flammability Test (MIL-STD-202, Method 111):

Meets Needle Flame test per UL Category D (Flaming Time <3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD Classification:

AT-3XX11/3XX33 Class 1

HEWLETT® PACKARD

NPN Silicon Bipolar Transistor

Reliability Data

AT-41511
AT-41533

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-883. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

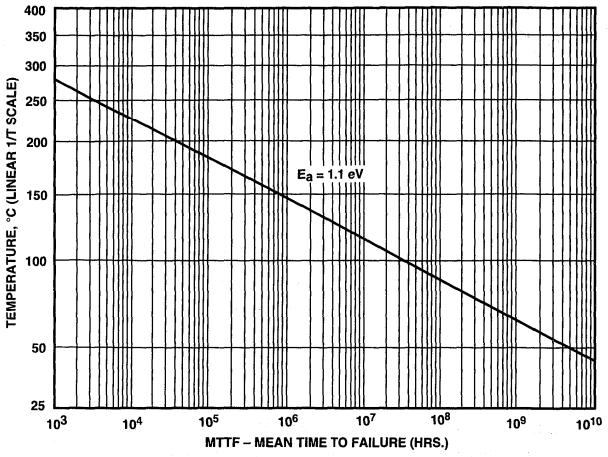
Test Name	Test Condition	Units Tested	Total Device Hrs.	Total Failed	Failure Rate (%/1K Hours)
High Temperature Operating Life (O.L.)	T_j = 150°C	77	77,000	0	0
HTRB	T_A = 121°C V_{CB} = 16 V	76	76,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1eV, and the device thermal resistance on stress board of 130°C/W, and is listed in the following table.

Junction Temp. T_j (°C)	Point(1)		90% Confidence Level(2)	
	MTTF* (hours)	FIT(3)	MTTF (hours)	FIT(3)
175	1.3×10^5	7692	5.65×10^4	17692
150	6.94×10^5	1440	3.02×10^5	3314
125	4.57×10^6	218.8	1.68×10^7	503.3
100	3.87×10^7	25.8	1.99×10^6	59.4
55	4.13×10^9	0.242	1.79×10^9	0.56

*MTTF data calculated from high temperature Operating Life tests.



Notes:
1. The point MTTF is simply the total device hours divided by the number of failures.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF)

C. Example of Failure Rate Calculation:

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day × 5 days/wk) ÷ 168 hrs/wk ≅ 25%

Then the point failure rate per year is:

$(25.8 \times 10^{-9}) \times (25\%) \times (8760 \text{ hrs/yr}) = 5.65 \times 10^{-3}$ % per year

Likewise, the 90% confidence level failure rate per year is:

$(59.4 \times 10^{-9}) \times (25\%) \times (8760 \text{ hrs/yr}) = 1.3 \times 10^{-2}$ % per year

2. Environmental and Mechanical Tests

Test Name	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Thermal Shock	1056	-65°C to 150°C, 5 min. dwell, 200 cycles	77	0
Temperature Cycle	1051	-65°C to 150°C, 10 min. dwell, 200 cycles	77	0
AutoClave	HP GSS 12-109	121°C, 15 PSIG, 96 hrs	76	0

3. Flammability Test

(MIL-STD-202, Method 111):

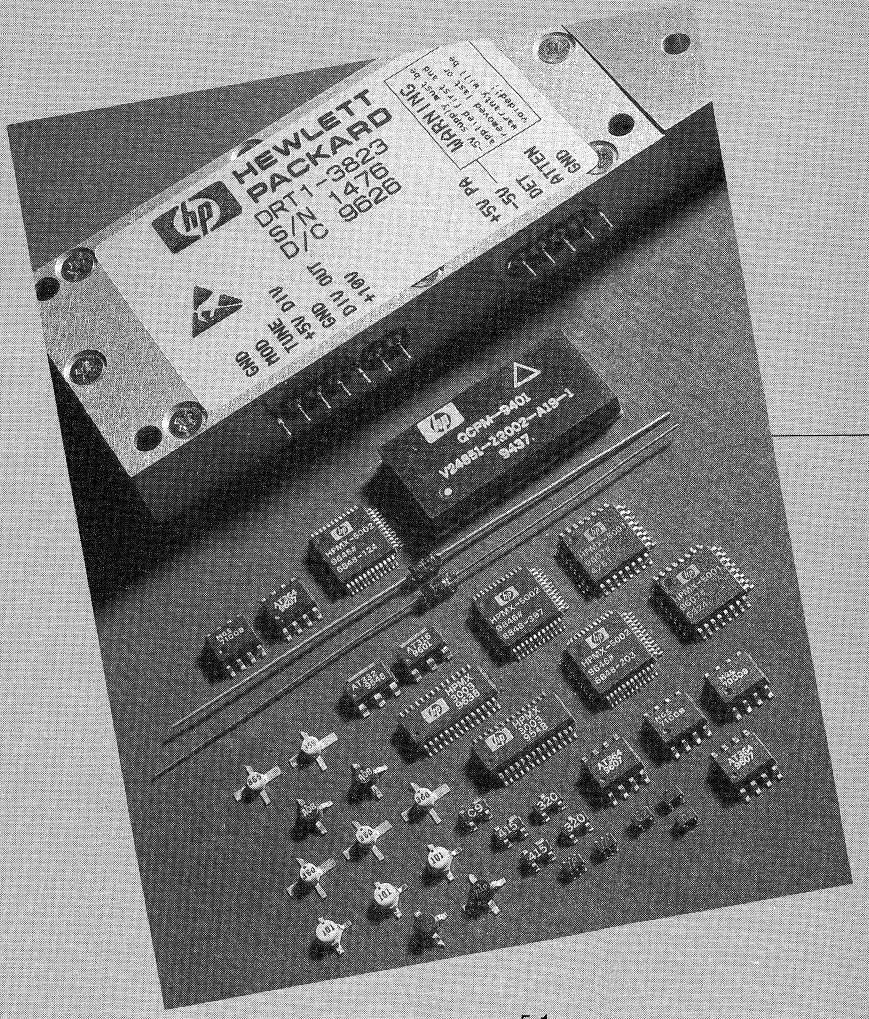
Meets Needle Flame test per UL Category D (Flaming Time <3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD Classification:

AT-41511/41533 Class I

HEWLETT® PACKARD

Gallium Arsenide Field Effect Transistors (GaAs FETs)



Gallium Arsenide Field Effect Transistors

Characteristics

The Gallium Arsenide field effect transistor is a semiconductor device with amplification due to voltage gain. The advantages GaAs FETs have over other transistor types stem from the intrinsic high mobility of electrons in gallium arsenide. This high mobility translates into semiconductors with superior high performance characteristics in the microwave region, including high f_T, high f_{MAX}, and very low noise figure.

GaAs FETs find wide applications as the semiconductor device of choice at frequencies above 4 GHz (where the gain of most microwave silicon processes is diminishing) both as amplifiers and oscillators, or as low noise amplifiers in applications demanding optimum noise performance.

The performance of a GaAs FET is determined primarily by the gate width and length. The gate length is the short dimension of the gate and sets the "high frequenc" aspects of performance. In general, shorter gate lengths result in superior performance (although the gate must have aufficient thickness to support the current density necessary for reliability). The gate length is a primary feature of the process used. The gate width determines the active periphery, and sets the transconductance (g_m) and saturated drain current (I_{DSS}) of the FET. In addition to establishing the power producing capability, the gate width also sets the sparameters of the device, and therefore the optimum frequency of operation. In general, shorter widths work better at high frequencies. The gate width is set by the geometry or mask design. It is fairly common for the same mask type to be used with different processes to create FETs with the same gate width but different performance characteristics.

GaAs FET Product Families

Hewlett-Packard manufactures FETs using a series of processes tailored for the end application. Part numbers for these devices begin with alpha characters "ATF". The first digit of the part number delineates process. The second digit defines the geometry. The third digit represents an assembly sort, e.g. for noise figure. The final two digits indicate the package type.

ATF-lx series

The ATF-lx process is optimized for low noise figure. This process uses vapor phase epi and a nominal 0.25 micron gate length to produce MESFETs with superior noise figures for LNA applications such as TVRO or GPS receivers, and all kinds of communications receivers. This process also results in devices with phase noise approximately 10 dB lower than that produced by the gain (ATF-2x) process. The nominal figures of merit for this process are an f_T of 40 GHz and and f_{MAX} of 100 GHz.

Two geometries are available:

- ATF-l0xxx: 500 micron gate width device optimum for 2-8 GHz applications
- ATF-13xxx: 250 micron gate width device optimum for 4-16 GHz applications

ATF-2x series

The ATF-2x process is optimized for gain. This process uses ion implantation and a nominal 0.25 micron gate length to produce MESFETs with good gain and power. Typical uses include gain stages and medium power oscillator applications. The robust gate used results in a device with

superior longevity. The nominal figures of merit for this process are an f_T of 40 GHz and and f_{MAX} of 100 GHz.

Three geometries are available:

- ATF-21xxx: 750 micron gate width device optimum for 1-6 GHz applications
- ATF-25xx: 500 micron gate width device optimum for 2-8 GHz applications
- ATF-26xxx: 250 micron gate width device optimum for 4-16 GHz applications

ATF-3x series

The ATF-3x process is Hewlett-Packard's high performance Pseudomorphic High Electron Mobility Transistor (PHEMT) process. This process uses MBE material to create a GaAs – AlGaAs – InAlGaAs structure that results in superior mobility to standard MESFET or HEMT devices. This process is optimized to give the lowest noise figure for critical receiver applications such as DBS block converters. The nominal figures of merit for this process are an f_T of 60 GHz and an f_{MAX} of 150 GHz.

The geometry available is:

- ATF-36xxx: 200 micron gate width device optimum for 2-18 GHz applications

ATF-4x series

The ATF-4x process is optimized for power. This process uses a double recessed 0.5 micron gate length to produce MESFETs with high breakdowns, and superior power producing capability. Typical uses include driver and power amplifiers up to several watts. The nominal figures of merit or this process are an f_T of 20 GHz and an f_{MAX} of 50 GHz.

Three geometries are available:

- ATF-44xxx: 5000 micron gate width device for 2-8 GHz applications
- ATF-45xxx: 2500 micron gate width device for 2-8 GHz applications
- ATF-46xxx: 1250 micron gate width device for 2-10 GHz applications

Application Information

The following application information is either published in this catalog or available from your local Hewlett-Packard sales office, authorized distributor, or representative.

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Application Notes

Abstracts

HEWLETT® PACKARD

Using the ATF-10236 in Low Noise Amplifier Applications in the UHF through 1.7 GHz Frequency Range

Application Note 1076

Introduction

GaAs FET devices are typically used in low-noise amplifiers in the microwave frequency region where silicon transistors can't provide the required gain and noise performance. There are, however, many applications in the frequency range below 2 GHz where the low noise figures and high gain of GaAs FETs can improve receiver sensitivity. Typical applications include low noise amplifiers (LNAs) in the 800 to 900 MHz frequency range for use in celluar telephone and pager applications and spread spectrum transceiver applications. Additional applications include the 1228 and 1575 MHz frequencies used for Global Positioning System (GPS) applications. Other applications include VHF mobile radio, IMMARSAT, and WEFAX, just to name a few.

This application note describes two low-noise amplifiers that use the Hewlett-Packard ATF-10236 low noise GaAs FET device. Both designs use identical circuit topology with the only differences being in the proper choice of three inductors depending on the frequency of operation. The designs are centered at 900 MHz and 1575 MHz, but can be scaled for any frequency within the region of 400 to 1700 MHz. Each amplifier has a usable bandwidth of about 30 to 40 percent.

Using a high-gain, high-frequency GaAs FET at VHF poses special problems. Of greatest concern is the problem of designing the amplifier for unconditional stability. Typically, GaAs FETs have greater gain as frequency is decreased, e.g., 25 dB maximum stable gain at 500 MHz. A second problem is that matching the typical microwave GaAs FET at lower frequencies for minimum noise figure does not necessarily produce minimum input VSWR.

Achieving the lowest possible noise figure requires matching the device to Γ_{opt} (the source match required for minimum noise figure). At higher microwave frequencies this will generally produce a reasonable input VSWR, since Γ_{opt} and the complex conjugate of the device input reflection coefficient S_{11} are usually close on the Smith Chart. At lower frequencies, special consideration needs to be given to the input circuit design and to the tradeoffs required to ensure low noise figure while still achieving moderate gain, low VSWR and unconditional stability.

Device Family

This application note will discuss the use of the ATF-10236 series of low noise GaAs FET devices. The device has a 500 micron gate periphery and is most suitable for applications in the VHF through 4 GHz frequency range. The device is tested for noise figure and gain at 4 GHz where it is typically used in satellite TVRO applications. The ATF-10136 is the premium device being specified at 0.6 dB maximum noise figure while the ATF-10236 is specified at a 1.0 dB maximum and the ATF-10736 is specified at a 1.4 dB maximum all at 4 GHz. Typically a three stage device lineup is used at C band with the ATF-10136 device being used as the first stage followed by the ATF-10236 followed by the ATF-10736. The higher noise figure of the second and third stages has minimal effect on the over all cascade noise figure. A three stage low-noise amplifier with greater than 30 dB of gain is

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generally required at C band to overcome filter/mixer losses.

While there is considerable difference in noise figure at 4 GHz between the three devices (i.e. 0.8 dB), the difference in the 1 to 2 GHz frequency range is less than several tenths of a dB. In actual circuits built on low cost FR-4 dielectric material, the ATF-10236 device is capable of a 0.5 dB noise figure at 900 MHz and a 0.75 dB noise figure at 1575 MHz. Most commercial applications at frequencies below 2 GHz generally do not require the high gain of a three stage cascade so generally a single stage LNA is used followed by a bipolar device or a silicon MMIC. Cascading the ATF-10236 with a 3.5 dB noise figure MMIC such as the MSA-0686, will still result in about a 1 dB noise figure LNA with 25 to 30 dB gain.

The Hewlett-Packard ATF-10236 is supplied in the low cost commercial 0.100 inch "micro-X" metal/ceramic package. Examination of the data sheet reveals that the device is capable of a 0.6 dB noise figure at frequencies below 2 GHz with an associated gain of greater than 16 dB. The noise parameters and S-parameters of this transistor are summarized in Table 1.

Design Technique

Obtaining the lowest possible noise figure from the device requires that the input matching network convert the nominal 50 Ω source impedance to Γ_{opt}. This produces a deliberate impedance mismatch that, while minimizing amplifier noise figure, produces a high input VSWR. The ideal situation is where Γ_{opt} is the complex conjugate of S_{11} (i.e., S_{11}*). For this condition, minimum noise figure is achieved when the device is matched for minimum VSWR. This situation occurs predominantly above 2 GHz and tends to diverge at lower frequencies, where S_{11} approaches 1.

High input VSWR has varying significance, depending on the application. Most noteworthy is the increased uncertainty of the noise figure measurement due to reflections between the noise source and amplifier input. Having a noise source with a very low output VSWR and one whose VSWR has minimal change between the "on" and "off" states will minimize this uncertainty. One such noise source is the Hewlett-Packard HP346A with a nominal 5 dB Excess Noise Ratio (ENR). Similarly, when the amplifier is connected to a receive antenna, high input VSWR creates added uncertainty in overall system performance. The effect is difficult to analyze unless an isolator is placed at the input to the amplifier. The use of an isolator, however, adds excessive loss and, at VHF frequencies, the size of the isolator is often prohibitively large.

To examine the alternatives, constant noise figure and constant gain circles can be constructed to assess the impact of trading increased noise figure for a decrease in input VSWR and a corresponding increase in amplifier gain. In most instances, the result is a much higher noise figure than really desired. One option is to use source feedback. This subject has already been covered by several authors (References 1-3). Source feedback, in the form of source inductance, can improve input VSWR with minimal noise figure degradation. The drawback of utilizing source inductance is a gain reduction of up to several decibels. However, GaAs FET devices often have more gain than desired at low frequencies, so the penalty is not severe.

The effect of source inductance on amplifier input match is best studied with the help of a computer simulation. The microwave design simulation program from Hewlett-Packard EEsof called Touchstone™ is used to analyze S_{11} of the amplifier with the proposed output matching network. S_{11} was measured looking directly into the gate of the device with the source inductance added between the source and ground. With the ATF-10236 at 500 MHz, adding the equivalent source inductance of two 0.10 inch leads causes the value of S_{11} to decrease from 0.970 to 0.960. Angle remains relatively constant at about -20 degrees. Γ_{opt} remains relatively unchanged with the addition of source inductance. Comparing S_{11} to Γ_{opt} at 500 MHz now shows them to be nearly identical. The result is that minimum noise figure and minimum VSWR will coincide more closely with one another when matching the device for minimum noise figure. Plotting Γ_{opt} for the ATF-10236 device from 450 MHz through 2 GHz in Figure 1 shows that Γ_{opt} lies very near the $R/Z_0=1$ curve. This implies that a series inductance will provide the necessary match to attain minimum noise figure.

The simplest way to incorporate source inductance is to use the device source leads. Using device leads as inductors produces

Table 1. Scattering and Noise Parameters for the Hewlett-Packard ATF-10236 GaAs FET, Vds = 2 volts and Ids = 25 mA
Scattering Parameters: Common Source, Zo = 50 Ω

Freq	S11		S21			S21			S22	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.97	-20	15.1	5.68	162	-32.8	.023	76	.47	-11
1.0	.93	-41	14.9	5.58	143	-26.0	.050	71	.45	-23
2.0	.77	-81	13.6	4.76	107	-21.3	.086	51	.36	-38

Noise Parameters

Frequency GHz	Noise Figure dB	Gamma Mag	Optimum Ang	Rn/50 normalized
0.5	0.45	0.93	18	0.75
1.0	0.5	0.87	36	0.63
2.0	0.6	0.73	74	0.33

approximately 1.3 nH per 0.100 inch of source lead, or 0.65 nH for two source leads in parallel. With the help of Touchstone™, the effect of the lead inductance can be analyzed by simulating the inductance as a high-impedance transmission line. The TUNE mode is invaluable for determining the optimum lead length for a given performance. Table 2 shows the effect of lead length on gain, noise figure, stability, and input and output VSWR at 900 MHz. It is clear that lead lengths of 0.06 inch or less have a minor effect on noise figure while improving input match substantially. Gain does suffer, but this is not a major concern.

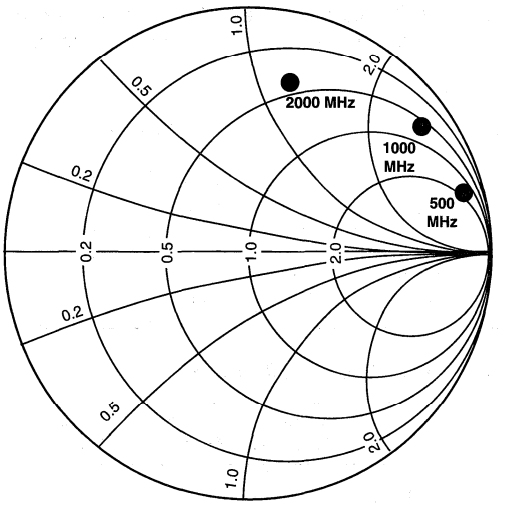


Figure 1. ATF-10236 Γ_o vs. Frequency at V_{ds} = 2 volts and I_{ds} = 25 mA.

An added benefit of using source inductance is enhanced stability as evidence by the Rollett stability factor, k. Excessive source inductance can have an adverse effect on stability at the higher frequencies. In the case of the 900 MHz amplifier, zero length source leads create potential instability at low frequencies while longer source lead length creates potential instability at high frequencies, i.e. 6.6 GHz. It is determined that 0.060 inch source lead length is an optimum choice based on all parameters. The optimum source lead length varies with frequency of operation. At 1575 MHz, 0.020 inch source lead length provides

optimum performance with unconditional stability up to 12 GHz. Decreasing source lead length improves stability at 12 GHz while making k<1 at 400 MHz. Adding series resistance in the output matching circuit increases stability over a wide frequency range. The effect of adding a series resistor R10 on amplifier performance is also shown in Table 2.

Achieving the associated gain of which the device is capable is difficult since the device is not inherently stable. It is not enough that the amplifier be stable at the operating frequency – it must be stable at all frequencies. Any out-of-band oscillation will make the amplifier unusable.

The simplest technique to ensure broad-band stability is to resistively load the drain. Resistive loading produces a constant impedance on the device over a wide frequency range. In the case of the ATF-10236, a 50 Ω resistor and a small amount of series inductance is used to load the output of the device. The series inductance provides some impedance matching. This produces acceptable gain while ensuring a good output match and retaining stability over as wide a bandwidth as possible.

The amplifier circuit is shown in Figure 2. For simplicity, the original LNA used the self- biasing technique to set the bias point. The loss in noise figure associated with the bypassed source resistor topology is no greater than 0.1 dB at these frequencies. The 33 Ω resistor between the source and ground sets the drain current while the 100 Ω resistor sets the drain voltage. There is some interaction, however, between the two resistors. The supply voltage is regulated by the TL05 5 volt regulator U2. The disadvantage of the self biasing technique is that variations in Pinchoff Voltage (V_p) and Saturated Drain Current (I_{dss}) that may occur from one production run to another may dictate the need to change the value of the source resistor. The calculation to determine the source resistor R_S is as follows.

$$R_S = \frac{[\, V_p \ (1 - \sqrt{I_d / I_{dss}}\,) \,]}{I_d}$$

Assuming typical device parameters of:

I_{dss} = 130 mA
V_p = -1.3 volts
I_d = 25 mA

yields: R_S = 29.2 ohms

This agrees favorably with the 33 Ω resistor used in the actual amplifier.

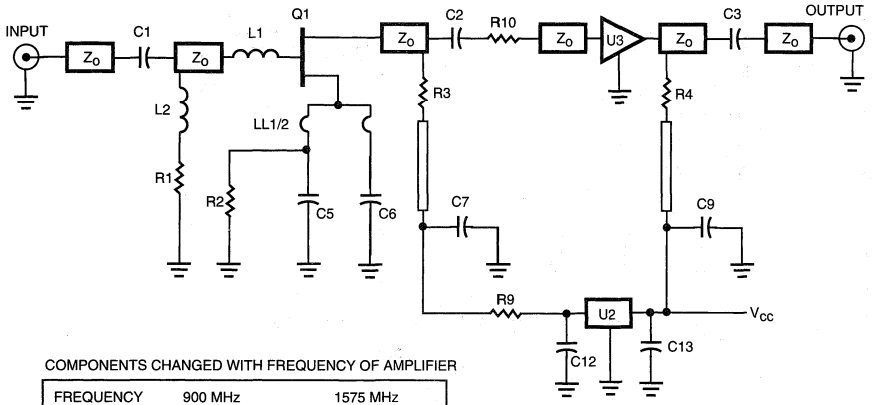
The preferred alternative in a production environment is the use of an active bias network as described in Figure 3. Although active biasing does add cost by requiring extra components, including a way of generating a

Table 2. Simulated 900 MHz amplifier performance vs. source lead length , R10 = 0 Ω.

Lead Length LL1	Noise Figure	Gain	$\|S_{11}\|^2$	$\|S_{22}\|^2$	K at 900 MHz	K at 6.6 GHz	K at 10 GHz
0 inch	0.54 dB	20.1 dB	-4.9 dB	-8.8 dB	0.58	2.94	1.65
0.06 inch	0.56 dB	18.0 dB	-12.2 dB	-12.7dB	1.011	2.39	1.09
0.2 inch	0.62 dB	14.4 dB	-12.7 dB	-18.0 dB	1.57	0.35	1.47

Simulated 900 MHz amplifier performance vs. source lead length , R10 = 16 Ω.

Lead Length LL1	Noise Figure	Gain	$\|S_{11}\|^2$	$\|S_{22}\|^2$	K at 900 MHz	K at 6.6 GHz	K at 7.5 GHz	K at 10 GHz
0 inch	0.56 dB	18.7 dB	-4.6 dB	-12.0 dB	0.66	4.05	3.05	2.15
0.06 inch	0.58 dB	16.6 dB	-11.7 dB	-13.6 dB	1.22	3.36	2.50	1.15
0.2 inch	0.65 dB	13.2 dB	-14.7 dB	-13.3 dB	1.96	0.35	-0.14	1.98



COMPONENTS CHANGED WITH FREQUENCY OF AMPLIFIER

FREQUENCY	900 MHz	1575 MHz
RFC1	0.33 µH	0.18 µH
L1	5T #26 0.075" ID CLOSEWOUND	2T #28 0.050" ID CLOSEWOUND
LL1/LL2	0.060"	0.020"

COMPONENTS COMMON TO ALL AMPLIFIERS:

C1, C2, C3 = 100 pF CHIP CAPACITOR
C5, C6, C7, C9 = 1000 pF CHIP CAPACITOR
C12, C13 = 0.1 µF CAPACITOR
Q1 = HEWLETT-PACKARD ATF-10236 GaAs FET
R1 = 100 Ω CHIP RESISTOR
R2 = 27 Ω CHIP RESISTOR
R3, R9 = 50 Ω CHIP RESISTOR
R4 = ADJUST FOR DESIRED MMIC CURRENT
R10 = 5 TO 25 Ω CHIP RESISTOR USED TO IMPROVE STABILITY AND OUTPUT RETURN LOSS (SEE TEXT)
U2 = 5 VOLT REGULATOR, TOKO TK11650U
U3 = HEWLETT-PACKARD MSA-SERIES MMIC PROVIDES ADDITIONAL GAIN - OPTIONAL
Z_O = 50 Ω MICROSTRIPLINE

Figure 2. Schematic of the GaAs FET amplifier using passive biassing. The only change required to modify the frequency operation is the proper choice of RFC1, L1, and LL1/LL2.

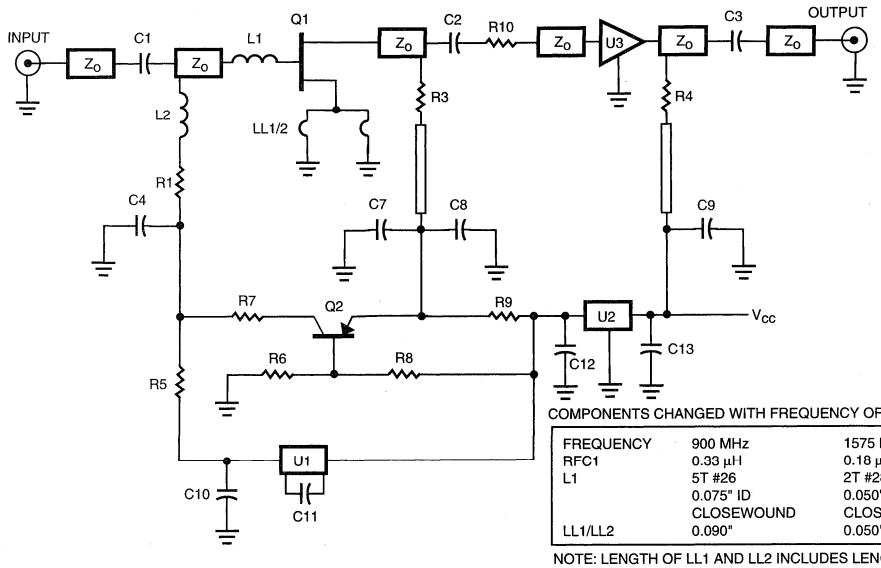
negative voltage, the advantages generally outweigh the disadvantages. Active biasing offers the advantage that variations in V_P and I_{dss} won't necessitate a change in either the source or drain resistor value for a given bias condition. The active bias network automatically sets V_{gs} for the desired drain voltage and drain current.

The active biasing scheme for FETs requires that the source leads be grounded and an additional supply be used to generate the negative voltage required at the gate for typical operation. Direct grounding the FET source leads has the additional advantage of not requiring bypass capacitors to bypass a source resistor that would typically be used for self biasing in a single supply circuit. When the source bypass capacitors are removed , the source lead length must be increased as suggested in Figure 3 to offset the decrease in series inductance. When active biasing is used, the cold end of the 100 ohm resistor, R1, in the gate network must be bypassed to ground with a 1000 pF capacitor instead of being dc grounded. This allows gate voltage to be applied.

Referring to Figure 3, resistors R6 and R8 provide a regulated voltage at the base of Q2. The voltage is increased by 0.7 volts by virtue of the emitter-base junction of Q2 and then applied to the drain of Q1 through resistor R3. Since R3 is included in the RF matching circuit, the voltage drop across R3 must be taken into account when designing the bias circuitry. Resistor R9 is connected between two regulated voltage points and therefore sets the drain current. Q1 gate is connected to a voltage divider consisting of R5 and R7 connected between the collector of Q2 and a negative voltage converter. The gate voltage can then assume a value necessary to sustain the desired drain voltage and current as predetermined by R6, R8, and R9.

Measurements On Amplifiers

The actual measured performance of the amplifiers compares favorably to that predicted by the computer simulation. Table 3 summarizes the gain, noise figure



COMPONENTS CHANGED WITH FREQUENCY OF AMPLIFIER

FREQUENCY	900 MHz	1575 MHz
RFC1	0.33 µH	0.18 µH
L1	5T #26 0.075" ID CLOSEWOUND	2T #28 0.050" ID CLOSEWOUND
LL1/LL2	0.090"	0.050"

NOTE: LENGTH OF LL1 AND LL2 INCLUDES LENGTH OF COPPER STRAP USED TO REPLACE C5 AND C6.

COMPONENTS COMMON TO ALL AMPLIFIERS:
C1, C2, C3 = 100 pF CHIP CAPACITOR
C4, C7, C9 = 1000 pF CHIP CAPACITOR
C5, C6, = NOT REQUIRED, REPLACE WITH COPPER STRAP
C8, C12, C13 = 0.1 µF CHIP CAPACITOR
C10, C11 = 10 µF CHIP CAPACITOR
Q1 = HEWLETT-PACKARD ATF-10236 GaAs FET
Q2 = SIEMENS SMBT 2907A PNP TRANSISTOR
R1 = 100 Ω CHIP RESISTOR
R2 = NOT REQUIRED
R3 = 50 Ω CHIP RESISTOR
R4 = ADJUST FOR DESIRED MMIC CURRENT
R5, R7 = 10K Ω CHIP RESISTOR
R6 = 1.1K Ω CHIP RESISTOR
R8 = 1K Ω CHIP RESISTOR
R9 = 70 Ω CHIP RESISTOR
R10 = 5 TO 25 Ω CHIP RESISTOR USED TO IMPROVE STABILITY AND OUTPUT RETURN LOSS (SEE TEXT)
U1 = LINEAR TECHNOLOGY LTC1044CS8 VOLTAGE CONVERTER
U2 = 5 VOLT REGULATOR, TOKO TK11650U
U3 = HEWLETT-PACKARD MSA-SERIES MMIC PROVIDES ADDITIONAL GAIN - OPTIONAL
Z_O = 50 Ω MICROSTRIPLINE

Figure 3. Schematic of the GaAs FET amplifier using passive biasing. The only change required to modify the frequency operation is the proper choice of RFC1, L1, and LL1/LL2.

and VSWR parameters. The noise figure of the 900 MHz amplifier is actually a little lower than the simulation would predict while the gain is very comparable. The input return loss measured 5.6 dB versus 12.2 dB according to the simulation. The difference between measured and simulated may be due to the loss of the RF choke in the input circuit. The input VSWR could be improved by increasing source inductance while paying careful attention to stability. The last alternative is to sacrifice some noise figure for a better input match. Output return loss measured 13.2 dB which compares favorably to the 12.7 dB predicted by the computer simulation.

The noise figure of the 1575 MHz amplifier was measured at 0.73 dB which is higher than the 0.45 dB as predicted. This can be explained by the dielectric board losses of the FR-4. The loss of the FR-4 accounts for 0.3 dB of loss at 1575 MHz. This was verified by cutting off the input section of the board , attaching two SMA connectors and carefully measuring the loss. Measured gain with the output series resistor R10 measured 12.5 dB which is within 1.3 dB of the computer simulation. Gain increases to 14.3 dB without R10. Input return loss measured 6.7 dB while the output return loss measured 15 dB which is fairly close to the computer simulation. Stability is very good with no problems noted when cascading stages.

The swept gain plots (included in Figures 4-5) show the wide bandwidth of these amplifiers. Low noise figure is also retained over the bandwidth. The 900 MHz

Table 3. Measured amplifier performance vs. computer simulation (* indicates R10 = 16 Ω, ** indicates R10 = 0 Ω)

Frequency		Noise Figure	Gain	$\|S_{11}\|^2$	$\|S_{22}\|^2$
900 MHz	measured	0.46 dB	16.7 dB	-5.6 dB	-13.2 dB
	simulated	0.56 dB	18.0 dB	-12.2 dB	-12.7 dB
1575 MHz	measured	0.73 dB	12.5 dB * 14.3 dB **	-6.7 dB	-15.0 dB
	simulated	0.85 dB	13.8 dB	-8.3 dB	-12.2 dB

amplifier has a maximum of 0.5 dB noise figure between 800 and 1000 MHz. Similarly, the 1575 MHz amplifier has less than a 1 dB noise figure from 1200 MHz to 1700 MHz.

At frequencies above 2 GHz, the ATF-10236 is rated for minimum noise figure when operated at Vds of 2 V, and Id of 25 mA. At frequencies below 2 GHz, it was empirically determined that an additional 0.1 dB reduction in noise figure is possible if the device is rebiased. At 900 MHz, 1 V gave the lowest noise figure while 1.5 volts is optimum for 1575 MHz.

Using The Design At Other Frequencies

The basic amplifier design can be adapted for any frequency in the 400 to 1600 MHz range. Scaling the input inductor (L1) will allow operation on a different frequency. The graph shown in Figure 6 gives some idea of the relationship of L1 vs. frequency. Source feedback should be adjusted accordingly. The ATF-10236 has been used successfully in circuits operating at as low as 150 MHz with similar results.

GaAs FET Demonstration Board

A demonstration board built on 0.031 inch FR-4/G-10 is shown in Figures 7 and 8. The board as shown can be set up with either passive or active biasing. If desired an additional gain stage in the form of a silicon MMIC such as the Hewlett-Packard MSA series can be used for additional gain at a slight increase in overall cascade noise figure. A later improved version of the artwork has the locations of R1 and L2 reversed. The mounting pad for R1 and L2 has an adverse effect on noise figure. It is therefore better to have the RF choke first then followed by the resistor since the impedance of the choke is higher than that of the resistor.

An additional resistor R10 can be added in series with capacitor C2 in order to improve stability and output return loss of the first stage. As an example, the use of a 16 Ω resistor at R10 will decrease gain by about 1 dB while improving output match and stability. It may also help when cascading the FET stage with the MMIC or another device.

The measured loss of the input microstripline excluding the blocking capacitor C1 is 0.3 dB at 1600 MHz and 0.15 dB at 900 MHz. Keep this loss in mind when evaluating the devices as most computer simulations appear to be optimistic about dielectric board losses and therefore give an optimistic (lower) prediction of noise figure.

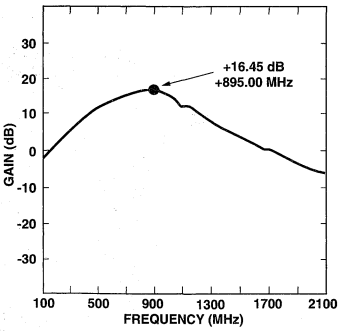


Figure 4. Typical swept gain performance of 900 MHz amplifier.

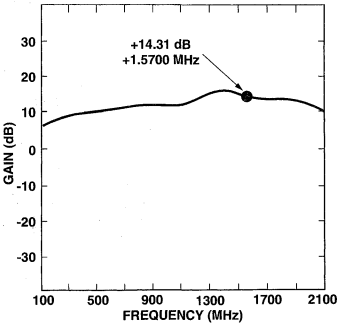


Figure 5. Typical swept gain performance of 1575 MHz amplifier.

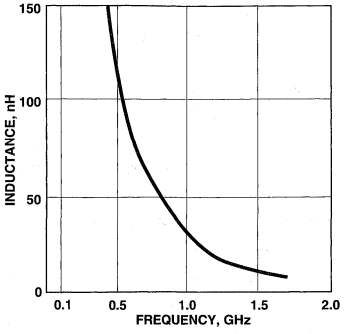


Figure 6. Inductance L1 vs. optimum frequency.

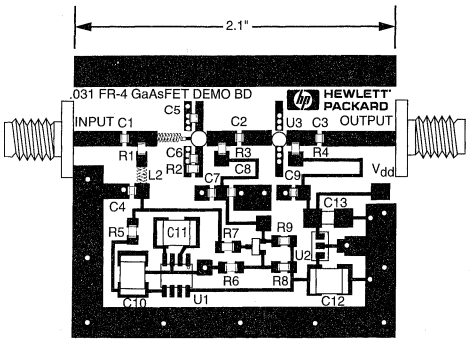


Figure 7. GaAs FET Demo board showing component placement. For best peformance reverse the location of R1 and L2 (see text).

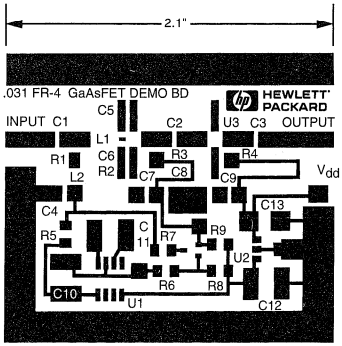


Figure 8. GaAs FET Demo board 1X artwork.

In Case Of Difficulty

Generally the noise figure should be within a couple or three tenths of a dB of that indicated in the performance table and gain within a few dB. If the noise figure or gain is not as expected then check the bias conditions. Is the V_{ds} between 1 and 2 volts and drain current 20 to 25 mA? If the bias voltage and current is adjustable, does performance maximize at the rated bias conditions or at some other set of values? If so, then the problem may be excessive source inductance which is causing a high frequency oscillation. If a device is oscillating at any frequency, even an out-of-the-band frequency, it may be difficult to obtain rated performance. Shorten the source lead length or find a source bypass capacitor with lower parasitic inductance. The design assumed 0.4 nH of associated inductance for the 1000 pF source bypass capacitors. If the problem is inband stability, then the solution is to add series resistance between the drain and output connector. This in series with blocking capacitor C2. Additional gain reduction can also be had by decreasing the length of the shunt output inductor between R3 and C7. In some cases, higher than expected noise figure can be attributed to noise from the dc to dc converter or the PNP transistor used for active biasing. Additional use of 0.1 µF bypass capacitors at C4 and C8 may be necessary. The use of a lossy or low Q RF choke for L2 can contribute to an increase in noise figure. The use of small molded RF chokes for L2 works well in prototypes. For surface mount applications be sure to choose a high Q wire-wound choke such as those made by CoilCraft.

In some instances, the enclosure can cause undesirable feedback across the circuit board which can cause instabilities. This phenomena is true of any amplifier design. A cross sectional view of the housing can be viewed as a piece of waveguide whose dimensions, both width and height, determine the band of frequencies that it may pass with minimal attenuation. A combination of the amplifier response along with the housing response could contribute to instabilities if not controlled. The use of low profile surface mount components will minimize this effect. Making sure that the cover is no closer to the printed circuit board than is necesary will minimize coupling from the cover. It is preferred to have the cover at least 0.3 to 0.5 inches above the circuit board. RF Absorptive material such as ECOSORB™ can be used on the cover to minimize reflections if the cover has to be in close proximity to the board. The use of a metal divider hanging down from the cover is also another method of breaking up enclosure effects.

Amplifier Tuning

Due to the inherent broad bandwidth of these amplifiers, they should require no RF tuning in production. With the use of active biasing, the ampifiers should power up at the proper bias point without any further adjustment required. The frequency at which minimum input VSWR will occur corresponds automatically with minimum noise figure and maximum gain. As shown in the foregoing data, the noise figure varies very little over a wide bandwidth, so it might be advantageous to tune for minimum input VSWR as opposed to noise figure. Without the source inductance, the input VSWR will be considerably higher.

Since the noise matching network is low Q it does offer broad bandwidth and insensitivity to tolerance on the series inductor. According to the computer simulation, varying the input inductor L1 from its nominal value of 7 nH to a low of 5 nH to a high of 10 nH increases the noise figure less than 0.2 dB. To minimize cost, the lumped inductor can be replaced by a microstripline .010 inches wide by 0.28 inches long at the expense of 0.2 to 0.3 dB increase in noise figure. See computer simulation in the Appendix.

The simple series L/R matching network in the output circuit forces a good broadband low VSWR output match. Due to the finite amount of reverse isolation of the device, the output match is affected by the input match and vice versa. Therefore the frequency of best output VSWR is somewhat dependent on where the input network is optimum.

Power Output

The use of heavy resistive loading in the output circuit to obtain broadband stability can be expected to limit the power output capability of the amplifier. Despite the resistive loading the 900 MHz amplifier has a measured 1 dB gain compression point of 5 mW when biased at a V_{ds} of 1 volt and I_{ds} of 20 mA.

Operation At Reduced Current

For applications that are more current conscious, the 900 MHz amplifier was tested at various drain currents from 1.5 mA to 25 mA with a constant Vds of 1 volt. The graph shown in Figure 9 reflects typical performance at reduced drain current without readjusting either the input or output impedance match. The S Parameters shown in Tables 4, 5, and 6 can be used to help design an amplifier for a specific low current application. The noise parameters at the nominal bias (Table 1) will provide a good starting point for a design at lower current. The final design is best optimized on the bench.

Table 4. Scattering and Noise Parameters for the Hewlett-Packard ATF-10236 GaAs FET, Vds = 1 volt and Ids = 10 mA

Freq	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.1	.99	-4	3.66	177	.006	83	.35	-2
0.5	.99	-17	3.62	164	.031	80	.35	-13
1.0	.98	-36	3.52	147	.060	66	.34	-28
2.0	.92	-69	3.25	120	.117	44	.30	-60

Table 5. Scattering and Noise Parameters for the Hewlett-Packard ATF-10236 GaAs FET, Vds = 1 volt and Ids = 5 mA

Freq	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.1	.99	-3	2.67	178	.004	98	.50	-2
0.5	.99	-15	2.66	165	.033	76	.50	-12
1.0	.99	-32	2.63	149	.068	68	.49	-25
2.0	.95	-62	2.49	123	.128	44	.44	-50

Table 6. Scattering and Noise Parameters for the Hewlett-Packard ATF-10236 GaAs FET, Vds = 1 volt and Ids = 2 mA

Freq	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.1	.999	-3	1.60	178	.009	76	.68	-3
0.5	.999	-13	1.60	167	.036	78	.67	-11
1.0	.99	-28	1.61	151	.075	69	.66	-22
2.0	.97	-55	1.56	126	.143	48	.62	-43

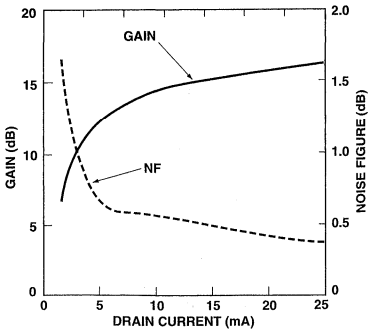


Figure 9. Noise figure and gain performance of the 900 MHz LNA at V_{ds} = 1 volt and various drain currents.

Other Applications

The basic ATF-10236 amplifier circuit can also be successfully used as a mixer for either upconverting or downconverting an input signal. As a downconverter, use the RF input as the input port and use the RF output port as the local oscillator input port. Only a few milliwatts of LO is required at this port. This is termed a drain pumped mixer. The IF can be taken off of the drain bias decoupling line. The drain bias decoupling line should be bypassed with a fairly low value of capacitance such that the normally low frequency of the IF can still pass through and be coupled out to the IF port through a low pass matching network. Mixer design is covered in more detail in application note AN-G005.

Conclusion

The results show that high-frequency GaAs FETs can be used very successfully in the VHF through 1700 MHz frequency range with very simple circuit techniques. Noise figures of 0.5 dB at 900 MHz and 0.73 dB at 1575 MHz are possible using the inexpensive ATF-10236 GaAs FET device on an inexpensive epoxy glass dielectric printed circuit board.

The single-element input matching network provides very good performance in this frequency range and offers the greatest bandwidth and least sensitivity to manufacturing tolerances. The resistive loading in the output network provides the best broadband stable performance by sacrificing some in-band gain. The computer simulation programs are instrumental in analyzing overall amplifier performance.

References

1. L. Besser, "Stability Considerations of Low Noise Transistor Amplifiers With Simultaneous Noise and Power Match," Low Noise Microwave Transistors and Amplifiers, H. Fukui, Editor, IEEE Press, 1981, pp. 272-274.

2. G.D. Vendelin, "Feedback Effects on the Noise Performance of GaAs MESFETs," Low Noise Microwave Transistors and Amplifiers, H. Fukui, Editor, IEEE Press, 1981, pp.. 294-296.

3. D. Williams, W. Lum, S. Weinreb, "L-Band Cryogenically Cooled GaAs FET Amplifiers," Microwave Journal, October 1980, p. 73.

4. G. Gonzalez, Microwave Transistor Amplifiers, Prentice- Hall, 1984, pp. 131-133.

5. G.D. Vendelin, Design of Amplifiers and Oscillators by the S-Parameter Method, Wiley, 1982, pp. 53-59.

Applications

The application notes represented by these abstracts are available from your local Hewlett-Packard sales office or nearest Hewlett-Packard authorized distributor or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

Applications Literature

High Frequency Transistor Primer Series

Primer 2
Noise and S-Parameter Characterization
Publication No. 5091-8350E

Primer 3
Thermal Properties
Publication No. 300124

Primer 3A
Thermal Resistance
Publication No. 300126

Primer 4
GaAs FET Characteristics
Publication No. 5966-0779E

General Application Notes

AN A001
Notes on Choke Network Design
Designing bias decoupling networks for bipolar transistors and GaAs FET devices that provide stable device performance.
Publication No. 5091-8824E

AN A002
Design of a 4 GHz LNA for a TVRO Earth Station
Design techniques for a low noise amplifier are presented along with a discussion of active bias circuits.
Publication No. 5091-8823E

AN A004R
Electrostatic Discharge Damage and Control
Identifying and preventing ESD damage to semiconductor devices
Publication No. 5091-8803E

AN A005
Transistor Chip Use
Discussion of procedures for proper storage, die attach, and bonding for discrete transistors
Publication No. 5091-8802E

AN A006
Mounting Considerations for Packaged Microwave Semiconductors
Mechanical, thermal, and soldering information
Publication No. 5091-8696E

AN A007
4 GHz Televisions Receive Only LNB Design
A Low Noise Block Down-converter design for the 4 GHz TVRO market is presented in the note. The LNB consists of a low noise amplifier using the ATF-10X36 family of devices, a 4 GHz mixer using the MSF series of self-oscillating mixers, along with a 950 50 1450 MHz IF amplifier.
Publication No. 5091-8825E

AN A008 Microwave Oscillator Design
Using S-Parameters to predict frequency of oscillation
Publication No. 5964-3431E

AN A009 Direct Broadcast Satellite Systems
This note takes a system level look at the individual components that make up a low noise block downconverter.
Publication No. 5091-8819E

AN G001
ATF-13136 12 GHz Demonstration Amplifier
Discussed the design, construction, and performance of a low noise 11.7 to 12.2 GHz amplifier using the ATF-13136.

Publication No. 5091-9055E

AN G002
ATF-10136 4 GHz Demonstration Amplifier
Discusses the design, construction, and performance of a low noise 3.7 to 4.2 GHz amplifier using the ATF-10136.

Publication No. 5091-4863E

AN G004
S-Band Low Noise Amplifiers Using the ATF-10136 and ATF-13284
Discusses the design, construction, and performance of a low noise amplifier for 2.4 GHz using microstripline construction. Biasing techniques are also discussed.

Publication No. 5091-9311E

AN G005
Active GaAs FET Mixer Using the ATF-10136, ATF-13736, and ATF-13484
Active mixers can provide moderate (5 dB) noise figures and conversion gain. This note discusses the various methods by which the local oscillator signal is injected and the advantages and disadvantages of each technique. Actual circuits are presented along with measured test results.

Publication No. 5091-3744E

AN 1064
Low Noise and Moderate Power Amplifiers Using the ATF-21186
The note covers the use of the ATF-21186 in low power and moderate amplifiers in the VHF and L Band frequency range.

Publication No. 5962-6875E

AN 1091
1 and 2 Stage 10.7 to 12.7 GHz Amplifiers Using the ATF-36163
Low Noise PHEMT 1 and 2 stage low noise amplifiers for the Direct Broadcast Satellite market are described using the ATF-36163 low noise PHEMT in the low cost surface mount SOT-363 (SC-70) package.

Publication No. 5965-1235E

AN 1097
L and S Band Amplifiers Using the ATF-36163 Low Noise PHEMT
A 1-stage low noise amplifier is described that has less than 1 dB noise figure and 16 dB gain in the 2.0 to 2.4 GHz frequency range.

Publication No. 5965-5956E

AN 1128
L Band Amplifier Using the ATF-36077 Low Noise PHEMT
This application note describes the use of the ATF-36077 in low noise amplifier applications in the 900 MHz through 1800 MHz frequency range.

Publication No. 5966-0783E

AN 1129
Low Noise Amplifier for 2.3 GHz Using the ATF-36077 Low Noise PHEMT
This application note describes the use of the ATF-36077 in a low noise amplifier for 2.3 GHz ISM/MMDS applications.

Publication No. 5966-0782E

Gallium Arsenide Field Effect Transistors Selection Guide

NF_o and G_a are specified at a low noise bias point, while $P_{1\,dB}$ and $G_{1\,dB}$ are specified at bias points which optimize these parameters.

Low Noise PHEMTs (Typical Specifications @ 25°C Case Temperature)

Part Number	Gate Width (mm)	Optimum Frequency Range (GHz)	Test Frequency (GHz)	V_{dd} (V)	NF_o (dB)	G_a (dB)	$P_{1\,dB}$ (dBm)	Package	Page No.
ATF-36077	200	1.5 - 18	12	1.5	0.5	12.0	+5	70 mil SM	5-75
ATF-36163	200	1.5 - 18	12	1.5	1.2	10.0	+5	SOT-363 (SC-70)	5-79

Low Noise MESFETs (Typical Specifications @ 25°C Case Temperature)

Part Number	Gate Width (mm)	Optimum Frequency Range (GHz)	Test Frequency (GHz)	V_{dd} (V)	NF_o (dB)	G_a (dB)	$P_{1\,dB}$[1] (dBm)	Package	Page No.
ATF-13100	250	2 - 18	12	2.5	1.1	9.5	+17.5	chip	5-33
ATF-13336	250	2 - 16	12	2.5	1.4	9.0	+17.5	micro-X SM	5-36
ATF-13736	250	2 - 16	12	2.5	1.8	9.0	+17.5	micro-X SM	5-39
ATF-13786	250	1 - 12	10	3.0	—	7.5[2]	+16.5	85 mil plastic SM	5-43
ATF-26836	250	2 - 16	12	5.0	2.2	9.0[3]	+18.0	micro-X SM	5-67
ATF-26884	250	2 - 16	12	5.0	2.2	9.0[3]	+18.0	85 mil plastic	5-71
ATF-10100	500	0.5 - 12	4	2.0	0.55	14.0	+21.0	chip	5-19
ATF-10136	500	0.5 - 12	4	2.0	0.5	13.0	+20.0	micro-X SM	5-23
ATF-10236	500	0.5 - 12	4	2.0	0.8	13.0	+20.0	micro-X SM	5-26
ATF-10736	500	0.5 - 12	4	2.0	1.2	13.0	+20.0	micro-X SM	5-29
ATF-25170	500	0.5 - 10	4	3.0	0.8	14.0	+21.0	70 mil stripline	5-57
ATF-25570	500	0.5 - 10	4	3.0	1.0	14.0	+20.5	70 mil stripline	5-60
ATF-25735	500	0.5 - 10	4	3.0	1.2	13.0	+19.0	micro-X SM	5-63
ATF-21170	750	0.5 - 6	4	3.0	0.9	13.0	+23.0	70 mil stripline	5-46
ATF-21186	750	0.5 - 6	2	2.0	0.65	13.0	+19.0	85 mil plastic SM	5-49

Notes:
1. $P_{1\,dB}$ @ power bias
2. $G_{1\,dB}$
3. Tuned small signal gain

Gallium Arsenide Field Effect Transistors Selection Guide, continued

Medium Power MESFETs (Typical Specifications @ 25°C Case Temperature)

Part Number	Gate Width (mm)	Optimum Frequency Range (GHz)	Test Frequency (GHz)	V_{dd} (V)	$P_{1\,dB}$ (dBm)	$G_{1\,dB}$ (dBm)	Package	Part No.
ATF-44101	5000	2 - 8	4	9.0	+32.0	8.5	100 mil flange	5-89
ATF-45101	2500	2 - 8	4	9.0	+29.0	10.0	100 mil flange	5-92
ATF-45171	2500	2 - 8	4	9.0	+29.0	10.5	70 mil flange	5-95
ATF-46101	1250	2 - 10	4	9.0	+27.0	10.0	100 mil flange	5-98
ATF-46171	1250	2 - 10	4	9.0	+27.0	11.0	70 mil flange	5-101

HEWLETT® PACKARD

0.5 – 12 GHz Low Noise Gallium Arsenide FET

Technical Data

ATF-10100

Features

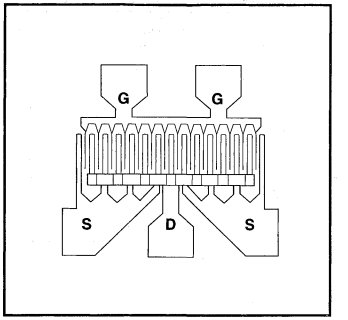
- **Low Noise Figure:** 0.5 dB Typical at 4 GHz
- **Low Bias:** V_{DS} = 2 V, I_{DS} = 25 mA
- **High Associated Gain:** 14.0 dB Typical at 4 GHz
- **High Output Power:** 21.0 dBm Typical $P_{1\,dB}$ at 4 GHz

Description

The ATF-10100 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor chip. Its premium noise figure makes this device appropriate for use in the first stage of low noise amplifiers operating in the 0.5-12 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

Chip Outline



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB		0.4 0.55 0.8	 0.7
G_A	Gain @ NF_O; V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB	 12.0 	17.0 14.0 12.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dBm		21.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dB		15.0	
g_m	Transconductance: V_{DS} = 2 V, V_{GS} = 0 V		mmho	80	140	
I_{DSS}	Saturated Drain Current: V_{DS} = 2 V, V_{GS} = 0 V		mA	70	130	180
V_P	Pinchoff Voltage: V_{DS} = 2 V, I_{DS} = 1 mA		V	-3.0	-1.3	-0.8

Note:
1. RF performance is determined by packaging and testing 10 devices per wafer.

ATF-10100 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+5
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-7
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	430
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature[4]	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 225°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[4]

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 4.4 mW/°C for T_{CASE} > 78°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See APPLICATIONS PRIMER IIIA for more information.

Part Number Ordering Information

Part Number	Devices Per Tray
ATF-10100-GP3	50

ATF-10100 Noise Parameters: V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	NF_O dB	Γ_{opt}		$R_N/50$
		Mag	Ang	
1.0	0.4	0.78	13	0.40
2.0	0.4	0.55	27	0.29
4.0	0.55	0.39	65	0.22
6.0	0.8	0.41	105	0.16
8.0	1.0	0.46	144	0.10

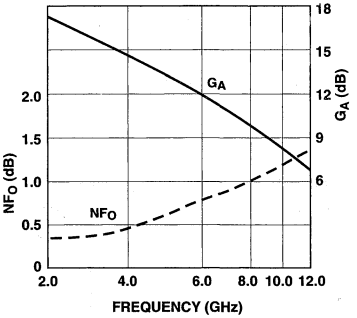


Figure 1. Optimum Noise Figure and Associated Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 25 mA, T_A = 25°C.

ATF-10100 Typical Performance, T_A = 25°C

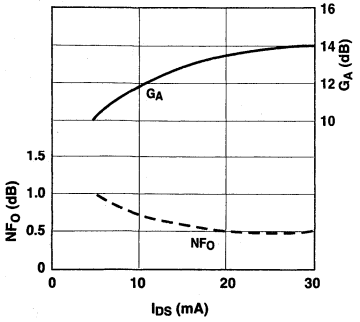


Figure 2. Optimum Noise Figure and Associated Gain vs. I_{DS}. V_{DS} = 2 V, f = 4.0 GHz.

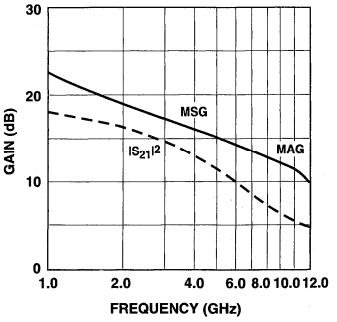


Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 25 mA.

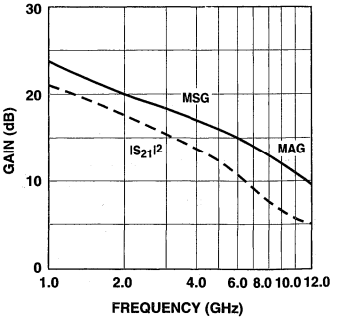


Figure 4. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 4 V, I_{DS} = 70 mA.

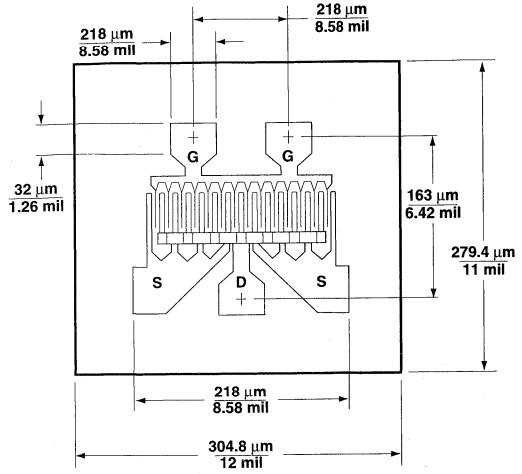
Typical Scattering Parameters, Common Source, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 2 V, I_{DS} = 25 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
1.0	.93	-46	17.7	7.63	148	-25.5	.053	64	.33	-56
2.0	.83	-78	15.6	6.08	127	-21.4	.085	52	.31	-63
3.0	.78	-94	13.9	4.97	114	-19.8	.102	45	.30	-72
4.0	.72	-104	12.4	4.18	103	-18.7	.116	41	.29	-80
5.0	.70	-120	11.2	3.65	92	-17.9	.127	36	.25	-90
6.0	.68	-139	10.0	3.18	80	-17.6	.132	31	.19	-113
7.0	.71	-157	8.6	2.69	69	-17.5	.133	25	.18	-156
8.0	.72	168	7.4	2.35	60	-17.5	.133	22	.20	-178
9.0	.71	-177	6.5	2.12	53	-17.4	.135	19	.22	174
10.0	.70	175	6.0	1.99	46	-16.9	.143	17	.22	169
11.0	.70	167	5.5	1.88	38	-16.6	.148	15	.23	164
12.0	.70	162	5.0	1.77	31	-16.3	.154	13	.24	153
13.0	.70	159	4.5	1.68	25	-15.8	.162	11	.26	143
14.0	.70	155	4.1	1.61	20	-15.5	.168	10	.28	133
15.0	.73	149	3.9	1.56	14	-15.0	.177	8	.30	123
16.0	.77	138	3.2	1.45	5	-14.7	.184	6	.32	119
17.0	.76	134	1.8	1.23	0	-14.4	.190	5	.35	114
18.0	.77	134	1.3	1.16	-1	-13.9	.201	4	.38	106

Typical Scattering Parameters, Common Source, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 4 V, I_{DS} = 70 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
1.0	.87	-60	20.6	10.72	136	-26.4	.048	55	.33	-59
2.0	.74	-96	17.5	7.50	113	-23.5	.067	43	.29	-66
3.0	.72	-112	15.2	5.77	101	-22.2	.078	39	.28	-69
4.0	.67	-122	13.4	4.68	91	-21.3	.086	38	.27	-72
5.0	.67	-137	12.0	3.97	81	-20.6	.093	36	.24	-77
6.0	.68	-154	10.5	3.36	70	-20.3	.097	35	.17	-95
7.0	.73	-168	9.0	2.81	61	-20.1	.099	33	.13	-127
8.0	.74	-177	7.7	2.44	54	-19.8	.102	31	.12	-159
9.0	.75	175	6.8	2.19	47	-19.6	.105	31	.12	-165
10.0	.75	166	6.2	2.04	39	-18.9	.113	29	.13	-171
11.0	.75	156	5.6	1.90	32	-18.4	.120	27	.13	-177
12.0	.74	150	5.1	1.79	25	-17.9	.128	26	.14	173
13.0	.74	148	4.6	1.69	19	-16.9	.143	25	.15	166
14.0	.75	145	4.2	1.62	14	-16.2	.155	24	.17	154
15.0	.76	140	3.9	1.57	9	-15.7	.164	21	.21	142
16.0	.77	135	3.2	1.45	-1	-15.5	.168	18	.24	133
17.0	.79	130	1.8	1.23	-6	-15.3	.171	18	.28	125
18.0	.80	125	1.3	1.16	-6	-14.4	.191	18	.32	117

ATF-10100 Chip Dimensions



Note: Die thickness is 4.5 mil, and backside metallization is 200 Å Ti and 2000 Å Au.

HEWLETT® PACKARD

0.5 – 12 GHz Low Noise Gallium Arsenide FET

Technical Data

ATF-10136

Features

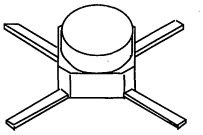
- **Low Noise Figure:** 0.5 dB Typical at 4 GHz
- **Low Bias:** V_{DS} = 2 V, I_{DS} = 20 mA
- **High Associated Gain:** 13.0 dB Typical at 4 GHz
- **High Output Power:** 20.0 dBm Typical $P_{1\,dB}$ at 4 GHz
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and Reel Packaging Option Available** [1]

Description

The ATF-10136 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its premium noise figure makes this device appropriate for use in the first stage of low noise amplifiers operating in the 0.5-12 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB		0.4 0.5 0.8	 0.6
G_A	Gain @ NF_O; V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB	 12.0 	16.5 13.0 11.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dBm		20.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dB		12.0	
g_m	Transconductance: V_{DS} = 2 V, V_{GS} = 0 V		mmho	70	140	
I_{DSS}	Saturated Drain Current: V_{DS} = 2 V, V_{GS} = 0 V		mA	70	130	180
V_P	Pinchoff Voltage: V_{DS} = 2 V, I_{DS} = 1 mA		V	-4.0	-1.3	-0.5

Note:

1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors."

ATF-10136 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+5
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-7
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	430
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature[4]	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 350°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[5]

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 2.9 mW/°C for T_{CASE} > 25°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See APPLICATIONS PRIMER IIIA for more information.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-10136-TR1	1000	7"
ATF-10136-STR	10	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices."

ATF-10136 Noise Parameters: V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	NF_O dB	Γ_{opt}		$R_N/50$
		Mag	Ang	
0.5	0.35	0.93	12	0.80
1.0	0.4	0.85	24	0.70
2.0	0.4	0.70	47	0.46
4.0	0.5	0.39	126	0.36
6.0	0.8	0.36	-170	0.12
8.0	1.1	0.45	-100	0.38

ATF-10136 Typical Performance, T_A = 25°C

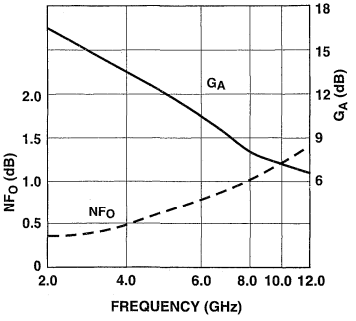


Figure 1. Optimum Noise Figure and Associated Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 25 mA, T_A = 25°C.

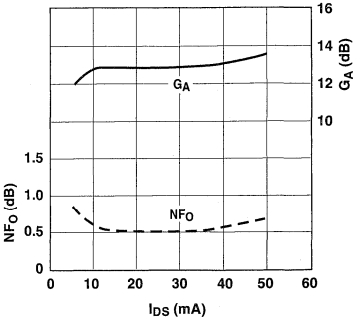


Figure 2. Optimum Noise Figure and Associated Gain vs. I_{DS}. V_{DS} = 2 V, f = 4.0 GHz.

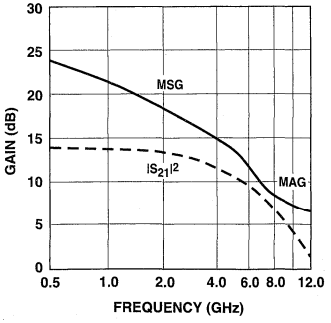
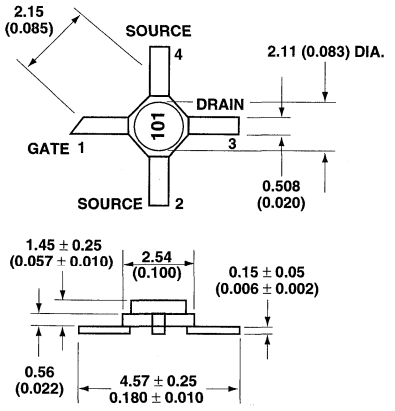


Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 25 mA.

Typical Scattering Parameters, Common Source, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 2 V, I_{DS} = 25 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.98	-18	14.5	5.32	163	-34.0	.020	78	.35	-9
1.0	.93	-33	14.3	5.19	147	-28.4	.038	67	.36	-19
2.0	.79	-66	13.3	4.64	113	-22.6	.074	59	.30	-31
3.0	.64	-94	12.2	4.07	87	-19.2	.110	44	.27	-42
4.0	.54	-120	11.1	3.60	61	-17.3	.137	31	.22	-49
5.0	.47	-155	10.1	3.20	37	-15.5	.167	13	.16	-54
6.0	.45	162	9.2	2.88	13	-14.3	.193	-2	.08	-17
7.0	.50	120	8.0	2.51	-10	-13.9	.203	-19	.16	45
8.0	.60	87	6.4	2.09	-32	-13.6	.210	-36	.32	48
9.0	.68	61	4.9	1.75	-51	-13.6	.209	-46	.44	38
10.0	.73	42	3.6	1.52	-66	-13.7	.207	-58	.51	34
11.0	.77	26	2.0	1.26	-82	-13.8	.205	-73	.54	27
12.0	.80	14	1.0	1.12	-97	-14.0	.200	-82	.54	15

36 micro-X Package Dimensions



Notes:
1. Dimensions are in millimeters (inches)
2. Tolerances: in .xxx = ± 0.005
   mm .xx = ± 0.13

HEWLETT® PACKARD

0.5 – 12 GHz Low Noise Gallium Arsenide FET

Technical Data

ATF-10236

Features

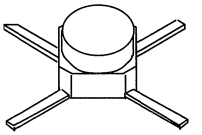
- **Low Noise Figure:** 0.8 dB Typical at 4 GHz
- **Low Bias:** V_{DS} = 2 V, I_{DS} = 20 mA
- **High Associated Gain:** 13.0 dB Typical at 4 GHz
- **High Output Power:** 20.0 dBm Typical P_{1dB} at 4 GHz
- **Cost Effective Ceramic Microstrip Package**
- **Tape-And-Reel Packaging Option Available** [1]

Description

The ATF-10236 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its low noise figure makes this device appropriate for use in the first and second stages of low noise amplifiers operating in the 0.5-12 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB		0.6 0.8 1.0	 1.0
G_A	Gain @ NF_O; V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB	 12.0 	16.5 13.0 10.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dBm		20.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dB		12.0	
g_m	Transconductance: V_{DS} = 2 V, V_{GS} = 0 V		mmho	80	140	
I_{DSS}	Saturated Drain Current: V_{DS} = 2 V, V_{GS} = 0 V		mA	70	130	180
V_P	Pinchoff Voltage: V_{DS} = 2 V, I_{DS} = 1 mA		V	-3.0	-1.3	-0.8

Note:

1. Refer to PACKAGING section, "Tape-and-Reel Packaging for Surface Mount Semiconductors."

ATF-10236 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+5
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-7
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	430
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature[4]	°C	175

Thermal Resistance:	θ_{jc} = 350°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1μm Spot Size[5]

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 2.9 mW/°C for T_{CASE} > 25°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-10236-TR1	1000	7"
ATF-10236-STR	10	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices."

ATF-10236 Noise Parameters: V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	NF_O dB	Γ_{opt}		$R_N/50$
		Mag	Ang	
0.5	0.45	0.93	18	0.75
1.0	0.5	0.87	36	0.63
2.0	0.6	0.73	74	0.33
4.0	0.8	0.45	148	0.15
6.0	1.0	0.42	-137	0.12
8.0	1.3	0.49	-80	0.45

ATF-10236 Typical Performance, T_A = 25°C

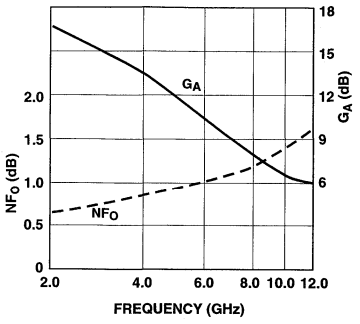


Figure 1. Optimum Noise Figure and Associated Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 25 mA, T_A = 25°C.

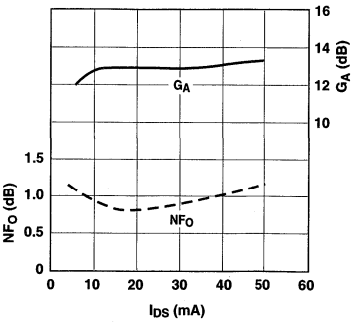


Figure 2. Optimum Noise Figure and Associated Gain vs. I_{DS}. V_{DS} = 2 V, f = 4.0 GHz.

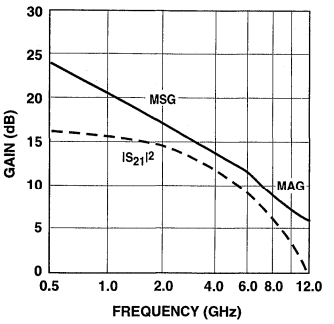


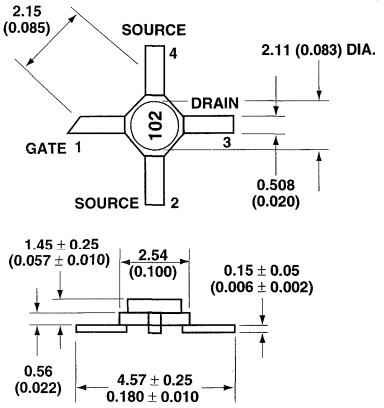
Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 25 mA.

Typical Scattering Parameters, Common Source, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 2 V, I_{DS} = 25 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.97	-20	15.1	5.68	162	-32.8	.023	76	.47	-11
1.0	.93	-41	14.9	5.58	143	-26.0	.050	71	.45	-23
2.0	.77	-81	13.6	4.76	107	-21.3	.086	51	.36	-38
3.0	.59	-114	12.2	4.06	80	-18.4	.120	35	.30	-51
4.0	.48	-148	10.9	3.51	52	-16.5	.149	18	.23	-67
5.0	.46	166	9.6	3.03	26	-15.3	.172	3	.10	-67
6.0	.53	125	8.5	2.65	1	-14.5	.189	-14	.09	48
7.0	.62	96	6.9	2.22	-20	-14.4	.191	-28	.24	55
8.0	.71	73	4.9	1.75	-39	-14.5	.189	-41	.37	51
9.0	.75	54	3.3	1.47	-55	-14.7	.184	-46	.46	42
10.0	.78	39	2.1	1.28	-72	-14.9	.180	-59	.51	34
11.0	.82	26	0.3	1.04	-86	-14.9	.179	-71	.54	26
12.0	.84	12	-0.5	0.95	-101	-15.0	.177	-82	.54	17

A model for this device is available in the DEVICE MODELS section.

36 micro-X Package Dimensions



Notes:
1. Dimensions are in millimeters (inches)
2. Tolerances: in .xxx = ± 0.005
   mm .xx = ± 0.13

HEWLETT® PACKARD

0.5 – 12 GHz General Purpose Gallium Arsenide FET

Technical Data

ATF-10736

Features

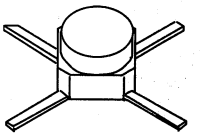
- **High Associated Gain:** 13.0 dB Typical at 4 GHz
- **Low Bias:** V_{DS} = 2 V, I_{DS} = 25 mA
- **High Output Power:** 20.0 dBm typical $P_{1\,dB}$ at 4 GHz
- **Low Noise Figure:** 1.2 dB Typical at 4 GHz
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available** [1]

Description

The ATF-10736 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its noise figure makes this device appropriate for use in the gain stages of low noise amplifiers operating in the 0.5-12 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconcnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB		0.9 1.2 1.4	 1.4
G_A	Gain @ NF_O; V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB	 12.0 	16.5 13.0 10.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dBm		20.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dB		12.0	
g_m	Transconductance: V_{DS} = 2 V, V_{GS} = 0 V		mmho	70	140	
I_{DSS}	Saturated Drain Current: V_{DS} = 2 V, V_{GS} = 0 V		mA	70	130	180
V_P	Pinchoff Voltage: V_{DS} = 2 V, I_{DS} = 1 mA		V	-4.0	-1.3	-0.5

Note:

1. Refer to PACKAGING section, "Tape-and-Reel Packaging for Surface Mount Semiconductors."

ATF-10736 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+5
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-7
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Total Power Dissipation[2,3]	mW	430
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature[4]	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 350°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1μm Spot Size[5]

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 2.9 mW/°C for T_{CASE} > 25°C.
4. Storage above +150°C may tarnish the leads of this package difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-10736-TR1	1000	7"
ATF-10736-STR	10	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices."

ATF-10736 Noise Parameters: V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	NF_O dB	Γ_{opt}		$R_N/50$
		Mag	Ang	
1.0	0.8	0.88	41	0.52
2.0	0.9	0.75	85	0.27
4.0	1.2	0.48	159	0.08
6.0	1.4	0.46	-122	0.08
8.0	1.7	0.53	-71	0.43

ATF-10736 Typical Performance, T_A = 25°C

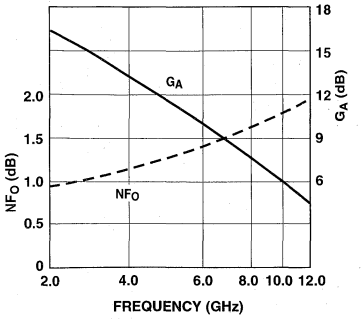


Figure 1. Optimum Noise Figure and Associated Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 25 mA, T_A = 25°C.

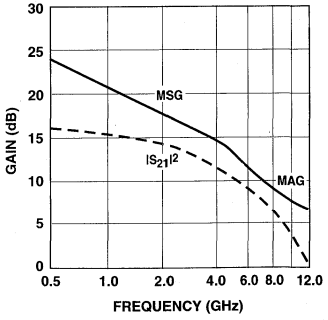


Figure 2. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 25 mA.

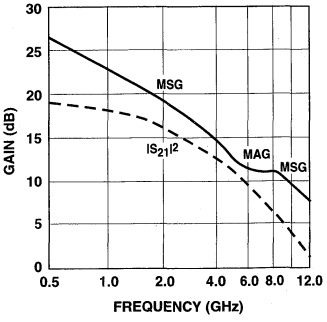


Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 4 V, I_{DS} = 70 mA.

Typical Scattering Parameters, Common Source, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 2 V, I_{DS} = 25 mA

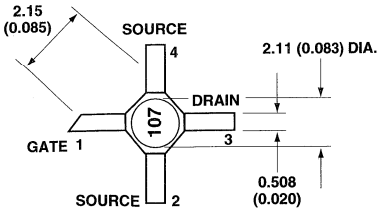
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.96	-20	15.4	5.90	162	-32.4	.024	77	.50	-10
1.0	.92	-40	15.2	5.77	144	-26.7	.046	66	.48	-21
2.0	.77	-76	13.8	4.92	109	-21.3	.086	52	.39	-34
3.0	.59	-107	12.5	4.20	83	-20.0	.111	40	.33	-45
4.0	.49	-136	11.2	3.64	57	-17.3	.137	24	.26	-61
5.0	.43	-179	10.0	3.15	32	-15.5	.167	9	.14	-65
6.0	.49	138	8.6	2.74	8	-14.9	.179	-5	.05	22
7.0	.57	106	7.3	2.32	-13	-14.8	.183	-18	.19	60
8.0	.68	81	5.6	1.92	-32	-14.7	.185	-33	.33	57
9.0	.73	62	4.2	1.62	-50	-14.8	.183	-40	.42	46
10.0	.77	47	3.0	1.41	-66	-14.8	.182	-52	.46	38
11.0	.82	36	1.0	1.12	-81	-14.6	.186	-67	.50	27
12.0	.85	22	-0.2	0.98	-97	-14.5	.189	-75	.51	15

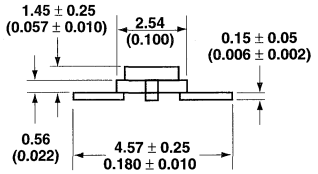
Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 4 V, I_{DS} = 70 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.90	-32	19.0	8.95	147	-34.9	.018	77	.40	-7
1.0	.79	-53	18.0	7.96	128	-28.6	.037	70	.38	-17
2.0	.57	-96	15.5	5.99	90	-22.5	.075	56	.34	-38
3.0	.43	-129	13.3	4.60	64	-19.5	.106	43	.31	-50
4.0	.36	-163	11.6	3.78	39	-17.3	.136	31	.28	-51
5.0	.35	156	10.1	3.21	16	-15.6	.166	14	.22	-45
6.0	.47	110	8.8	2.76	-11	-14.5	.189	-5	.15	-4
7.0	.65	78	7.0	2.23	-36	-14.2	.196	-23	.28	35
8.0	.77	58	5.1	1.80	-56	-14.1	.198	-38	.42	37
9.0	.83	44	3.5	1.50	-72	-14.2	.195	-48	.51	33
10.0	.86	30	2.4	1.32	-88	-14.5	.188	-64	.55	26
11.0	.87	16	1.1	1.13	-106	-14.8	.182	-77	.60	18
12.0	.91	1	0.1	0.99	-123	-15.3	.171	-91	.65	7

A model for this device is available in the DEVICE MODELS section.

36 micro-X Package Dimensions





Notes:
1. Dimensions are in millimeters (inches)
2. Tolerances: in .xxx = ± 0.005
   mm .xx = ± 0.13

HEWLETT® PACKARD

2–18 GHz Low Noise Gallium Arsenide FET

Technical Data

ATF-13100

Features

- **Low Noise Figure:** 1.1 dB Typical at 12 GHz
- **High Associated Gain:** 9.5 dB Typical at 12 GHz
- **High Output Power:** 17.5 dBm Typical $P_{1\,dB}$ at 12 GHz

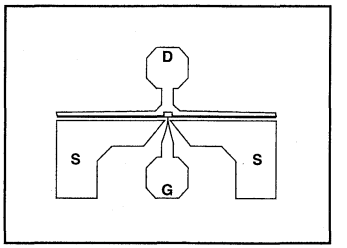
Description

The ATF-13100 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor chip. This device is designed for use in low noise, wideband amplifier and oscillator applications in the 2-18 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

The recommended mounting procedure is to die attach at a stage temperature of 300°C using a gold-tin preform under forming gas. Assembly can be preformed with either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2.5 V, I_{DS} = 20 mA	f = 8.0 GHz	dB		0.8	
		f = 12.0 GHz	dB		1.1	1.2
		f = 15.0 GHz	dB		1.5	
G_A	Gain @ NF_O; V_{DS} = 2.5 V, I_{DS} = 20 mA	f = 8.0 GHz	dB		12.0	
		f = 12.0 GHz	dB	9.0	9.5	
		f = 15.0 GHz	dB		8.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dBm		17.5	
$G_{1\,dB}$	1 dB Compressed Gain; V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dB		8.5	
g_m	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	30	55	
I_{DSS}	Saturated Drain Current; V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	-3.0	-1.5	-0.8

Note:

1. RF performance is determined by assembling and testing 10 samples per wafer.

ATF-13100 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+5
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-6
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	225
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 250°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[4]

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 4 mW/°C for $T_{MOUNTING\ SURFACE}$ > 119°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Tray
ATF-13100-GP3	50

ATF-13100 Noise Parameters: V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Γ_{opt}		$R_N/50$
		Mag	Ang	
4.0	0.4	0.60	30	0.32
6.0	0.7	0.32	68	0.21
8.0	0.8	0.25	102	0.15
12.0	1.1	0.23	-165	0.09
16.0	1.5	0.32	-112	0.21

ATF-13100 Typical Performance, T_A = 25°C

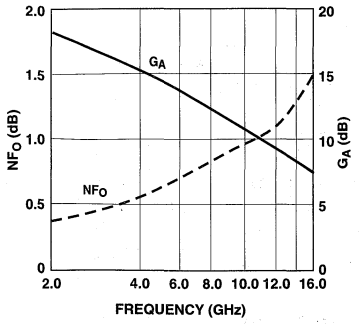


Figure 1. Optimum Noise Figure and Associated Gain vs. Frequency. V_{DS} = 2.5 V, I_{DS} = 20 mA, T_A = 25°C.

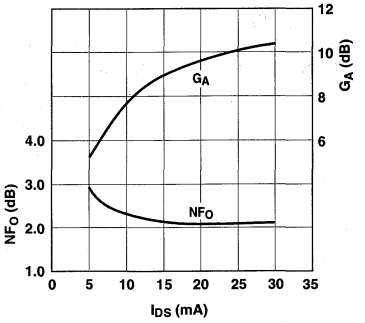


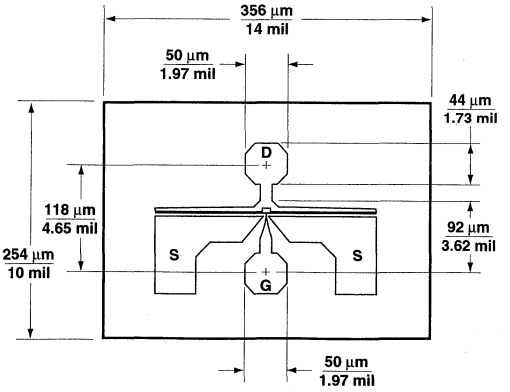
Figure 2. Optimum Noise Figure and Associated Gain vs. I_{DS}. V_{DS} = 2.5 V, f = 12.0 GHz.

Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{DS} = 2.5$ V, $I_{DS} = 20$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
2.0	.96	-27	13.4	4.68	153	-26.9	.045	75	.55	-16
3.0	.92	-41	13.4	4.65	140	-23.6	.066	67	.52	-24
4.0	.85	-58	13.1	4.54	126	-21.4	.085	59	.49	-33
5.0	.79	-76	12.9	4.40	113	-19.8	.102	50	.44	-41
6.0	.73	-95	12.4	4.19	100	-18.7	.116	42	.38	-48
7.0	.68	-113	12.0	3.97	87	-18.0	.126	34	.30	-54
8.0	.63	-132	11.4	3.71	75	-17.5	.134	25	.24	-64
9.0	.62	-151	10.9	3.51	63	-17.1	.140	18	.18	-75
10.0	.59	-167	10.3	3.27	53	-16.8	.144	11	.13	-84
11.0	.59	173	9.7	3.07	40	-16.5	.149	2	.08	-104
12.0	.57	155	9.0	2.83	30	-16.5	.150	-9	.02	160
13.0	.60	136	8.6	2.69	19	-16.4	.151	-16	.08	106
14.0	.64	116	7.9	2.47	7	-16.4	.151	-25	.15	103
15.0	.67	98	7.1	2.26	-6	-16.4	.152	-34	.23	100
16.0	.73	83	5.8	1.96	-16	-16.9	.143	-40	.31	90
17.0	.77	72	4.6	1.70	-26	-17.0	.141	-45	.36	82
18.0	.80	63	3.5	1.50	-35	-17.4	.135	-48	.40	72

A model for this device is available in the DEVICE MODELS section.

ATF-13100 Chip Dimensions



Note: Die thickness is 4.5 mil, and backside metallization is 200 Å Ti and 2000 Å Au.

HEWLETT® PACKARD

2–16 GHz Low Noise Gallium Arsenide FET

Technical Data

ATF-13336

Features

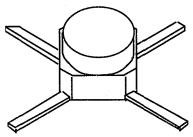
- **Low Noise Figure:** 1.4 dB Typical at 12 GHz
- **High Associated Gain:** 9.0 dB Typical at 12 GHz
- **High Output Power:** 17.5 dBm Typical $P_{1\,dB}$ at 12 GHz
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available**[1]

Description

The ATF-13336 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its premium noise figure makes this device appropriate for use in low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2.5 V, I_{DS} = 20 mA	f = 8.0 GHz	dB		1.2	
		f = 12.0 GHz	dB		1.4	1.6
		f = 14.0 GHz			1.6	
G_A	Gain @ NF_O: V_{DS} = 2.5 V, I_{DS} = 20 mA	f = 8.0 GHz	dB		11.5	
		f = 12.0 GHz	dB	8.0	9.0	
		f = 14.0 GHz	dB		7.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dBm		17.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dB		8.5	
g_m	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	25	55	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
V_P	Pinch-off Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	-4.0	-1.5	-0.5

Note:

1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

ATF-13336 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+5
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-6
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	225
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 400°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 µm Spot Size[5]

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 2.5mW/°C for T_{CASE} > 85°C.
4. Storage above +150°C may tarnish the leads of this package difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-13336-TR1	1000	7"
ATF-13336-STR	10	strip

ATF-13336 Noise Parameters: V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Γ_{opt}		$R_N/50$
		Mag	Ang	
4.0	0.8	.63	93	.27
6.0	1.1	.47	138	.10
8.0	1.2	.40	-153	.20
12.0	1.4	.52	-45	.88
14.0	1.6	.57	-2	1.3

ATF-13336 Typical Performance, T_A = 25°C

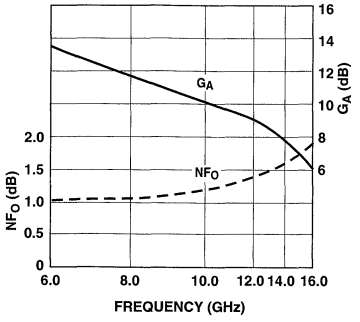


Figure 1. Optimum Noise Figure and Associated Gain vs. Frequency. V_{DS} = 2.5 V, I_{DS} = 20 mA, T_A = 25°C.

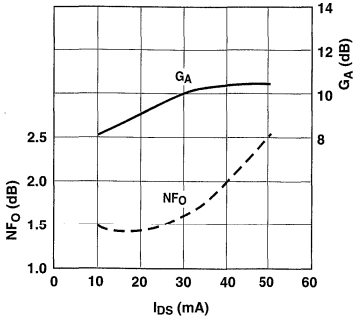


Figure 2. Optimum Noise Figure and Associated Gain vs. I_{DS}. V_{DS} = 2.5 V, f = 12.0 GHz.

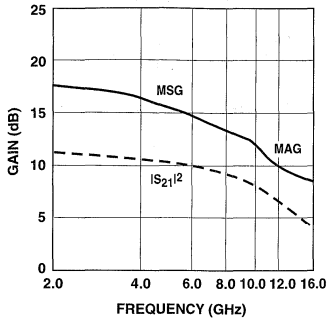


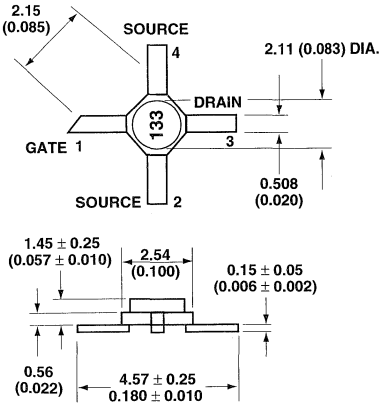
Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 2.5 V, I_{DS} = 20 mA.

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
2.0	.96	-51	10.6	3.39	127	-27.1	.044	57	.61	-41
3.0	.88	-75	10.3	3.28	106	-23.4	.060	33	.58	-51
4.0	.86	-96	10.1	3.19	86	-22.6	.074	25	.57	-57
5.0	.79	-117	9.9	3.13	66	-20.6	.093	12	.54	-65
6.0	.69	-142	10.2	3.22	46	-18.9	.114	1	.49	-79
7.0	.60	-178	10.1	3.21	21	-17.6	.132	-18	.42	-97
8.0	.54	141	9.8	3.10	-4	-17.3	.137	-33	.31	-112
9.0	.56	103	8.9	2.80	-26	-16.7	.147	-48	.21	-121
10.0	.56	74	8.3	2.60	-48	-16.5	.150	-63	.09	-145
11.0	.58	44	7.6	2.39	-68	-16.8	.145	-78	.07	89
12.0	.63	20	6.7	2.17	-90	-17.5	.133	-95	.16	43
13.0	.65	3	6.0	2.00	-108	-18.3	.121	-107	.19	21
14.0	.66	-7	5.5	1.89	-126	-18.9	.114	-121	.19	-4
15.0	.70	-19	4.9	1.76	-144	-19.0	.112	-129	.16	-28
16.0	.72	-34	4.4	1.66	-175	-19.2	.110	-142	.14	-32

A model for this device is available in the DEVICE MODELS section.

36 micro-X Package Dimensions



Notes:
1. Dimensions are in millimeters (inches)
2. Tolerances: in .xxx = ± 0.005
   mm .xx = ± 0.13

2–16 GHz Low Noise Gallium Arsenide FET

Technical Data

ATF-13736

Features

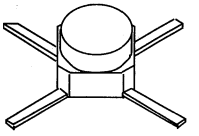
- **Low Noise Figure:** 1.8 dB Typical at 12 GHz
- **High Associated Gain:** 9.0 dB Typical at 12 GHz
- **High Output Power:** 17.5 dB Typical at 12 GHz
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

The ATF-13736 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its noise figure makes this device appropriate for use in the gain stages of low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2.5 V, I_{DS} = 20 mA	f = 8.0 GHz	dB		1.5	
		f = 12.0 GHz	dB		1.8	2.2
		f = 14.0 GHz	dB		2.1	
G_A	Gain @ NF_O: V_{DS} = 2.5 V, I_{DS} = 20 mA	f = 8.0 GHz	dB		11.5	
		f = 12.0 GHz	dB	8.0	9.0	
		f = 14.0 GHz	dB		7.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f =12.0 GHz	dBm		17.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dB		8.5	
g_m	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	25	55	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
V_P	Pinch-off Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	-4.0	-1.5	-0.5

Note:

1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

ATF-13736 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+5
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-6
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	225
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature[4]	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 400°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[5]

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 2.5 mW/°C for T_{CASE} > 85°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-13736-TR1	1000	7"
ATF-13736-STR	10	strip

ATF-13736 Noise Parameters: V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Γ_{opt}		$R_N/50$
		Mag	Ang	
4.0	1.1	.71	102	.10
6.0	1.3	.55	147	.07
8.0	1.5	.46	-144	.19
12.0	1.8	.50	-40	.88
14.0	2.1	.52	-2	1.17

ATF-13736 Typical Performance, T_A = 25°C

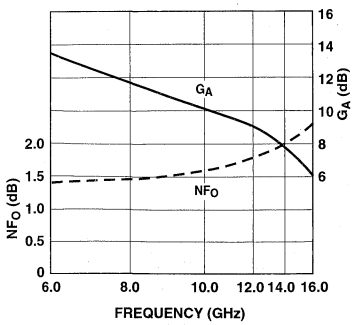


Figure 1. Optimum Noise Figure and Associated Gain vs. Frequency. V_{DS} = 2.5 V, I_{DS} = 20 mA, T_A = 25°C.

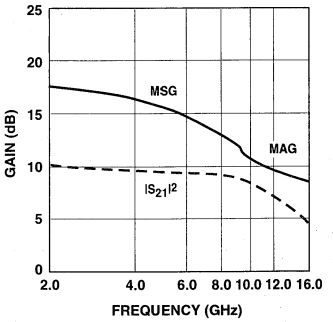


Figure 2. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 2.5 V, I_{DS} = 20 mA.

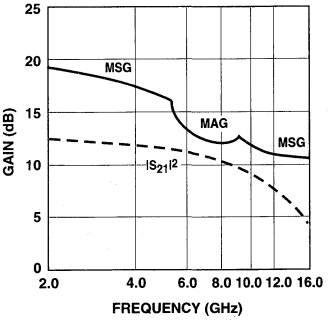


Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 2.5 V, I_{DS} = 20 mA.

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

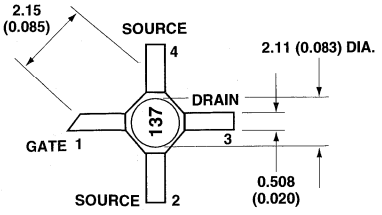
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
2.0	.94	-46	11.0	3.56	128	-26.4	.048	55	.59	-36
3.0	.86	-70	10.2	3.23	109	-25.2	.055	40	.57	-47
4.0	.84	-90	9.8	3.08	91	-23.1	.070	31	.56	-55
5.0	.77	-110	9.6	3.02	69	-20.9	.090	18	.52	-63
6.0	.68	-135	9.9	3.14	51	-19.3	.109	7	.47	-75
7.0	.59	-170	9.9	3.13	24	-18.0	.126	-12	.39	-92
8.0	.54	149	9.5	2.99	-1	-17.6	.132	-27	.30	-112
9.0	.56	112	8.8	2.75	-22	-16.9	.143	-43	.19	-121
10.0	.58	86	8.1	2.53	-43	-16.4	.152	-58	.11	-140
11.0	.60	63	7.6	2.41	-66	-16.5	.149	-73	.09	92
12.0	.64	39	7.0	2.24	-90	-17.1	.140	-81	.15	47
13.0	.68	20	6.4	2.08	-106	-17.6	.132	-90	.19	21
14.0	.70	9	6.0	1.99	-130	-18.0	.126	-97	.19	-3
15.0	.72	-1	5.2	1.83	-145	-18.2	.123	-111	.15	-26
16.0	.74	-17	4.6	1.70	-177	-18.4	.120	-129	.11	-34

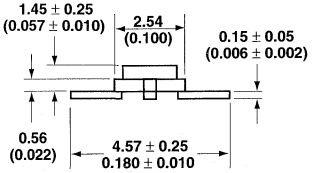
Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 4 V, I_{DS} = 40 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
2.0	.88	-44	13.5	4.73	130	-26.4	.048	64	.67	-28
3.0	.76	-68	13.0	4.47	107	-24.9	.057	52	.61	-39
4.0	.68	-90	12.4	4.19	86	-22.5	.075	39	.57	-46
5.0	.56	-113	12.0	4.00	66	-21.0	.089	32	.52	-52
6.0	.42	-145	11.8	3.90	44	-19.8	.102	21	.44	-61
7.0	.37	161	11.5	3.74	20	-18.6	.117	9	.31	-75
8.0	.47	116	10.5	3.36	-3	-17.9	.128	-5	.17	-95
9.0	.57	90	9.4	2.96	-23	-17.2	.138	-19	.05	-143
10.0	.63	70	8.9	2.77	-41	-17.4	.135	-28	.06	128
11.0	.69	51	7.9	2.47	-63	-17.7	.131	-39	.17	100
12.0	.77	33	7.1	2.26	-82	-18.0	.126	-52	.26	75
13.0	.82	21	6.0	2.00	-101	-18.6	.118	-65	.35	62
14.0	.85	13	5.4	1.86	-117	-19.2	.110	-75	.39	54
15.0	.83	1	4.8	1.73	-134	-19.7	.104	-83	.41	49
16.0	.81	-17	4.4	1.65	-154	-19.8	.102	-103	.42	41

A model for this device is available in the DEVICE MODELS section.

36 micro-X Package Dimensions





Notes:
1. Dimensions are in millimeters (inches)
2. Tolerances: in .xxx = ± 0.005
   mm .xx = ± 0.13

HEWLETT® PACKARD

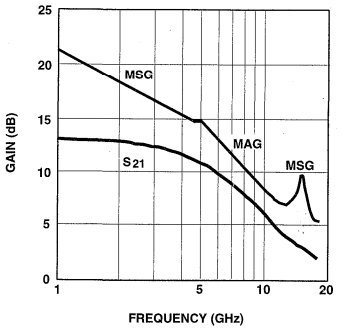
Surface Mount Gallium Arsenide FET for Oscillators

Technical Data

ATF-13786

Features

- **Low Cost Surface Mount Plastic Package**
- **High f_{MAX}:** 60 GHz Typical
- **Low Phase Noise at 10 GHz:** -110 dBc/Hz @ 100 kHz Typical
- **Output Power at 10 GHz:** up to 10 dBm
- **Tape-and-Reel Packaging Option Available**

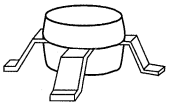


Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency.
V_{DS} = 3 V, I_{DS} = 40 mA.

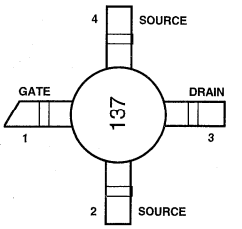
Description

Hewlett-Packard's ATF-13786 is a low cost Gallium Arsenide Schottky barrier-gate field effect transistor housed in a surface mount plastic package. This device is designed for use in low cost, surface mount oscillators operating over the RF and microwave frequency ranges. The ATF-13786 has sufficient gain for easy use as a negative R cell, without excess gain that can lead to unwanted oscillations and mode jumping. The gate structure used in the fabrication of this device results in phase noise performance superior to that of most other MESFETs. These features make this device particularly well suited for low power (< +10 dBm) commercial oscillator applications such as are encountered in DBS, TVRO, and MMDS television receivers, or hand-held transceivers operating in the 900 MHz, 2.4 GHz, and 5.7 GHz ISM bands.

85 mil Plastic Surface Mount Package



Pin Configuration



This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization assure a rugged, reliable device.

ATF-13786 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	4
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-6
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	225
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to +150

Notes:
1. Operation of this device above any one of these conditions may cause permanent damage.
2. T_{CASE} = 25°C (T_{CASE} is defined to be the temperature at the ends of pins 2 and 4 where they contact the circuit board).
3. Derate at 3.1 mW/°C for T_C > 60°C.

Thermal Resistance[2]: θ_{jc} = 325°C/W

ATF-13786 Electrical Specifications, T_C = 25°C, V_{DS} = 3 V, I_{DS} = 40 mA[4]
(unless noted)

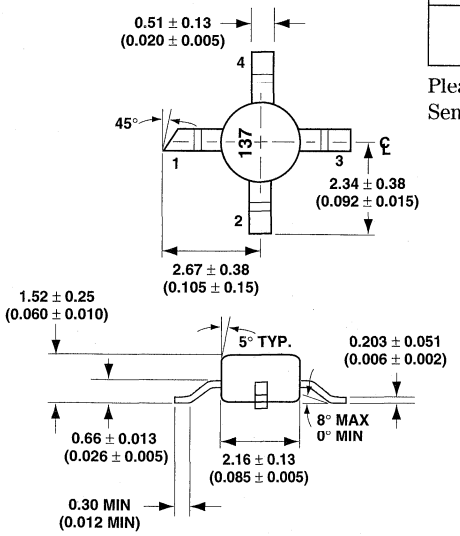
Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21}\|^2$	Insertion Power Gain	f = 10 GHz	dB		6.0	
$P_{1\,dB}$	Power at 1 dB Gain Compression	f = 10 GHz	dBm	15	16.5	
$G_{1\,dB}$	1 dB Compressed Gain	f = 10 GHz	dB	6.5	7.5	
PN	Phase Noise (100 kHz offset)[5]	f = 10 GHz	dBc/Hz		-110	
g_m	Transconductance	V_{DS} = 3 V, V_{GS} = 0 V	mS	25	55	
I_{DSS}	Saturated Drain Current	V_{DS} = 3 V, V_{GS} = 0 V	mA	50	70	100
V_P	Pinchoff Voltage	V_{DS} = 3 V, I_{DS} = 1 mA	V	-2.0	-1.5	-0.5
V_{BDG}	Gate - Drain Breakdown Voltage	I_{DG} = 0.1 mA	V	6.5	7	

Notes:
4. Recommended maximum bias conditions for use as an oscillator.
5. The superior phase noise of this product results from the use of a gate structure optimized for noise performance. Typical performance of 10 GHz parallel resonated, lightly coupled oscillator using high Q dielectric resonator.

Typical Scattering Parameters, Common Source, $Z_O = 50\Omega$, $V_{DS} = 3$ V, $I_{DS} = 40$ mA

Frequency GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
1	0.97	-23	4.80	157	0.03	77	0.46	-13
2	0.88	-46	4.60	135	0.06	66	0.42	-25
3	0.78	-68	4.35	117	0.08	58	0.36	-35
4	0.67	-95	4.02	95	0.11	47	0.28	-48
5	0.57	-125	3.61	75	0.12	37	0.19	-65
6	0.52	-157	3.20	57	0.13	28	0.12	-93
7	0.53	176	2.84	41	0.14	21	0.08	-147
8	0.57	160	2.54	31	0.14	18	0.10	171
9	0.60	143	2.27	16	0.14	12	0.15	148
10	0.63	130	2.04	4	0.15	6	0.19	134
11	0.64	117	1.82	-9	0.14	0	0.25	122
12	0.67	107	1.65	-19	0.14	-4	0.30	113
13	0.72	99	1.55	-29	0.14	-8	0.35	109
14	0.76	97	1.47	-35	0.14	-9	0.39	111
15	0.78	90	1.40	-46	0.14	-14	0.41	108
16	0.77	83	1.32	-58	0.14	-20	0.42	104
17	0.74	77	1.26	-68	0.14	-28	0.43	98
18	0.73	69	1.23	-80	0.14	-36	0.42	93

85 mil Plastic Surface Mount Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Part Number Ordering Information

Part Number	Devices per Reel	Reel Size
ATF-13786-TR1	1000	7"
ATF-13786-STR	10	strip

Please refer to the "Tape-and-Reel Packaging for Surface Mount Semiconductors" data sheet for more detailed information.

0.5–6 GHz Low Noise Gallium Arsenide FET

Technical Data

ATF-21170

Features

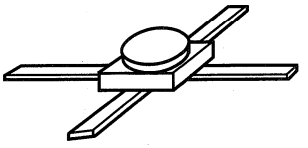
- **Low Noise Figure:** 0.9 dB Typical at 4 GHz
- **High Associated Gain:** 13.0 dB Typical at 4 GHz
- **High Output Power:** 23.0 dBm Typical $P_{1\,dB}$ at 4 GHz
- **Hermetic Gold-Ceramic Microstrip Package**

Description

The ATF-21170 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. This device is designed for use in low noise or medium power amplifier applications in the 0.5-6 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 750 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

70 mil Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 20 mA	f = 2.0 GHz	dB		0.6	
		f = 4.0 GHz	dB		0.9	1.1
		f = 6.0 GHz	dB		1.2	
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 20 mA	f = 2.0 GHz	dB		16.0	
		f = 4.0 GHz	dB	12.0	13.0	
		f = 6.0 GHz	dB		10.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} =5 V, I_{DS} = 80 mA	f = 4.0 GHz	dBm		23.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 5 V, I_{DS} = 80 mA	f = 4.0 GHz	dB		13.0	
g_m	Transconductance: V_{DS} =3 V, V_{GS} = 0 V		mmho	70	120	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	80	120	200
V_P	Pinch-off Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	-3.0	-1.5	-0.8

ATF-21170 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+7
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-8
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	600
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 250°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 µm Spot Size[4]

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 4 mW/°C for T_{CASE} > 25°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

ATF-21170 Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Γ_{opt}		$R_N/50$
		Mag	Ang	
0.5	0.4	.93	17	.90
1.0	0.5	.85	35	.70
2.0	0.6	.70	70	.46
4.0	0.9	.59	148	.14
8.0	1.2	.54	-177	.09

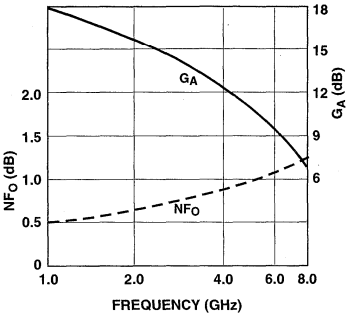


Figure 1. Optimum Noise Figure and Associated Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 20 mA, T_A = 25°C.

ATF-21170 Typical Performance, T_A = 25°C

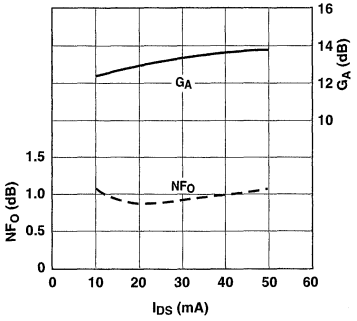


Figure 2. Optimum Noise Figure and Associated Gain vs. I_{DS}. V_{DS} = 3 V, f = 4.0 GHz.

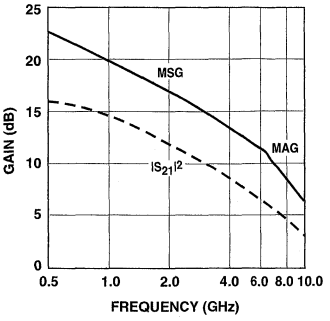


Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 20 mA.

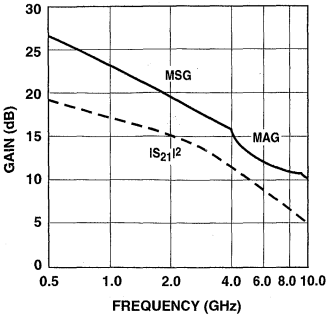


Figure 4. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 5 V, I_{DS} = 80 mA.

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 3 V, I_{DS} = 20 mA

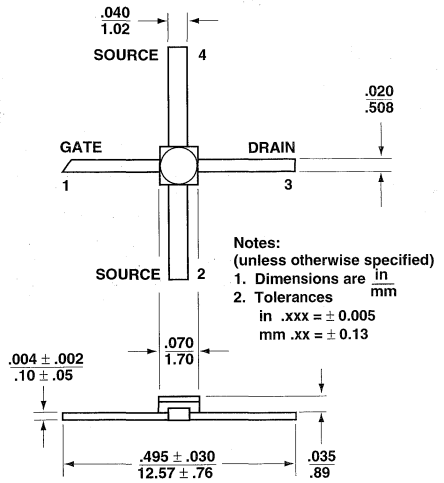
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.96	-31	15.5	5.93	157	-29.4	.034	72	.46	-23
1.0	.91	-55	14.2	5.14	137	-24.3	.061	56	.42	-42
2.0	.82	-95	12.1	4.05	106	-20.4	.096	36	.39	-70
3.0	.74	-123	10.2	3.23	82	-19.5	.106	21	.35	-91
4.0	.70	-147	8.8	2.74	61	-18.7	.116	9	.33	-109
5.0	.65	-170	7.3	2.33	41	-18.2	.123	-1	.30	-127
6.0	.64	167	6.3	2.07	22	-17.7	.131	-10	.29	-145
7.0	.65	146	5.4	1.86	4	-17.5	.134	-17	.26	-167
8.0	.66	126	4.5	1.67	-13	-17.0	.141	-28	.26	164
9.0	.66	107	3.4	1.48	-30	-16.6	.148	-39	.26	140
10.0	.67	87	2.2	1.29	-47	-16.2	.155	-50	.25	114

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 5 V, I_{DS} = 80 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.95	-43	18.3	8.24	149	-32.4	.024	67	.49	-17
1.0	.89	-64	17.4	7.28	133	-29.9	.032	59	.46	-26
2.0	.78	-106	14.6	5.36	101	-25.2	.055	44	.40	-45
3.0	.69	-133	12.4	4.18	79	-23.4	.068	34	.38	-60
4.0	.64	-160	10.7	3.42	56	-22.7	.073	31	.36	-81
5.0	.60	175	9.1	2.85	37	-21.7	.082	24	.35	-100
6.0	.61	154	7.9	2.47	18	-20.4	.095	19	.33	-115
7.0	.61	136	6.9	2.22	2	-19.3	.108	12	.31	-132
8.0	.63	120	6.2	2.05	-14	-17.9	.127	7	.27	-152
9.0	.64	102	5.3	1.85	-32	-16.6	.148	0	.27	-179
10.0	.64	86	4.5	1.68	-48	-15.3	.172	-13	.29	165

A model for this device is available in the DEVICE MODELS section.

70 mil Package Dimensions



HEWLETT® PACKARD

0.5–6 GHz General Purpose Gallium Arsenide FET

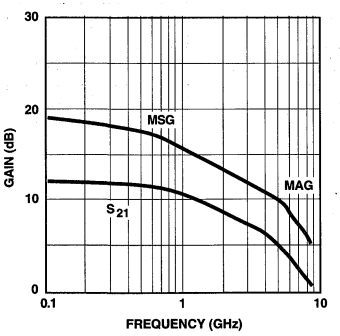
Technical Data

ATF-21186

Features

- **Low Noise Figure:** 0.5 dB Typ. @ 2 GHz
- **High Output Power:** 19 dBm Typ. P_{1dB} @ 2 GHz
- **High MSG:** 13.5 dB Typ. @ 2 GHz
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Note:
1. Refer to "Tape-and-Reel Packaging for Surface Mount Semiconductors".

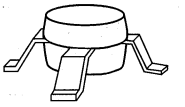


ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 15 mA.

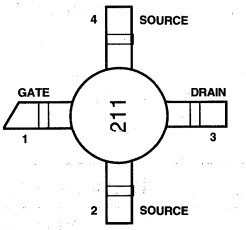
Description

Hewlett–Packard's ATF-21186 is a low cost Gallium Arsenide Schottky barrier-gate field effect transistor housed in a surface mount plastic package. This general purpose device is designed for use in low noise amplifiers, gain stages, driver amplifiers, and oscillators operating over the VHF, UHF, and microwave frequency ranges. High gain with two volt operation makes this part attractive for low voltage, battery operated systems. The low noise figure is appropriate for commercial systems demanding good sensitivity, such as GPS receiver front-ends and MMDS television receivers. The output power is sufficient for use as the driver stage in many hand-held transceivers operating in the 900 MHz through 2.4 GHz bands, including in cellular phones, PCN, and ISM band spread spectrum applications.

85 mil Plastic Surface Mount Package



Pin Configuration



This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 750 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

ATF-21186 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	5
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-6
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	400
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to +150

Thermal Resistance[2]: θ_{jc} = 225°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C (T_{CASE} is defined to be the temperature at the ends of pins 2 and 4 where they contact the circuit board).
3. Derate at 4.4 mW/°C for T_C > 60°C.

ATF-21186 Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_o	Optimum Noise Figure	f = 1 GHz	dB		0.4	
	V_{DS} = 2 V, I_{DS} = 15 mA	f = 2 GHz			0.5	0.75
		f = 4 GHz			0.6	
G_A	Associated Gain	f = 1 GHz	dB		14.2	
	V_{DS} = 2 V, I_{DS} = 15 mA	f = 2 GHz		12.0	12.6	
		f = 4 GHz			9.1	
$P_{1\,dB}$	Power at 1 dB Gain Compression	f = 1 GHz	dBm		19.0	
	V_{DS} = 3 V, I_{DS} = 70 mA	f = 2 GHz			19.0	
		f = 4 GHz			18.0	
$G_{1\,dB}$	1 dB Compressed Gain	f = 1 GHz	dB		18.0	
	V_{DS} = 3 V, I_{DS} = 70 mA	f = 2 GHz			14.0	
		f = 4 GHz			8.5	
g_m	Transconductance	V_{DS} = 3 V, V_{GS} = 0 V	mS	70	120	
I_{DSS}	Saturated Drain Current	V_{DS} = 3 V, V_{GS} = 0 V	mA	80	120	200
V_P	Pinchoff Voltage	V_{DS} = 3 V, I_{DS} = 1 mA	V	-3.0	-1.5	-0.8

ATF-21186 Typical Performance, T_A = 25°C

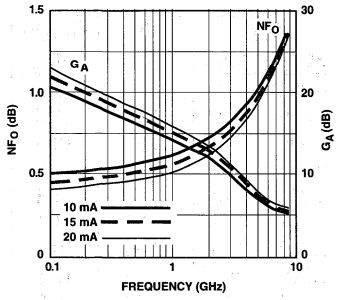


Figure 1. ATF-21186 Optimum Noise Figure and Associated Gain vs. Frequency and I_{DS}, V_{DS} = 2 V.

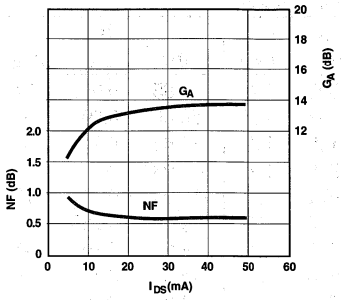


Figure 2. ATF-21186 Optimum Noise Figure and Associated Gain vs. I_{DS}, f = 2 GHz, V_{DS} = 2 V.

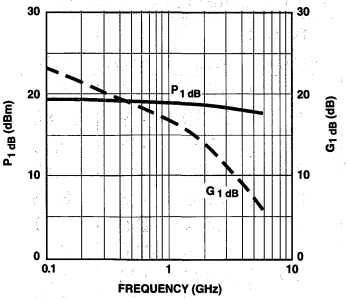


Figure 3. ATF-21186 Power Output at 1 dB Compression and 1 dB Compressed Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 70 mA.

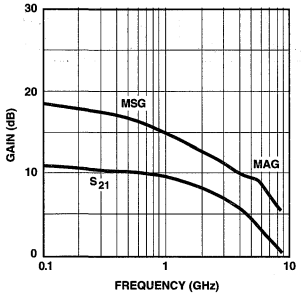


Figure 4. ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 10 mA.

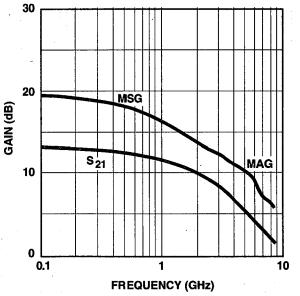


Figure 5. ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 20 mA.

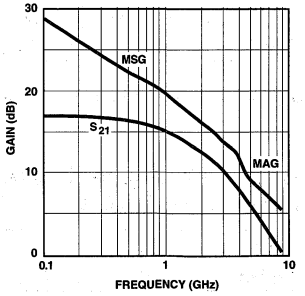


Figure 6. ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 70 mA.

ATF-21186 Typical Scattering Parameters,

Common Source, Z_o = 50 Ω, V_{DS} = 2 V, I_{DS} = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K	G_{max}[1]
(GHz)	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	—	(dB)
0.5	0.961	-25	11.12	3.599	157	-25.85	0.051	71	0.376	-25	0.22	18.5
1.0	0.910	-49	10.60	3.388	137	-20.36	0.096	57	0.360	-50	0.27	15.5
1.5	0.851	-73	9.96	3.149	118	-17.66	0.131	43	0.339	-73	0.33	13.8
2.0	0.794	-95	9.27	2.906	100	-16.03	0.158	31	0.314	-95	0.40	12.6
2.5	0.743	-118	8.53	2.671	83	-15.04	0.177	19	0.291	-118	0.47	11.8
3.0	0.694	-139	7.71	2.429	67	-14.52	0.188	9	0.272	-143	0.57	11.1
3.5	0.659	-160	6.85	2.201	52	-14.29	0.193	-1	0.270	-169	0.66	10.6
4.0	0.643	180	5.97	1.989	37	-14.29	0.193	-9	0.290	167	0.75	10.1
4.5	0.643	161	5.05	1.789	24	-14.38	0.191	-17	0.324	148	0.83	9.7
5.0	0.658	143	4.12	1.606	11	-14.66	0.185	-24	0.367	133	0.90	9.4
5.5	0.682	128	3.16	1.438	-1	-14.94	0.179	-29	0.410	121	0.95	9.0
6.0	0.707	115	2.19	1.286	-12	-15.29	0.172	-34	0.453	111	1.00	8.7
6.5	0.735	104	1.25	1.155	-23	-15.55	0.167	-38	0.490	102	1.02	7.5
7.0	0.758	95	0.32	1.038	-33	-15.81	0.162	-41	0.526	94	1.05	6.7
7.5	0.780	86	-0.59	0.934	-42	-15.97	0.159	-44	0.559	85	1.08	6.0
8.0	0.801	77	-1.49	0.842	-51	-16.08	0.157	-47	0.595	78	1.08	5.6

Note:

1. G_{max} = MAG for K ≥ 1 and G_{max} = MSG for K < 1

ATF-21186 Typical Noise Parameters,

Common Source, Z_o = 50 Ω, V_{DS} = 2 V, I_D = 10 mA

Frequency	F_{min}	Γ_{opt}		$R_n/50$	G_a
GHz	dB	Mag.	Ang.	—	dB
0.5	0.37	0.95	11	1.738	13.8
1.0	0.41	0.89	25	0.819	12.3
1.5	0.45	0.84	42	0.553	11.4
2.0	0.49	0.79	60	0.387	11.1
2.5	0.53	0.74	79	0.265	10.4
3.0	0.57	0.71	100	0.179	10.0
3.5	0.61	0.68	120	0.111	9.2
4.0	0.65	0.66	142	0.057	8.7
4.5	0.69	0.64	162	0.028	7.9
5.0	0.73	0.65	-175	0.021	7.4
5.5	0.77	0.68	-155	0.042	7.1
6.0	0.81	0.73	-139	0.095	6.6
6.5	0.85	0.77	-123	0.202	6.4
7.0	0.89	0.81	-111	0.362	6.1
7.5	0.93	0.84	-98	0.596	5.8
8.0	0.97	0.86	-88	0.873	5.4

ATF-21186 Typical Scattering Parameters,

Common Source, Z_o = 50 Ω, V_{DS} = 2 V, I_{DS} = 15 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K	G_{max}[1]
(GHz)	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	—	(dB)
0.5	0.957	-27	12.56	4.248	156	-26.38	0.048	71	0.303	-28	0.22	19.5
1.0	0.898	-53	11.95	3.959	136	-21.11	0.088	57	0.291	-57	0.29	16.5
1.5	0.833	-77	11.19	3.627	116	-18.42	0.120	44	0.277	-82	0.37	14.8
2.0	0.772	-100	10.37	3.300	99	-16.89	0.143	32	0.261	-106	0.45	13.6
2.5	0.721	-123	9.52	2.992	82	-15.86	0.161	22	0.251	-132	0.53	12.7
3.0	0.675	-145	8.59	2.689	66	-15.34	0.171	12	0.247	-158	0.63	12.0
3.5	0.646	-165	7.65	2.413	51	-15.04	0.177	3	0.261	177	0.73	11.3
4.0	0.636	175	6.71	2.164	37	-14.90	0.180	-4	0.292	156	0.81	10.8
4.5	0.642	156	5.74	1.936	24	-14.90	0.180	-11	0.334	139	0.88	10.3
5.0	0.660	139	4.76	1.730	11	-14.99	0.178	-17	0.380	125	0.94	9.9
5.5	0.685	124	3.78	1.545	0	-15.09	0.176	-23	0.424	114	0.98	9.4
6.0	0.712	112	2.80	1.380	-11	-15.24	0.173	-27	0.466	106	1.01	8.5
6.5	0.739	102	1.86	1.239	-21	-15.39	0.170	-32	0.502	97	1.03	7.6
7.0	0.762	92	0.94	1.114	-31	-15.49	0.168	-36	0.537	89	1.04	6.9
7.5	0.783	84	0.04	1.005	-40	-15.55	0.167	-39	0.567	81	1.06	6.3
8.0	0.803	75	-0.84	0.908	-49	-15.60	0.166	-44	0.601	74	1.06	5.9

Note:

1. G_{max} = MAG for K ≥ 1 and G_{max} = MSG for K < 1

ATF-21186 Typical Noise Parameters,

Common Source, Z_o = 50 Ω, V_{DS} = 2 V, I_D = 15 mA

Frequency	F_{min}	Γ_{opt}		$R_n/50$	G_a
GHz	dB	Mag.	Ang.	—	dB
0.5	0.35	0.950	13	1.633	15.8
1.0	0.39	0.870	27	0.639	14.2
1.5	0.43	0.810	45	0.420	13.4
2.0	0.46	0.760	63	0.302	12.6
2.5	0.50	0.710	82	0.209	11.7
3.0	0.54	0.670	102	0.138	10.8
3.5	0.57	0.635	121	0.088	9.8
4.0	0.61	0.614	143	0.047	9.1
4.5	0.64	0.605	165	0.025	8.5
5.0	0.68	0.612	-172	0.022	8.0
5.5	0.72	0.650	-152	0.042	7.6
6.0	0.75	0.696	-136	0.088	7.2
6.5	0.79	0.742	-121	0.174	7.0
7.0	0.83	0.782	-109	0.301	6.6
7.5	0.86	0.810	-96	0.471	6.3
8.0	0.90	0.840	-86	0.715	6.0

ATF-21186 Typical Scattering Parameters,

Common Source, Z_o = 50 Ω, V_{DS} = 2 V, I_{DS} = 20 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K	G_{max}[1]
(GHz)	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	—	(dB)
0.5	0.955	-29	13.44	4.698	156	-26.75	0.046	71	0.251	-32	0.23	20.1
1.0	0.888	-55	12.75	4.340	134	-21.51	0.084	57	0.246	-63	0.31	17.1
1.5	0.819	-80	11.91	3.938	115	-18.86	0.114	44	0.240	-91	0.40	15.4
2.0	0.756	-104	11.00	3.547	97	-17.33	0.136	33	0.233	-117	0.49	14.2
2.5	0.704	-127	10.07	3.186	80	-16.36	0.152	23	0.233	-143	0.58	13.2
3.0	0.662	-149	9.07	2.840	65	-15.76	0.163	14	0.242	-169	0.67	12.4
3.5	0.638	-170	8.07	2.532	50	-15.39	0.170	6	0.266	168	0.77	11.7
4.0	0.633	171	7.07	2.257	37	-15.19	0.174	-1	0.304	148	0.85	11.1
4.5	0.643	153	6.07	2.012	24	-15.14	0.175	-7	0.349	133	0.91	10.6
5.0	0.663	136	5.07	1.793	12	-15.09	0.176	-13	0.397	121	0.96	10.1
5.5	0.690	122	4.07	1.597	0	-15.14	0.175	-19	0.441	111	0.99	9.6
6.0	0.717	110	3.08	1.425	-10	-15.19	0.174	-24	0.482	103	1.01	8.4
6.5	0.744	100	2.14	1.280	-20	-15.24	0.173	-28	0.517	95	1.02	7.7
7.0	0.767	91	1.22	1.151	-29	-15.29	0.172	-33	0.550	87	1.04	7.1
7.5	0.788	83	0.34	1.040	-38	-15.29	0.172	-37	0.579	79	1.04	6.5
8.0	0.807	74	-0.54	0.940	-47	-15.34	0.171	-41	0.611	72	1.05	6.1

Note:

1. G_{max} = MAG for K ≥ 1 and G_{max} = MSG for K < 1

ATF-21186 Typical Noise Parameters,

Common Source, Z_o = 50 Ω, V_{DS} = 2 V, I_D = 20 mA

Frequency	F_{min}	Γ_{opt}		$R_n/50$	G_a
GHz	dB	Mag.	Ang.	—	dB
0.5	0.33	0.95	13	1.543	16.1
1.0	0.37	0.88	28	0.659	14.6
1.5	0.41	0.82	46	0.423	13.8
2.0	0.45	0.77	64	0.294	12.8
2.5	0.48	0.70	83	0.191	12.0
3.0	0.52	0.65	103	0.124	11.0
3.5	0.56	0.62	123	0.079	10.0
4.0	0.59	0.60	146	0.042	9.4
4.5	0.63	0.59	168	0.024	8.7
5.0	0.67	0.60	-170	0.023	8.2
5.5	0.70	0.64	-150	0.044	7.7
6.0	0.74	0.68	-134	0.089	7.3
6.5	0.78	0.73	-118	0.176	7.0
7.0	0.81	0.77	-107	0.289	6.6
7.5	0.85	0.80	-96	0.446	6.3
8.0	0.89	0.83	-84	0.654	5.9

ATF-21186 Typical Scattering Parameters,

Common Source, Z_o = 50 Ω, V_{DS} = 3 V, I_{DS} = 70 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K	G_{max}[1]
(GHz)	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	—	(dB)
0.5	0.933	-34	17.12	7.181	152	-28.64	0.037	71	0.240	-34	0.28	22.9
1.0	0.841	-65	16.05	6.348	129	-23.74	0.065	57	0.222	-66	0.41	19.9
1.5	0.755	-92	14.80	5.493	109	-21.21	0.087	46	0.204	-93	0.53	18.0
2.0	0.688	-117	13.54	4.755	91	-19.74	0.103	38	0.188	-118	0.64	16.6
2.5	0.643	-140	12.33	4.135	75	-18.64	0.117	30	0.182	-145	0.73	15.5
3.0	0.613	-161	11.14	3.607	61	-17.92	0.127	23	0.186	-171	0.82	14.5
3.5	0.601	179	10.01	3.167	47	-17.33	0.136	17	0.209	165	0.91	13.7
4.0	0.608	161	8.94	2.799	35	-16.77	0.145	11	0.247	146	0.96	12.9
4.5	0.628	145	7.89	2.480	23	-16.36	0.152	6	0.293	131	0.99	12.1
5.0	0.657	130	6.85	2.201	11	-16.03	0.158	0	0.342	120	1.02	10.7
5.5	0.689	116	5.84	1.959	0	-15.76	0.163	-5	0.390	110	1.02	9.9
6.0	0.720	106	4.85	1.748	-10	-15.60	0.166	-11	0.434	103	1.03	9.2
6.5	0.750	96	3.90	1.567	-19	-15.39	0.170	-16	0.474	95	1.02	8.9
7.0	0.774	88	2.98	1.410	-29	-15.24	0.173	-21	0.510	87	1.01	8.4
7.5	0.797	80	2.08	1.271	-38	-15.09	0.176	-26	0.542	79	1.01	8.1
8.0	0.817	72	1.22	1.151	-46	-14.99	0.178	-31	0.578	72	1.00	8.1

Note:

1. G_{max} = MAG for K ≥ 1 and G_{max} = MSG for K < 1

ATF-21186 Typical Noise Parameters,

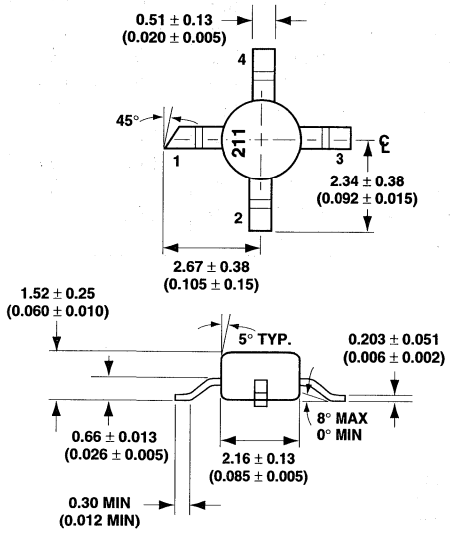
Common Source, Z_o = 50 Ω, V_{DS} = 3 V, I_D = 70 mA

Frequency	F_{min}	Γ_{opt}		$R_n/50$	G_a
GHz	dB	Mag.	Ang.	—	dB
0.5	0.40	0.94	16	1.510	19.5
1.0	0.44	0.84	34	0.565	18.0
1.5	0.49	0.74	53	0.322	16.5
2.0	0.54	0.67	72	0.223	15.0
2.5	0.59	0.61	92	0.153	13.7
3.0	0.63	0.57	115	0.098	12.7
3.5	0.68	0.55	137	0.060	11.7
4.0	0.73	0.54	162	0.034	11.0
4.5	0.78	0.55	-175	0.029	10.3
5.0	0.82	0.59	-155	0.045	9.6
5.5	0.87	0.63	-136	0.092	9.2
6.0	0.92	0.68	-121	0.167	8.7
6.5	0.97	0.73	-109	0.282	8.4
7.0	1.01	0.78	-98	0.466	8.0
7.5	1.06	0.82	-87	0.738	7.6
8.0	1.11	0.85	-78	1.089	7.3

Part Number Ordering Information

Part Number	Devices per Reel	Reel Size
ATF-21186-TR1	1000	7"
ATF-21186-STR	10	strip

85 mil Plastic Surface Mount Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

0.5–10 GHz Low Noise Gallium Arsenide FET

Technical Data

ATF-25170

Features

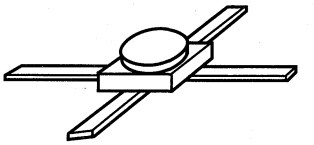
- **Low Noise Figure:** 0.8 dB Typical at 4 GHz
- **High Associated Gain:** 14.0 dB Typical at 4 GHz
- **High Output Power:** 21.0 dBm Typical $P_{1\,dB}$ at 4 GHz
- **Hermetic Gold-Ceramic Microstrip Package**

Description

The ATF-25170 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. Its noise figure makes this device appropriate for use in low noise amplifiers operating in the 0.5-10 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

70 mil Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 20 mA	f = 4.0 GHz	dB		0.8	1.0
		f = 6 0 GHz	dB		1.0	
		f = 8.0 GHz	dB		1.2	
G_A	Gain @ NF_O: V_{DS} =3 V, I_{DS} = 20 mA	f = 4.0 GHz	dB	13.0	14.0	
		f = 6.0 GHz	dB		11.5	
		f = 8.0 GHz	dB		9.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} =5 V, I_{DS} =50 mA	f = 4.0 GHz	dBm		21.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} =5 V, I_{DS} =50 mA	f = 4.0 GHz	dB		15.0	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	50	80	
I_{DSS}	Saturated Drain Current: V_{DS} =3 V, V_{GS} = 0 V		mA	50	100	150
V_P	Pinch-off Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	-3.0	-2.0	-0.8

ATF-25170 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+7
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-8
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	450
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 300°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[4]

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 3.3 mW/°C for $T_{MOUNTING\ SURFACE}$ >40°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

ATF-25170 Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Γ_{opt}		$R_N/50$
		Mag	Ang	
1.0	0.6	.89	24	.78
2.0	0.7	.77	50	.53
4.0	0.8	.63	105	.33
6.0	1.0	.66	147	.06
8.0	1.2	.62	-159	.11

ATF-25170 Typical Performance, T_A = 25°C

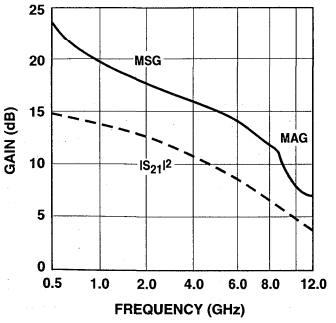


Figure 1. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 20 mA.

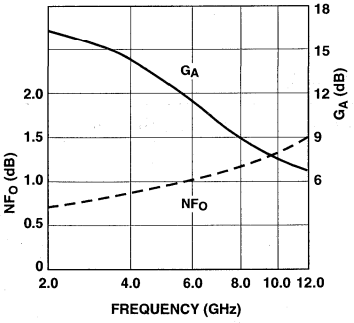


Figure 2. Optimum Noise Figure and Associated Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 20 mA.

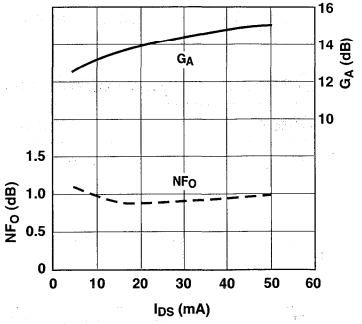


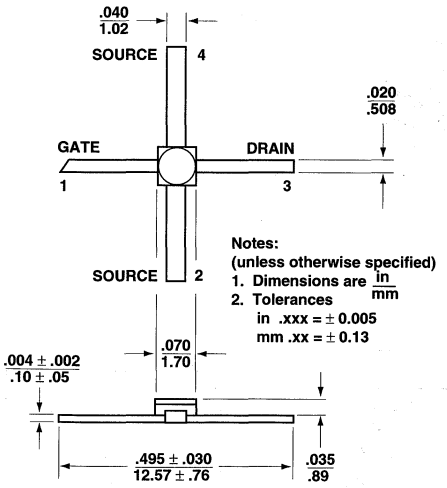
Figure 3. Optimum Noise Figure and Associated Gain vs. I_{DS}. V_{DS} = 3 V, f = 4.0 GHz.

Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{DS} = 3$ V, $I_{DS} = 20$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.98	-23	13.6	4.80	160	-32.8	.023	76	.50	-23
1.0	.96	-38	13.0	4.46	147	-23.6	.037	67	.48	-30
2.0	.88	-66	11.5	3.75	121	-23.6	.066	50	.44	-45
3.0	.80	-86	10.2	3.23	102	-21.8	.081	41	.41	-55
4.0	.77	-106	9.3	2.93	82	-19.7	.103	28	.38	-65
5.0	.71	-127	8.5	2.66	62	-18.6	.118	17	.35	-78
6.0	.65	-149	7.9	2.47	42	-17.7	.130	6	.30	-93
7.0	.60	-173	7.3	2.33	24	-16.5	.149	-4	.26	-111
8.0	.56	161	6.8	2.20	5	-15.8	.162	-16	.22	-134
9.0	.56	136	6.2	2.05	-14	-15.1	.175	-26	.21	-166
10.0	.55	118	5.4	1.87	-31	-15.0	.178	-35	.21	173
11.0	.53	108	4.9	1.76	-46	-14.9	.180	-42	.22	164
12.0	.53	95	4.7	1.71	-62	-14.8	.183	-52	.23	159

A model for this device is available in the DEVICE MODELS section.

70 mil Package Dimensions



0.5 – 10 GHz General Purpose Gallium Arsenide FET

Technical Data

ATF-25570

Features

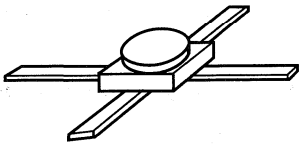
- **High Output Power:** 20.5 dBm Typical $P_{1\,dB}$ at 4 GHz
- **Low Noise Figure:** 1.0 dB Typical at 4 GHz
- **High Associated Gain:** 14.0 dB Typical at 4 GHz
- **Hermetic Gold-Ceramic Microstrip Package**

Description

The ATF-25570 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. This device is designed for use in general purpose amplifier and oscillator applications in the 0.5-10 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

70 mil Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 20 mA	f = 4.0 GHz	dB		1.0	1.3
		f = 6.0 GHz			1.2	
		f = 8.0 GHz			1.4	
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 20 mA	f = 4.0 GHz	dB	13.0	14.0	
		f = 6.0 GHz			11.0	
		f = 8.0 GHz			8.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} =5 V, I_{DS} = 50 mA	f = 4.0 GHz	dBm		20.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} =5 V, I_{DS} =50 mA	f = 4.0 GHz	dB		13.0	
g_m	Transconductance: V_{DS} =3 V, V_{GS} = 0 V		mmho	50	80	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	50	100	150
V_P	Pinch-off Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	-3.0	-2.0	-0.8

ATF-25570 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+7
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-8
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	450
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 300°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[4]

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 3.3 mW/°C for T_{CASE} > 40°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

ATF-25570 Typical Performance, T_A = 25°C

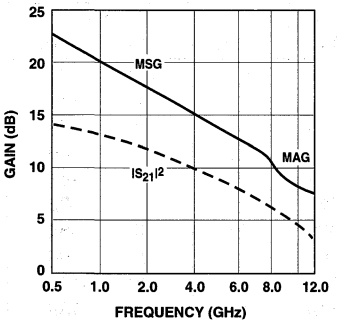


Figure 1. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 20 mA.

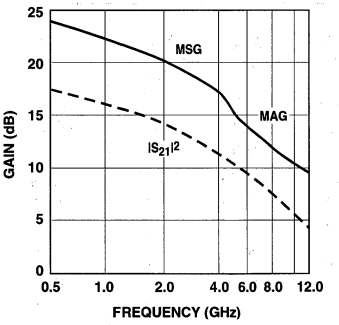


Figure 2. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 5 V, I_{DS} = 50 mA.

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 3 V, I_{DS} = 20 mA

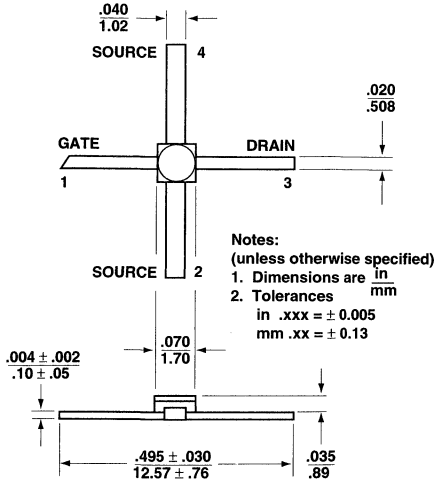
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.98	-24	14.0	5.02	160	-28.9	.036	71	.56	-24
1.0	.96	-41	13.4	4.70	145	-26.2	.049	62	.55	-33
2.0	.84	-76	12.3	4.14	115	-22.5	.075	44	.49	-51
3.0	.78	-100	10.8	3.48	94	-20.9	.090	33	.46	-60
4.0	.72	-123	9.6	3.01	73	-19.8	.102	20	.42	-76
5.0	.68	-142	8.5	2.67	54	-18.8	.114	9	.38	-88
6.0	.63	-162	7.8	2.45	36	-18.3	.121	0	.35	-101
7.0	.60	175	7.2	2.30	18	-17.5	.133	-7	.30	-118
8.0	.58	150	6.3	2.06	-1	-17.0	.141	-16	.26	-138
9.0	.59	128	5.6	1.90	-19	-16.7	.146	-28	.25	-167
10.0	.60	113	4.7	1.72	-36	-16.4	.151	-35	.26	172
11.0	.60	104	4.1	1.61	-48	-16.1	.157	-40	.28	155
12.0	.59	91	3.9	1.56	-68	-15.9	.160	-44	.30	146

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 5 V, I_{DS} = 50 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.97	-27	16.2	6.49	156	-32.0	.025	63	.59	-21
1.0	.94	-45	15.5	5.95	141	-29.9	.032	57	.60	-28
2.0	.81	-82	13.5	4.72	111	-26.2	.049	45	.58	-39
3.0	.73	-105	11.7	3.86	91	-24.9	.057	41	.55	-50
4.0	.66	-128	10.3	3.29	70	-23.4	.068	37	.52	-62
5.0	.61	-148	9.2	2.88	52	-22.5	.075	32	.49	-72
6.0	.57	-170	8.5	2.65	34	-21.6	.083	30	.48	-84
7.0	.56	167	7.6	2.41	16	-20.2	.097	28	.45	-98
8.0	.57	145	6.8	2.19	-1	-19.2	.110	18	.42	-115
9.0	.59	127	6.0	2.00	-18	-18.5	.119	12	.40	-136
10.0	.60	115	5.2	1.82	-35	-17.8	.129	4	.40	-159
11.0	.60	108	4.7	1.72	-47	-17.5	.134	1	.42	-176
12.0	.57	93	4.5	1.67	-64	-16.9	.143	-10	.44	173

A model for this device is available in the DEVICE MODELS section.

70 mil Package Dimensions



0.5–10 GHz General Purpose Gallium Arsenide FET

Technical Data

ATF-25735

Features

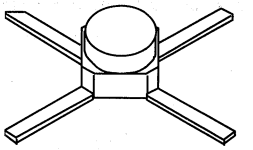
- **High Output Power:** 19.0 Bm Typical $P_{1\,dB}$ at 4 GHz
- **High Gain:** 12.5 dB Typical $G_{1\,dB}$ at 4 GHz
- **Low Noise Figure:** 1.2 dB Typical at 4 GHz
- **Cost Effective Ceramic Microstrip Package**

Description

The ATF-25735 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. This device is designed for use in general purpose amplifier and oscillator applications in the 0.5-10 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

35 micro-X Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 20 mA	f = 2. 0 GHz	dB		1.0	
		f = 4.0 GHz			1.2	1.5
		f = 6.0 GHz			1.4	
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 20 mA	f = 2.0 GHz	dB		15.0	
		f = 4.0 GHz		11.5	13.0	
		f =.6.0 GHz			10.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} =5 V, I_{DS} = 50 mA	f = 4.0 GHz	dBm		19.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 5 V, I_{DS} =50 mA	f = 4.0 GHz	dB		12.5	
g_m	Transconductance: V_{DS} =3 V, V_{GS} = 0 V		mmho	50	80	
I_{DSS}	Saturated Drain Current: V_{DS} =3 V, V_{GS} = 0 V		mA	50	100	150
V_P	Pinch-off Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	-3.0	-2.0	-0.8

ATF-25735 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+7
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-8
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	450
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature[4]	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 325°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[5]

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 3 mW/°C for T_{CASE} > 29°C.
4. Storage above +150°C may tarnish the leads of this package difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

ATF-25735 Typical Performance, T_A = 25°C

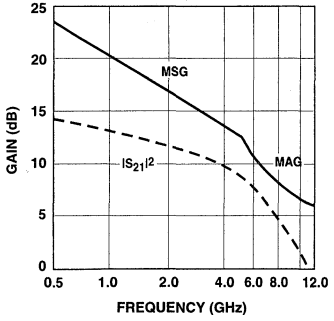


Figure 1. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 20 mA.

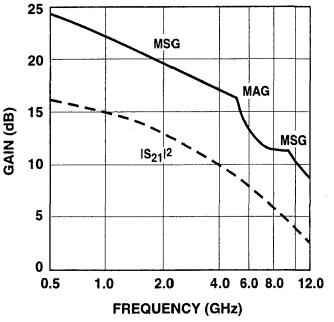


Figure 2. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 5 V, I_{DS} = 50 mA.

Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{DS} = 3$ V, $I_{DS} = 20$ mA

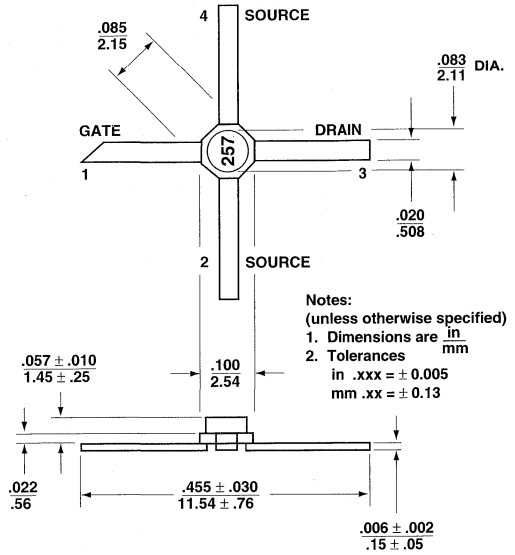
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.98	-22	13.9	4.95	159	-32.0	.025	77	.52	-12
1.0	.94	-45	13.3	4.61	142	-27.1	.044	64	.52	-20
2.0	.85	-82	12.2	4.06	110	-21.6	.083	45	.46	-41
3.0	.70	-116	11.0	3.54	81	-19.3	.109	24	.38	-61
4.0	.58	-152	10.0	3.17	54	-17.7	.131	12	.35	-81
5.0	.50	165	8.9	2.78	27	-16.7	.146	-7	.29	-97
6.0	.52	122	7.7	2.43	1	-16.1	.156	-20	.18	-112
7.0	.59	90	6.3	2.06	-23	-15.8	.162	-34	.07	-161
8.0	.65	66	5.1	1.79	-43	-15.5	.167	-46	.09	107
9.0	.69	44	3.8	1.55	-63	-15.3	.172	-53	.15	76
10.0	.73	32	2.7	1.36	-82	-15.4	.170	-65	.18	53
11.0	.79	20	1.1	1.14	-100	-15.5	.168	-78	.21	24
12.0	.84	7	-0.2	.98	-119	-15.7	.161	-93	.26	-5

Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{DS} = 5$ V, $I_{DS} = 50$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	.93	-21	16.0	6.29	156	-34.0	.020	69	.56	-10
1.0	.88	-42	15.4	5.89	140	-29.6	.033	62	.53	-21
2.0	.78	-81	14.1	5.08	108	-24.4	.060	49	.47	-43
3.0	.65	-112	12.6	4.27	83	-22.6	.074	39	.44	-55
4.0	.55	-142	11.4	3.73	58	-21.0	.089	28	.41	-64
5.0	.48	-176	10.6	3.37	36	-19.7	.104	20	.37	-69
6.0	.47	142	9.7	3.04	10	-18.3	.122	6	.28	-83
7.0	.56	104	8.4	2.64	-14	-17.5	.134	-6	.14	-105
8.0	.65	80	7.0	2.25	-35	-16.7	.146	-17	.07	172
9.0	.73	61	5.8	1.94	-53	-16.1	.157	-26	.14	113
10.0	.78	47	4.7	1.71	-72	-15.4	.169	-40	.20	94
11.0	.80	34	3.6	1.51	-90	-15.1	.176	-53	.27	68
12.0	.85	18	2.7	1.36	-109	-14.8	.181	-64	.36	45

A model for this device is available in the DEVICE MODELS section.

35 micro-X Package Dimensions



HEWLETT® PACKARD

2–16 GHz General Purpose Gallium Arsenide FET

Technical Data

ATF-26836

Features

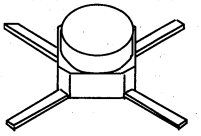
- **High Output Power:** 18.0 dBm Typical $P_{1\,dB}$ at 12 GHz
- **High Gain:** 9.0 dB Typical G_{SS} at 12 GHz
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

The ATF-26836 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. This device is designed for use in oscillator applications and general purpose amplifier applications in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G_{SS}	Tuned Small Signal Gain: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dB	7.0	9.0	
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 10 mA	f = 12.0 GHz	dB		2.2	
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 10 mA	f = 12.0 GHz	dB		6.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dBm	15.0	18.0	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	15	35	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	30	50	90
V_P	Pinch-off Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	-3.5	-1.5	-0.5

Note:

1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors."

ATF-26836 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+7
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-8
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	275
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature[4]	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 350°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[5]

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 2.9 mW/°C for T_{CASE} >79°C.
4. Storage above +150°C may tarnish the leads of this package difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-26836-TR1	1000	7"
ATF-26836-STR	10	strip

ATF-26836 Typical Performance, T_A = 25°C

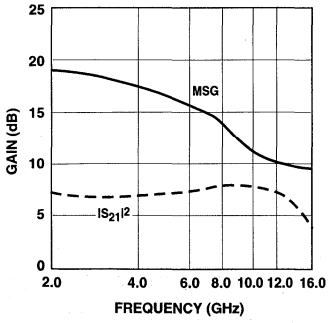


Figure 1. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 5 V, I_{DS} = 30 mA.

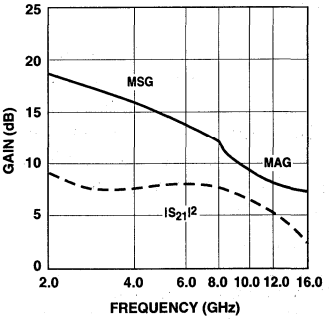


Figure 2. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 10 mA.

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 3 V, I_{DS} = 10 mA

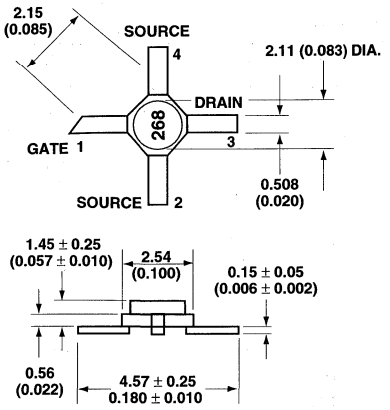
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
2.0	.94	-38	8.2	2.57	138	-27.1	.044	60	.74	-26
3.0	.90	-55	7.8	2.45	120	-24.9	.057	51	.71	-35
4.0	.84	-72	7.6	2.41	102	-22.9	.072	44	.71	-44
5.0	.75	-92	8.0	2.50	82	-20.6	.093	30	.66	-53
6.0	.64	-117	8.1	2.55	61	-19.3	.109	15	.60	-64
7.0	.52	-155	8.3	2.60	37	-18.1	.124	5	.51	-78
8.0	.49	163	7.9	2.47	14	-17.5	.133	-12	.41	-92
9.0	.52	126	7.2	2.30	-7	-16.9	.143	-21	.30	-106
10.0	.56	100	6.4	2.10	-28	-16.8	.144	-32	.24	-125
11.0	.61	78	5.6	1.91	-47	-17.1	.140	-41	.18	-154
12.0	.67	58	4.7	1.71	-66	-17.1	.139	-49	.15	168
13.0	.69	45	3.9	1.57	-83	-17.3	.137	-61	.17	134
14.0	.72	35	3.0	1.42	-98	-17.2	.138	-66	.19	107
15.0	.72	22	2.5	1.33	-115	-17.2	.138	-77	.23	89
16.0	.72	13	2.0	1.26	-128	-17.4	.135	-85	.27	71

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 5 V, I_{DS} = 30 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
2.0	.94	-44	9.0	2.82	130	-30.2	.031	65	.80	-31
3.0	.86	-63	8.5	2.65	110	-28.4	.038	56	.80	-43
4.0	.78	-81	8.0	2.51	89	-26.9	.045	47	.79	-52
5.0	.68	-97	7.9	2.49	71	-25.5	.053	41	.78	-58
6.0	.57	-118	8.1	2.53	51	-24.4	.060	39	.76	-67
7.0	.43	-151	8.5	2.65	28	-22.4	.076	38	.73	-80
8.0	.37	165	8.5	2.66	3	-20.6	.093	30	.69	-99
9.0	.40	122	8.0	2.52	-20	-18.0	.126	15	.64	-119
10.0	.47	96	7.7	2.42	-42	-16.4	.152	3	.66	-140
11.0	.55	75	7.5	2.37	-66	-15.1	.176	-4	.63	-166
12.0	.61	53	7.4	2.35	-88	-13.8	.205	-19	.64	168
13.0	.71	33	7.4	2.34	-116	-13.2	.220	-39	.71	132
14.0	.71	10	6.7	2.17	-143	-13.5	.212	-56	.78	104
15.0	.65	-10	5.7	1.93	-170	-14.0	.200	-72	.85	79
16.0	.58	-30	4.2	1.62	166	-14.9	.180	-93	.98	61

A model for this device is available in the DEVICE MODELS section.

36 micro-X Package Dimensions



Notes:
1. Dimensions are in millimeters (inches)
2. Tolerances: in .xxx = ± 0.005
   mm .xx = ± 0.13

HEWLETT® PACKARD

2–16 GHz General Purpose Gallium Arsenide FET

Technical Data

ATF-26884

Features

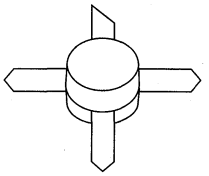
- **High Output Power:** 18.0 dBm Typical $P_{1\,dB}$ at 12 GHz
- **High Gain:** 9.0 dB Typical G_{SS} at 12 GHz
- **Low Cost Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

Description

The ATF-26884 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. This device is designed for use in oscillator applications and general purpose amplifier applications in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

84 Plastic Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G_{SS}	Tuned Small Signal Gain: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dB	7.0	9.0	
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 10 mA	f = 12.0 GHz	dB		2.2	
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 10 mA	f = 12.0 GHz	dB		6.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dBm	15.0	18.0	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	15	35	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	30	50	90
V_P	Pinch-off Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	-3.5	-1.5	-0.5

Note:

1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors."

ATF-26884 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+7
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-8
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	275
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +150

Thermal Resistance:	θ_{jc} = 300°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 µm Spot Size[4]

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 3.3 mW/°C for T_{CASE} > 92.5°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-26884-TR1	1000	7"
ATF-26884-STR	10	strip

ATF-26884 Typical Performance, T_A = 25°C

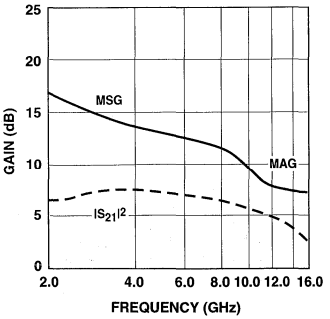


Figure 1. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 10 mA.

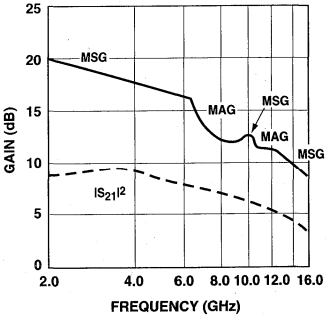


Figure 2. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 5 V, I_{DS} = 30 mA.

Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{DS} = 3\ V$, $I_{DS} = 10\ mA$

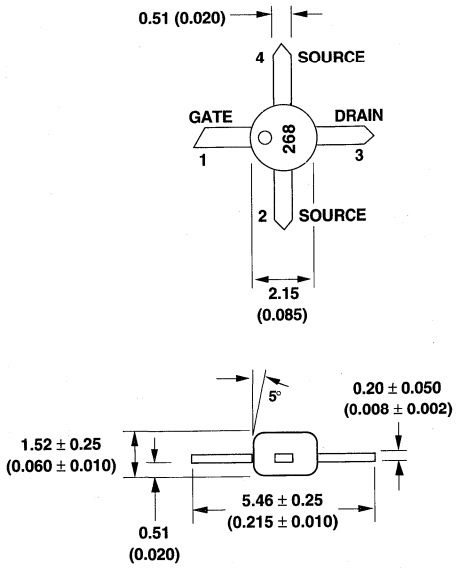
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
2.0	.96	-36	6.9	2.21	142	-26.6	.047	64	.81	-25
3.0	.91	-56	7.4	2.35	123	-23.0	.071	50	.77	-38
4.0	.86	-78	7.6	2.39	103	-20.6	.093	36	.70	-50
5.0	.79	-97	7.2	2.30	86	-19.5	.106	25	.66	-61
6.0	.73	-113	6.8	2.20	71	-18.9	.114	16	.62	-70
7.0	.67	-127	6.4	2.10	56	-18.4	.120	9	.61	-78
8.0	.62	-144	6.4	2.08	41	-17.9	.128	1	.58	-88
9.0	.57	-168	6.2	2.03	23	-17.5	.134	-8	.54	-101
10.0	.53	168	5.8	1.96	6	-17.3	.136	-16	.47	-116
11.0	.52	147	5.2	1.81	-10	-17.2	.138	-22	.41	-133
12.0	.49	124	4.9	1.76	-22	-17.1	.140	-26	.39	-143
13.0	.52	103	4.6	1.70	-36	-16.7	.146	-31	.37	-154
14.0	.56	80	4.0	1.58	-54	-16.3	.153	-37	.35	-171
15.0	.60	65	3.3	1.46	-72	-16.3	.153	-42	.35	173
16.0	.65	52	2.9	1.40	-83	-16.3	.153	-48	.37	132
17.0	.68	40	2.3	1.30	-99	-16.0	.158	-56	.41	101
18.0	.69	30	1.3	1.16	-112	-15.9	.159	-72	.47	87

Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{DS} = 5\ V$, $I_{DS} = 30\ mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
2.0	.94	-41	9.2	2.88	138	-30.8	.029	65	.84	-23
3.0	.87	-65	9.5	2.97	118	-27.3	.043	51	.80	-34
4.0	.79	-89	9.3	2.93	97	-25.5	.053	40	.74	-44
5.0	.71	-109	8.7	2.73	79	-24.9	.057	35	.71	-53
6.0	.64	-126	8.1	2.54	64	-24.4	.060	33	.69	-60
7.0	.57	-142	7.5	2.38	50	-24.0	.063	31	.69	-67
8.0	.52	-162	7.2	2.30	35	-23.1	.070	30	.69	-76
9.0	.48	174	6.9	2.21	18	-21.9	.080	28	.67	-87
10.0	.48	149	6.5	2.11	1	-20.4	.095	24	.63	-100
11.0	.48	130	5.9	1.97	-14	-19.7	.104	22	.57	-114
12.0	.49	108	5.6	1.91	-25	-18.1	.125	20	.55	-122
13.0	.53	88	5.2	1.82	-39	-16.2	.155	18	.54	-132
14.0	.57	69	4.7	1.71	-55	-15.2	.173	5	.52	-146
15.0	.62	56	4.1	1.60	-75	-14.8	.182	-1	.52	-165
16.0	.70	44	3.7	1.53	-87	-13.8	.205	-16	.52	165
17.0	.75	33	3.0	1.41	-103	-12.9	.226	-28	.54	135
18.0	.74	24	2.3	1.30	-117	-13.6	.210	-44	.63	114

A model for this device is available in the DEVICE MODELS section.

84 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

2–18 GHz Ultra Low Noise Pseudomorphic HEMT

Technical Data

ATF-36077

Features

- **PHEMT Technology**
- **Ultra-Low Noise Figure:**
  0.5 dB Typical at 12 GHz
  0.3 dB Typical at 4 GHz
- **High Associated Gain:**
  12 dB Typical at 12 GHz
  17 dB Typical at 4 GHz
- **Low Parasitic Ceramic Microstrip Package**
- **Tape-and-Reel Packing Option Available**

Applications

- **12 GHz DBS LNB (Low Noise Block)**
- **4 GHz TVRO LNB (Low Noise Block)**
- **Ultra-Sensitive Low Noise Amplifiers**

Note: 1. See Noise Parameter Table.

Description

Hewlett-Packard's ATF-36077 is an ultra-low-noise Pseudomorphic High Electron Mobility Transistor (PHEMT), packaged in a low parasitic, surface-mountable ceramic package. Properly matched, this transistor will provide typical 12 GHz noise figures of 0.5 dB, or typical 4 GHz noise figures of 0.3 dB. Additionally, the ATF-36077 has very low noise resistance, reducing the sensitivity of noise performance to variations in input impedance match, making the design of broadband low noise amplifiers much easier. The premium sensitivity of the ATF-36077 makes this device the ideal choice for use in the first stage of extremely low noise cascades.

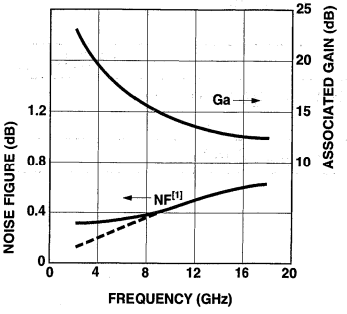
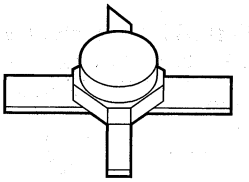
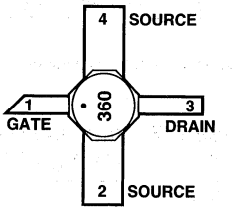


Figure 1. ATF-36077 Optimum Noise Figure and Associated Gain vs. Frequency for V_{DS} = 1.5 V, I_D = 10 mA.

77 Package



Pin Configuration



The repeatable performance and consistency make it appropriate for use in Ku-band Direct Broadcast Satellite (DBS) Television systems, C-band Television Receive Only (TVRO) LNAs, or other low noise amplifiers operating in the 2-18 GHz frequency range.

This GaAs PHEMT device has a nominal 0.2 micron gate length with a total gate periphery (width) of 200 microns. Proven gold based metalization systems and nitride passivation assure rugged, reliable devices.

5965-8726E

ATF-36077 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain – Source Voltage	V	+3
V_{GS}	Gate – Source Voltage	V	-3
V_{GD}	Gate-Drain Voltage	V	-3.5
I_D	Drain Current	mA	I_{dss}
P_T	Total Power Dissipation[3]	mW	180
$P_{in\ max}$	RF Input Power	dBm	+10
T_{ch}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2,3]:
$\theta_{ch-c} = 60°C/W$

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Measured at P_{diss} = 15 mW and T_{ch} = 100°C.
3. Derate at 16.7 mW/°C for T_C > 139°C.

ATF-36077 Electrical Specifications,

T_C = 25°C, Z_O = 50 Ω, V_{ds} = 1.5 V, I_{ds} = 10 mA, (unless otherwise noted).

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF	Noise Figure[1]	f = 12.0 GHz	dB		0.5	0.6
G_A	Gain at NF[1]	f = 12.0 GHz	dB	11.0	12.0	
g_m	Transconductance	V_{DS} = 1.5 V, V_{GS} = 0 V	mS	50	55	
I_{dss}	Saturated Drain Current	V_{DS} = 1.5 V, V_{GS} = 0 V	mA	15	25	45
$V_{p\ 10\%}$	Pinch-off Voltage	V_{DS} = 1.5 V, I_{DS} = 10% of I_{dss}	V	-1.0	-0.35	-0.15

Note:
1. Measured in a fixed tuned environment with Γ source = 0.54 at 156°; Γ load = 0.48 at 167°.

ATF-36077 Characterization Information,

T_C = 25°C, Z_O = 50 Ω, V_{ds} = 1.5 V, I_{ds} = 10 mA, (unless otherwise noted).

Symbol	Parameters and Test Conditions		Units	Typ.
NF	Noise Figure (Tuned Circuit)	f = 4 GHz	dB	0.3[2]
		f = 12 GHz	dB	0.5
G_A	Gain at Noise Figure (Tuned Circuit)	f = 4 GHz	dB	17
		f = 12 GHz	dB	12
$S_{12\ off}$	Reverse Isolation	f = 12 GHz, V_{DS} = 1.5 V, V_{GS} = -2 V	dB	14
P_{1dB}	Output Power at 1 dB Gain Compression	f = 4 GHz	dBm	5
		f = 12 GHz	dBm	5
$V_{GS\ 10\ mA}$	Gate to Source Voltage for I_{DS} = 10 mA	V_{DS} = 1.5 V	V	-0.2

Note:
2. See noise parameter table.

ATF-36077 Typical Scattering Parameters,

Common Source, Z_O = 50 Ω, V_{DS} = 1.5 V, I_D = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
1.0	0.99	-17	14.00	5.010	163	-36.08	0.016	78	0.60	-14
2.0	0.97	-33	13.81	4.904	147	-30.33	0.030	66	0.59	-28
3.0	0.94	-49	13.53	4.745	132	-27.25	0.043	54	0.57	-41
4.0	0.90	-65	13.17	4.556	116	-25.32	0.054	43	0.55	-54
5.0	0.86	-79	12.78	4.357	102	-24.04	0.063	33	0.53	-66
6.0	0.82	-93	12.39	4.162	88	-23.17	0.069	24	0.50	-78
7.0	0.78	-107	12.00	3.981	75	-22.58	0.074	16	0.48	-89
8.0	0.75	-120	11.64	3.820	62	-22.17	0.078	8	0.46	-99
9.0	0.72	-133	11.32	3.682	49	-21.90	0.080	1	0.44	-109
10.0	0.69	-146	11.04	3.566	37	-21.71	0.082	-6	0.42	-119
11.0	0.66	-159	10.81	3.473	25	-21.57	0.083	-13	0.40	-129
12.0	0.63	-172	10.63	3.401	13	-21.44	0.085	-19	0.38	-139
13.0	0.61	175	10.50	3.349	1	-21.32	0.086	-25	0.37	-149
14.0	0.60	161	10.41	3.315	-12	-21.19	0.087	-32	0.35	-160
15.0	0.58	147	10.36	3.296	-24	-21.04	0.089	-39	0.33	-171
16.0	0.57	131	10.34	3.289	-37	-20.87	0.091	-47	0.31	177
17.0	0.56	114	10.34	3.289	-50	-20.69	0.092	-55	0.29	164
18.0	0.57	97	10.35	3.291	-64	-20.53	0.094	-65	0.26	148

ATF-36077 Typical "Off" Scattering Parameters,

Common Source, Z_O = 50 Ω, V_{DS} = 1.5 V, I_D = 0 mA, V_{GS} = -2 V

Freq.	S_{11}		S_{21}			S_{21}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
11.0	0.96	-139	-14.2	0.19	-43	-14.2	0.19	-43	0.97	-125
12.0	0.95	-152	-14.0	0.20	-56	-14.0	0.20	-56	0.97	-137
13.0	0.94	-166	-13.8	0.20	-69	-13.8	0.20	-68	0.96	-149

ATF-36077 Typical Noise Parameters,

Common Source, Z_O = 50 Ω, V_{DS} = 1.5 V, I_D = 10 mA

Freq. GHz	F_{min}[1] dB	Γ_{opt} Mag.	Γ_{opt} Ang.	R_n/Z_o -
1	0.30	0.95	12	0.40
2	0.30	0.90	25	0.20
4	0.30	0.81	51	0.17
6	0.30	0.73	76	0.13
8	0.37	0.66	102	0.09
10	0.44	0.60	129	0.05
12	0.50	0.54	156	0.03
14	0.56	0.48	-174	0.02
16	0.61	0.43	-139	0.05
18	0.65	0.39	-100	0.09

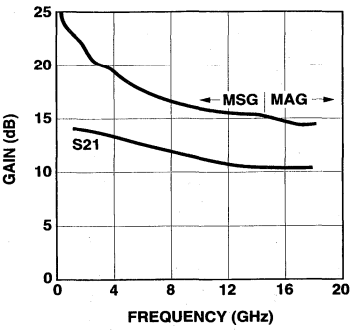
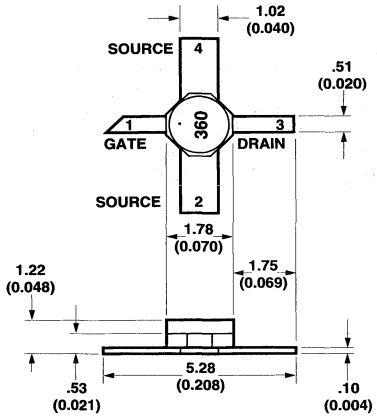


Figure 2. Maximum Available Gain, Maximum Stable Gain and Insertion Power Gain vs. Frequency. V_{DS} = 1.5 V, I_D = 10 mA.

Note:

1. The F_{min} values at 2,4, and 6 GHz have been adjusted to reflect expected circuit losses that will be encountered when matching to the optimum reflection coefficient (Γ_{opt}) at these frequencies. The theoretical F_{min} values for these frequencies are: 0.10 dB at 2 GHz, 0.20 dB at 4 GHz, and 0.29 dB at 6 GHz. Noise parameters are derived from associated s parameters, packaged device measurements at 12 GHz, and die level measurements from 6 to 18 GHz.

77 Package Dimensions



TYPICAL DIMENSIONS ARE IN MILLIMETERS (INCHES).

Part Number Ordering Information

Part Number	No. of Devices	Container
ATF-36077-TRI[2]	1000	7" Reel
ATF-36077-STR	10	strip

Note:

2. For more information, see "Tape and Reel Packaging for Semiconductor Devices," in "Communications Components" Designer's Catalog.

HEWLETT® PACKARD

1.5 – 18 GHz Surface Mount Pseudomorphic HEMT

Technical Data

ATF-36163

Features

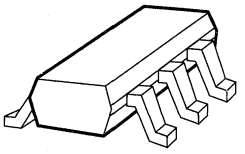
- **Low Minimum Noise Figure:**
  1 dB Typical at 12 GHz
  0.6 dB Typical at 4 GHz
- **Associated Gain:**
  9.4 dB Typical at 12 GHz
  15.8 dB Typical at 4 GHz
- **Maximum Available Gain:**
  11 dB Typical at 12 GHz
  17 dB Typical at 4 GHz
- **Low Cost Surface Mount Small Plastic Package**
- **Tape-and-Reel Packaging Option Available**

Applications

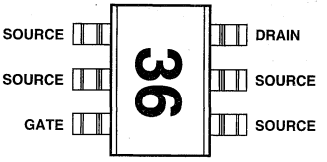
- **12 GHz DBS Downconverters**
- **4 GHz TVRO Downconverters**
- **S or L Band Low Noise Amplifiers**

Surface Mount Package

SOT-363 (SC-70)



Pin Connections and Package Marking



Note: Package marking provides orientation and identification.

Description

The Hewlett-Packard ATF-36163 is a low-noise Pseudomorphic High Electron Mobility Transistor (PHEMT), in the SOT-363 (SC-70) package. When optimally matched for minimum noise figure, it will provide a noise figure of 1 dB at 12 GHz and 0.6 dB at 4 GHz.

Additionally, the ATF-36163 has low noise-resistance, which reduces the sensitivity of noise performance to variations in input impedance match. This feature makes the design of broad band low noise amplifiers much easier. The performance of the ATF-36163 makes this device the ideal choice for use in the 2nd or 3rd stage of low noise cascades. The repeatable performance and consistency make it appropriate for use in Ku-band Direct Broadcast Satellite (DBS) TV systems, C-band TV Receive Only (TVRO) LNAs, Multichannel Multipoint Distribution Systems (MMDS), X-band Radar detector and other low noise amplifiers operating in the 1.5 – 18 GHz frequency range.

This GaAs PHEMT device has a nominal 0.2 micron gate length with a total gate periphery (width) of 200 microns. Proven gold-based metallization system and nitride passivation assure rugged, reliable devices.

5965-4747E

ATF-36163 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain - Source Voltage	V	+3
V_{GS}	Gate - Source Voltage	V	-3
V_{GD}	Gate Drain Voltage	V	-3.5
I_D	Drain Current	mA	I_{dss}
P_T	Total Power Dissipation	mW	180
$P_{in\ max}$	RF Input Power	dBm	+10
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance:
$\theta_{ch-c} = 160°C/W$

Note:
1. Operation of this device above any one of these parameters may cause permanent damage.

ATF-36163 Electrical Specifications

$T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{ds} = 1.5$ V, $I_{ds} = 10$ mA, (unless otherwise noted).

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF	Noise Figure[1]	f =12.0 GHz	dB		1.2	1.4[1]
G	Gain at NF[1]	f = 12.0 GHz	dB	9	10	
g_m	Transconductance	V_{DS} = 1.5 V, V_{GS} = 0 V	mS	50	60	
I_{dss}	Saturated Drain Current	V_{DS} = 1.5 V, V_{GS} = 0 V	mA	15	25	40
$V_{p\ 10\%}$	Pinchoff Voltage	V_{DS} = 1.5 V, I_{DS} = 10% of I_{dss}	V	-1.0	-0.35	-0.15
BV_{GDO}	Gate Drain Breakdown Voltage	I_G = 30 µA	V			-3.5

Note:
1. Measured in a test circuit tuned for a typical device.

ATF-36163 Typical Parameters

$T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{ds} = 2$ V, $I_{ds} = 15$ mA, (unless otherwise noted).

Symbol	Parameters and Test Conditions		Units	Typ.
F_{min}	Minimum Noise Figure ($\Gamma_{source} = \Gamma_{opt}$)	f = 4 GHz	dB	0.6
		f = 12 GHz	dB	1.0
G_a	Associated Gain	f = 4 GHz	dB	15.8
		f = 12 GHz	dB	9.4
G_{max}	Maximum Available Gain[1]	f = 4 GHz	dB	17.2
		f = 12 GHz	dB	10.9
P_{1dB}	Output Power at 1 dB Gain Compression	f = 4 GHz	dBm	5
	under the power matched condition	f = 12 GHz	dBm	5
V_{GS}	Gate to Source Voltage for I_{DS} = 15 mA	V_{DS} = 2.0 V	V	-0.2

Note:
1. G_{max} = MAG for $K > 1$ and G_{max} = MSG for $K \leq 1$, which is shown on the S-parameters tables.

ATF-36163 Typical Scattering Parameters, Common Source, Z_O = 50 Ω, V_{DS} = 1.5 V, I_D = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K	G_{max}[1]
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	—	dB
0.5	0.99	-11	12.85	4.39	168	-37.72	0.01	79	0.51	-9	0.11	25.24
1	0.98	-22	12.70	4.31	158	-31.70	0.03	71	0.50	-18	0.17	22.26
2	0.96	-42	12.48	4.21	138	-26.02	0.05	55	0.48	-36	0.24	19.28
3	0.93	-61	12.37	4.15	118	-22.73	0.07	40	0.45	-53	0.33	17.56
4	0.87	-83	12.30	4.12	97	-20.45	0.10	23	0.40	-71	0.43	16.38
5	0.81	-106	12.16	4.06	76	-18.71	0.12	6	0.34	-92	0.51	15.43
6	0.75	-131	11.94	3.95	55	-17.52	0.13	-12	0.27	-116	0.58	14.73
7	0.67	-158	11.47	3.75	33	-16.77	0.15	-30	0.18	-144	0.69	14.12
8	0.61	176	11.01	3.55	12	-16.36	0.15	-45	0.10	174	0.79	13.69
9	0.57	143	10.47	3.34	-10	-15.97	0.16	-61	0.12	93	0.85	13.22
10	0.57	108	9.66	3.04	-32	-15.92	0.16	-77	0.22	53	0.91	12.80
11	0.59	76	8.53	2.67	-54	-16.48	0.15	-93	0.33	28	0.99	12.50
12	0.63	50	7.39	2.34	-74	-17.14	0.14	-106	0.41	9	1.07	10.65
13	0.67	26	6.10	2.02	-93	-18.27	0.12	-119	0.49	-8	1.18	9.64
14	0.72	6	4.81	1.74	-111	-19.74	0.10	-129	0.56	-22	1.30	8.99
15	0.78	-11	3.49	1.50	-128	-21.41	0.09	-138	0.63	-33	1.38	8.81
16	0.82	-24	2.20	1.29	-146	-23.10	0.07	-144	0.67	-43	1.44	8.70
17	0.87	-38	0.59	1.07	-164	-25.04	0.06	-151	0.73	-53	1.46	8.79
18	0.90	-52	-1.63	0.83	178	-29.12	0.04	-159	0.78	-65	1.80	8.58

Note:
1. G_{max} = MAG for K > 1 and G_{max} = MSG for K ≤ 1.

ATF-36163 Typical Noise Parameters

Common Source, Z_O = 50 Ω, V_{DS} = 1.5 V, I_D = 10 mA

Freq.	F_{min}	G_a	Γ_{opt}		R_n/Z_O
GHz	dB	dB	Mag.	Ang.	-
2	0.48	18.77	0.78	28	0.38
3	0.53	16.75	0.75	41	0.32
4	0.57	15.17	0.68	55	0.26
5	0.61	14.14	0.60	71	0.20
6	0.66	13.23	0.55	88	0.15
7	0.71	12.06	0.48	105	0.12
8	0.77	11.22	0.38	119	0.10
9	0.83	10.50	0.32	138	0.07
10	0.89	10.02	0.23	170	0.07
11	0.97	9.44	0.18	-141	0.09
12	1.05	8.92	0.20	-92	0.13
13	1.14	8.45	0.26	-46	0.21
14	1.24	8.12	0.36	-16	0.32
15	1.37	8.08	0.48	4	0.44
16	1.51	8.11	0.59	19	0.60
17	1.68	7.97	0.64	34	0.79
18	1.89	7.59	0.70	51	1.15

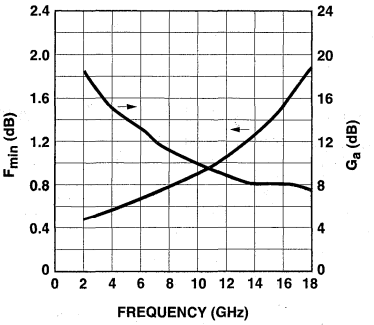


Figure 1. ATF-36163 Minimum Noise Figure and Associated Gain vs. Frequency for V_{DS} = 1.5 V, I_D = 10 mA.

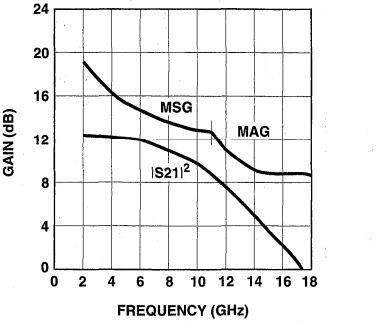


Figure 2. Maximum Available Gain, Maximum Stable Gain & Insertion Power Gain vs. Frequency for V_{DS} = 1.5 V, I_D = 10 mA.

ATF-36163 Typical Scattering Parameters, Common Source, Z_O = 50 Ω, V_{DS} = 1.5 V, I_D = 15 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K	G_{max}[1]
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	—	dB
0.5	0.99	-12	13.56	4.76	168	-38.42	0.01	79	0.45	-9	0.12	25.82
1	0.98	-22	13.40	4.68	157	-32.40	0.02	71	0.45	-18	0.18	22.86
2	0.96	-43	13.16	4.55	137	-26.56	0.05	56	0.43	-36	0.26	19.87
3	0.92	-63	13.00	4.47	116	-23.22	0.07	40	0.40	-52	0.35	18.13
4	0.86	-85	12.87	4.40	96	-21.01	0.09	24	0.35	-70	0.46	16.94
5	0.80	-108	12.68	4.30	75	-19.25	0.11	7	0.28	-92	0.55	15.98
6	0.74	-133	12.38	4.16	53	-18.13	0.12	-11	0.21	-116	0.62	15.25
7	0.66	-160	11.85	3.91	31	-17.39	0.14	-28	0.13	-146	0.74	14.62
8	0.59	173	11.33	3.68	11	-16.95	0.14	-42	0.06	156	0.84	14.14
9	0.56	141	10.74	3.44	-11	-16.54	0.15	-58	0.12	73	0.90	13.63
10	0.56	106	9.89	3.12	-33	-16.42	0.15	-73	0.23	44	0.95	13.16
11	0.59	74	8.74	2.74	-54	-16.83	0.14	-88	0.34	23	1.03	11.78
12	0.63	49	7.59	2.40	-74	-17.39	0.14	-102	0.42	6	1.10	10.62
13	0.68	25	6.29	2.06	-93	-18.42	0.12	-115	0.50	-10	1.19	9.72
14	0.73	5	5.01	1.78	-110	-19.74	0.10	-124	0.57	-23	1.29	9.15
15	0.79	-12	3.70	1.53	-127	-21.31	0.09	-133	0.64	-34	1.35	8.99
16	0.83	-25	2.43	1.32	-144	-22.85	0.07	-139	0.68	-44	1.39	8.93
17	0.87	-38	0.84	1.10	-163	-24.73	0.06	-148	0.73	-54	1.39	9.06
18	0.91	-53	-1.33	0.86	180	-28.87	0.04	-155	0.78	-66	1.67	8.92

Note:
1. G_{max} = MAG for K > 1 and G_{max} = MSG for K ≤ 1.

ATF-36163 Typical Noise Parameters

Common Source, Z_O = 50 Ω, V_{DS} = 1.5 V, I_D = 15 mA

Freq.	F_{min}	G_a	Γ_{opt}		R_n/Z_O
GHz	dB	dB	Mag.	Ang.	-
2	0.49	18.87	0.84	28	0.38
3	0.54	17.20	0.74	42	0.31
4	0.58	15.75	0.66	57	0.25
5	0.63	14.49	0.59	72	0.19
6	0.68	13.61	0.54	90	0.15
7	0.73	12.36	0.46	106	0.11
8	0.79	11.54	0.37	121	0.09
9	0.85	10.82	0.30	140	0.08
10	0.91	10.32	0.21	174	0.08
11	0.99	9.73	0.17	-133	0.10
12	1.07	9.22	0.20	-83	0.14
13	1.17	8.68	0.26	-40	0.22
14	1.27	8.41	0.38	-12	0.34
15	1.40	8.36	0.49	7	0.46
16	1.54	8.37	0.60	21	0.64
17	1.72	8.10	0.62	35	0.85
18	1.93	8.00	0.71	52	1.18

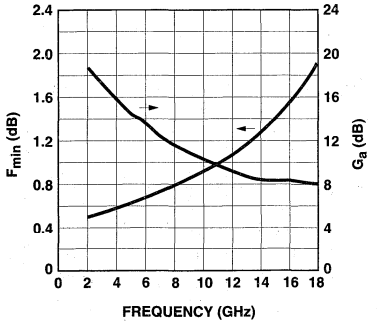


Figure 3. ATF-36163 Minimum Noise Figure and Associated Gain vs. Frequency for V_{DS} = 1.5 V, I_D = 15 mA.

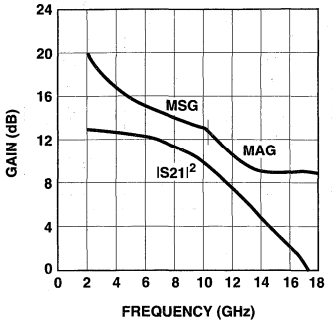


Figure 4. Maximum Available Gain, Maximum Stable Gain & Insertion Power Gain vs. Frequency for V_{DS} = 1.5 V, I_D = 15 mA.

ATF-36163 Typical Scattering Parameters, Common Source, Z_O = 50 Ω, V_{DS} = 2.0 V, I_D = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K	Gmax[1]
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	–	dB
0.5	0.99	-11	13.06	4.50	168	-37.72	0.01	79	0.55	-9	0.11	25.46
1	0.99	-22	12.90	4.42	158	-32.04	0.03	71	0.55	-18	0.16	22.46
2	0.96	-42	12.69	4.31	138	-26.38	0.05	56	0.53	-35	0.24	19.50
3	0.93	-62	12.57	4.25	118	-22.97	0.07	40	0.50	-52	0.32	17.77
4	0.87	-83	12.51	4.22	97	-20.72	0.09	23	0.44	-70	0.42	16.61
5	0.81	-106	12.38	4.16	76	-18.94	0.11	6	0.38	-90	0.51	15.67
6	0.75	-131	12.15	4.05	55	-17.79	0.13	-12	0.31	-112	0.58	14.98
7	0.67	-157	11.70	3.84	33	-17.08	0.14	-30	0.21	-137	0.69	14.38
8	0.60	176	11.25	3.65	13	-16.65	0.15	-44	0.13	-168	0.79	13.96
9	0.57	144	10.73	3.44	-10	-16.25	0.15	-60	0.10	115	0.85	13.50
10	0.56	109	9.95	3.14	-32	-16.25	0.15	-76	0.18	61	0.91	13.10
11	0.58	77	8.86	2.77	-53	-16.77	0.15	-91	0.29	32	1.00	12.52
12	0.62	50	7.75	2.44	-73	-17.39	0.14	-104	0.37	12	1.08	10.82
13	0.67	26	6.49	2.11	-93	-18.56	0.12	-117	0.46	-5	1.19	9.85
14	0.72	6	5.24	1.83	-110	-19.91	0.10	-126	0.53	-19	1.31	9.24
15	0.78	-10	3.96	1.58	-128	-21.51	0.08	-134	0.60	-30	1.38	9.07
16	0.82	-24	2.68	1.36	-146	-23.10	0.07	-139	0.65	-40	1.42	9.03
17	0.87	-37	1.08	1.13	-165	-24.88	0.06	-147	0.71	-50	1.38	9.28
18	0.91	-52	-1.16	0.88	177	-28.64	0.04	-153	0.78	-63	1.63	9.06

Note:
1. G_{max} = MAG for K > 1 and G_{max} = MSG for K ≤ 1.

ATF-36163 Typical Noise Parameters

Common Source, Z_O = 50 Ω, V_{DS} = 2.0 V, I_D = 10 mA

Freq.	F_{min}	G_a	Γ_{opt}		R_n/Z_O
GHz	dB	dB	Mag.	Ang.	-
2	0.46	18.60	0.84	28	0.38
3	0.50	16.75	0.76	41	0.31
4	0.54	15.55	0.67	56	0.25
5	0.59	14.20	0.61	70	0.20
6	0.63	13.37	0.55	88	0.15
7	0.68	12.12	0.49	103	0.12
8	0.74	11.35	0.39	118	0.10
9	0.80	10.59	0.33	135	0.07
10	0.86	10.11	0.23	165	0.07
11	0.94	9.57	0.17	-145	0.09
12	1.02	9.08	0.18	-93	0.12
13	1.11	8.59	0.24	-47	0.19
14	1.22	8.30	0.34	-16	0.30
15	1.35	8.29	0.47	5	0.42
16	1.51	8.32	0.58	19	0.57
17	1.69	8.07	0.60	34	0.76
18	1.92	7.68	0.66	50	1.10

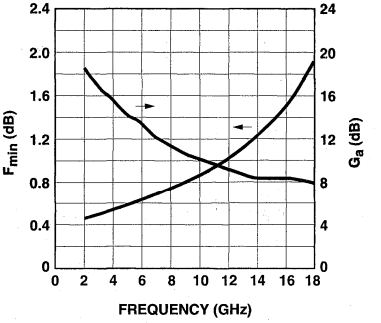


Figure 5. ATF-36163 Minimum Noise Figure and Associated Gain vs. Frequency for V_{DS} = 2.0 V, I_D = 10 mA.

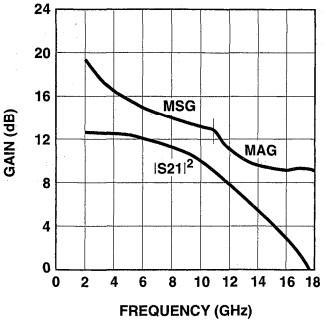


Figure 6. Maximum Available Gain, Maximum Stable Gain & Insertion Power Gain vs. Frequency for V_{DS} = 2.0 V, I_D = 10 mA.

ATF-36163 Typical Scattering Parameters, Common Source, Z_O = 50 Ω, V_{DS} = 2 V, I_D = 15 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K	Gmax[1]
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	–	dB
0.5	0.99	-12	13.85	4.93	168	-38.42	0.01	79	0.51	-9	0.12	26.10
1	0.98	-22	13.70	4.84	157	-32.40	0.02	71	0.50	-18	0.17	23.11
2	0.96	-43	13.45	4.70	137	-26.74	0.05	56	0.48	-35	0.26	20.13
3	0.92	-63	13.29	4.62	117	-23.48	0.07	40	0.45	-52	0.35	18.40
4	0.86	-85	13.16	4.55	96	-21.31	0.09	24	0.40	-69	0.46	17.22
5	0.79	-108	12.96	4.45	75	-19.58	0.11	7	0.33	-90	0.55	16.26
6	0.73	-133	12.67	4.30	53	-18.42	0.12	-10	0.26	-112	0.62	15.54
7	0.65	-160	12.13	4.04	32	-17.72	0.13	-28	0.17	-136	0.75	14.93
8	0.59	173	11.63	3.81	11	-17.27	0.14	-42	0.09	-171	0.84	14.46
9	0.55	141	11.06	3.57	-11	-16.83	0.14	-57	0.09	93	0.90	13.95
10	0.56	107	10.23	3.25	-32	-16.77	0.15	-72	0.19	51	0.96	13.50
11	0.58	75	9.11	2.86	-53	-17.14	0.14	-87	0.30	27	1.04	11.93
12	0.63	49	8.00	2.51	-73	-17.72	0.13	-99	0.38	9	1.11	10.85
13	0.68	26	6.75	2.17	-92	-18.71	0.12	-112	0.47	-7	1.20	10.00
14	0.73	6	5.49	1.88	-110	-20.00	0.10	-121	0.54	-20	1.30	9.45
15	0.78	-11	4.22	1.63	-127	-21.41	0.09	-129	0.61	-31	1.35	9.30
16	0.83	-24	2.99	1.41	-145	-22.73	0.07	-135	0.66	-41	1.36	9.31
17	0.88	-38	1.42	1.18	-164	-24.44	0.06	-143	0.72	-51	1.31	9.56
18	0.91	-52	-0.79	0.91	178	-27.96	0.04	-149	0.78	-63	1.50	9.44

Note:

1. G_{max} = MAG for K > 1 and G_{max} = MSG for K ≤ 1.

ATF-36163 Typical Noise Parameters

Common Source, Z_O = 50 Ω, V_{DS} = 2.0 V, I_D = 15 mA

Freq.	F_{min}	G_a	Γ_{opt}		R_n/Z_O
GHz	dB	dB	Mag.	Ang.	-
2	0.48	18.97	0.83	28	0.37
3	0.52	17.27	0.74	41	0.31
4	0.56	15.75	0.67	56	0.25
5	0.61	14.54	0.60	71	0.19
6	0.65	13.68	0.55	89	0.15
7	0.70	12.47	0.46	104	0.11
8	0.76	11.66	0.37	118	0.09
9	0.82	10.94	0.31	136	0.08
10	0.88	10.44	0.21	168	0.07
11	0.95	9.88	0.15	-137	0.09
12	1.03	9.38	0.18	-85	0.13
13	1.12	8.90	0.25	-41	0.21
14	1.23	8.63	0.36	-13	0.32
15	1.35	8.59	0.48	7	0.44
16	1.49	8.63	0.58	20	0.60
17	1.65	8.68	0.65	34	0.79
18	1.86	8.32	0.70	51	1.10

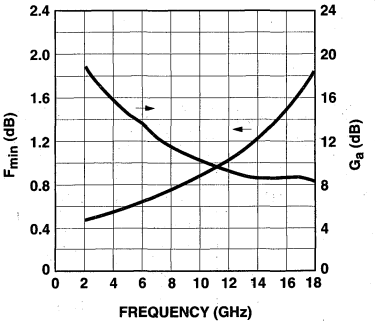


Figure 7. ATF-36163 Minimum Noise Figure and Associated Gain vs. Frequency for V_{DS} = 2 V, I_D = 15 mA.

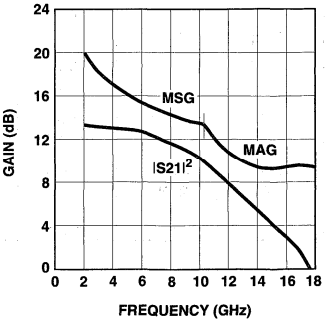


Figure 8. Maximum Available Gain, Maximum Stable Gain & Insertion Power Gain vs. Frequency for V_{DS} = 2 V, I_D = 15 mA.

ATF-36163 Typical "Off" Scattering Parameters, Common Source, Z_O = 50 Ω, V_{DS} = 0 V, V_{GS} = 0 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	0.998	-10	-46.02	0.01	80	-46.02	0.01	86	0.703	170
1	0.993	-20	-39.17	0.01	81	-39.17	0.01	83	0.701	160
2	0.99	-37	-32.77	0.02	75	-32.77	0.02	76	0.70	139
3	0.98	-55	-28.64	0.04	67	-28.64	0.04	68	0.71	119
4	0.96	-74	-25.35	0.05	56	-25.19	0.06	57	0.73	99
5	0.94	-95	-22.62	0.07	42	-22.50	0.08	42	0.74	81
6	0.92	-118	-20.45	0.10	27	-20.45	0.10	27	0.75	63
7	0.89	-142	-18.79	0.12	11	-18.71	0.12	11	0.77	46
8	0.86	-168	-17.02	0.14	-6	-17.02	0.14	-5	0.78	30
9	0.84	162	-15.70	0.16	-24	-15.70	0.16	-24	0.81	16
10	0.83	128	-14.85	0.18	-44	-14.85	0.18	-44	0.83	3
11	0.83	94	-14.66	0.19	-64	-14.66	0.19	-64	0.84	-10
12	0.85	64	-14.85	0.18	-83	-14.85	0.18	-83	0.85	-22
13	0.86	36	-15.76	0.16	-101	-15.76	0.16	-101	0.87	-34
14	0.87	12	-17.14	0.14	-116	-17.08	0.14	-115	0.89	-44
15	0.90	-8	-18.71	0.12	-129	-18.71	0.12	-129	0.89	-53
16	0.93	-24	-20.45	0.10	-140	-20.45	0.10	-140	0.90	-62
17	0.93	-39	-23.35	0.07	-154	-23.10	0.07	-152	0.90	-71
18	0.93	-53	-27.96	0.04	-161	-28.18	0.04	-161	0.90	-81

ATF-36163 Typical "Off" Scattering Parameters, Common Source, Z_O = 50 Ω, V_{DS} = 2.0 V, V_{GS} = -1.5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.5	0.97	-8	-34.89	0.02	82	-34.89	0.02	81	0.999	-7
1	0.98	-16	-28.87	0.04	74	-28.87	0.04	73	0.998	-14
2	0.99	-30	-22.85	0.07	59	-22.97	0.07	59	0.995	-29
3	0.98	-43	-19.33	0.11	44	-19.33	0.11	44	0.98	-43
4	0.97	-57	-16.71	0.15	29	-16.71	0.15	30	0.97	-57
5	0.96	-72	-14.42	0.19	14	-14.47	0.19	14	0.95	-74
6	0.94	-87	-12.62	0.23	-2	-12.65	0.23	-2	0.94	-91
7	0.92	-103	-10.90	0.29	-20	-10.96	0.28	-20	0.92	-107
8	0.89	-119	-9.60	0.33	-37	-9.63	0.33	-37	0.89	-125
9	0.85	-136	-8.09	0.39	-56	-8.09	0.39	-56	0.83	-148
10	0.79	-158	-6.73	0.46	-79	-6.73	0.46	-79	0.79	-174
11	0.74	177	-5.85	0.51	-106	-5.87	0.51	-106	0.75	156
12	0.72	149	-5.71	0.52	-136	-5.71	0.52	-136	0.73	123
13	0.71	114	-6.54	0.47	-170	-6.52	0.47	-170	0.74	86
14	0.75	74	-8.95	0.36	155	-8.92	0.36	156	0.79	50
15	0.82	35	-12.80	0.23	123	-12.69	0.23	123	0.85	18
16	0.89	5	-18.49	0.12	94	-18.20	0.12	95	0.90	-8
17	0.91	-21	-24.88	0.06	79	-24.44	0.06	84	0.91	-30
18	0.92	-42	-27.54	0.04	70	-27.96	0.04	69	0.90	-50

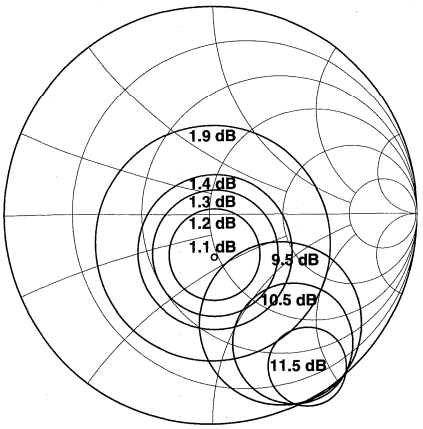


Figure 9. Smith Chart with Noise Figure and Available Gain Circles at 12 GHz, V_{DS} = 1.5 V, I_D = 10 mA.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters and to specify Γ_{opt} for the Noise Parameters are shown in Figure 10. As seen in the illustration, the reference planes are located at the extremities of the package leads.

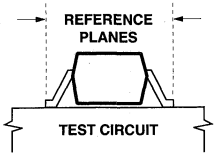


Figure 10. Reference Planes.

SOT-363 PCB Layout

A PCB pad layout for the miniature SOT-363 (SC-70) package used by the ATF-36163 is shown in Figure 11 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads.

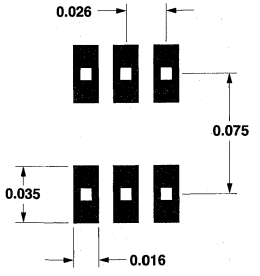
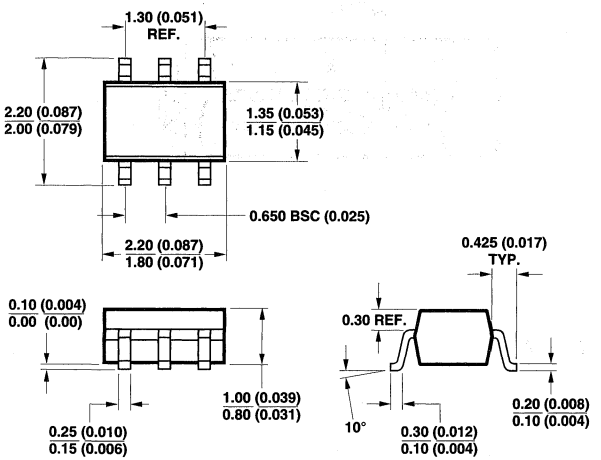


Figure 11. PCB Pad Layout (Dimensions in Inches).

Package Dimensions

Outline 63 (SOT-363/SC-70)

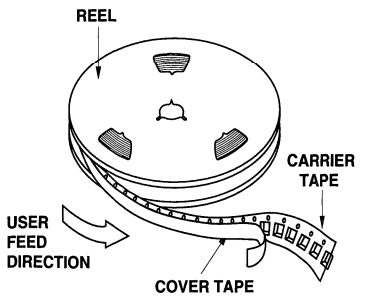


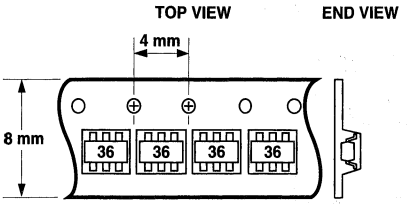
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Part Number Ordering Information

Part Number	No. of Devices	Container
ATF-36163-TR1	3000	7" Reel
ATF-36163-BLK	100	antistatic bag

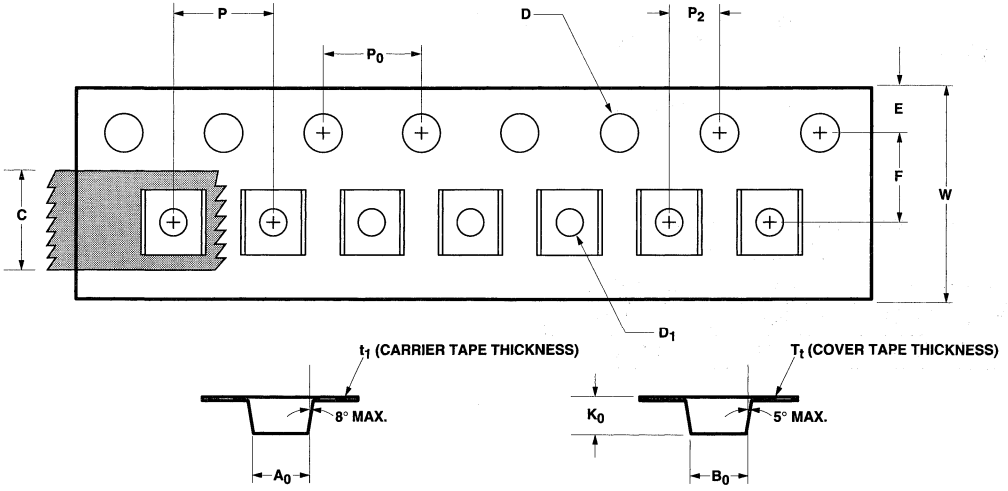
Device Orientation





Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

2–8 GHz Medium Power Gallium Arsenide FET

Technical Data

ATF-44101

Features

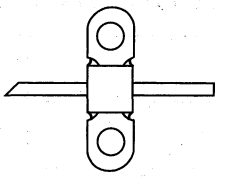
- **High Output Power:** 32.0 dBm Typical $P_{1\,dB}$ at 4 GHz
- **High Gain at 1 dB Compression:** 8.5 dB Typical $G_{1\,dB}$ at 4 GHz
- **High Power Efficiency:** 35% Typical at 4 GHz
- **Hermetic Metal-Ceramic Stripline Package**

Description

The ATF-44101 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 8 GHz frequency range. This nominally .5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between source fingers. Total gate periphery is 5 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

This device is suitable for applications in space, airborne, military ground and shipboard, and commercial environments. It is supplied in a hermetic high reliability package with low parasitic reactance and minimum thermal resistance.

100 mil Flange



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} =9 V, I_{DS} = 500 mA	f = 4.0 GHz f = 6.0 GHz	dBm	31.0	32.0 31.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 500 mA	f = 4.0 GHz f = 6.0 GHz	dB	7.5	8.5 5.5	
η_{add}	Efficiency @ P_{1dB}: V_{DS} = 9 V, I_{DS} = 500 mA	f = 4.0 GHz	%		35	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 500 mA		mmho		300	
I_{DSS}	Saturated Drain Current: V_{DS} = 1.75 V, V_{GS} = 0 V		mA	800	1300	1500
V_P	Pinch-off Voltage: V_{DS} = 2.5 V, I_{DS} = 25 mA		V	-5.4	-4.0	-2.0

ATF-44101 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+14
V_{GS}	Gate-Source Voltage	V	-7
V_{GD}	Gate-Drain Voltage	V	-16
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	W	6.5
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 43 mW/°C for T_{CASE} > 25°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Thermal Resistance:	θ_{jc} = 23°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[4]

ATF-44101 Typical Performance, T_A = 25°C

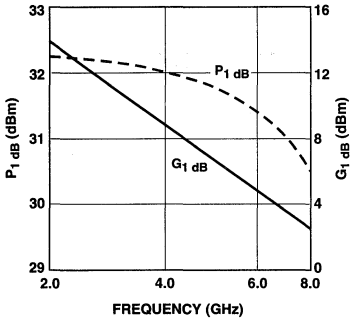


Figure 1. Power Output @ 1 dB Gain Compression and 1 dB Compressed Gain vs. Frequency. V_{DS} = 9 V, I_{DS} = 500 mA.

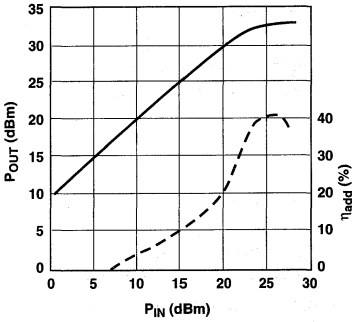


Figure 2. Output Power and Power Added Efficiency vs. Input Power. V_{DS} = 9 V, I_{DS} = 500 mA, f = 4 GHz.

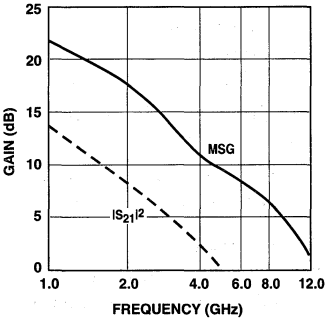


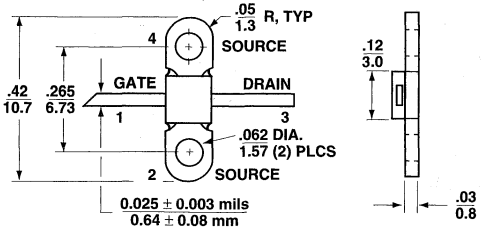
Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 9 V, I_{DS} = 500 mA.

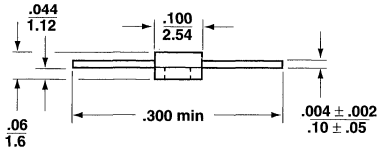
Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{DS} = 9\ V$, $I_{DS} = 500\ mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
1.0	.88	-125	13.4	4.69	104	-28.2	.039	31	.29	-154
2.0	.87	-161	8.1	2.53	74	-26.7	.046	21	.38	-164
3.0	.87	-178	4.8	1.73	54	-26.7	.046	22	.44	-167
4.0	.87	168	2.5	1.34	35	-25.7	.052	17	.47	-175
5.0	.88	153	0.8	1.10	16	-25.5	.053	13	.49	175
6.0	.88	136	-0.8	.91	-5	-23.6	.066	0	.52	160
7.0	.89	122	-2.5	.75	-25	-23.4	.068	-7	.56	144
8.0	.89	114	-4.2	.62	-39	-22.7	.073	-13	.62	132
9.0	.88	109	-5.5	.53	-52	-22.2	.078	-18	.68	124
10.0	.86	103	-6.7	.46	-64	-20.9	.090	-24	.72	118
11.0	.81	91	-6.9	.45	-78	-19.3	.108	-33	.73	112
12.0	.77	74	-7.5	.42	-95	-17.2	.138	-49	.73	101

A model for this device is available in the DEVICE MODELS section.

100 mil Flange Dimensions





Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ± 0.005
   mm .xx = ± 0.13

Package marking code is 441

HEWLETT® PACKARD

2–8 GHz Medium Power Gallium Arsenide FET

Technical Data

ATF-45101

Features

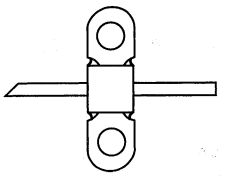
- **High Output Power:** 29.0 dBm Typical $P_{1\,dB}$ at 4 GHz
- **High Gain at 1dB Compression:** 10.0 dB Typical $G_{1\,dB}$ at 4 GHz
- **High Power Efficiency:** 38% Typical at 4 GHz
- **Hermetic Metal-Ceramic Stripline Package**

Description

The ATF-45101 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 8 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 2.5 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

This device is suitable for applications in space, airborne, military ground and shipboard, and commercial environments. It is supplied in a hermetic high reliability package with low parasitic reactance and minimum thermal resistance.

100 mil Flange Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz f = 8.0 GHz	dBm	28.0	29.0 28.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz f = 8.0 GHz	dB	9.0	10.0 4.0	
η_{add}	Efficiency @ P_{1dB}: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz	%		38	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 250 mA		mmho		200	
I_{DSS}	Saturated Drain Current: V_{DS} = 1.75 V, V_{GS} = 0 V		mA	400	600	800
V_P	Pinch-off Voltage: V_{DS} = 2.5 V, I_{DS} = 12.5 mA		V	-5.4	-4.0	-2.0

ATF-45101 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+14
V_{GS}	Gate-Source Voltage	V	-7
V_{GD}	Gate-Drain Voltage	V	-16
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	W	3.6
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 42°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[4]

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 24 mW/°C for T_{CASE} > 24°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

ATF-45101 Typical Performance, T_A = 25°C

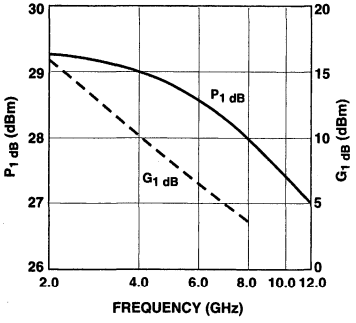


Figure 1. Power Output @ 1 dB Gain Compression and 1 dB Compressed Gain vs. Frequency. V_{DS} = 9 V, I_{DS} = 250 mA.

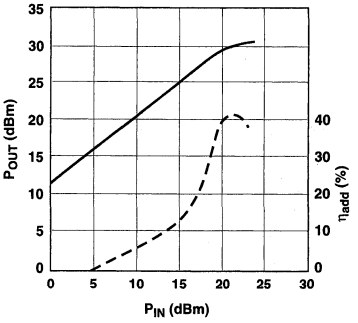


Figure 2. Output Power and Power Added Efficiency vs. Input Power. V_{DS} = 9 V, I_{DS} = 250 mA, f = 4.0 GHz.

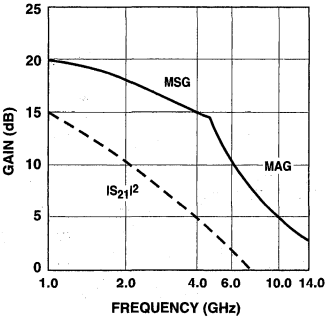


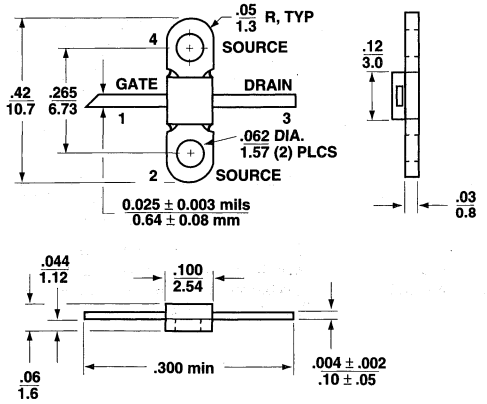
Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 9 V, I_{DS} = 250 mA.

Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{DS} = 9\ V$, $I_{DS} = 250\ mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
1.0	.89	-88	14.9	5.54	119	-26.2	.049	43	.31	-63
2.0	.83	-135	10.8	3.48	82	-26.0	.050	18	.33	-108
3.0	.81	-158	7.6	2.40	58	-25.8	.051	7	.39	-129
4.0	.84	-174	5.4	1.86	38	-25.5	.053	3	.46	-144
5.0	.82	-170	3.8	1.55	18	-25.2	.055	-2	.50	-154
6.0	.81	152	2.6	1.36	-2	-24.4	.060	-8	.52	-168
7.0	.81	133	1.2	1.15	-25	-23.9	.064	-15	.55	173
8.0	.81	122	-0.3	.97	-42	-23.5	.067	-20	.59	154
9.0	.80	113	-1.8	.81	-60	-22.6	.074	-31	.64	137
10.0	.79	107	-3.2	.69	-73	-22.0	.079	-40	.68	123
11.0	.77	94	-4.6	.59	-91	-21.5	.084	-45	.72	113
12.0	.73	82	-5.8	.51	-106	-20.3	.097	-55	.76	99
13.0	.68	69	-6.7	.46	-123	-18.3	.121	-63	.78	89
14.0	.64	56	-7.1	.44	-137	-15.9	.161	-79	.80	79

A model for this device is available in the DEVICE MODELS section.

100 mil Flange Package Dimensions



Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ± 0.005
   mm .xx = ± 0.13

Package marking code is 451

HEWLETT® PACKARD

2–8 GHz Medium Power Gallium Arsenide FET

Technical Data

ATF-45171

Features

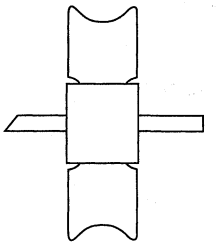
- **High Output Power:** 29.0 dBm Typical $P_{1\,dB}$ at 4 GHz
- **High Gain at 1dB Compression:** 10.5 dB Typical $G_{1\,dB}$ at 4 GHz
- **High Power Efficiency:** 38% Typical at 4 GHz
- **Hermetic Metal-Ceramic Stripline Package**

Description

The ATF-45171 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 8 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 2.5 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

This device is suitable for applications in space, airborne, military ground and shipboard, and commercial environments. It is supplied in a hermetic high reliability package with low parasitic reactance and minimum thermal resistance.

70 mil Flange Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression:	f = 4.0 GHz	dBm	28.0	29.0	
	V_{DS} = 9 V, I_{DS} = 250 mA	f = 8.0 GHz			28.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz	dB	9.5	10.5	
		f = 8.0 GHz			4.5	
η_{add}	Efficiency @ $P_{1\,dB}$: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz	%		38	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 250 mA		mmho		200	
I_{DSS}	Saturated Drain Current: V_{DS} = 1.75 V, V_{GS} = 0 V		mA	400	600	800
V_P	Pinch-off Voltage: V_{DS} = 2.5 V, I_{DS} =12.5 mA		V	-5.4	-4.0	-2.0

5965-8734E

ATF-45171 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+14
V_{GS}	Gate-Source Voltage	V	-7
V_{GD}	Gate-Drain Voltage	V	-16
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	W	3.6
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 42°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 µm Spot Size[4]

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 24 mW/°C for T_{CASE} > 24°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

ATF-45171 Typical Performance, T_A = 25°C

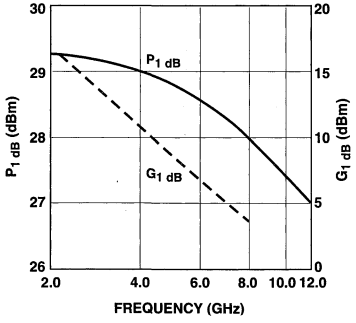


Figure 1. Power Output @ 1 dB Gain Compression and 1 dB Compressed Gain vs. Frequency. V_{DS} = 9 V, I_{DS} = 250 mA.

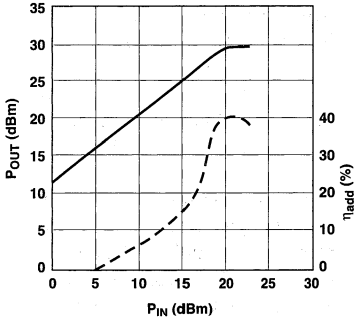


Figure 2. Output Power and Power Added Efficiency vs. Input Power. V_{DS} = 9 V, I_{DS} = 250 mA, f = 4.0 GHz.

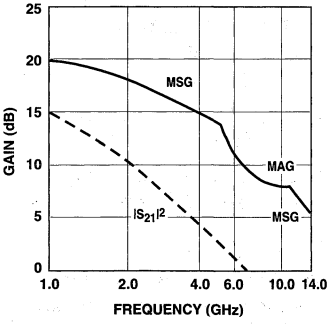


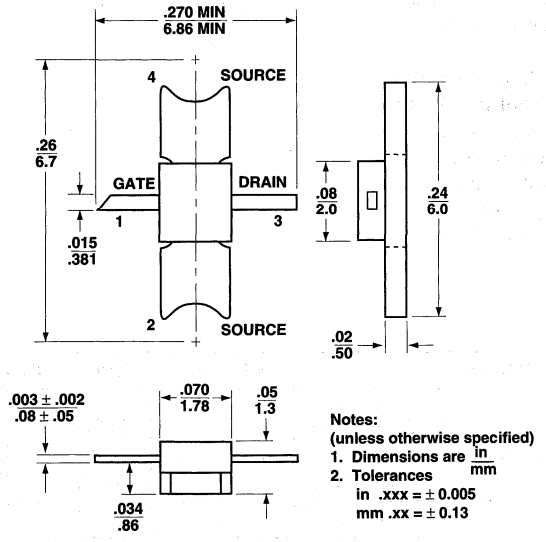
Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 9 V, I_{DS} = 250 mA.

Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{DS} = 9$ V, $I_{DS} = 250$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
1.0	.91	-83	14.5	5.30	122	-26.7	.046	46	.37	-46
2.0	.83	-137	10.8	3.45	83	-26.4	.048	19	.26	-91
3.0	.83	-167	7.4	2.34	54	-26.0	.050	5	.31	-131
4.0	.86	174	4.4	1.66	32	-25.5	.053	2	.43	-155
5.0	.86	162	2.1	1.28	12	-25.1	.055	0	.52	-167
6.0	.85	152	0.7	1.09	-3	-24.7	.058	-2	.56	-176
7.0	.84	138	0.1	1.01	-22	-24.4	.060	-6	.59	173
8.0	.84	124	-0.9	.90	-40	-23.8	.064	-13	.62	154
9.0	.85	114	-2.5	.75	-59	-23.4	.068	-19	.66	135
10.0	.85	106	-4.3	.61	-70	-22.5	.075	-25	.71	123
11.0	.85	100	-5.2	.55	-81	-21.6	.083	-30	.76	119
12.0	.83	95	-6.2	.49	-90	-20.8	.091	-39	.79	111
13.0	.80	76	-6.7	.46	-107	-19.3	.109	-50	.81	98
14.0	.77	59	-8.0	.40	-125	-18.9	.113	-61	.83	78

A model for this device is available in the DEVICE MODELS section.

70 mil Flange Package Dimensions



Package marking code is 451

HEWLETT® PACKARD

2–10 GHz Medium Power Gallium Arsenide FET

Technical Data

ATF-46101

Features

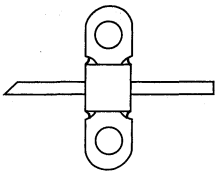
- **High Output Power:** 27.0 dBm Typical $P_{1\,dB}$ at 4 GHz
- **High Gain at 1 dB Compression:** 12.0 dB Typical $G_{1\,dB}$ at 4 GHz
- **High Power Efficiency:** 38% Typical at 4 GHz

Description

The ATF-46101 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 10 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 1.25 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

This device is suitable for applications in space, airborne, military ground and shipboard, and commercial environments. It is supplied in a hermetic high reliability package with low parasitic reactance and minimum thermal resistance.

100 mil Flange Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz f = 8.0 GHz	dBm	25.0	27.0 26.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz f = 8.0 GHz	dB	9.0	10.0 5.0	
η_{add}	Efficiency @ P_{1dB}: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz	%		38	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 125 mA		mmho		100	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	200	330	450
V_P	Pinch-off Voltage: V_{DS} = 2.5 V, I_{DS} = 5 mA		V	-5.4	-3.5	-2.0

Note:
1. RF Performance is determined by packaging and testing 10 samples per wafer.

ATF-46101 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+14
V_{GS}	Gate-Source Voltage	V	-7
V_{GD}	Gate-Drain Voltage	V	-16
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	W	2.0
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 75°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[4]

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 13 mW/°C for T_{CASE} > 25°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

ATF-46101 Typical Performance, T_A = 25°C

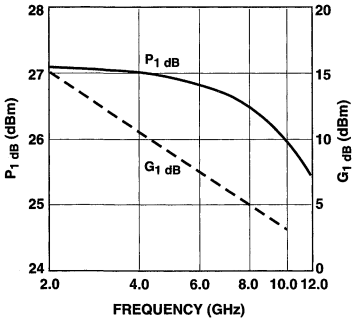


Figure 1. Power Output @ 1 dB Gain Compression and 1 dB Compressed Gain vs. Frequency. V_{DS} = 9 V, I_{DS} = 125 mA.

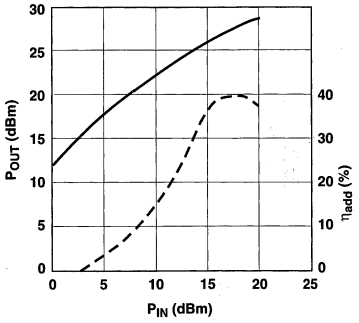


Figure 2. Output Power and Power Added Efficiency vs. Input Power. V_{DS} = 9 V, I_{DS} = 125 mA, f = 4.0 GHz.

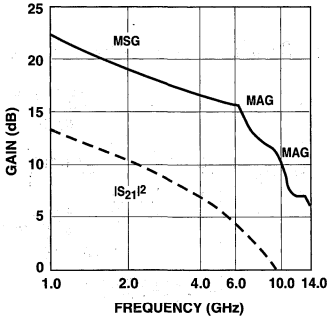


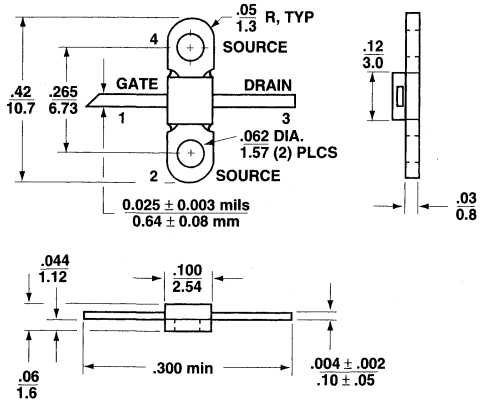
Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 9 V, I_{DS} = 125 mA.

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, T_A = 25°C, V_{DS} = 9 V, I_{DS} = 125 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
1.0	.94	-56	12.8	4.37	135	-31.4	.027	52	.64	-28
2.0	.86	-101	10.7	3.41	98	-27.3	.043	30	.59	-56
3.0	.82	-131	8.4	2.64	71	-26.9	.045	18	.58	-79
4.0	.82	-152	6.7	2.16	48	-26.4	.048	9	.62	-98
5.0	.80	-173	5.4	1.86	26	-26.0	.050	-1	.63	-112
6.0	.79	165	4.3	1.64	5	-25.8	.051	-12	.65	-126
7.0	.78	143	3.1	1.43	-18	-25.4	.054	-24	.65	-145
8.0	.78	131	1.6	1.20	-36	-24.7	.058	-37	.70	-166
9.0	.77	123	0.3	1.03	-55	-23.9	.064	-40	.73	173
10.0	.76	118	-1.2	.87	-72	-23.1	.070	-52	.76	158
11.0	.67	104	-2.0	.79	-91	-22.6	.074	-57	.79	146
12.0	.60	86	-2.7	.73	-110	-21.2	.087	-66	.83	136
13.0	.54	71	-3.5	.67	-133	-19.7	.104	-79	.87	124
14.0	.50	64	-4.0	.63	-154	-15.9	.160	-99	.92	115

A model for this device is available in the DEVICE MODELS section.

100 mil Flange Package Dimensions



Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ± 0.005
   mm .xx = ± 0.13

Package marking code is 461

HEWLETT® PACKARD

2–10 GHz Medium Power Gallium Arsenide FET

Technical Data

ATF-46171

Features

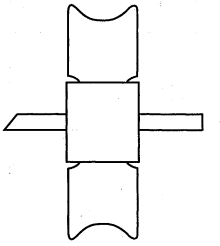
- **High Output Power:** 27.0 dBm Typical $P_{1\,dB}$ at 4 GHz
- **High Gain at 1 dB Compression:** 11.0 dB Typical $G_{1\,dB}$ at 4 GHz
- **High Power Efficiency:** 38% Typical at 4 GHz
- **Hermetic Metal-Ceramic Stripline Package**

Description

The ATF-46171 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 10 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 1.25 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

This device is suitable for applications in space, airborne, military ground and shipboard, and commercial environments. It is supplied in a hermetic high reliability package with low parasitic reactance and minimum thermal resistance.

70 mil Flange Package



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz f = 8.0 GHz	dBm	25.0	27.0 26.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz f = 8.0 GHz	dB	10.0	11.0 6.0	
η_{add}	Efficiency @ P_{1dB}: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz	%		38	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 125 mA		mmho		100	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	200	330	450
V_P	Pinch-off Voltage: V_{DS} = 2.5 V, I_{DS} = 5 mA		V	-5.4	-3.5	-2.0

5965-8729E

ATF-46171 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	+14
V_{GS}	Gate-Source Voltage	V	-7
V_{GD}	Gate-Drain Voltage	V	-16
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	W	2.0
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Thermal Resistance:	θ_{jc} = 75°C/W; T_{CH} = 150°C
Liquid Crystal Measurement:	1 µm Spot Size[4]

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE\ TEMPERATURE}$ = 25°C.
3. Derate at 13 mW/°C for T_{CASE} > 25°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

ATF-46171 Typical Performance, T_A = 25°C

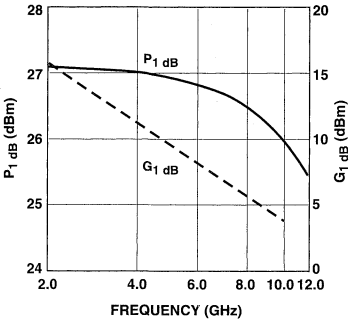


Figure 1. Power Output @ 1 dB Gain Compression and 1 dB Compressed Gain vs. Frequency. V_{DS} = 9 V, I_{DS} = 125 mA.

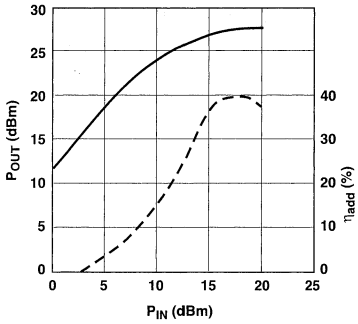


Figure 2. Output Power and Power Added Efficiency vs. Input Power. V_{DS} = 9 V, I_{DS} = 125 mA, f = 4.0 GHz.

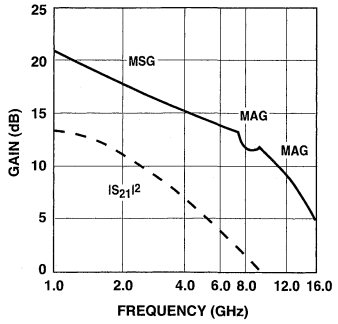


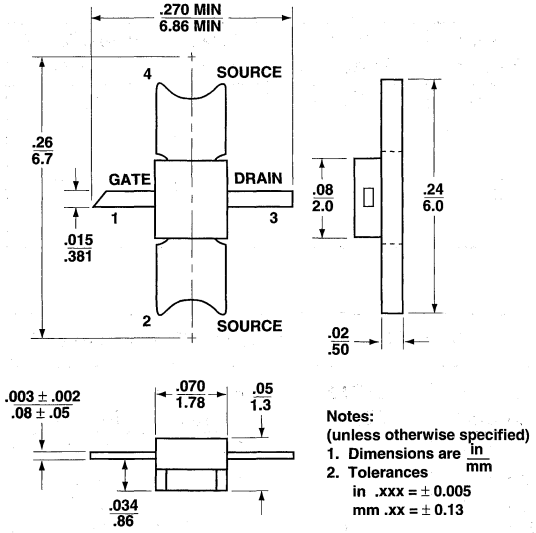
Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. V_{DS} = 9 V, I_{DS} = 125 mA.

Typical Scattering Parameters, Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{DS} = 9$ V, $I_{DS} = 125$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
1.0	.95	-54	12.7	4.30	138	-29.4	.034	63	.71	-22
2.0	.84	-106	11.0	3.56	99	-26.7	.046	30	.60	-44
3.0	.81	-145	8.9	2.80	67	-25.7	.052	13	.52	-71
4.0	.81	-172	6.6	2.14	40	-25.0	.056	2	.52	-101
5.0	.80	171	4.6	1.70	18	-24.4	.060	-3	.58	-122
6.0	.79	159	3.1	1.44	1	-24.0	.063	-6	.63	-135
7.0	.78	141	2.2	1.29	-18	-23.5	.067	-10	.63	-147
8.0	.77	123	1.4	1.17	-36	-23.0	.071	-14	.64	-164
9.0	.79	108	-0.1	.99	-58	-22.5	.075	-17	.67	171
10.0	.79	100	-1.4	.85	-73	-22.0	.079	-21	.74	152
11.0	.78	93	-2.5	.75	-86	-21.6	.083	-24	.76	142
12.0	.76	85	-3.5	.67	-97	-20.6	.093	-32	.79	133
13.0	.73	67	-4.3	.61	-118	-19.5	.106	-49	.80	119
14.0	.71	47	-5.8	.51	-138	-19.0	.112	-66	.83	98
15.0	.73	35	-7.5	.42	-157	-18.6	.118	-71	.85	83
16.0	.75	26	-8.9	.36	-157	-18.3	.121	-78	.90	72

A model for this device is available in the DEVICE MODELS section.

70 mil Flange Package



Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ± 0.005
   mm .xx = ± 0.13

Package marking code is 461

HEWLETT® PACKARD

Low Noise Gallium Arsenide FET

Reliability Data

ATF-10XXX
ATF-13XXX

Description

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-883. Data was gathered from the product qualification, reliability monitor, and engineering evaluation for the LYG GaAs process. For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

Test Name	Test Condition	Units Tested	Total Device Hrs.	Total Failed	Failure Rate (%/1K Hours)
High Temperature Operating Life (O.L.)	Nominal Bias at T_{ch} = 175°C, 1000 hrs.	150	15,000	0	0
High Temperature Storage (HTS)*	Ambient Temperature T_A = 150°C, 1000 hrs.	225	225,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.2eV, and the device thermal resistance of the stress board is 130°C/W, and listed in the following table.

Junction Temp. T_J (°C)	Point(1)		90% Confidence Level(2)	
	MTTF* (hours)	MTTF FIT(3)	MTTF (hours)	FIT(3)
175	3×10^{-6}	333	0.5×10^{-6}	2000
150	2×10^{-7}	50	9.5×10^{-8}	105
100	2×10^{-9}	.05	9.5×10^{-8}	1.05
47	8×10^{-11}	.001	3.5×10^{-11}	.0003

*MTTF data calculated from high temperature Operating Life tests.

C. Example of Failure Rate Calculation:

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

$(5 \times 10^{-10}) \times (25\%) \times (8760 \text{ hrs/yr}) = 1.1 \times 10^{-6}$ % per year

Likewise, the 90% confidence level failure rate per year is:

$(1.0 \times 10^{-9}/\text{hr}) \times (25\%) \times (8760 \text{ hrs/yr}) = 2.2 \times 10^{-6}$% per year

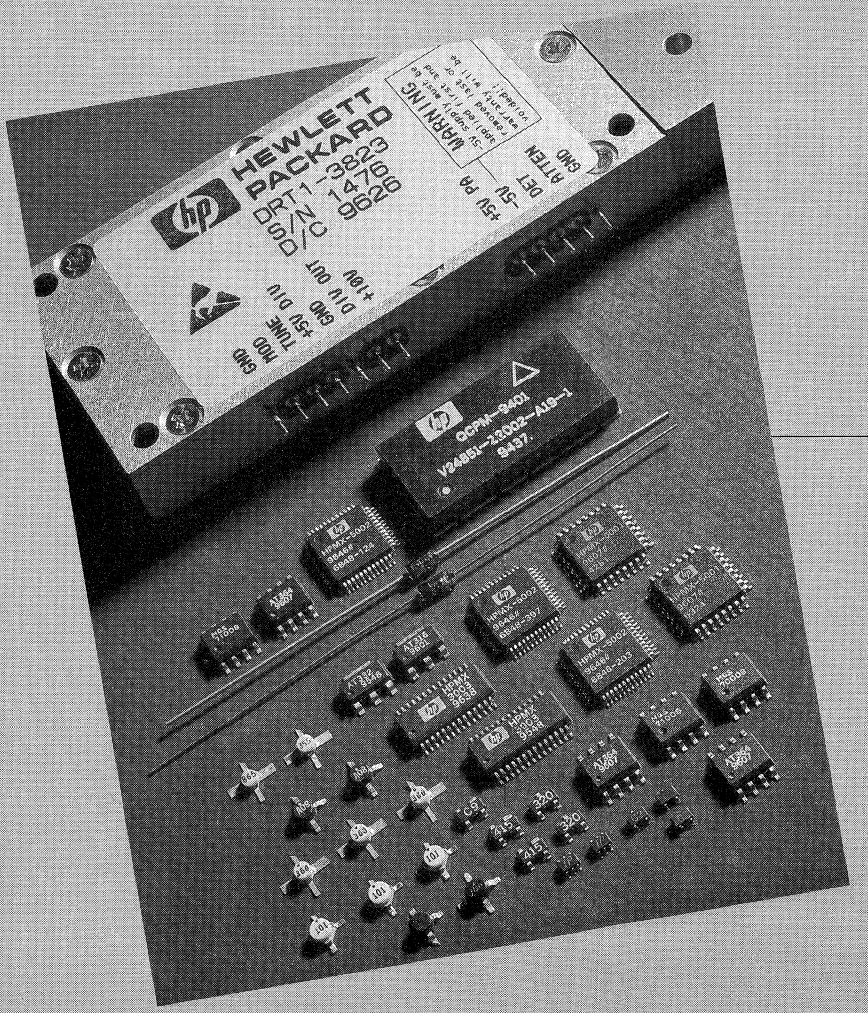
2. Environmental Tests

Test Name	MIL-STD-883 Reference	Test Conditions	Units Tested	Units Failed
Thermal Shock	1011	-65/150°C, 100 cycles	368	0
Temperature Cycle	1010	-65 to 150°C, 100 cycles	368	0
Moisture Resistance	—	+121°C, 100% RH, 96 hrs	290	0
Mechanical Shock*	2002	1500 G's, 0.5 msec. Pulse	135	0
Acceleration*	2001	20,000 G's, 1 min. all axis	135	0
Solderability	2003	245°C, 5 seconds dwell	245	0

* Applicable to ceramic packages only

HEWLETT® PACKARD

RFIC and MMIC Amplifiers



RFIC and MMIC Amplifiers

Characteristics

Hewlett-Packard offers a broad line of Radio Frequency Integrated Circuit (RFIC) and Monolithic Microwave Integrated Circuit (MMIC) amplifiers for use in all aspects of the communications industry.

Processes

A variety of processes are used to fabricate Hewlett-Packard RFICs and MMICs. These processes are specifically designed to optimize each product family for maximum performance.

SAT process:
Hewlett-Packard's state-of-the-art 10 GHz f_T, 25 GHz f_{MAX} silicon transistor process is used to manufacture the MSA line of RFIC amplifiers. Diffused resistors are added to this joined-backside-collector process to create RF feedback and bias elements.

ISOSAT Process:
Trench isolation is coupled with the SAT transistor engine to create a process optimized for high speed analog integrated circuits. Material and processing enhancements raise the nominal f_T of this process to above 15 GHz. Design flexibility is enhanced through the addition of second metal capability, and by the availability of such on-chip elements as capacitors, diodes, and high valued resistors. This process also utilizes polyimide as an inter-metal dielectric and scratch protection.

MESFET process:
Hewlett-Packard has a number of Gallium Arsenide MESFET processes, variously optimized for gain, noise performance, or power.

PHEMT process:
GaAs MMICs processed using this technology are targeted for markets putting a premium on low noise figure and improved device-to-device consistency.

Product Families

The HMMC series of GaAs MMICs are designed for high performance applications in the microwave and millimeter wave frequency ranges. These devices, supplied only as chips, are fabricated on the MESFET and PHEMT processes. MMIC amplifiers are available in a variety of combinations of performance with frequencies up to 50 GHz, output power up to +19 dBm, and noise figure as low as 2.5 dB.

The HPMX-3002 is a special purpose medium power amplifier designed for driver applications in the 150 to 960 MHz range. This device, fabricated on the ISOSAT process, also incorporates a power control feature.

The INA series is a family of multi-stage, matched RFIC amplifiers featuring high gain and low noise figure. These general purpose amplifiers are broad-band in nature and provide a simple solution to many LNA and IF applications. INA amplifiers are fabricated on the ISOSAT process.

The IVA series of RFIC amplifiers are fabricated on the ISOSAT process and feature variable gain for use in applications such as AGC.

The MGA family of integrated circuit amplifiers are fabricated with the MESFET and PHEMT processes. These products offer a wide range of performance features up to high frequencies, including low noise figure and medium output power. Amplifiers

in the MGA series are either matched or partially matched to 50 Ω.

The MSA series of RFIC amplifiers are two-transistor Darlington feedback, 50 Ω gain blocks. These simple ICs, fabricated on the SAT process, provide the designer with a wide selection of easy to use broad-band, general purpose amplifiers suitable for many different RF and IF applications. Members of this family are differentiated by output power, noise figure, bias requirements, and specialty performance features such a bandwidth or dynamic range.

Application Information

The following application information is either published in this catalog or available from your local Hewlett-Packard sales office, authorized distributor, or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

Application Notes

Abstracts

HEWLETT® PACKARD

Using the MGA-87563 GaAs MMIC in Low Noise Amplifier Applications in the 800 Through 2500 MHz Frequency Range

Application Note 1116

Introduction

This application note describes the use of the Hewlett-Packard MGA-87563 in low noise amplifier (LNA) applications in the 800 through 2500 MHz frequency range. The MGA-87563 is capable of producing an LNA with a 1.6 dB noise figure and 12 dB of associated gain when biased at 4.5 mA from a 3 volt power supply. This IC is housed in a miniature inexpensive plastic surface mount SOT-363 (SC-70) package.

LNA Designs

Three LNA designs will be presented in this application note. The first design covers the 800 to 950 MHz frequency range, and can be used for cellular, paging, or 902-928 MHz ISM applications. The second design covers the commercial GPS frequency at 1575 MHz. The third design covers the 2400 to 2500 MHz frequency range for ISM applications. These designs can easily be scaled to other frequencies using the basic design information presented here.

All LNAs described here were designed using HP-EESOF's Touchstone™ for Windows and the S and Noise parameter data published in the MGA-87563 data sheet. The reference plane for both the S and Noise parameters is shown in Figure 1.

The layout for the amplifiers is shown in Figure 2. The layout is intended to be a general prototype board that can be adapted for various frequencies.

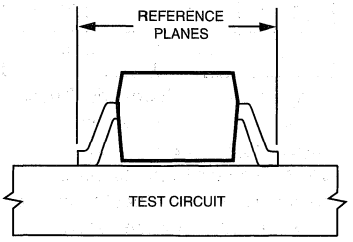


Figure 1. Reference plane for MGA-87563 S and Noise Parameter data.

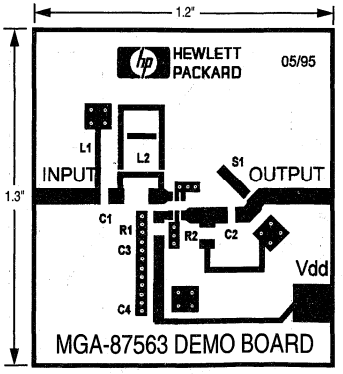


Figure 2. MGA-87563 Demonstration Board.

900 MHz LNA Design

The 900 MHz circuit was designed to achieve optimal noise performance in the 900 to 950 MHz frequency range. The component labels appearing in the following paragraphs refer to the positions indicated in Figure 2.

The input match was designed to present Γ_{opt}, as defined by the device noise parameters, to the input of the MGA-87563. This match consists of a 100 pF blocking capacitor at C1 followed by an 18 nH series lumped inductor (Coilcraft, Cary, Ill. part number 1008CS-180). Both of the etched inductors L1 and L2 are removed from the board by carefully using a sharp knife to sever the traces from the through transmission lines. The 18 nH inductor bridges the same transmission line segments as did the now removed L2.

The output match consists of a series 10 pF capacitor at C2 and a shunt RL network. The inductor of the RL is board etch; the resistor is 10 Ω at R2. A 16 Ω resistor at R1 provides bias decoupling and port termination. The bypass capacitor at C3 should be 100 pF. The bypass capacitor at C4 provides additional decoupling that may be

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required when cascading several active gain stages; a high value (1000 pF or greater) should be used.

The noise and gain performance of this 900 MHz LNA was measured using a Hewlett-Packard 8970A noise figure meter. The MGA-87563 was biased at a device voltage of 3 volts, resulting in a device current of 4.5 mA. The resulting performance is shown in Table I.

Gain and return loss information was also measured using a scalar analyzer. Figure 3 shows the LNA has a nominal 15 dB of gain from 800 to 1000 MHz. Figure 4 shows the output return loss to be 26 dB at 850 MHz and greater than 20 dB from 750 to 900 MHz. Figure 5 shows the input return loss to be 8.5 dB at 850 MHz.

The amplifier output third order intercept point (IP_3) was then measured. The results are summarized in Table II. The first two measurements were taken by varying the supply voltage to the circuit just described. Raising the supply voltage has only a minor effect on IP_3. For the last two measurements, a double-stub tuner was attached to the output port of the circuit and adjusted to minimize third order distortion. These measurements indicate that improving the output loadline will add several dB to the linear output power. They also indicate that the resistive output loading at R2 lowers the linear output power significantly.

Table I - 900 MHz LNA, Gain and Noise Figure performance with V_d = 3 V

Freq. (MHz)	Gain (dB)	Noise Figure (dB)
400	0.66	6.50
500	4.66	4.62
600	9.56	3.45
700	12.47	2.77
800	14.78	2.35
850	15.20	2.22
900	15.37	2.14
950	15.22	2.08
1000	14.87	2.09
1050	14.41	2.13
1100	13.76	2.18
1150	12.90	2.32
1200	12.34	2.50
1300	11.29	2.97
1400	10.98	3.70

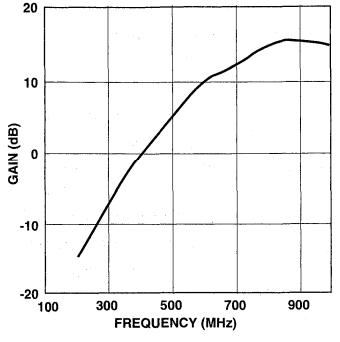


Figure 3. 900 MHz LNA, associated gain at minimum noise figure with V_d = 3 V

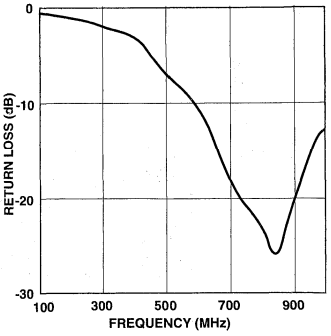


Figure 4. 900 MHz LNA, output return loss with V_d = 3 V

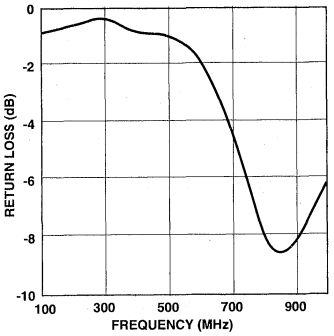


Figure 5. 900 MHz LNA, input return loss with V_d = 3 V

Table II . 900 MHz LNA IP_3 performance under varying conditions.

Device Voltage	Output IP_3	Conditions
3 V	+6 dBm	S22 conjugate match
5 V	+7 dBm	S22 conjugate match
5 V	+9 dBm	W/ output double stub tuner and R2 = 10 Ω
5 V	+12 dBm	W/ output tuner and R2 = 0 Ω

GPS LNA Design

The GPS LNA circuit was designed to achieve optimal noise performance at 1575 MHz. The component labels appearing in the following paragraphs refer to the positions indicated in Figure 2.

The input match was designed to present Γ_{opt} at 1575 MHz, as defined by the device noise parameters, to the input of the MGA-87563. The match consists of a series inductor, implemented using the entire etched trace on the circuit board at L2. This is accomplished by cutting out the small horizontal piece of transmission line at L2 and then jumpering in the

longer "trombone section". The combined total length of the "trombone section" at L2 will be approximately 0.8". The shunt inductor at L1 is removed for operation at frequencies below 2 GHz.

The output match of the MGA-87563 is sufficiently good at 1575 MHz that no additional output matching was needed.

A value of 100 pF was used for both the input (C1) and output (C2) blocking capacitors. A 25 Ω resistor at R1 provides bias decoupling and port termination. The bypass capacitor at C3 should be 100 pF. The bypass capacitor at C4 provides additional decoupling that may be required when cascading several active gain stages; a high value (1000 pF or greater) should be used. If desired, a 50 Ω resistor placed at R2 will provide low frequency loading of the device. This termination reduces low frequency gain and enhances low frequency stability.

The performance of the LNA at a device voltage of 5 volts is shown in Table III.

2400 MHz LNA Design

The 2400 MHz LNA was designed to provide an optimum noise match from 2400 through 2500 MHz, making it useful for applications that operate in the 2400 to 2483 MHz ISM band. The component labels appearing in the following paragraphs refer to positions shown in Figure 6. The input match consists of a shunt inductor at L1 and a series inductor at L2. Both of these inductors use the traces as originally etched on the circuit board shown in Figure 2 without modification. The output is conjugately matched with a simple shunt open circuited stub (S1) on the output 50 Ω microstripline. The open circuited stub (S1) will have to be jumpered into the circuit with a piece of foil. 22 pF capacitors were used for both the input (C1) and output (C2) blocking capacitors.

A 16 Ω chip resistor placed at R1 and decoupled by a 100 pF capacitor at C3 provides a proper termination for the device power terminal. An additional bypass capacitor (100 to 1000 pF) placed further down the power supply line at location C4 may be required to further decouple the supply terminal especially if this stage is to be cascaded with an additional stage. Proper decoupling of device V_{CC} terminals of cascaded amplifier stages is required if stable operation is to be obtained.

If desired, a 50 Ω resistor placed at R2 will provide low frequency loading of the device. This termination reduces low frequency gain and enhances low frequency stability.

The MGA-87563 has 3 ground leads, all of which need to be well grounded for proper RF performance. This can be especially critical at 2.4 GHz where common lead inductance can significantly decrease gain.

The performance of the GPS LNA as measured on the HP 8970 Noise Figure Meter is shown in Table IV.

At 2.4 GHz, the loss of the FR-4/G-10 epoxy glass material can add several tenths of a dB to noise figure and lower gain by double the amount. Taking this into account,

Table III - GPS LNA, Gain and Noise Figure performance with V_d = 5 V.

Freq. (MHz)	Gain (dB)	Noise Figure (dB)
1000	11.88	2.97
1100	12.16	2.60
1200	11.80	2.45
1300	12.59	2.20
1400	14.16	2.18
1500	14.38	2.02
1600	14.97	2.02

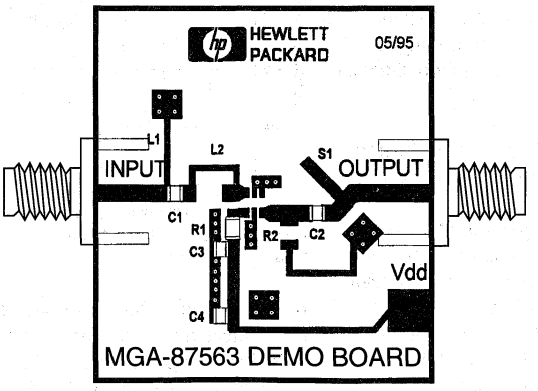


Figure 6. LNA showing component placement for 2.4 GHz.

Table IV . 2400 MHz LNA NF and Ga with V_d = 3.

Freq. (MHz)	Gain (dB)	Noise Figure (dB)
1700	10.4	2.60
1800	13.8	2.57
1900	11.3	2.45
2000	11.9	2.38
2100	13.3	2.06
2200	12.8	2.02
2300	12.9	2.12
2400	11.5	2.05
2500	11.5	2.14
2600	10.5	2.25
2700	10.9	2.29
2800	10.3	2.33
2900	9.8	2.35
3000	9.6	3.42

the performance of the LNA shown in Table IV, which includes board losses, agrees very well with data sheet performance.

The following swept plots were taken on a scalar analyzer. Figure 7 shows 12 dB gain from 2400 to 2500 MHz. Figure 8 shows the output return loss to be between 20 and 21 dB from 2400 to 2500 MHz. Figure 9 shows the input return loss to be 8 dB from 2400 to 2500 MHz.

The 2.4 GHz amplifier was tested for third order intermodulation distortion (IP_3) performance. Two signals were injected into the amplifier at an individual power level of approximately -26.3 dBm. At the output of the amplifier, the desired signals were at a power level of -14.8 dBm and the undesired third order signals were averaged at -53.5 dBc. This results in a IP_3 of +12 dBm referenced to the output port. The bias point for these measurements was 5.6 mA at a device voltage of 3 volts. The P1dB was also measured and found to be at -2 dBm referenced to the output.

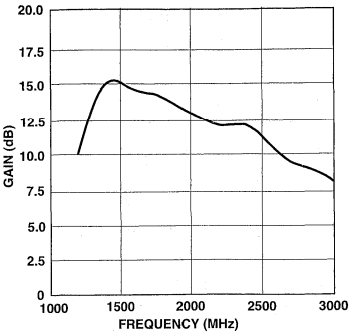


Figure 7. 2400 MHz LNA associated gain at minimum noise figure with V_d = 5 V

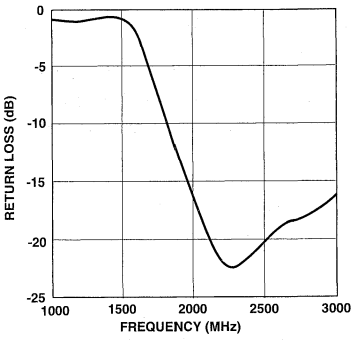


Figure 8. 2400 MHz LNA output return loss with V_d = 5 V

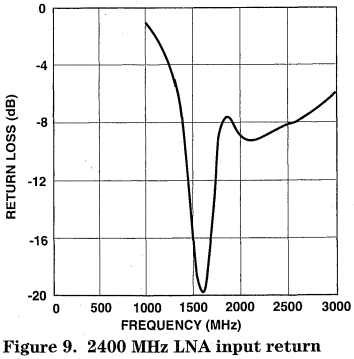


Figure 9. 2400 MHz LNA input return loss with V_d = 5 V

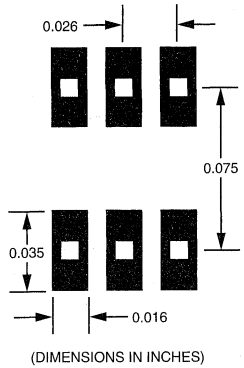


Figure 10. PCB Pad Layout.

SOT-363 PCB Layout

PCB pad layout for the miniature SOT-363 (SC-70) package is shown in Figure 10. Dimensions are in inches. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads.

Conclusion

The MGA-87563 can provide low noise amplification with minimal current draw for a wide variety of battery-powered applications. Circuits for 900 MHz, 1575 MHz, and 2400 MHz have been demonstrated.

Biasing MSA Series RF Integrated Circuits

Application Note S003

Bias Point Selection

Like discrete transistors, the MSA Series of RF Integrated Circuits can be operated at different bias points to achieve different performance results. These Monolithic Silicon Amplifiers have an internal structure consisting of a Darlington connected pair of bipolar transistors embedded in a matrix of resistors. Since this structure is current controlled, the bias point of an MSA can best be described by specifying the total device current, I_d.

Both power and gain can be adjusted by varying I_d. Curves of typical performance as a function of bias are shown on the individual MSA data sheets. Table 1 lists the range of bias currents over which the various MSAs can be expected to operate. The column labeled "Minimum Recommended Operation" represents the lowest level at which HP recommends operating the MSA. Operation of the MSA below this threshold causes the IC to be partially turned off; performance becomes unpredictable, and stability problems can result when the device is operated over temperature. There is no intrinsic reliability problem associated with operation below this bias level, however. The column labeled "Guaranteed Performance" lists the bias level at which HP specifies and tests device performance. It represents a "typical" operating bias point. The "Maximum Recommended Operation" column lists HP's recommendation for the highest level of bias for the MSA. In particular, significant improvements in P_{1dB} and (to a lesser extent) gain can be obtained for the MSA-06 and

Table 1. MSA Typical Operating Currents

Geometry	Minimum Recommended Current (mA)	Guaranteed Performance (mA)	Maximum Recommended Current (mA)	Absolute Maximum (mA)
01	13	17	25	40
02	18	25	40	60
03	20	35	50	80
04	30	50	70	85–100
0420	30	90	110	120
05	60	80	100	135
0520	80	165	200	225
06	12	16	20–25	40–50
07	15	22	30–40	60–50
08	20	36	40	80–65
09/99	25	35	45	80
10	150	325	400	425
11	40	60	70–75	80–100
20	—	32	—	50
31	—	29	—	50

MSA-07 geometries when operated at higher currents – refer to the product data sheets for more information. Typically operation at currents above the "maximum recommended" level yields minimal returns in terms of improved performance, and causes a noticeable decrease in device life expectancy. HP suggests that this value be used as an upper limit when selecting device operating point. The "Absolute Maximum" column lists the value of I_d beyond which catastrophic device failure can be anticipated. It represents the most current the MSA can ever be expected to handle without being destroyed.

In general, the maximum device current ratings are thermally limited. The thermal conductivity properties of the 200 mil BeO (20) package are good enough to allow a chip mounted in this package to be rated significantly higher in current handling capability than the same chip mounted in any of the other package options. Conversely, the thermal properties of the plastic packages (04, 05, 85, 86, and especially 11) requires a lowering of the maximum allowable current. For this reason some devices have ranges of "maximum recommended" and "absolute maximum" currents; refer to the individual product data sheets for details. The style 20 package performance is sufficiently different to be listed separately in Table 1.

Bias Circuitry Options

Once an appropriate bias point has been chosen, circuitry must be provided to ensure that the MSA operates at that bias point. To be effective, this circuitry must establish an appropriate bias point across the entire operating temperature range the MSA will experience. The internal resistors on the MSA have a temperature coefficient of –0.08%/°C; the on-chip transistors increase in β at a rate of +0.7%/°C. If the bias current I_d is to remain constant over a broad temperature range, the bias circuitry must decrease the device voltage V_d at higher temperatures and increase V_d at lower temperatures.

A number of possible biasing schemes are described in detail below.

Voltage Source On Collector

The simplest bias scheme available is to provide a fixed voltage to the "collector" or output terminal of the MSA. This voltage can be supplied either from a voltage regulator or from a power supply. It must be provided through an RFC (Radio Frequency "Choke," or high-value inductor) to keep the high frequency signal isolated from the DC circuitry. A large-value capacitor (e.g., 1 μF) should be connected from the DC side of the RFC to Ground to provide a low-impedance path to any signal that does get past the RFC. DC blocking capacitors (or alternatively transformers, if the MSA is to be operated at very low frequencies or at DC) must be used to isolate both the input of the MSA from the drive source and the output of the MSA from the load. The entire circuit is shown in Figure 1.

Because of its very narrow temperature operating range and sensitivity to V_d this bias scheme is not appropriate for most production circuits. It finds its major applications in laboratory testing of devices utilizing variable power supplies to provide the bias. With this bias scheme, temperature variations on the order of 25°C will cause significant alterations in performance; temperature variations on the order of 75°C can destroy devices by causing them to draw too much current. Device-to-device variations may also yield a MSA that draws an excessively high current if V_d is fixed, even at room temperature.

Collector Bias Stabilization Resistor

The fixed collector voltage bias circuit described above can be changed into a temperature-compensated bias circuit with the addition of a bias stabilization resistor in the collector feed. This resistor acts as a simple feedback element. As the temperature increases, the MSA tries to draw more and more current. Since this current is supplied through a resistor, the MSA bias voltage V_d decreases as I_d tries to increase: V_{CC} stays fixed; I_d increases with temperature causing the voltage drop $I_d R_C$ across R_C to increase, thus lowering V_d and "throttling back" on the bias current I_d.

Note that the amount of feedback is proportional to the voltage drop across R_C, and hence to the value of R_C. For effective compensation over normal operating temperature ranges (–25°C to +100°C), a voltage drop of at least 4 volts is recommended.

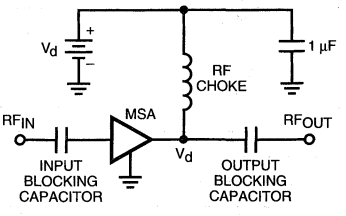


Figure 1. Fixed Collector Voltage Bias Circuit

Remember that R_C itself will change in resistance as the temperature changes. By selecting a bias resistor with an appropriate temperature coefficient the temperature compensation of this circuit can be "fine tuned." Carbon composite resistors typically have a temperature coefficient of +0.10%/°C, and work particularly well as bias stabilization resistors.

A side benefit of using a bias stabilization resistor is that it is often of high enough impedance that an RFC is no longer needed to keep the high frequency signal out of the DC bias. It is recommended that an RFC still be used if the MSA is being used near saturation; otherwise R_C appears in parallel with the load resistance and can cause enough of a shift in load impedance to reduce both gain and saturated power by 1 to 2 dB.

The circuitry needed for a bias stabilization resistor scheme is shown in Figure 2. MSAs were designed with this bias scheme in mind and many of the devices are available with R_C built onto the amplifier chip. Since devices incorporating internal bias stabilization resistors require independent access to the V_{CC} port, one ground lead is given up to make room for the extra connection that must now be provided. Some high-frequency performance is therefore sacrificed with these devices due to their increased common lead inductance.

± Supply Bias

Sometimes the designer does not have available the higher voltages necessary to use the bias stabilization resistor method described above, but does have available both positive and negative voltages. Under these circumstances the MSA may be DC "floated" and the difference between the two voltage supplies used to provide the voltage drop necessary to use a stabilization resistor. A schematic showing this technique is shown in Figure 3.

An RFC is needed in the path to the negative voltage supply, again to keep the RF signal separated from the DC. The most critical elements are the capacitors used to "float" the MSA. These must provide excellent high frequency grounding throughout the entire frequency range of operation. This means that large valued capacitors must be used to ensure good low frequency operation ($1/(2\pi fC) < 1\ \Omega$ at f_{min}), and that low parasitic inductance capacitors must be used to ensure good high frequency grounding ($2\pi fL) < 1\ \Omega$ at f_{max}). These requirements sometimes necessitate the use of multiple bypass capacitors. Typically, it is not possible to avoid some degradation in gain at higher frequencies if this bias scheme is used.

Active Bias

Active bias circuitry can be used to provide temperature stability without requiring the large voltage drop or relatively high dissipated power needed with a bias stabilization resistor. A simple realization using a resistively-biased PNP transistor as a current source is shown in Figure 4.

In this circuit R_1 and R_2 form a resistive divider that establishes the bias point of the PNP bias transistor. R_3 provides a "bleed path" for any excess bias current;

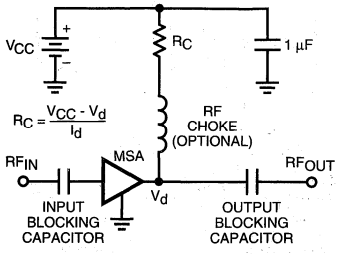


Figure 2. Collector Bias Stabilization Resistor Bias Circuit

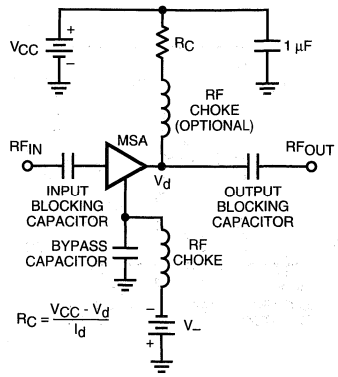


Figure 3. ± Power Supplies Bias Circuit

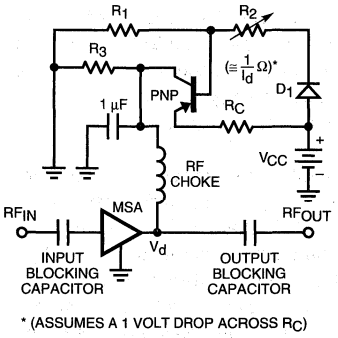


Figure 4. Active Bias Circuit

it is a safety feature that can be omitted from minimum element realizations of this circuit. D_1 is also an optional element; its purpose is to provide temperature compensation by tracking the voltage variation with temperature of the emitter-to-base junction of the PNP bias transistor. For this reason, when it is included it is often realized using the E-B junction of a second PNP transistor identical to the bias transistor, connected with its collector-base junction shorted.

R_C is a feedback element that keeps I_d constant. If the device current starts to increase, the voltage drop across R_C also increases, turning off the E-B junction of the PNP transistor, and hence decreasing the bias voltage V_d applied to the MSA. For best circuit operation, there should be at least a 0.5 to 1 volt drop across R_C. The PNP transistor is acting in the saturated mode with both junctions forward biased. The voltage drop needed across the emitter to collector junction of this transistor will therefore be equal to its $V_{CE\,sat}$ - typically only several tenths of a volt. Thus, the total voltage difference needed between V_{CC} and V_d is only about 1.3 volts for this circuit, as compared to the 4 volts or so needed by the bias stabilization resistor for good bias stability over temperature.

A side effect of the PNP bias transistor operating in the saturated mode is that this bias requires some extra "charge up" time at turn-on and "discharge" time at turn-off. How much extra time is required will depend on the time constants of the PNP transistor.

Systems requiring wide dynamic range operation or AGC (automatic gain control) often require that the MSAs operate at variable operating points. If R_2 is made variable, this bias scheme will work well for such applications.

Current Adjust Passive Bias

It is possible to design a simple passive bias circuit that allows the designer to adjust the MSA bias current I_d while using a fixed voltage power supply. This allows operation of the MSA at bias points other than those established by its internal bias circuitry, e.g., operation at the data sheet value of I_d but with a lower V_d than specified on the device data sheet. The schematic for such a circuit is shown in Figure 5.

This circuit works by supplying an external "base" voltage to the MSA that can be adjusted by using a variable resistor, R. Decreasing R will raise the voltage on the input of the IC, and hence increase its bias current. R must be connected in series with an RFC to prevent it from degrading the input impedance of the MSA.

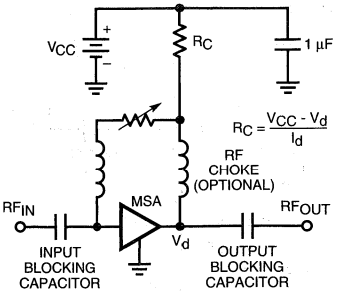


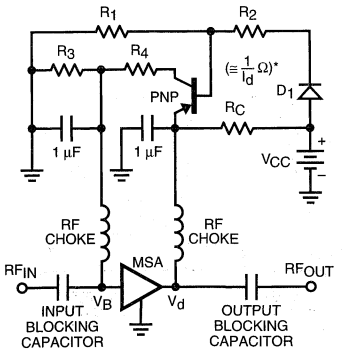
Figure 5. Current Adjust Passive Bias

Note that this circuit works only to increase the MSA bias current beyond some minimum value established by the device's internal bias resistors and the voltage V_d. If R were connected from the input of the MSA to ground (instead of to R_C), an analogous circuit that would decrease bias current as R was decreased in value would result.

Current Adjust Active Bias

Figure 6 shows a circuit that combines the features of adjustable (offset) bias current and active bias. The "base" voltage applied to the MSA is set by the output voltage of the PNP bias transistor. The bias applied to this PNP transistor is established by the voltage divider formed by R_1 and R_2. Adjusting the value of R_2 therefore determines the MSA bias current I_d.

R_4 is present to decrease the power dissipation of the bias transistor. Given the relatively low "collector" to "base" voltages required to operate most MSAs, this element can be omitted at the designer's discretion. R_3 once



* (ASSUMES A 1 VOLT DROP ACROSS R_C)

Figure 6. Current Adjust Active Bias Circuit

again serves as a bias current "safety bleed path."

RF chokes and bypass capacitors are used in both "collector" and "base" feeds to keep the DC and RF circuitry separate.

This circuit provides excellent bias stability over temperature. Due to the feedback function of R_C, increases in I_d resulting from rises in temperature are compensated for by a lowering of V_B. This results from the increased voltage drop across R_C turning off the PNP bias transistor.

Note that the "base" current provided to the MSA by the PNP is much less than the "collector" current of the MSA. This indicates that the PNP transistor is not operating in the saturated mode in this circuit, as it was in the active bias circuit described above. This circuit will therefore have a much faster response time than will the previously described active bias circuit.

An important consideration when using this circuit is that it changes bias point by changing bias load line, that is, it adjusts V_d and I_d simultaneously. This circuit is therefore not readily adaptable to situations where the designer wishes to continuously vary the operating point of the MSA. It is best suited for situations where the designer has a specific "non-standard" bias point in mind that must be closely maintained over temperature.

A saturated variant of this bias results if the RFC connecting the output of the MSA to the emitter of the PNP is moved to connect the output of the MSA to the collector of the PNP. Such a bias functions as a hybrid between the active bias scheme of Figure 4 and the current adjust passive bias of Figure 5. It allows operation from low voltage power supplies (minimum voltage drop required for the PNP, ability to raise I_d by decreasing R_4) while simultaneously allowing a sweeping of bias points for AGC type operation by varying R_2.

Conclusions

A variety of bias circuits that can be used with MSAs have been shown. The simplest scheme (a constant voltage source) is not acceptable for most applications because of poor temperature stability. The next simplest scheme (the bias stabilization resistor) is the most widely used bias method due to its low cost and stable performance over temperature. Its major drawback is the relatively large voltage drop required across the stabilization resistor for good bias stability over temperature. Bias schemes that address this problem by using two power supplies (± supply bias) or active bias (active bias circuit) were also shown. Finally, bias schemes that allow the user to alter the MSA operating point from the design operating point have been included (current adjust passive bias, current adjust active bias).

HEWLETT® PACKARD

INA Series RFIC Amplifiers

Application Note S012

Introduction

The INA series amplifiers are part of Hewlett-Packard's product line of silicon bipolar RF Integrated Circuits built with HP's ISOlated Self Aligned Transistor (ISOSAT™) process. These devices are 50 ohm cascadable gain blocks that feature high insertion gains and low noise figures. They represent an extension of the technology used in HP's MSA product family of RFIC amplifiers.

The INA Series Product Family

The INA part numbers impart information about the product. The prefix INA designates a standard (catalog) ISOSAT-based low Noise Amplifier. The first two digits following the hyphen designate die type. The third digit is reserved for performance selections. The last two digits designate package type.

The INA products covered in this note are:

INA-01:

Low noise:	1.7 dB
Low frequency:	500 MHz f_{3dB}
Very high gain:	32.5 dB
Higher power:	+11 dBm P_{1dB}
Moderate bias:	35 mA

INA-02:

Low noise:	2.0 dB NF
Moderate frequency:	1.0 GHz f_{3dB}
Very high gain:	31.5 dB
Higher power:	+11 dBm P_{1dB}
Moderate bias:	35 mA

INA-03:

Low noise:	2.5 dB NF
High frequency:	2.8 GHz f_{3dB}
High gain:	25 dB
Low power:	+1 dBm P_{1dB}
High efficiency bias:	12 mA

INA-10:

Moderate noise:	3.5 dB NF
High frequency:	1.8 GHz f_{3dB}
High gain:	25 dB
Higher power:	+10 dBm P_{1dB}
Moderate bias:	50 mA

The package options available are:
00 - chip form - unpackaged die

70 - "hermetic stripline" package - 70 mil surface mount gold/ alumina high reliability microstripline package for premium performance applications.

84 - surface mount "micro-plastic" package - 85 mil, low cost plastic microstripline package with superior microwave performance.

86 - surface mount "micro-plastic" package - 85 mil, low cost surface mountable plastic microstripline package with leads formed and trimmed for automated assembly; some high frequency performance is lost due to the higher parasitics of the formed leads.

Note: Some die-package combinations may not be available. Contact your HP representative for specific products.

Product Design and Performance Features

The INA Circuit

All amplifiers in the INA product line have similar circuit topologies. The design utilizes a two stage cascade consisting in general of a single input transistor driving a Darlington connected output pair. Resistive feedback is used to set the RF performance.

In the most typical realization, the first stage has minimal feedback supplied only by a shunt resistor. This yields the best noise performance, and also causes the first stage to provide most of the RFIC gain. The collector of the first stage directly drives the base of the output stage, without any interstage blocking capacitor that

would limit low frequency performance. The second stage is heavily fed back using both series and shunt resistors, and sets the match, gain, and flatness of the RFIC. Additional resistors complete the DC biasing network. A typical schematic is shown in Fig. 1.

Consequent Performance Features

The topology described above results in a number of significant performance characteristics for the INA series products.

The low noise figures of INAs result directly from the circuit design. The bias point of the first stage is selected to provide excellent noise performance. The omission of a first stage emitter resistor from the design also keeps the noise figure of the devices very low. INAs have noise figures as low as 1.7 dB at 500 MHz and 2 dB at 2 GHz.

INAs have high gains and excellent reverse isolation. The high gains of 25 to 35 dB in a single transistor package follow from the use of two stages of amplification in cascade. The reverse isolation results from the lack of a direct feedback path from the input of the RFIC to the output. This is in contrast to single stage feedback amplifiers, where the shunt feedback resistor provides a direct path from output to input, and necessarily reduces device $|S_{12}|$. Typical values for INA reverse isolation are on the order of 30 dB, compared to only 15 dB for most single stage feedback amplifiers.

The performance of INA RFICs is predominantly current controlled. This follows from the use of silicon bipolar transistors as the active devices. Device performance is consequently characterized and guaranteed at a certain current level, not at an applied voltage.

The performance parameter most affected by bias is P_{1dB}. In general, there is a relatively narrow range of current over which INAs function as designed. At low bias currents, one or more stages of the cascade will be turned off, causing low gain and poor match. High reflected powers and instability over temperature are symptomatic of operation in this "not quite-turned-on" region. Although there is no reliability risk inherent in low current operation, HP does not recommend this kind of use due to the unpredictability of performance. Once sufficient current is drawn for the device to be fully operative, adding more bias current predominantly effects P_{1dB} and has limited effect on gain. Representative performance for the INA-01170 shows a 4 dB increase in P_{1dB} but only a 1 dB gain variation over this product's recommended I_d range. The maximum allowable I_d is set by current density and thermal transfer; exceeding this limit can potentially damage the INA. A recommended operating current range is included on the data sheet of each INA series product.

The INA amplifiers have a bias point that is very temperature stable. This results from the resistive scheme used to DC bias these devices. Examination of the device current (I_d) versus device voltage (V_d) curves shows INAs have a much lower slope than do single stage resistive feedback amplifiers. Thus, INA series devices maintain a relatively constant bias current when operated over temperature at a fixed V_d. Test data reveals that although the least variation in gain occurs when the INA series RFICs are operated from a current source, it is possible to operate these devices directly from a voltage source (i.e. with no bias stabilization resistor) if the temperature range is not too broad. Data comparing current controlled performance to voltage controlled performance is given in Fig. 2. A further difference in bias characteristics between INA series and MSA series amplifiers is that the device voltage of an INA increases with temperature (dV/dT is positive), whereas single stage feedback amplifiers have negative temperature coefficients.

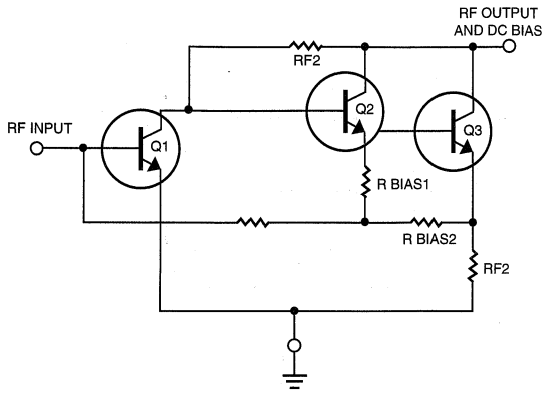


Figure 1. Typical Schematic for INA RFICs.

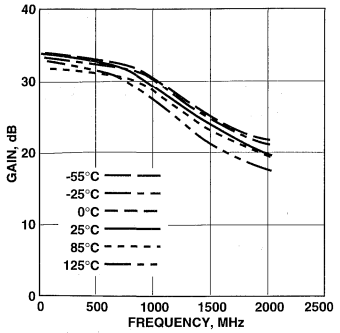


Figure 2a. Gain vs. Frequency Over Temperature INA-02170 Bias = 35 mA (Fixed).

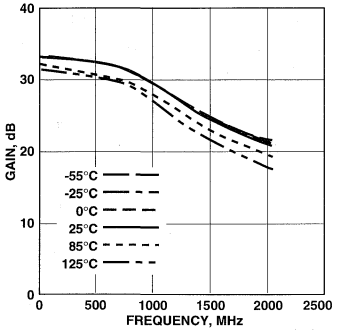


Figure 2b. Gain vs. Frequency Over Temperature INA-02170 Bias = 7.35 V (Fixed).

Emitter Inductance and Performance

As a direct result of their circuit topology, the performance of INAs is extremely sensitive to ground path ("emitter") inductance. The two stage design creates the possibility of a feedback loop being formed through the ground returns of the stages. If the path to ground provided by the external circuit is "long" (high in impedance) compared to the path back through the ground return of the other stage, then instability can occur (see Fig. 3). This phenomena can show up as a "peaking" in the gain versus frequency response (perhaps creating a negative gain slope amplifier), an increase in input VSWR, or even as return gain (a reflection coefficient greater than unity) at the input of the RFIC.

The "bottom line" is that *excellent grounding is critical* when using INAs. The use of plated through holes or equivalent minimal path ground returns *right at the device* is essential. A corollary is that designs should be done on the thinnest practical substrate. The parasitic inductance of a pair of via holes passing through .032" thick pc board is approximately 0.1 nH, while that of a pair of via holes passing through .062" thick board is closer to 0.5 nH. HP does not recommend using the INA family on boards thicker than 32 mils.

The various resistor values used in the designs make some members of the INA family more sensitive to this phenomena than others. The INA-03 geometry is most sensitive to this effect; the INA-01, INA-02 and INA-10 can tolerate somewhat higher inductance in the ground path. The package version selected also effects ground path sensitivity. Devices in the 70 style package, which has the lowest associated parasitic inductance, will be the least sensitive to ground path inductance. Devices in the 86 package, with its formed leads and higher associated inductances, will be less tolerant.

When used in chip form, the lengths of the bond wires become critical. As the bonds from the two emitter ground pads to system ground are made longer, the loop impedance increases and the tendancy towards oscillations diminishes. There is, however, a trade-off in that the gain-bandwidth of the amplifier decreases fairly rapidly as these wires are lengthened.

These stability effects are entirely predictable. A circuit simulation using the data sheet S-parameters and including a description of the ground return path (via model or equivalent "emitter" inductance) will give an accurate picture of the performance that can be expected. Device characterizations are made with the ground leads of the INA directly contacting a solid copper block (system ground) at a distance of 2 to 4 mils from the body of the package. Thus the informa-

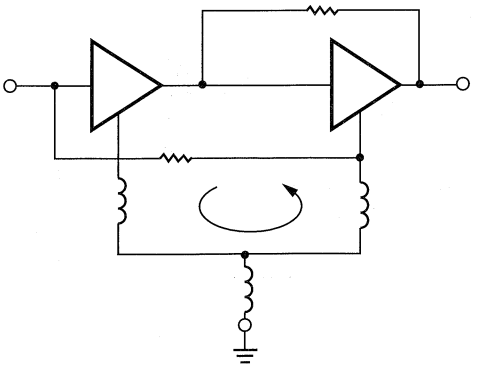


Figure 3. INA Potential Ground Loop.

tion in the data sheet is a true description of the performance capability of the RFIC, and contains minimal contributions from fixturing.

Circuit Design

RF Circuitry

Impedance Matching

The resistive feedback incorporated into each INA series device creates a gain block that is matched to 50 Ω on both input and output ports. In most cases the matches are sufficiently good that the benefit from additional matching is minimal. Improvements in gain from additional matching would typically be on the order of only tenths of a decibel. Thus the most common RF circuit consists simply of 50 Ω transmission lines.

Of course, if system requirements are for extremely low VSWRs, additional RF matching to achieve this could be devised using the device S-parameters. Arbitrarily good performance is achievable in narrow bands. It is also possible to design an input match for improved noise performance. Noise figure can typically be lowered by a few tenths of a dB at the cost of increased input reflection coefficient.

Note: Excess source inductance will significantly alter the match of the INA, causing an increase in S_{11}. Remember to include source inductance (such as a via hole description) in any simulations for predictions of performance.

INA-03xxx VSWRs

The VSWRs of the INA-03xxx are higher than those of other members of the INA family. In most cases, the match remains good enough that this is not a design issue. If, however, the designer wishes to improve the output match of this device, this can be done by placing an external resistor in parallel with the device output.

An appropriate circuit for improving the output match of the INA-03170 is shown in Fig. 4. In this circuit, the choke network consists of a resistor R_C of appropriate value well bypassed to ground at the terminal away from the RFIC. If an additional voltage drop is required to bias the INA-03170 from the available power supply, a resistor R_{BIAS} can be connected in series with R_C.

By varying the value of R_C, different circuit performance can be achieved. This has been demonstrated using an amplifier built on a 20 mil thick PTFE-fiberglass circuit board, into which various values of resistor were substituted. For the lower values of R_C tested. additional R_{BIAS} was added after the bypass capacitor to keep the overall voltage drop between supply and device constant.

An R_C value of 430 Ω (effectively no shunt resistive matching) yielded a circuit with 27 dB of low frequency gain, an f_{1dB} of 900 MHz, an input VSWR of 3.1:1 worst case and an output VSWR of 3.2:1 worst case. An R_C of 180 Ω had the effect of flattening the gain response, both by reducing low frequency gain and by peaking high frequency gain. For this circuit low frequency gain was 25.7 dB, f_{1db} was 2.4 GHz, worst input VSWR was 3.0:1 and worst output VSWR was 2.6:1. Reducing the value of R_C still further to 100 Ω yielded an ultra-flat gain response to 1 GHz, and an upward gain slope versus frequency between 1 GHz and 2 GHz. This circuit had a low frequency gain of 24.5 dB, a f_{1db} of 1.8 GHz, a worst input VSWR of 3.0:1 and a worst output VSWR of 2.2:1. Complete data for these amplifiers is shown in Figures 5 through 7.

A trade-off involved in using this technique is that output match is improved by absorbing some of the output power; consequently the P_{1dB} of the resulting amplifier will decrease by 1 to 2 dBm from the level specified on the data sheet.

DC Circuitry

Blocking Capacitors

The INA series amplifiers are designed to be used with DC blocking capacitors on both the input and output terminals. These capacitors ensure that the RF loads provided to the RFIC do not shift

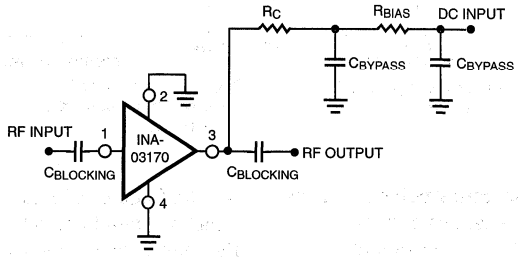


Figure 4. Using R_C to Adjust INA-03170 Output Match.

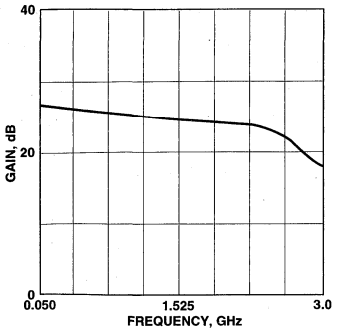


Figure 5a. Gain vs. Frequency INA-03170 with R_C = 430 Ω.

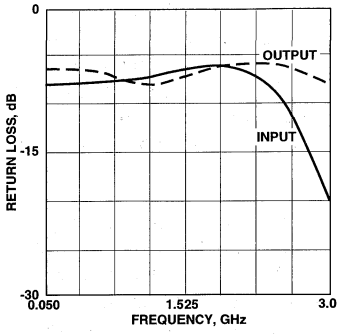


Figure 5b. Input and Output Return Loss vs. Frequency INA-03170 with R_C = 430 Ω.

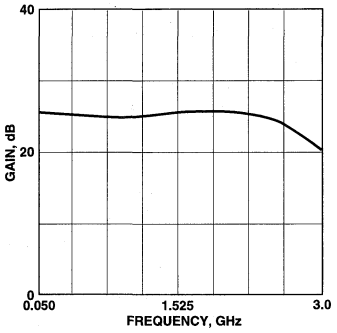


Figure 6a. Gain vs. Frequency INA-03170 with R_C = 180 Ω.

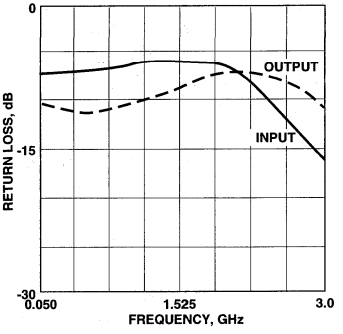


Figure 6b. Input and Output Return Loss vs. Frequency INA-03170 with R_C = 100 Ω.

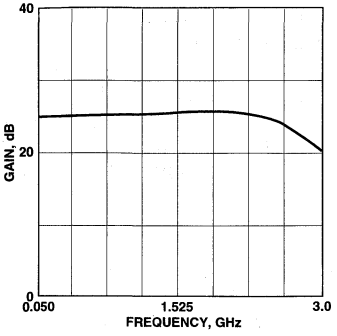


Figure 7a. Gain vs. Frequency INA-03170 with R_C = 100 Ω.

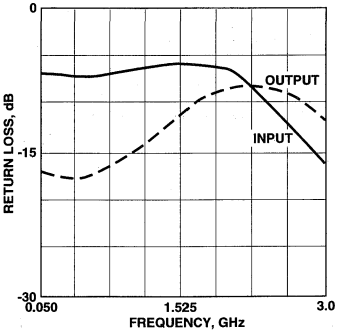


Figure 7b. Input and Output Return Loss vs. Frequency INA-03170 with R_C = 100 Ω.

the DC operating point set by the internal resistive networks. Blocking capacitors should provide a low series impedance (usually less than 10 Ω), throughout the frequency band over which the amplifier is to be used. Remember that at microwave frequencies, the reactive impedance of the blocking capacitor is the sum of the impedance provided by its capacitance [-1 / (2πfC)] and the impedance from its associated parasitic inductance (+2πfL). Dissipative loss (capacitor Q) will also contribute a resistive component to the impedance of the DC block. For best noise performance, high-Q capacitors should be used for input blocking, as any loss in front of the INA will add to the noise figure of the circuit.

Blocking capacitors may be used either above or below resonance, so long as their net series impedance is low. For narrow band applications, capacitors at resonance can be used, as this provides minimal insertion impedance [2πfL -1 / (2πfC) = 0 at resonance]. Typical values for blocking capacitors are on the order of 1000 pF, with associated parasitic inductances of 0.5 nH.

The value of blocking capacitor selected will usually determine the lowest frequency of operation of the circuit. As can be seen from the section on circuit topology, there is no internal low frequency limit inherent in the INA design.

One way to eliminate blocking capacitors is to separate DC and RF levels by "floating" the device using bypass capacitors. In this manner, an INA could be biased between a plus supply and a minus supply (Fig. 8), allowing a true DC input or output. Alternatively, the INA could be biased with the output at DC ground and the ground terminals at $-V_d$ (Fig. 9). The necessary criteria for any such configuration is that the input "base to emitter" voltage (1.6 V) and output "collector to emitter" voltage (V_d) are maintained. This constraint means that a cascade of two stages cannot be run at DC output. The sensitivity to

emitter inductance also necessitates excellent low parasitic bypassing if these schemes are used.

DC Bias

Since the performance of INAs is predominantly current controlled, it is anticipated that the typical bias of these devices will be from a current source. The most common realization of "current source" biasing is to use a dropping resistor from a fixed voltage source. This kind of biasing is shown in the "typical bias configuration" given on INA data sheets, and is repeated in Fig. 10. The value of the resistor R_{BIAS} sets the device operating current in that the volltage drop across this resistor must equal the difference between the supply voltage and the device operating voltage. Thus

$$I_d = \frac{V_{SUPPLY} - V_d}{R_{BIAS}}$$

Such a resistor also acts as a collector feedback element, and helps to stabilize the DC bias point of the INA over temperature. To provide effective feedback the voltage drop across R_{BIAS} should be at least 2 V, with higher voltage drops resulting in bias points that are even more stable over temperature. The temperature coefficient of R_{BIAS} will also play a role; resistors with positive temperature coefficients will provide more feedback versus temperature than will resistors with negative coefficients.

In cases where the designer does not have a 2 V difference between the supply voltage and the required device voltage, a simple PNP current source offers a reasonable biasing option. This circuit has the advantage of requiring only a 1 V difference between the supply

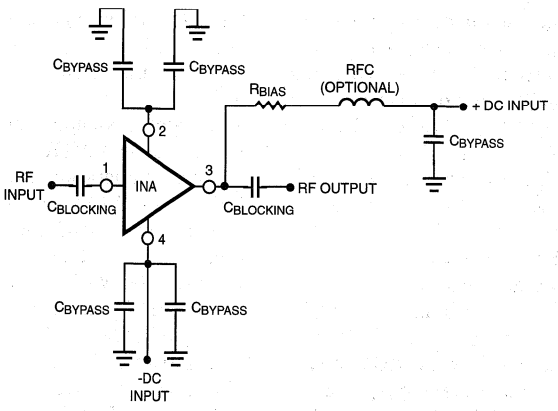


Figure 8. Biasing From ±Supply.

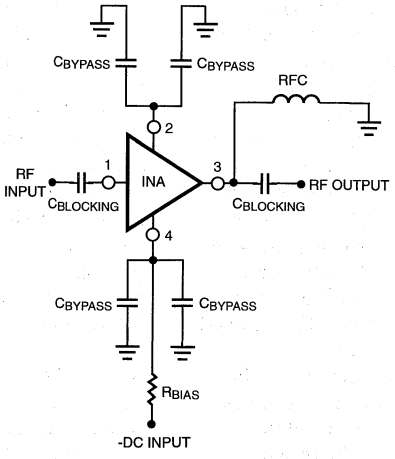


Figure 9. Biasing From a Negative Supply.

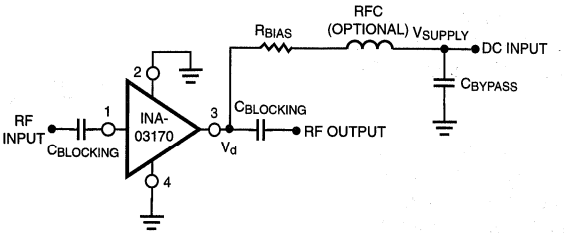


Figure 10. Biasing With a Stabilization Resistor.

voltage and the device operating voltage. A schematic for this circuit is shown in Fig. 11. Other biasing possibilities are discussed in Hewlett-Packard Application Note AN-S003: *Biasing MSA Series RFICs;* these circuits are also applicable to INA series RFICs.

Choke Networks

As with most microwave devices, RFCs or "chokes" must be used in conjunction with the DC biasing to prevent the very low AC impedance of the power supply from unduly loading the output of INAs. The important point to remember is that the choke network is a load appearing in parallel with the RF circuitry and termination. As a "rule of thumb," the total series impedance appearing between the INA output (bias) terminal and the power supply should be at least 10 times greater than that of the designed load impedance if the choke network is not to effect circuit performance. (The section on INA-03 VSWRs above is an example of a case where the choke network is specifically designed to alter circuit performance, and is therefore an exception to this rule.) In the typical bias stabilization resistor scheme, this means that the sum of the resistance of the stabilization resistor (R_{BIAS}) plus the impedance added by a series inductor acting as an RF choke ($2\pi fL$) should add up to at least 500 ohms (10 x nominal 50 Ω load).

Consider as an example an INA-03170 biased from a 12 V supply. From the data sheet, this device has a nominal device voltage V_d of 4.5 V. The device operating current is 12 mA, so the bias stabilization resistor has a value of (12 V - 4.5 V) / 0.012 A = 625 Ω. Since this value is greater than 500 Ω, no inductor needs to be used with this circuit.

As a second example, consider biasing the INA-01170 from a 12 V supply, for operation down to 10 MHz. The INA-01170 operates at a device current of 35 mA and has a typical device voltage of 5.5 volts. Now R_b = (12 V - 5.5 V)/.035 A = 186 Ω. An RFC providing (500 Ω - 186 Ω) = 314 Ω additional impedance must now be added to the choke system to avoid loading the output of the INA. Worst case will be at 10 MHz, so the value of the inductor should be at least 314 Ω / [2π(10 x 10^6 Hz)] = 5 μH. Since the 5 μH inductor is needed to add additional choke impedance, the bypass capacitor to ground must be attached on the power supply end of this element, not between it and R_{BIAS}. In theory the RFC can either precede or follow the bias resistor with identical results; empirical observations show that placing the resistor as the first element from the INA often yields better performance results.

Note that the appropriate value for the RF choke will be determined by the lowest frequency of operation required. For very low frequency operation, lossy elements such as ferrite beads can also be used to provide additional choke impedance.

INA Applications

50 Ω Gain Block/Low Noise Amplifier

The INA series was designed to function as low noise 50 Ω gain blocks. A circuit board to demonstrate their performance has been laid out using the circuit considerations discussed above. The substrate selected was epoxy-glass, having a dielectric constant of 4.8. Board of 32 mil thickness was used to minimize the parasitic inductance of the via holes. The layout is shown to scale in Fig. 11.

An assembly drawing (including component values) for an INA-02170 circuit using this board is shown in Fig. 12. The performance of the resulting amplifier is given in Table 1; this data is in good agreement with the expected performance from the data sheet characterization.

Multiplier/Harmonic Generator

The output spectrum of any amplifier will include harmonically

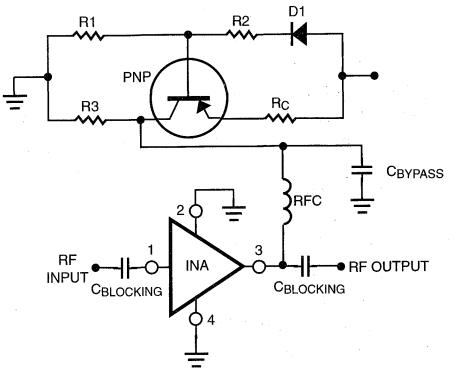


Figure 11. PNP Active Bias.

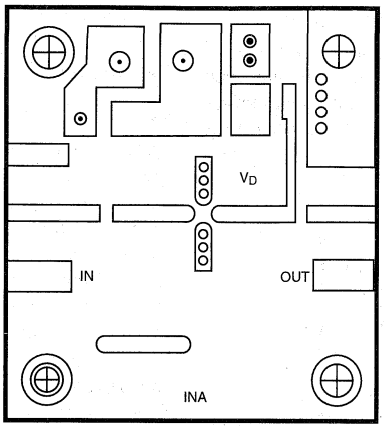


Figure 12. INA Circuit Board 2x Actual Size.

Table 1. INA-02170 Demonstration Amplifier Performance 12 V, 35 mA bias.

Freq MHz	S_{21} dB	S_{12} dB	Input VSWR	Output VSWR	k Factor	Az dB
100	33.56	-38.96	1.22	1.64	1.15	66.84
200	33.23	-41.11	1.41	1.61	1.37	65.88
300	32.88	-40.36	1.62	1.62	1.32	65.04
400	32.48	-39.68	1.84	1.59	1.28	64.54
500	32.09	-39.89	2.07	1.63	1.30	64.58
600	31.64	-39.07	2.30	1.64	1.24	65.10
700	31.09	-41.18	2.50	1.70	1.47	66.33
800	30.44	-37.58	2.64	1.76	1.18	68.02
900	29.57	-38.89	2.70	1.81	1.34	68.87
1000	28.62	-38.40	2.65	1.86	1.39	66.79
1100	27.59	-38.68	2.55	1.94	1.56	63.54
1200	26.44	-36.05	2.44	1.97	1.39	60.55
1300	25.30	-35.92	2.25	2.02	1.54	58.21
1400	24.12	-34.46	2.11	2.01	1.53	56.28
1500	22.93	-35.59	1.97	2.01	1.92	54.75
1600	21.76	-34.33	1.83	1.99	1.94	53.54
1700	20.59	-33.15	1.71	1.99	1.96	52.58
1800	19.48	-33.85	1.58	1.95	2.39	51.87
1900	18.51	-33.15	1.50	1.92	2.49	51.28
2000	17.53	-32.42	1.44	1.91	2.57	50.68
2100	16.46	-32.22	1.38	1.94	2.81	50.06
2200	15.40	-33.10	1.35	1.97	3.46	49.33
2300	14.41	-32.54	1.31	1.96	3.63	48.61
2400	13.43	-33.57	1.29	1.96	4.54	47.87
2500	12.85	-33.84	1.26	1.95	5.01	47.30
2600	12.04	-33.16	1.32	1.95	5.04	46.65
2700	10.86	-32.79	1.36	2.07	5.38	45.90
2800	10.20	-35.23	1.43	2.06	7.62	45.55
2900	8.94	-33.22	1.50	2.22	6.75	44.80
3000	8.24	-34.99	1.52	2.08	9.10	44.24

related components (2f, 3f, etc.) as well as the fundamental signal. By maximizing the harmonic output of an INA , the device becomes useful as a comb generator or frequency multiplier. As a comb generator, the entire output spectrum is used; for frequency multiplier use filters are typically added at the output of the INA to select the desired harmonic component.

To maximize harmonic output, the INA should be operated in hard saturation, with the RF input level approximately equal to the rated output power of the device. Note that each INA amplifier has a maximum RF input signal level listed in the ratings table on its data sheet; driving at input levels greater than this value can potentially shorten the operating lifetime of the INA. The bias point (device current) can also be adjusted to maximize harmonic output. Most commonly, bias current is increased from the nominal operating point, though this may vary with frequency of use and drive level. For use as a multiplier, the phasing of (electrical distance to) the filter used at the output is also a variable that will effect harmonic signal strength.

For maximal signal strength, the output (multiplied) signals should occur at frequencies within the normal 3 dB passband of the INA amplifier. The high f_{3dB} and relatively low P_{1dB} of the INA-03 geometry make it particularly appropriate for use as a multiplier. Typical output spectra for this device are shown in Fig. 14. No filters were used in the generation of this data. Figure 14a shows the output spectrum for an input signal of -2 dBm at 100 MHz with the bias optimized to 25 mA. Useful signals (30 dB down from input) occur to

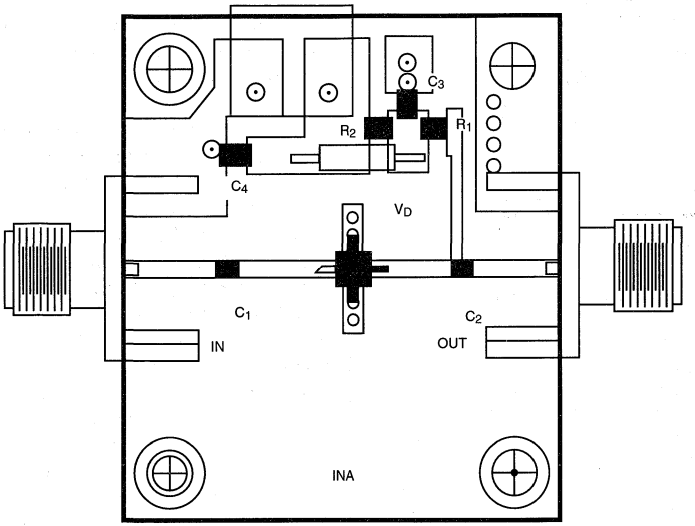
past 1 GHz. Figure 14b shows the output spectrum for an input signal of +10 dBm at 1 GHz; for this data the bias was optimized to 12 mA. Useful signals occur to 10 GHz.

Limiting Amplifier

The output power of a limiting amplifier should be constant over a wide range of input signal levels. The high gain and hard saturating characteristics of the INA family amplifiers make them appropriate for this kind of application.

The bias current at which an INA is operated will determine the power level at which it saturates. Thus for proper limiting, the bias point cannot be allowed to shift as a function of RF drive. The DC bias network must therefore provide a stiff current source for best results in limiting applications. An active bias circuit based on a pnp transistor is preferable to a simple dropping resistor as it will hold the bias current more constant. The cleanest output signal with lowest harmonics is obtained when the amplifier is operated at bias levels near its typical operating level.

RF output vs. RF input curves for an INA-02170 operated at 100 MHz, 1 GHz, and 2 GHz, with a bias current of 35 mA, are shown in Fig. 15. The flat saturation characteristic shown indicates that this INA can be successfully used as a limiting amplifier. Best limiting performance occurs within the 3 dB passband of the device. Again, remember that the input drive level into the INA should not exceed the maximum rating listed on the data sheet.



VIA HOLES: 0.031; 1/2 OZ. COPPER (EDC) TO FILL PLATED THRU HOLES
SCREW HOLES: 0.110
MATERIAL: 0.031 THICK FR-4 OR G-10, 1/2 OZ. COPPER BOTH SIDES
PLATING; 1 OZ. TIN LEAD BOTH SIDES

C_1 = 0.015 µF	L_1 = 10 µF
C_2 = 0.015 µF	R_1 = 180 Ω
C_3 = NOT USED	R_2 = NOT USED
C_4 = 0.015 µF	DEVICE = INA-02170

Figure 13. Assembly Drawing for INA-02170 Demonstration Amplifier.

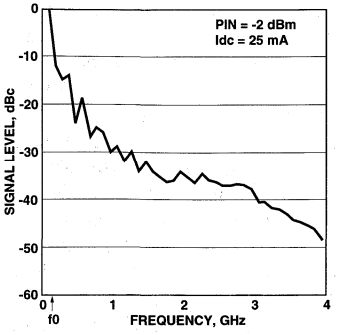


Figure 14a. Harmonic Generation vs. Frequency INA-03170, fo = 100 MHz.

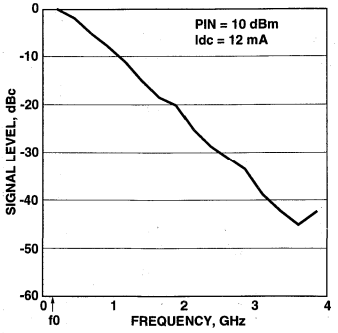


Figure 14b. Harmonic Generation vs. Frequency INA-03170, fo = 1 GHz.

Gain Control Amplifier

If the insertion power gain of an amplifier is a strong function of its bias current, then by adjusting I_d the gain may also be controlled, creating a variable gain amplifier. Although the gain of the INA amplifiers is a function of bias current, only a limited range of gain control, typically 10 dB or less, is practical. If this amount of control is sufficient, it can be obtained using a bias scheme which provides for current adjustment. Such a circuit is described in

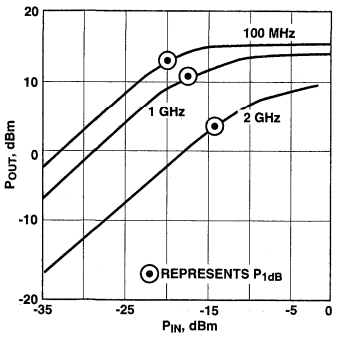


Figure 15. INA-02170 Limiting Characteristics I_d = 35 mA.

HP Application Note AN-S003: *Biasing MSA Series RFICs.* For applications requiring a wider range of gain control, a member of the HP IVA series of variable gain RFIC amplifiers is appropriate.

Transimpedance Amplifier

A transimpedance amplifier takes a current input and creates a voltage output. A very common use of such a circuit is in the receiving end of a fiber optics system, where the output current from a photodiode must be translated into usable RF energy. The low noise figure and high gain of the INA product make it a candidate for this function.

The circuitry for using an INA as a transimpedance amplifier is virtually identical to that for use as a conventional amplifier. The current from the photodiode is fed directly into the input of the INA amplifier, without the use of a blocking capacitor. The output of the INA usually drives a limiting or AGC amplifier before regeneration and de-multiplexing into the individual data channels. (Note that INA RFICs are also candidates for use in this conventional amplification role.)

The member of the INA family with the greatest potential as a transimpedance amplifier is the INA-02170. It has wider bandwidth than the INA-01170, better phase margin than the INA-03170, and lower noise performance than the INA-10386. Representational performance for this device includes a 65 dB transimpedance gain, a 600 MHz bandwidth, and 145 degrees of phase margin. Its equivalent input noise current is typically 7 pA/√Hz. It can handle input currents of ±1000 μA, and works well with photodiodes with 1 pF typical input impedances. A typical system application would be for the 622 Mb/s SONET system. For more information on the use of Hewlett-Packard gain blocks as transimpedance amplifiers, refer to Hewlett-Packard Application Note AN-S011: *Using Si MMIC Gain Blocks as Transimpedance Amplifiers.*

Applications

The application notes represented by these abstracts are available from your local Hewlett-Packard sales office or nearest Hewlett-Packard authorized distributor or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

AN-G006
MGA-64135 GaAs MMIC as a Variable-Gain Amplifier and Operation at Reduced V_{dd}
Documents the results of using the MGA-64135 GaAs MMIC amplifier as a variable gain amplifier providing up to 30 dB of gain control range and as a fixed gain stage operating at reduced device voltages, i.e., down to 4 V.
Publication No. 5091-3745E

AN-S001
Basic MODAMP MMIC Circuit Techniques
Circuit layout, board selection, and grounding techniques.
Publication No. 5091-9312E

AN-S002
Basic MODAMP MMIC Nomenclature
Overview of MODAMP MMIC geometries and packages.
Publication No. 5091-6490E

AN-S004
A Broadband IF Amplifier Using MSA-0235 and MSA-0335
Broadband, high gain cascade amplifier techniques.
Publication No. 5091-7614E

AN-S006
Using External Feedback to Achieve Flat Gain with the MSA-0885
0.1–3 GHz flat gain amplifier design using the MSA-0885.
Publication No. 5091-5075E

AN-S007
Using the MSA-0520 and the MSA-1023 Medium Power MODAMP Silicon MMIC Amplifiers
Power amplifier circuits and push-pull MSA-1023 amplifier.
Publication No. 5091-8822E

AN-S008
Designing with the MSA-9970
75 ohm, ultra flat, negative gain slope amplifiers.
Publication No. 5091-9313E

AN-S009
MODAMP Silicon MMIC Chip Use
Die attach, bonding, and bond diagrams for MSA series.
Publication No. 5091-9054E

AN-S010
A 5 GHz Bipolar Active Mixer
IAM-8x series Gilbert cell mixers.
Publication No. 5966-0453E

AN-S011
Using Silicon MMIC Gain Blocks as Transimpedance Amplifiers
Key specifications and performance evaluation.
Publication No. 5091-7798E

AN-S013
MagIC Active Mixers
The what, why, and how-to for IAM-8x series active mixers including a demonstration circuit.
Publication No. 5091-6488E

AN-S014
750–1250 MHz VCO
L band VCO using the AT-41411 with MSA-1104 buffer amplifier.
Publication No. 5966-0935E

AN-999
GaAS MMIC Assembly and Handling Guidelines
Mechanical, electrical and die attach considerations for the assembly and handling of GaAs MMICs.
Publication No. 5964-6644E

AN-1071
Battery Operation of the INA-03184
INA-03184 gain block powered by batteries.
Publication No. 5962-9463E

RFIC and MMIC Amplifiers Selection Guides

Fixed Gain RFIC Amplifiers (in order from lowest to highest frequency)

Part Number	Type	Frequency Range (GHz)	NF (dB)	Gain (dB)	P_{1dB} (dBm)	Supply Voltage (V)	Package	Page No.
MSA-2111	Si	DC - 0.5	3.3	16	+10	5	SOT-143	6-478
MSA-3111	Si	DC - 0.5	3.5	18.4	+9	7	SOT-143	6-482
MSA-3135	Si	DC - 0.6	3.2	19.6	+9	7	micro-X ceramic	6-482
MSA-3185	Si	DC - 0.5	3.5	18.7	+9	7	85 mil plastic	6-482
MSA-3186	Si	DC - 0.5	3.5	18.7	+9	7	85 mil SM plastic	6-482
INA-01100	Si	DC - 0.5	1.7	24	+10	8	die (chip)	6-84
INA-01170	Si	DC - 0.5	1.7	24	+11	8	70 mil stripline	6-87
HPMX-3002	Si	0.15 - 0.96	9.5	32	+22	6	SO-8	6-76
INA-02100	Si	DC - 1	2.0	29	+10	8	die (chip)	6-90
INA-02170	Si	DC - 1	2.0	29	+11	8	70 mil stripline	6-93
INA-02184	Si	DC - 0.8	2.0	28.5	+11	8	85 mil plastic	6-96
INA-02186	Si	DC - 0.8	2.0	28.5	+11	8	85 mil SM plastic	6-96
MSA-0600	Si	DC - 1	3.0	17.5	+1.5	5	die (chip)	6-362
MSA-0611	Si	DC - 0.7	3.0	16.5	+2	5	SOT-143	6-366
MSA-0635	Si	DC - 0.9	3.0	16.5	+2	5	micro-X ceramic	6-370
MSA-0636	Si	DC - 0.9	3.0	16.5	+2	5	trim lead micro-X	6-370
MSA-0670	Si	DC - 1	3.0	17.5	+2	5	70 mil stripline	6-374
MSA-0685	Si	DC - 0.8	3.2	16.5	+2	5	85 mil plastic	6-378
MSA-0686	Si	DC - 0.8	3.2	16.5	+2	5	85 mil SM plastic	6-382
INA-30311	Si	DC - 1	3.5	12.5	-11	3	SOT-143	6-140
INA-50311	Si	DC - 1	3.6	19	0	5	SOT-143	6-146
MSA-2011	Si	DC - 1	4.3	16.2	+9	7	SOT-143	6-470
MSA-2035	Si	DC - 1.1	3.7	17.3	+9	7	micro-X ceramic	6-470
MSA-2085	Si	DC - 1.1	3.7	16.6	+9	7	85 mil plastic	6-470
MSA-2086	Si	DC - 1.1	3.7	16.6	+9	7	85 mil SM plastic	6-470
MSA-0100	Si	DC - 1.3	6.0	17	+1.5	7	die (chip)	6-242
MSA-0104	Si	DC - 0.8	6.0	15	+1.5	7	145 mil plastic	6-246
MSA-0135	Si	DC - 1.2	6.0	16.5	+1.5	7	micro-X ceramic	6-250
MSA-0136	Si	DC - 1.2	6.0	16.5	+1.5	7	trim lead micro-X	6-250
MSA-0170	Si	DC - 1.3	6.0	16.5	+1.5	7	70 mil stripline	6-254
MSA-0185	Si	DC - 1	6.0	15	+1.5	7	85 mil plastic	6-258
MSA-0186	Si	DC - 0.9	6.0	15	+1.5	7	85 mil SM plastic	6-262

Selection Guide, continued

Fixed Gain RFIC Amplifiers (in order from lowest to highest frequency)

Part Number	Type	Frequency Range (GHz)	NF (dB)	Gain (dB)	P_{1dB} (dBm)	Supply Voltage (V)	Package	Page No.
INA-52063	Si	DC - 1.3	4.0	22	+7.8	5	SOT-363 (SC-70)	6-156
INA-12063	Si	DC - 1.5	2.2	15.8	0	3	SOT-363 (SC-70)	6-116
MSA-1100	Si	0.05 - 1.6	4.0	11	+17.5	8	die (chip)	6-450
MSA-1104	Si	0.05 - 1.3	4.2	10.5	+17.5	8	145 mil plastic	6-454
MSA-1105	Si	0.05 - 1.3	4.2	10.5	+17.5	8	85 mil SM plastic	6-458
MSA-1110	Si	0.05 - 1.6	4.0	11	+17.5	8	100 mil stripline	6-462
MSA-1120	Si	0.05 - 1.6	4.0	11	+17.5	8	200 mil BeO disk	6-466
INA-10386	Si	DC - 1.8	3.7	26.8	+10	6	85 mil SM plastic	6-112
MSA-9970	Si	DC - 2	-	16	+14.5	10	70 mil stripline	6-489
MSA-0700	Si	DC - 2.5	4.5	13	+5.5	5	die (chip)	6-386
MSA-0711	Si	DC - 1.9	5.0	12	+5.5	5	SOT-143	6-390
MSA-0735	Si	DC - 2.4	4.5	13	+5.5	5	micro-X ceramic	6-394
MSA-0736	Si	DC - 2.4	4.5	13	+5.5	5	trim lead micro-X	6-394
MSA-0770	Si	DC - 2.5	4.5	13	+5.5	5	70 mil stripline	6-398
MSA-0785	Si	DC - 2	5.0	12.5	+5.5	5	85 mil plastic	6-402
MSA-0786	Si	DC - 2	5.0	12.5	+5.5	5	85 mil SM plastic	6-406
MSA-0500	Si	0.02 - 2.8	6.5	8.5	+23	15	die (chip)	6-346
MSA-0504	Si	0.02 - 2.3	6.5	7	+18	12	145 mil plastic	6-350
MSA-0505	Si	0.02 - 2.3	6.5	7	+18	12	85 mil SM plastic	6-354
MSA-0520	Si	0.02 - 2.8	6.5	8.5	+23	15	200 mil BeO disk	6-358
MSA-1000	Si	0.05 - 2.6	7.0	8.5	+27	20	die (chip)	6-442
MSA-1023	Si	0.05 - 2.5	7.0	8.5	+27	20	230 mil BeO flange	6-446
INA-51063	Si	DC - 2.4	3.0	20.9	-2.5	5	SOT-363 (SC-70)	6-151
MSA-0200	Si	DC - 2.8	6.5	12	+4.5	7	die (chip)	6-266
MSA-0204	Si	DC - 1.8	6.5	11	+4.5	7	145 mil plastic	6-270
MSA-0235	Si	DC - 2.7	6.5	12	+4.5	7	micro-X ceramic	6-274
MSA-0236	Si	DC - 2.7	6.5	12	+4.5	7	trim lead micro-X	6-274
MSA-0270	Si	DC - 2.8	6.5	12	+4.5	7	70 mil stripline	6-278
MSA-0285	Si	DC - 2.6	6.5	12	+4.5	7	85 mil plastic	6-282
MSA-0286	Si	DC - 2.5	6.5	12	+4.5	7	85 mil SM plastic	6-286
MSA-0300	Si	DC - 2.8	6.0	12	+10	7	die (chip)	6-290
MSA-0304	Si	DC - 1.6	6.0	11	+10	7	145 mil plastic	6-294
MSA-0311	Si	DC - 2.3	6.0	11	+9	7	SOT-143	6-298
MSA-0335	Si	DC - 2.7	6.0	12	+10	7	micro-X ceramic	6-302
MSA-0336	Si	DC - 2.7	6.0	12	+10	7	trim lead micro-X	6-302
MSA-0370	Si	DC - 2.8	6.0	12	+10	7	70 mil stripline	6-306
MSA-0385	Si	DC - 2.5	6.0	12	+10	7	85 mil plastic	6-310
MSA-0386	Si	DC - 2.4	6.0	12	+10	7	85 mil SM plastic	6-314
INA-03100	Si	DC - 2.8	2.3	26	+2	7	die (chip)	6-102
INA-03170	Si	DC - 2.8	2.3	26	+1	7	70 mil stripline	6-105
INA-03184	Si	DC - 2.5	2.6	25	-2	7	85 mil plastic	6-108
INA-54063	Si	DC - 3	5	21	+10	5	SOT-363 (SC-70)	6-163

Selection Guide, continued

Fixed Gain RFIC Amplifiers (in order from lowest to highest frequency)

Part Number	Type	Frequency Range (GHz)	NF (dB)	Gain (dB)	P_{1dB} (dBm)	Supply Voltage (V)	Package	Page No.
MSA-0800	Si	DC - 0.4+	3.0	24	+12.5	10	die (chip)	6-410
MSA-0835	Si	DC - 0.4+	3.0	23	+12.5	10	micro-X ceramic	6-414
MSA-0836	Si	DC - 0.4+	3.0	23	+12.5	10	trim lead micro-X	6-414
MSA-0870	Si	DC - 0.4+	3.0	23.5	+12.5	10	70 mil stripline	6-418
MSA-0885	Si	DC - 0.4+	3.3	22.5	+12.5	10	85 mil plastic	6-422
MSA-0886	Si	DC - 0.4+	3.3	22.5	+12.5	10	85 mil SM plastic	6-426
MSA-0400	Si	DC - 4	6.5	8.5	+16	10	die (chip)	6-318
MSA-0404	Si	DC - 2.5	7.0	7.7	+11.5	7	145 mil plastic	6-322
MSA-0420	Si	DC - 4	6.5	8.5	+16	10	200 mil BeO disk	6-326
MSA-0435	Si	DC - 3.8	6.5	8.3	+12.5	7	micro-X ceramic	6-330
MSA-0436	Si	DC - 3.8	6.5	8.3	+12.5	7	trim lead micro-X	6-330
MSA-0470	Si	DC - 4	6.5	8.3	+12.5	7	70 mil stripline	6-334
MSA-0485	Si	DC - 3.6	7.0	8	+12.5	7	85 mil plastic	6-338
MSA-0486	Si	DC - 3.2	7.0	8	+12.5	7	85 mil SM plastic	6-342
MGA-87563	GaAs	0.5 - 4	1.6	12.5	-2	3	SOT-363 (SC-70)	6-234
MSA-0900	Si	0.05 - 6	6.0	8	+11.5	12	die (chip)	6-430
MSA-0910	Si	0.05 - 6	6.0	8	+11.5	12	100 mil stripline	6-434
MSA-0986	Si	0.05 - 5.5	6.0	7.5	+11.5	12	85 mil SM plastic	6-438
MGA-86563	GaAs	0.5 - 6	1.6	22.5	+4.2	5	SOT-363 (SC-70)	6-220
MGA-86576	GaAs	1.5 - 8	2.0	23	+6.4	5	SM ceramic	6-228
MGA-81563	GaAs	0.1 - 6	2.7	12.3	+14.8	3	SOT-363 (SC-70)	6-196
MGA-82563	GaAs	0.1 - 6	2.2	13.5	+17.3	3	SOT-363 (SC-70)	6-208
MGA-64135	GaAs	2 - 6	7.5	12	+12	10	micro-X ceramic	6-192
HMMC-5618	GaAs	6 - 20	5.5	14	+18	5	die (chip only)	6-64
HMMC-5620	GaAs	6 - 20	9	16	+14	5	die (chip only)	6-70
HMMC-5021	GaAs	2 - 22	5	8	+21	7	die (chip only)	6-28
HMMC-5022	GaAs	2 - 22	5	9.5	+21	7	die (chip only)	6-28
HMMC-5023	GaAs	21.2 - 26.5	2.5	24	+10	5	die (chip only)	6-34
HMMC-5026	GaAs	2 - 26.5	5	9.5	+21	7	die (chip only)	6-28
HMMC-5027	GaAs	2 - 26.5	11	6	+19	8	die (chip only)	6-47
HMMC-5040	GaAs	20 - 40	7	22	+18	4.5	die (chip only)	6-58
HMMC-5038	GaAs	37 - 40	4.8	23	+12	3	die (chip only)	6-53
HMMC-5025	GaAs	2 - 50	5-7	8.5	+10	5	die (chip only)	6-40

Variable Gain RFIC Amplifiers

Part Number	Type	Frequency Range (GHz)	NF (dB)	Gain (dB)	Gain Control Range (dB)	P_{1dB} (dBm)	Supply Voltage (V)	Package	Page No.
IVA-05128	Si	0.05 - 1.5	9	26	30	-2	5	8-pin SM Ceramic	6-173
IVA-05208	Si	DC - 1.8	9	30	30	-3	5	SO-8 SM plastic	6-177
IVA-05228	Si	DC - 1.8	9	30	30	-3	5	8-pin SM Ceramic	6-181
IVA-14208	Si	DC - 2.5	9	24	34	-2	6	SO-8 SM plastic	6-185
IVA-14228	Si	DC - 2.5	9	24	34	-2	6	8-pin SM Ceramic	6-185

HEWLETT® PACKARD

2–26.5 GHz GaAs MMIC Traveling Wave Amplifier

Technical Data

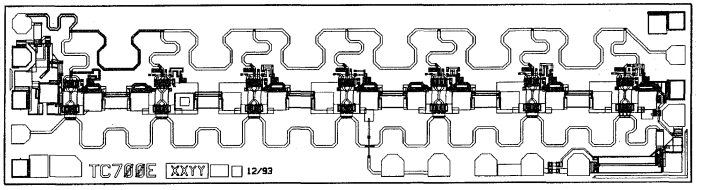
HMMC-5021 (2-22 GHz)
HMMC-5022 (2-22 GHZ)
HMMC-5026 (2-26.5 GHz)

Features

- **Wide-Frequency Range:** 2 - 26.5 GHz
- **High Gain:** 9.5 dB
- **Gain Flatness:** 0.75 dB
- **Return Loss:**
  Input: -14 dB
  Output: -13 dB
- **Low-Frequency Operation Capability:** < 2 GHz
- **Gain Control:**
  35 dB Dynamic Range
- **Moderate Power:**
  20 GHz: P_{-1dB}: 18 dBm
  P_{sat}: 20 dBm
  26.5 GHz: P_{-1dB}: 15 dBm
  P_{sat}: 17 dBm

Description

The HMMC-5021/22/26 is a broadband GaAs MMIC Traveling Wave Amplifier designed for high gain and moderate output power over the full 2 to 26.5 GHz frequency range. Seven MESFET cascode stages provide a flat gain response, making the HMMC-5021/22/26 an ideal wideband gain block. Optical lithography is used to produce gate lengths of ≈0.4 µm. The HMMC-5021/22/26 incorporates advanced MBE technology, Ti-Pt-Au gate metallization, silicon nitride passivation, and polyimide for scratch protection.



Chip Size:	2980 x 770 µm (117.3 x 30.3 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	75 x 75 µm (2.95 x 2.95 mils), or larger

Absolute Maximum Ratings

Symbol	Parameters/Conditions	Units	Min.	Max.[1]
V_{DD}	Positive Drain Voltage	V		8.0
I_{DD}	Total Drain Current	mA		250
V_{G1}	First Gate Voltage	V	-5	0
I_{G1}	First Gate Current	mA	-9	+5
V_{G2}[2]	Second Gate Voltage	V	-2.5	+3.5
I_{G2}	Second Gate Current	mA	-7	
P_{DC}	DC Power Dissipation	watts		2.0
P_{in}	CW Input Power	dBm		23
T_{ch}	Operating Channel Temp.	°C		+150
T_{case}	Operating Case Temp.	°C	-55	
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp. (for 60 seconds maximum)	°C		+300

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A = 25°C except for T_{ch}, T_{STG}, and T_{max}.
2. Minimum voltage on V_{G2} must not violate the following: $V_{G2}(min) > V_{DD} - 9$ volts.

HMMC-5021/22/26 DC Specifications/Physical Properties,[1] applies to all part numbers

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current (V_{DD} = 7.0 V, V_{G1} = 0 V, V_{G2} = open circuit)	mA	115	180	250
V_p	First Gate Pinch-off Voltage (V_{DD} = 7.0 V, I_{DD} = 16 mA, V_{G2} = open circuit)	V	-3.5	-1.5	-0.5
V_{G2}	Second Gate Self-Bias Voltage (V_{DD} = 7.0 V, V_{G1} = 0 V)	V		2.1	
I_{DSOFF} (V_{G1})	First Gate Pinch-off Current (V_{DD} = 7.0 V, V_{G1} = -3.5 V, V_{G2} = open circuit)	mA		4	
I_{DSOFF} (V_{G2})	Second Gate Pinch-Off Current (V_{DD} = 5.0 V, V_{G1} = 0 V, V_{G2} = -3.5 V)	mA		8	
$\theta_{ch\text{-}bs}$	Thermal Resistance ($T_{backside}$ = 25°C)	°C/W		36	

Note:
1. Measured in wafer form with T_{chuck} = 25°C. (Except $\theta_{ch\text{-}bs}$.)

HMMC-5021/22/26 RF Specifications, V_{DD} = 7.0 V, $I_{DD}(Q)$ = 150 mA, $Z_{in} = Z_o$ = 50 Ω[1]

Symbol	Parameters/Conditions	Units	2.0–22.0 GHz				2.0–26.5 GHz		
			HMMC-5021	HMMC-5022			HMMC-5026		
			Typ.	Min.	Typ.	Max.	Min.	Typ.	Max.
BW	Guaranteed Bandwidth	GHz	2-22	2		22	2		26.5
S_{21}	Small Signal Gain	dB	10	8.0	10	12	7.5	9.5	12
ΔS_{21}	Small Signal Gain Flatness	dB	±0.5		±0.5	±1.0		±0.75	±1.0
$RL_{in(min)}$	Minimum Input Return Loss	dB	16	10	16		10	14	
$RL_{out(min)}$	Minimum Output Return Loss	dB	13	10	13		10	13	
Isolation	Minimum Reverse Isolation	dB	32	20	32		20	30	
P_{-1dB}	Output Power at 1 dB Gain Comp.	dBm	18	15	18		12	15	
P_{sat}	Saturated Output Power	dBm	20	17	20		14	17	
$H_{2(max)}$	Max. Second Harm. (2 <f_o<20), [$P_o(f_o)$ = 17 dBm or P_{-1dB}, whichever is less.]	dBc	-25		-25	-20		-25	-20
$H_{3(max)}$	Max. Third Harm. (2 <f_o< 20), [$P_o(f_o)$ = 17 dBm or P_{-1dB}, whichever is less.]	dBc	-34		-34	-20		-34	-20
NF	Noise Figure	dB	8		8			10	

Notes:
1. Small-signal data measured in wafer form with T_{chuck} = 25°C. Large-signal data measured on individual devices mounted in an HP83040 Series Modular Microcircuit Package @ T_A = 25°C.
2. Performance may be extended to lower frequencies through the use of appropriate off-chip circuitry. Upper -3 dB corner frequency ≈ 29.5 GHz.

Applications

The HMMC-5021/22/26 series of traveling wave amplifiers are designed for use as general purpose wideband gain blocks in communication systems and microwave instrumentation. They are ideally suited for broadband applications requiring a flat gain response and excellent port matches over a 2 to 26.5 GHz frequency range. Dynamic gain control and low-frequency extension capabilities are designed into these devices.

Biasing and Operation

These amplifiers are biased with a single positive drain supply (V_{DD}) and a single negative gate supply (V_{G1}). The recommended bias conditions for the HMMC-5021/22/26 are V_{DD} = 7.0V, I_{DD} = 150 mA for best overall performance. To achieve this drain current level, V_{G1} is typically biased between -0.2V and -0.5V. No other bias supplies or connections to the device are required for 2 to 26.5 GHz operation. See Figure 3 for assembly information.

The auxiliary gate and drain contacts are used only for low-frequency performance extension below ≈1.0 GHz. When used, these contacts must be AC coupled only. (Do not attempt to apply bias to these pads.)
The second gate (V_{G2}) can be used to obtain 35 dB (typical) dynamic gain control. For normal operation, no external bias is required on this contact and its self-bias voltage is ≈+2.1 V. Applying an external bias between its open-circuit voltage and -2.5 volts will adjust the gain while maintaining a good input/output port match.

Assembly Techniques

Solder die-attach using a fluxless AuSu solder preform is the recommended assembly method. Gold thermosonic wedge bonding with 0.7 mil diameter Au wire is recommended for all bonds. Tool force should be 22 ± 1 gram, stage temperature should be 150 ± 2°C, and ultrasonic power and duration should be 64 ± 1 dB and 76 ± 8 msec, respectively. The bonding pad and chip backside metallization is gold.

For more detailed information see HP application note #999, "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

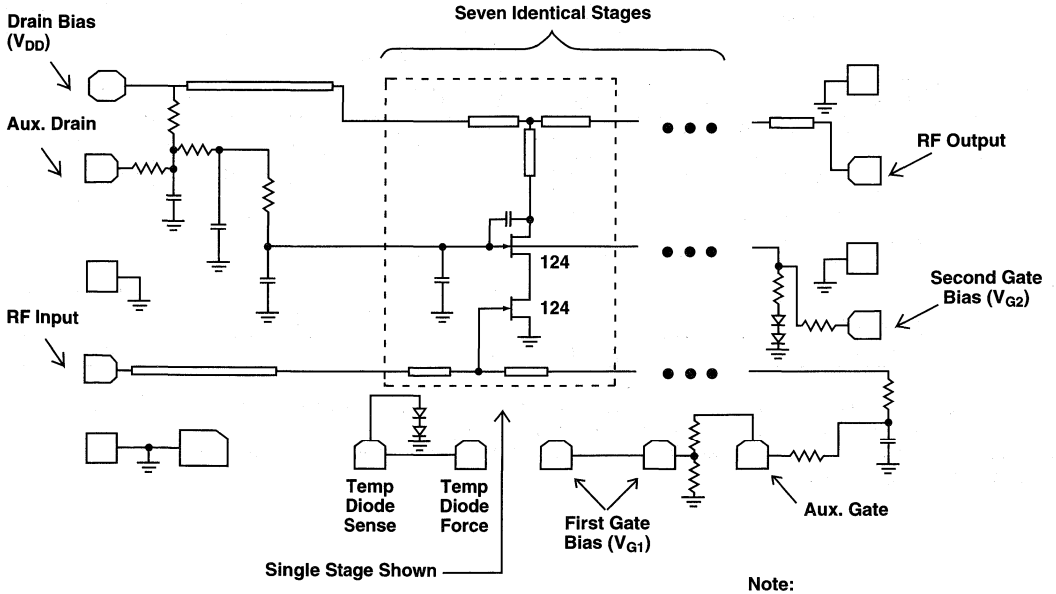


Figure 1. HMMC-5021/22/26 Schematic.

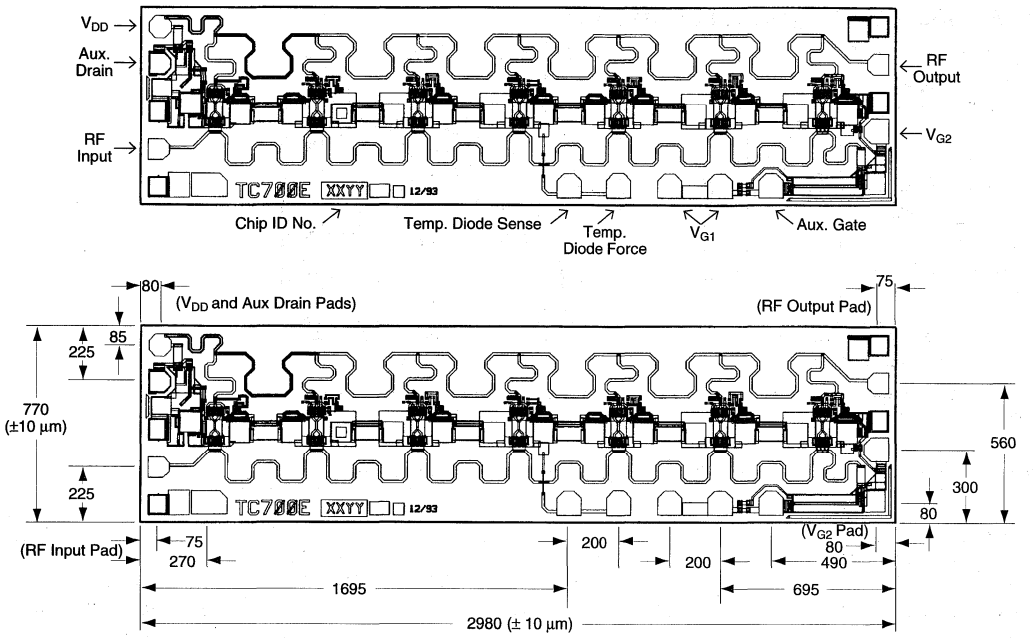
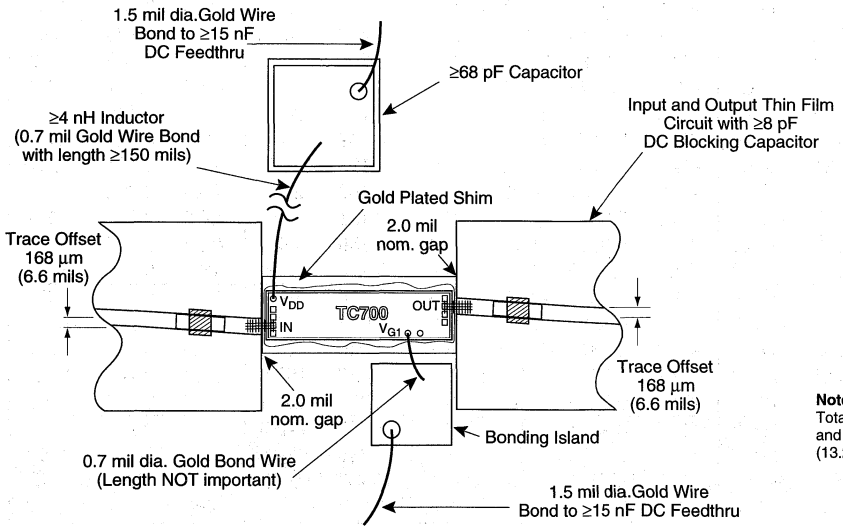


Figure 2. HMMC-5021/22/26 Bonding Pad Locations.

Notes:
All dimensions in microns.
Rectangular Pad Dim: 75 x 75 µm.
Octagonal Pad Dim: 90 µm dia.
All other dimensions ±5 µm (unless otherwise noted).
Chip thickness: 127 ± 15 µm.



Note:
Total offset between RF input and RF output pad is 335 µm (13.2 mils).

Figure 3. HMMC-5021/22/26 Assembly Diagram.

HMMC-5021/22/26 Typical Performance

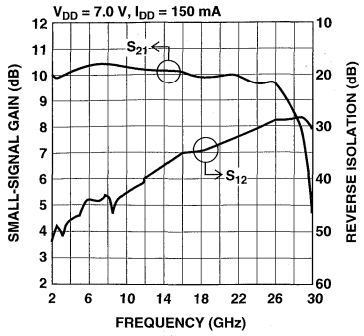


Figure 4. Typical Gain and Reverse Isolation vs. Frequency.

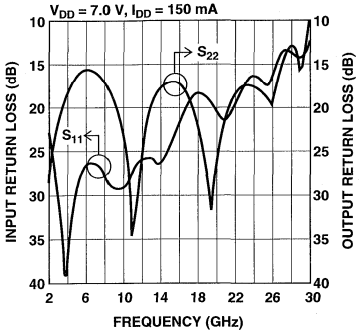


Figure 5. Typical Input and Output Return Loss vs. Frequency.

Typical Scattering Parameters[1], (T_{chuck} = 25°C, V_{DD} = 7.0 V, I_{DD} = 150 mA, Z_{in} = Z_{out} = 50 Ω

Freq.	S_{11}			S_{21}			S_{12}			S_{22}		
GHz	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
2.0	-22.6	0.074	-174.1	-53.1	0.0022	167.3	10.1	3.183	123.6	-28.9	0.036	77.3
3.0	-30.6	0.030	130.4	-51.0	0.0028	120.1	10.0	3.173	102.1	-21.6	0.083	64.1
4.0	-37.8	0.013	-19.8	-48.0	0.0040	95.0	10.2	3.225	78.2	-18.2	0.124	45.4
5.0	-29.4	0.034	-79.9	-46.8	0.0046	67.1	10.3	3.275	53.5	-16.3	0.153	23.4
6.0	-26.6	0.047	-113.8	-44.4	0.0060	36.0	10.4	3.303	28.1	-15.4	0.170	2.5
7.0	-26.6	0.047	-137.0	-44.1	0.0062	1.0	10.4	3.330	2.3	-15.7	0.165	-19.5
8.0	-27.7	0.041	-152.6	-43.4	0.0067	-27.5	10.5	3.331	-23.8	-17.0	0.141	-40.7
9.0	-29.0	0.035	-149.8	-44.3	0.0061	-31.8	10.4	3.312	-50.2	-19.2	0.110	-59.7
10.0	-29.0	0.036	-140.8	-43.0	0.0071	-53.6	10.3	3.282	-76.4	-24.3	0.061	-76.8
11.0	-27.3	0.043	-138.1	-41.6	0.0083	-74.8	10.2	3.253	-102.5	-35.1	0.018	-32.6
12.0	-26.2	0.049	-141.9	-40.0	0.0100	-96.9	10.2	3.227	-128.8	-24.6	0.059	21.0
13.0	-25.8	0.052	-148.5	-38.9	0.0113	-120.9	10.2	3.218	-155.4	-19.7	0.103	2.8
14.0	-26.4	0.048	-143.0	-38.1	0.0125	-145.6	10.1	3.204	177.8	-17.6	0.132	-21.2
15.0	-24.6	0.059	-131.7	-36.6	0.0148	-169.9	10.1	3.197	150.4	-17.0	0.141	-44.8
16.0	-21.6	0.083	-133.7	-35.3	0.0172	160.9	10.0	3.177	122.5	-17.1	0.140	-67.4
17.0	-19.4	0.107	-143.5	-35.0	0.0177	130.6	10.0	3.149	94.4	-18.5	0.119	-91.8
18.0	-18.3	0.121	-158.7	-34.7	0.0184	105.0	9.9	3.138	65.9	-21.8	0.081	-116.0
19.0	-18.7	0.116	-172.6	-33.9	0.0201	80.2	9.9	3.140	36.8	-28.9	0.036	-121.7
20.0	-20.3	0.097	-179.5	-33.3	0.0217	50.7	10.0	3.151	6.6	-28.5	0.038	-57.0
21.0	-21.8	0.082	-168.3	-32.7	0.0233	22.5	10.0	3.150	-24.9	-21.7	0.082	-59.1
22.0	-19.9	0.101	-155.3	-31.7	0.0259	-8.4	9.9	3.126	-57.5	-18.6	0.117	-81.5
23.0	-17.3	0.137	-158.8	-31.4	0.0268	-39.5	9.8	3.076	-91.0	-17.3	0.137	-103.3
24.0	-16.3	0.153	-169.9	-30.7	0.0291	-71.5	9.7	3.045	-125.5	-17.3	0.137	-123.8
25.0	-17.1	0.139	-175.4	-30.0	0.0317	-106.2	9.7	3.045	-162.2	-18.5	0.118	-135.3
26.0	-17.0	0.141	-165.0	-29.2	0.0345	-145.5	9.6	3.027	157.2	-19.4	0.107	-122.5
26.5	-15.7	0.163	-161.1	-29.0	0.0356	-166.7	9.5	2.970	135.4	-17.6	0.132	-114.2
27.0	-14.3	0.192	-162.7	-28.9	0.0357	171.7	9.2	2.876	112.9	-15.3	0.173	-116.0
28.0	-13.2	0.220	-175.7	-28.8	0.0362	126.3	8.5	2.648	65.8	-12.6	0.233	-138.1
29.0	-14.1	0.197	-176.9	-28.6	0.0371	73.0	7.7	2.433	10.3	-15.4	0.170	-144.7
30.0	-11.5	0.266	-171.6	-30.8	0.0287	4.8	4.6	1.689	-61.1	-8.7	0.369	-123.6

Note:

1. Data obtained from on-wafer measurements.

HMMC-5021/22/26 Typical Temperature Performance

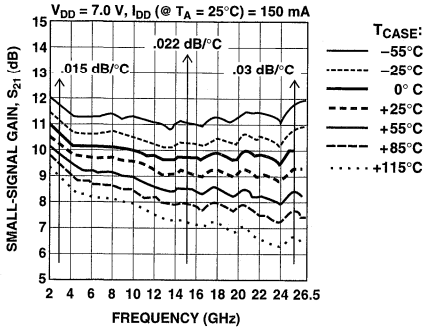


Figure 6. Typical Small-Signal Gain vs. Temperature.

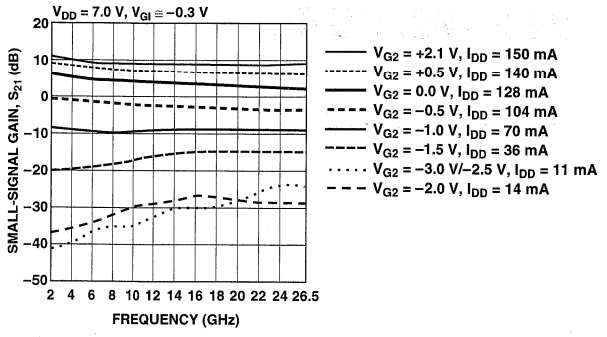


Figure 7. Typical Gain vs. Second Gate Control Voltage.

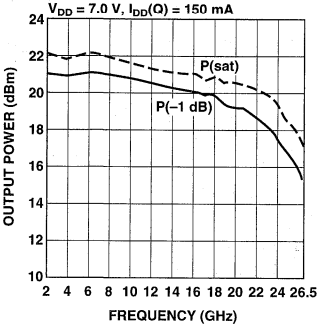


Figure 8. Typical 1 dB Gain Compression and Saturated Output Power.

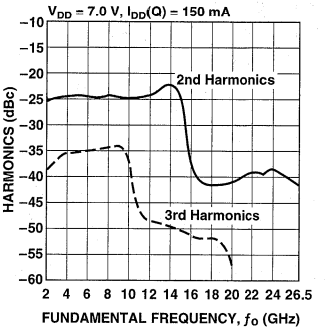


Figure 9. Typical Second and Third Harmonics vs. Fundamental Frequency at P_{OUT} = +17 dBm.

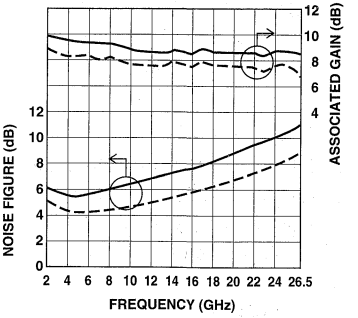


Figure 10. Typical Noise Figure Performance.

Note:

1. All data measured on individual devices mounted in an HP83040 Series Modular Microcircuit Package @ T_A = 25°C (except where noted).

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

HEWLETT® PACKARD

23 GHz LNA (21.2–26.5 GHz)

Technical Data

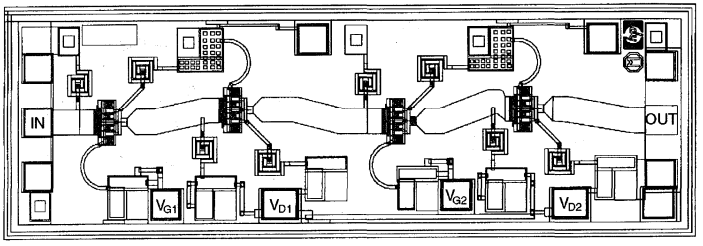
HMMC-5023

Features

- **Frequency Range:** 21.2–23.6 GHz and 24.5–26.5 GHz Specified 21–30 GHz Performance
- **Low Noise Temperature:** 226 K (2.5 dB N.F.) Typical
- **High Gain:** 24 dB Typical
- **50 Ω Input/Output Matching**
- **Single Supply Bias with Optional Bias Adjust:** 5 volts (@ 24 mA Typical)

Description

The HMMC-5023 MMIC is a high-gain low-noise amplifier (LNA) that operates from 21 GHz to over 30 GHz. By eliminating the complex tuning and assembly processes typically required by hybrid (discrete-FET) amplifiers, the HMMC-5023 is a cost-effective alternative in 21.2 –23.6 GHz and 24.5–26.5 GHz communications receivers. The device has good input and output match to 50 ohms and is unconditionally stable to more than 40 GHz. The backside of the chip is both RF and DC ground. This helps simplify the assembly process and reduces assembly related performance variations and costs. It is fabricated using a PHEMT integrated circuit structure that provides exceptional noise and gain performance.



Chip Size:	2980 x 620 µm (74 x 24.4 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	80 x 80 µm (3.1 x 3.1 mils), or larger

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{D1}, V_{D2}	Drain Supply Voltage	V	3	8
V_{D1}, V_{D2}	Gate Supply Voltage	V	0.4	2
I_{D1}	Drain Supply Current	mA		35
I_{D2}	Drain Supply Current	mA		35
P_{in}	RF Input Power[2]	dBm		15
T_{ch}	Operating Channel Temp.[3]	°C		+150
T_A	Backside Ambient Temp.	°C	-55	+140
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp.	°C		+300

Notes:

1. Absolute maximum rating for continuous operation unless otherwise noted.
2. Operating at this power level for extended (continuous) periods is not recommended.
3. Refer to *DC Specifications/Physical Properties* table for derating information.

HMMC-5023 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
V_{D1}, V_{D2}	Recommended Drain Supply Voltage	V	3	5	7
V_{G1}, V_{G2}	Gate Supply Voltage [$V_{D1} \le V_{D1}$(max), $V_{D2} \le V_{D2}$(max)]	V	0.4	0.8[2]	2
I_{D1}, I_{D2}	Input and Output Stage Drain Supply Current ($V_{G1} = V_{G2}$ = Open, $V_{D1} = V_{D2}$ = 5 Volts)	mA	12	35	
$I_{D1} + I_{D2}$	Total Drain Supply Current ($V_{G1} = V_{G2}$ = Open, $V_{D1} = V_{D2}$ = 5 Volts)	mA	13	24	30
$\theta_{ch\text{-}bs}$	Thermal Resistance[3] (Channel-to-Backside at T_{ch} = 150°C)	°C/Watt		75	
T_{ch}	Channel Temperature[4] (T_A = 140°C, MTTF = 10^6 hrs, $V_{G1} = V_{G2}$ = Open, $V_{D1} = V_D$ = 5 Volts)	°C		150	

Notes:
1. Backside ambient operating temperature T_A = 25°C unless otherwise noted.
2. Open circuit voltage at V_{G1} and V_{G2} when V_{D1} and V_{D2} are 5 volts.
3. Thermal resistance (in °C/Watt) at a channel temperature T (°C) can be estimated using this equation:
   $\theta(T)$ @ 75 x [T(°C)+273] / [150°C+273].
4. Derate MTTF by a factor of two for every 8°C above T_{ch}.

HMMC-5023 RF Specifications,

T_{op} = 25°C, $V_{D1} = V_{D2}$ = 5 V, $V_{G1} = V_{G2}$= Open, Z_O = 50 Ω, unless otherwise noted

Symbol	Parameters and Test Conditions	Units	21.2–23.6 GHz			24.5–26.5 GHz		
			Min.	Typ.	Max.	Min.	Typ.	Max.
BW	Operating Bandwidth	GHz	21.2		23.6	24.5		26.5
Gain	Small Signal Gain	dB	21	24	28	17	21	25
Δ Gain	Small Signal Gain Flatness	dB		±1			±1.5	
$(RL_{in})_{MIN}$	Minimum Input Return Loss	dB	10	12		12	20	
$(RL_{out})_{MIN}$	Minimum Output Return Loss	dB	8	10		8	10	
Isolation	Reverse Isolation	dB	40	50		40	48	
P_{-1dB}	Output Power @ 1 dB Gain Compression	dBm		10			10	
	Output Power @ 1 dB Gain Compression (V_D = 5 V, V_{G1}= Open, V_{D2} = 7 V, V_{G2} set for I_{D2} = 35 mA)	dBm		14			14	
P_{sat}	Saturated Output Power (@ 3 dB Gain Compression)	dBm		12			12	
2nd Harm.	Second Harmonic Power Level [f = $2f_o$, $P_{out}(f_o) = P_{-1dB}$, 21.2 GHz ≤ f_o ≤ 23.6 GHz]	dBc		-30			-30	
NF	Noise Figure, 22 GHz Noise Figure, 25 GHz	dB		2.5	3.0		2.8	3.3

HMMC-5023 Applications

The HMMC-5023 low noise amplifier (LNA) is designed for use in digital radio communication systems that operate within the 21.2 GHz to 23.6 GHz frequency band. High gain and low noise temperature make it ideally suited as a front-end gain stage. The MMIC solution is a cost effective alternative to hybrid assemblies.

Biasing and Operation

The HMMC-5023 has four cascaded gain stages as shown in Figure 1. The first two gain stages at the input are biased with the V_{D1} drain supply. Similarly the two output stages are biased with the V_{D2} supply. Standard LNA operation is with a single positive DC drain supply voltage ($V_{D1}=V_{D2}=5$ V) using the assembly diagram shown in Figure 9(a). If desired, the output stage DC supply voltage (V_{D2}) can be increased to improve output power capability while maintaining optimum low noise bias conditions for the input section. The output power may also be adjusted by applying a positive voltage at V_{G2} to alter the operating bias point for both output FETs. Increasing the voltage applied to V_{G2} (more positively) results in a more negative gate-to-source voltage and, therefore, lower drain current. Figures 9(b) and 9(c) illustrate how the device can be assembled for both independent drain supply operation and for output-stage gate bias control.

No ground wires are required since ground connections are made with plated through-holes to the backside of the device.

Assembly Techniques

Solder die attach using a fluxless gold-tin (AuSn) solder preform is the recommended assembly method. A conductive epoxy such as ABLEBOND® 71-1LM1 or ABLEBOND® 36-2 may also be used for die attaching provided the Absolute Maximum Thermal Ratings are not exceeded. The device should be attached to an electrically conductive surface to complete the DC and RF ground paths. Ground path inductance should be minimized (<10 pH) to assure stable operation. The backside metallization on the device is gold.

It is recommended that the RF input and RF output connections be made using either 500 line/inch (or equivalent) gold wire mesh, or dual 0.7 mil diameter gold wire. The RF wires should be kept as short as possible to minimize inductance. The bias supply wire can be a 0.7 mil diameter gold wire attached to either of the VDD bonding pads.

Thermosonic wedge is the preferred method for wire bonding to the gold bond pads. Mesh wires can be attached using a 2 mil round tacking tool and a tool force of approximately 22 grams with an ultrasonic power of roughly 55 dB for a duration of 76 ± 8 msec. A guided-wedge at an ultrasonic power level of 64 dB can be used for the 0.7 mil wire. The recommended wire bond stage temperature is 150 ± 2°C.

For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

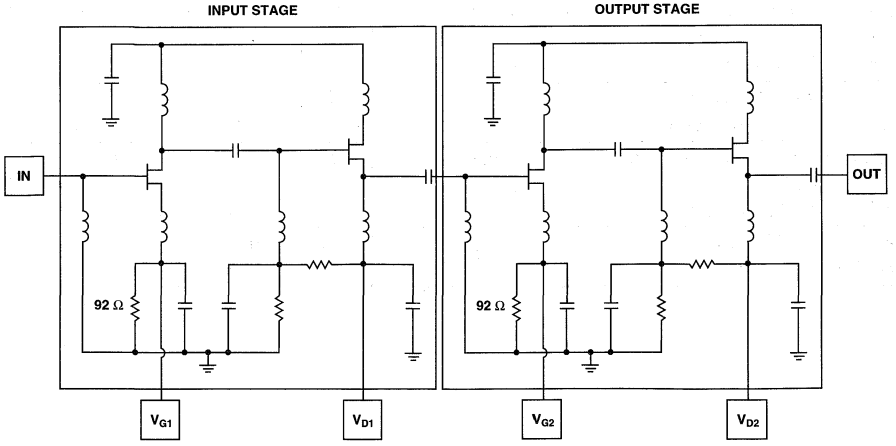


Figure 1. HMMC-5023 Simplified Schematic.

HMMC-5023 Typical Performance

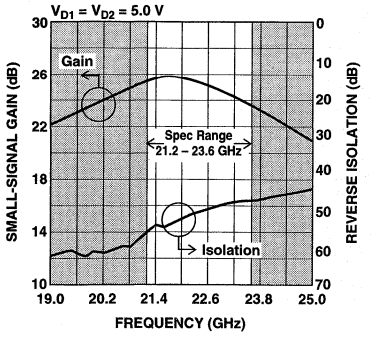


Figure 2. Gain and Isolation vs. Frequency.

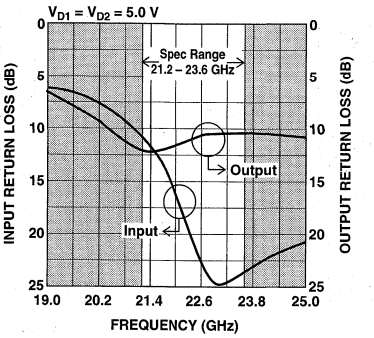


Figure 3. Input and Output Return Loss vs. Frequency.

Typical Scattering Parameters[1], ($T_{op} = 25°C, V_{D1} = V_{D2} = 5.0\,V, V_{G1} = V_{G2} = Open, Z_o = 50\,\Omega$

Freq.	S_{11}			S_{21}			S_{12}			S_{22}		
GHz	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
19.0	-6.3	0.486	61.9	-61.6	0.0008	122.7	22.3	13.090	83.3	-6.6	0.470	-179.1
19.2	-6.4	0.477	59.4	-61.6	0.0008	116.3	22.6	13.509	74.2	-6.9	0.450	175.7
19.4	-6.6	0.466	56.7	-61.0	0.0009	113.1	22.5	13.355	64.0	-7.4	0.427	169.7
19.6	-6.8	0.455	53.8	-61.3	0.0009	104.2	23.2	14.459	56.1	-7.9	0.403	163.5
19.8	-7.1	0.443	50.6	-62.3	0.0008	93.0	23.0	14.142	45.0	-8.4	0.381	156.5
20.0	-7.4	0.428	47.1	-61.2	0.0009	72.6	23.5	14.913	36.4	-8.9	0.358	148.8
20.2	-7.8	0.409	43.8	-61.3	0.0009	66.1	23.9	15.599	26.2	-9.5	0.333	139.9
20.4	-8.2	0.391	40.2	-60.9	0.0009	47.3	24.4	16.617	15.7	-10.2	0.309	130.7
20.6	-8.7	0.368	36.2	-59.5	0.0011	25.8	24.7	17.085	5.7	-10.8	0.290	119.5
20.8	-9.3	0.344	31.8	-59.6	0.0011	11.5	25.1	18.061	-4.7	-11.2	0.274	106.2
21.0	-10.0	0.318	27.4	-58.2	0.0012	-4.2	25.4	18.663	-15.3	-11.7	0.259	91.3
21.2	-10.8	0.288	22.9	-56.0	0.0016	-17.6	25.6	19.010	-26.6	-12.0	0.252	74.6
21.4	-11.8	0.256	18.4	-54.9	0.0018	-36.9	25.7	19.209	-38.7	-12.1	0.247	56.4
21.6	-13.1	0.220	14.9	-55.1	0.0018	-52.2	25.7	19.209	-51.3	-12.2	0.247	38.2
21.8	-14.7	0.185	12.1	-53.8	0.0020	-64.6	25.7	19.354	-61.4	-11.9	0.254	21.9
22.0	-16.5	0.149	11.0	-52.5	0.0024	-75.8	25.9	19.769	-74.0	-11.7	0.261	6.8
22.2	-18.5	0.118	12.1	-51.2	0.0028	-90.4	25.6	19.066	-85.2	-11.3	0.271	-6.6
22.4	-20.6	0.094	15.9	-50.5	0.0030	-100.3	25.6	19.113	-96.2	-11.0	0.282	-18.4
22.6	-22.7	0.074	22.8	-50.0	0.0031	-108.7	25.0	17.824	-107.5	-10.7	0.291	-28.7
22.8	-24.3	0.061	37.4	-49.3	0.0034	-118.9	25.1	17.943	-116.9	-10.5	0.298	-37.9
23.0	-24.9	0.057	54.0	-48.5	0.0037	-126.2	24.3	16.401	-127.6	-10.4	0.301	-45.5
23.2	-24.7	0.059	68.3	-47.6	0.0042	-134.9	24.2	16.279	-137.5	-10.4	0.300	-52.3
23.4	-24.2	0.061	78.9	-47.3	0.0043	-144.0	23.9	15.625	-146.3	-10.5	0.298	-58.0
23.6	-23.6	0.066	86.3	-47.2	0.0044	-148.9	23.2	14.469	-154.0	-10.6	0.295	-62.4
23.8	-23.3	0.068	93.5	-46.9	0.0045	-156.1	23.3	14.607	-163.4	-10.5	0.298	-65.9
24.0	-22.6	0.074	98.0	-46.4	0.0048	-161.1	22.4	13.168	-170.8	-10.6	0.296	-69.2
24.2	-22.2	0.078	100.8	-46.1	0.0049	-167.3	22.3	13.002	-179.0	-10.6	0.294	-72.0
24.4	-21.8	0.082	102.8	-45.5	0.0053	-171.7	21.6	12.087	173.1	-10.6	0.294	-74.7
24.6	-21.4	0.086	105.5	-45.6	0.0052	-176.4	21.8	12.350	166.3	-10.7	0.291	-76.8
24.8	-21.2	0.088	108.1	-44.9	0.0057	179.1	21.4	11.771	159.2	-10.8	0.289	-78.4
25.0	-20.9	0.091	293.2	-44.4	0.0061	353.0	21.0	11.257	331.9	-10.8	0.289	-79.3

Note:

1. Data obtained from wafer-probed measurements.

HMMC-5023 Typical Performance

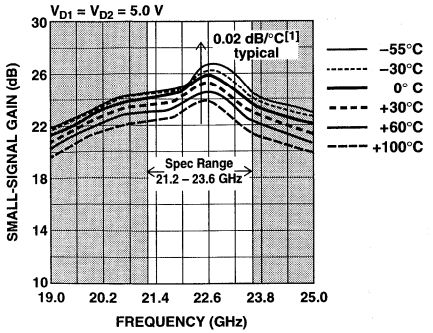


Figure 4. Small-Signal Gain vs. Frequency and Ambient Temperature[1].

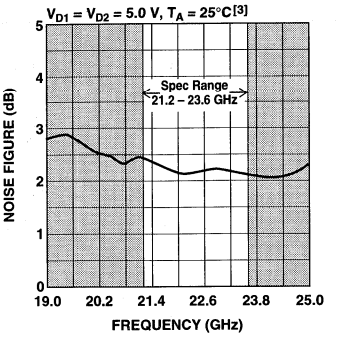


Figure 5. Noise Figure vs. Frequency[2].

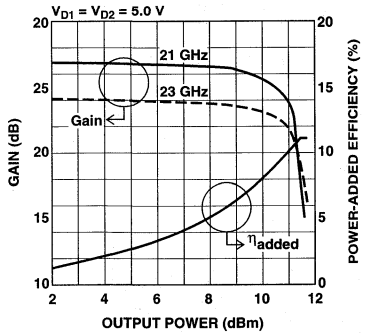


Figure 6. Gain Compression and Efficiency Characteristics[2].

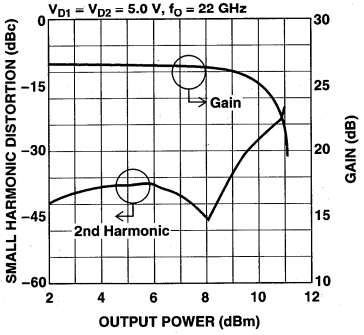


Figure 7. Second Harmonic and Gain Compression Characteristics[2].

Notes:

1. Device tested while mounted on a HP83040 Modular Microcircuit Fixture calibrated at the coaxial connectors. Test results shown have been degraded by the fixture due to loss and impedance mismatch errors. The temperature coefficient of the fixture alone is approximately 0.003 dB/°C at 20 GHz.
2. Data obtained from wafer-probed measurements.
3. The temperature coefficient of noise figure was measured for one device mounted on a HP83040 Modular Microcircuit Fixture. The uncorrected result, <0.014 dB/°C, includes the effects of the fixture.

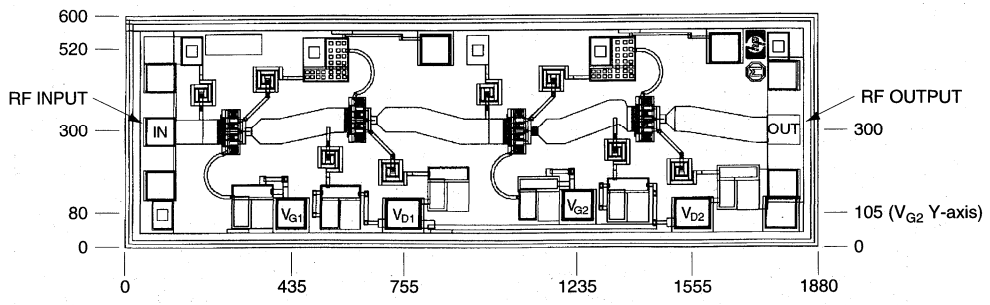


Figure 8. HMMC-5023 Bonding Pad Locations. (Dimensions are in micrometers)

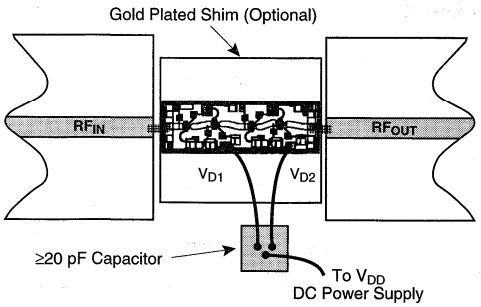


Figure 9a. Single DC Drain Supply.

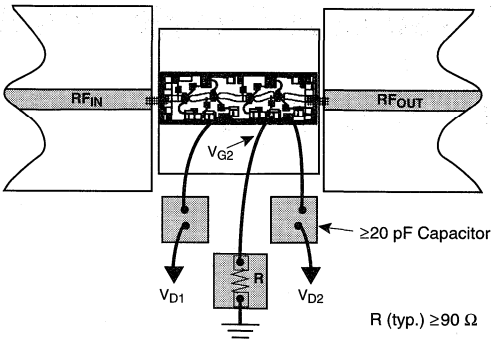
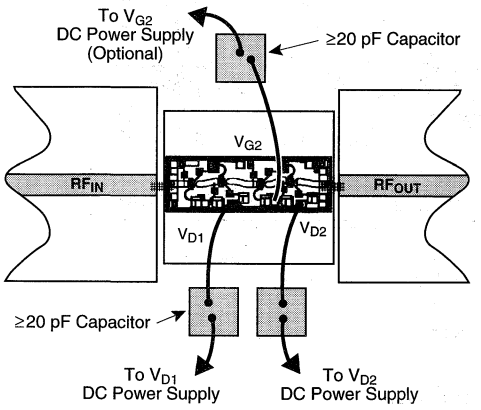


Figure 9b. Assembly for custom biasing of output gain stages using an external chip resistor.



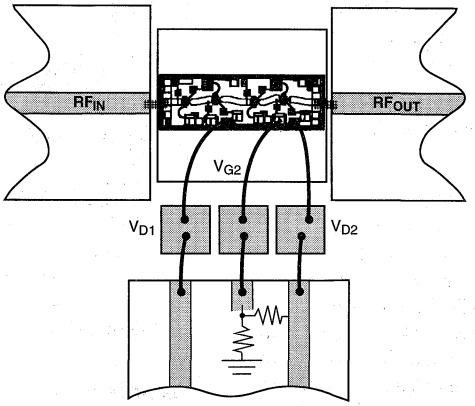


Figure 9c. A V_{G2} DC supply or a resistive divider network can also be used to bias the output stages for custom applications.

Figure 9. HMMC-5023 Assembly Diagram Examples.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

HEWLETT® PACKARD

2 – 50 GHz Distributed Amplifier

Technical Data

HMMC-5025

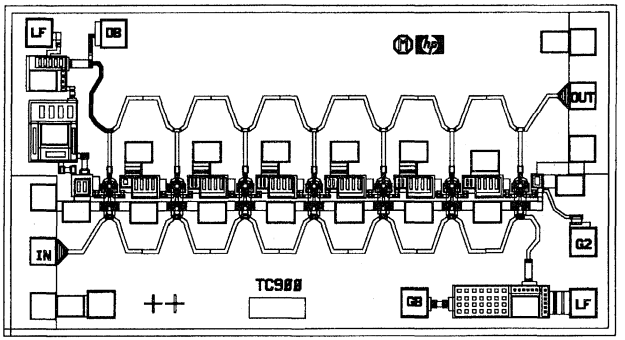
Features

- **Frequency Range:** 2 – 50 GHz
- **Small Signal Gain:** 8.5 dB
- **P_{-1dB} @ 40 GHz:** 12 dBm
- **Noise Figure:**
  < 6 dB @ 2 – 35 GHz
  < 10 dB @ 35 – 50 GHz
- **Return Loss:** In/Out: < -10 dB

Description

The HMMC-5025 was designed as a generic wide band distributed amplifier, covering the frequency span 2 – 50 GHz. It consists of seven stages. Each stage is made up of two cascoded FETs with gate peripheries of 48 mm per FET. Both input and output ports were designed to provide 50 ohm terminations. Bonding pads are provided in the layout to allow amplifier operation at frequencies lower than 2 GHz by means of external circuit components.

The HMMC-5025 is typically biased at V_{DD} = 5 volts and I_{DD} = 75 mA. The second gate is internally biased by means of a voltage divider network and an a.c. ground.



Chip Size: 1720 x 920 µm (67.7 x 36.2 mils)
Chip Size Tolerance: ±10 µm (±0.4 mils)
Chip Thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions: 80 x 80 µm (3.2 x 3.2 mils)

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{DD}	Positive Drain Voltage	V		7.0
I_{DD}	Total Drain Current	mA		170
V_{G1}	First Gate Voltage	V	-3.5	0
V_{G2}	Second Gate Voltage	mA	-3.0	+3.0
P_{DC}	DC Power Dissipation	watts		1.2
P_{in}	CW Input Power	dBm		20
T_{ch}	Operating Channel Temp.	°C		+150
T_{case}	Operating Case Temp.	°C	-55	
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp. (for 60 seconds maximum)	°C		+300

Note:

1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A = 25°C except for T_{ch}, T_{STG}, and T_{max}.

HMMC-5025 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current (V_{DD} = 5.0 V, V_{G1} = 0.0 V, V_{G2} = open circuit)	mA	130	150	170
V_p	First Gate Pinch-off Voltage (V_{DD} = 5.0 V, I_{DD} = 15 mA, V_{G2} = open circuit)	V	-1.7		-0.5
V_{G2}	Second Gate Self-Bias Voltage (V_{DD} = 5.0 V, I_{DD} = 75 mA)	V		2	
$I_{DSOFF}(V_{G1})$	First Gate Pinch-off Current (V_{DD} = 5.0 V, V_{G1} = -3.5 V, V_{G2} = open circuit)	mA		6	10
$I_{DSOFF}(V_{G2})$	Second Gate Pinch-off Current (V_{DD} = 5.0 V, I_{DD} = 75 mA, V_{G2} = -3.5 V)	mA		10	
$\theta_{ch\text{-}bs}$	Thermal Resistance ($T_{backside}$ = 25°C)	°C/W		63	

Note:
1. Measured in wafer form with T_{chuck} = 25°C. (Except $\theta_{ch\text{-}bs}$.)

HMMC-5025 RF Specifications[1], V_{DD} = 5.0 V, $I_{DD}(Q)$ = 75 mA, $Z_{in} = Z_o$ = 50 Ω

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
BW	Guaranteed Bandwidth[2]	GHz	2		50
S_{21}	Small Signal Gain	dB	7.0	8.5	
ΔS_{21}	Small Signal Gain Flatness	dB		±0.75	±1.5
RL_{in}	Input Return Loss	dB	10	15	
RL_{out}	Output Return Loss	dB	10	15	
S_{12}	Reverse Isolation	dB	20	30	
P_{1dB}	Output Power @ 1dB Gain Compression @ 40 GHz	dBm		12	
P_{sat}	Saturated Output Power @ 40 GHz	dBm		16	
H_2	Second Harmonic Power Level (2 < f_o < 26) $P_o(f_o)$ = 10 dBm	dBc		-35	
H_3	Third Harmonic Power Level (2 < f_o < 20) $P_o(f_o)$ = 10 dBm	dBc		-25	
NF	Noise Figure (2 – 35 GHz) Noise Figure (35 – 50 GHz)	dB		5.0 7.0	

Notes:
1. Small-signal data measured in wafer form with T_{chuck} = 25°C. Harmonic data measured on individual devices mounted in a microcircuit package at T_A = 25°C.
2. Performance may be extended to lower frequencies through the use of appropriate off-chip circuitry.

HMMC-5025 Applications

The HMMC-5025 traveling wave amplifier is designed for use as a general purpose wideband power stage in communication systems and microwave instrumentation. It is ideally suited for broadband applications requiring a flat gain response and excellent port matches over a 2 to 50 GHz frequency range. Dynamic gain control and low-frequency extension capabilities are designed into these devices.

Biasing and Operation

These amplifiers are biased with a single positive drain supply (V_{DD}) and a single negative gate supply (V_{G1}). The recommended bias conditions for best performance for the HMMC-5025 are V_{DD} = 5.0 V, I_{DD} = 75 mA. To achieve these drain current levels, V_{G1} is typically biased between -0.2V and -0.6V. No other bias supplies or connections to the device are required for 2 to 50 GHz operation. The gate voltage (V_{G1}) should be applied prior to the drain voltage (V_{DD}) during power up and removed after the drain voltage during power down.

The auxiliary gate and drain contacts are used only for low-frequency performance extension below ≈ 1.0 GHz. When used, these contacts must be AC coupled only. (Do not attempt to apply bias to these pads.) The second gate (V_{G2}) can be used to obtain 30 dB (typical) dynamic gain control. For normal operation, no external bias is required on this contact.

Assembly Techniques

Solder die-attach using a fluxless AuSu solder preform is the recommended assembly method. Gold thermosonic wedge bonding with 0.7 mil diameter Au wire is recommended for all bonds. Tool force should be 22 ± 1 gram, stage temperature should be 150 ± 2°C, and ultrasonic power and duration should be 64 ± 1 dB and 76 ± 8 msec, respectively. The bonding pad and chip backside metallization is gold.

For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

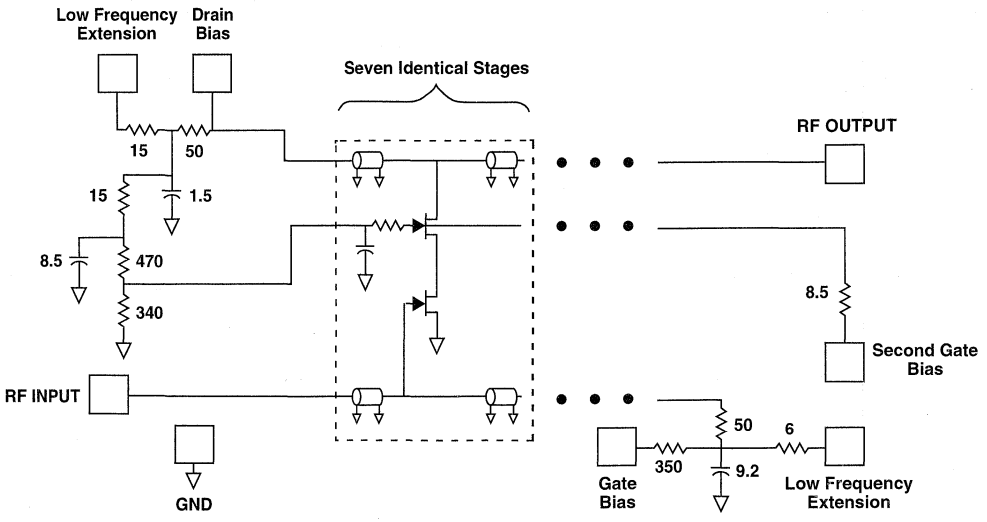


Figure 1. HMMC-5025 Schematic.

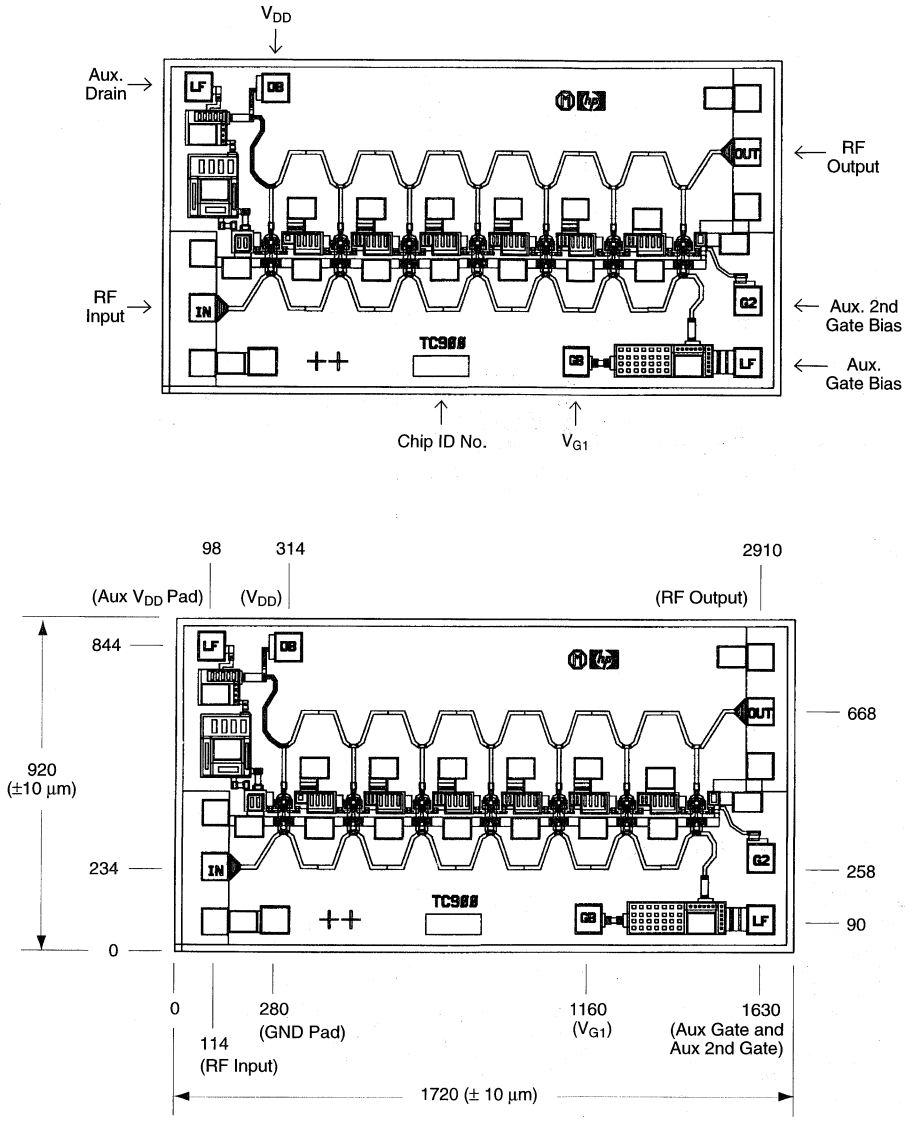


Figure 2. HMMC-5025 Bond Pad Locations.

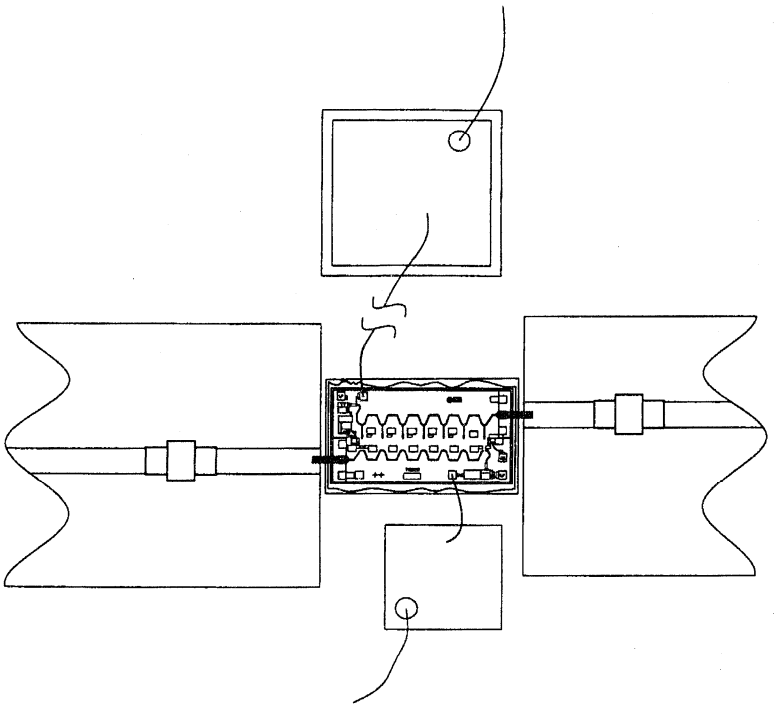


Figure 3. HMMC-5025 Assembly Diagram.

HMMC-5025 Typical Performance

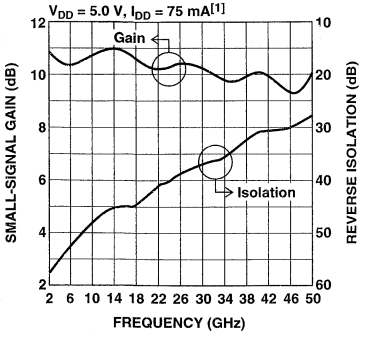


Figure 4. Typical Gain and Reverse Isolation vs. Frequency.

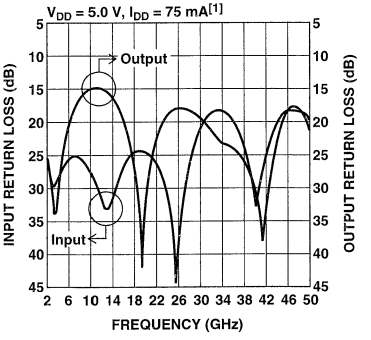


Figure 5. Typical Input and Output Return Loss vs. Frequency.

Note:
1. Data obtained from on-wafer measurements. T_{chuck} = 25°C.

HMMC-5025 Typical Scattering Parameters[1],

(T_{chuck} = 25°C, V_{DD} = 5.0 V, I_{DD} = 75 mA, Z_{in} = Z_o = 50 Ω

Freq.	S_{11}			S_{21}			S_{12}			S_{22}		
GHz	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
2	-24.6	0.059	-150.2	-52.0	0.0025	-110.2	8.5	2.660	147.8	-26.1	0.049	-64.0
3	-29.7	0.033	147.5	-49.1	0.0035	-130.2	8.4	2.630	139.6	-33.8	0.020	-23.6
4	-28.9	0.036	89.0	-47.1	0.0044	-146.4	8.4	2.630	129.8	-30.1	0.031	43.9
5	-27.0	0.045	56.2	-45.5	0.0053	-161.6	8.4	2.629	119.5	-24.6	0.059	55.9
6	-25.8	0.052	32.6	-44.2	0.0061	-176.8	8.4	2.643	108.9	-20.8	0.091	52.1
7	-25.2	0.055	12.7	-43.3	0.0068	169.3	8.5	2.668	98.1	-18.4	0.121	43.8
8	-25.4	0.054	-6.3	-42.6	0.0074	155.6	8.6	2.705	86.9	-16.7	0.147	33.4
9	-26.0	0.050	-25.3	-42.1	0.0078	143.8	8.8	2.743	75.5	-15.6	0.166	22.3
10	-27.4	0.043	-46.3	-41.7	0.0083	132.1	8.9	2.787	63.7	-15.0	0.178	10.7
11	-29.4	0.034	-70.4	-41.4	0.0085	121.9	9.0	2.823	51.6	-14.8	0.182	-0.9
12	-31.7	0.026	-102.9	-40.9	0.0090	112.3	9.1	2.853	39.3	-14.9	0.179	-12.6
13	-33.0	0.022	-145.8	-40.7	0.0093	104.5	9.2	2.874	26.9	-15.4	0.169	-24.2
14	-31.4	0.027	168.6	-40.3	0.0097	95.4	9.2	2.891	14.3	-16.3	0.153	-35.7
15	-29.1	0.035	136.8	-39.7	0.0104	88.5	9.2	2.891	1.8	-17.6	0.131	-47.3
16	-27.0	0.045	113.4	-39.0	0.0112	80.5	9.2	2.884	-10.8	-19.5	0.106	-59.3
17	-25.4	0.053	95.4	-38.4	0.0120	71.9	9.2	2.870	-23.3	-22.2	0.077	-72.0
18	-24.5	0.060	77.9	-37.7	0.0131	62.9	9.1	2.853	-35.7	-26.7	0.046	-86.1
19	-24.1	0.062	62.1	-37.1	0.0140	53.8	9.1	2.836	-48.1	-35.6	0.017	-114.9
20	-24.4	0.061	48.2	-36.3	0.0153	44.3	9.0	2.819	-60.3	-35.3	0.017	107.2
21	-25.0	0.056	37.0	-35.3	0.0172	32.7	9.0	2.806	-72.6	-27.0	0.045	80.0
22	-25.6	0.052	22.6	-35.1	0.0176	19.5	8.9	2.798	-84.7	-23.2	0.069	66.2
23	-27.7	0.041	7.2	-34.7	0.0184	8.9	8.9	2.796	-97.1	-21.0	0.089	54.9
24	-30.9	0.028	-8.2	-34.4	0.0191	-2.8	8.9	2.789	-109.5	-19.4	0.107	44.2
25	-38.4	0.012	-39.5	-34.3	0.0194	-14.7	8.9	2.789	-121.9	-18.6	0.118	33.6
26	-40.1	0.010	-169.3	-33.9	0.0202	-25.3	8.9	2.789	-134.5	-18.2	0.124	24.2
27	-30.9	0.029	156.0	-33.7	0.0206	-37.0	8.9	2.794	-147.2	-18.2	0.124	15.5
28	-26.0	0.050	138.6	-33.7	0.0206	-48.5	8.9	2.795	-160.1	-18.4	0.120	7.7
29	-23.1	0.070	122.8	-33.4	0.0213	-58.3	8.9	2.787	-173.1	-18.8	0.115	2.1
30	-21.0	0.089	110.2	-33.3	0.0216	-71.3	8.9	2.780	174.0	-19.6	0.105	-3.4
31	-19.8	0.102	95.3	-32.9	0.0228	-81.1	8.9	2.772	160.9	-20.5	0.095	-7.5
32	-18.9	0.114	82.3	-32.5	0.0236	-93.6	8.8	2.768	147.8	-21.3	0.086	-9.1
33	-18.6	0.117	70.4	-32.3	0.0244	-105.4	8.8	2.762	134.5	-22.4	0.076	-6.4
34	-18.5	0.118	58.6	-32.3	0.0244	-120.3	8.8	2.752	121.2	-23.0	0.071	-4.7
35	-19.0	0.112	46.2	-31.9	0.0254	-132.8	8.8	2.747	107.8	-23.5	0.067	-3.5
36	-20.0	0.100	35.6	-31.6	0.0264	-146.2	8.8	2.741	94.4	-23.7	0.066	-2.5
37	-21.5	0.084	26.4	-31.5	0.0266	-161.5	8.7	2.735	80.7	-24.4	0.060	-4.3
38	-24.0	0.063	18.8	-31.5	0.0267	-175.1	8.7	2.728	67.0	-25.4	0.054	-8.9
39	-27.6	0.042	18.9	-31.5	0.0266	171.1	8.7	2.723	53.0	-27.1	0.044	-11.8
40	-32.9	0.023	46.7	-31.4	0.0270	157.6	8.7	2.711	39.0	-30.4	0.030	-9.1
41	-30.3	0.031	99.2	-31.2	0.0276	140.9	8.6	2.703	24.8	-38.1	0.012	18.9
42	-25.5	0.053	107.1	-31.0	0.0282	125.0	8.6	2.695	10.5	-32.6	0.023	93.1
43	-22.2	0.078	102.7	-31.4	0.0270	115.6	8.6	2.689	-4.0	-26.2	0.049	94.9
44	-20.1	0.099	94.4	-31.1	0.0280	101.4	8.6	2.679	-18.1	-22.4	0.076	86.4
45	-19.0	0.112	85.3	-31.3	0.0272	87.2	8.5	2.672	-33.4	-20.2	0.098	75.3
46	-18.6	0.117	76.5	-30.5	0.0297	72.1	8.5	2.676	-48.5	-18.8	0.115	61.6
47	-18.3	0.121	69.8	-30.6	0.0297	49.9	8.6	2.686	-64.0	-18.0	0.126	48.2
48	-18.8	0.115	62.5	-30.7	0.0293	37.8	8.6	2.689	-79.8	-18.3	0.122	28.8
49	-19.3	0.108	59.9	-30.5	0.0300	20.0	8.6	2.691	-96.1	-19.5	0.106	6.1
50	-20.3	0.096	58.9	-30.3	0.0307	2.7	8.6	2.677	-293.0	-21.7	0.082	-22.7

Note:

1. Data obtained from on-wafer measurements.

HMMC-5025 Typical Performance

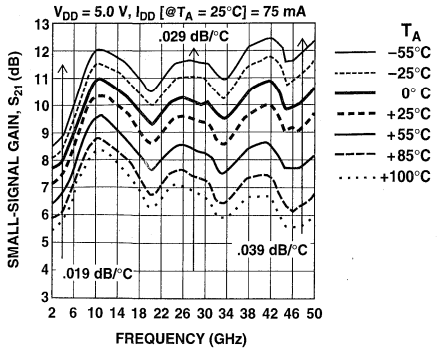


Figure 6. Typical Small-Signal Gain vs. Temperature.

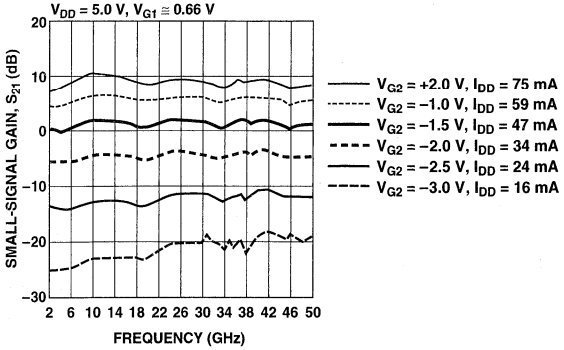


Figure 7. Typical Gain vs. Second Gate Control Voltage.

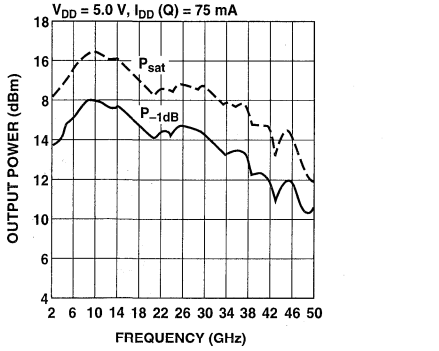


Figure 8. Typical 1 dB Gain Compression and Saturated Output Power vs. Frequency.

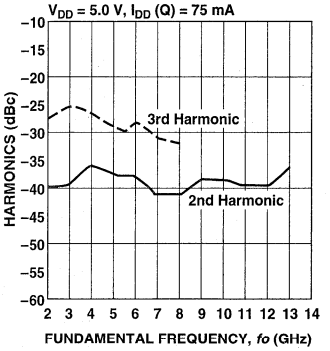


Figure 9. Typical Second and Third Harmonics vs. Fundamental Frequency at P_{OUT} = 10 dBm.

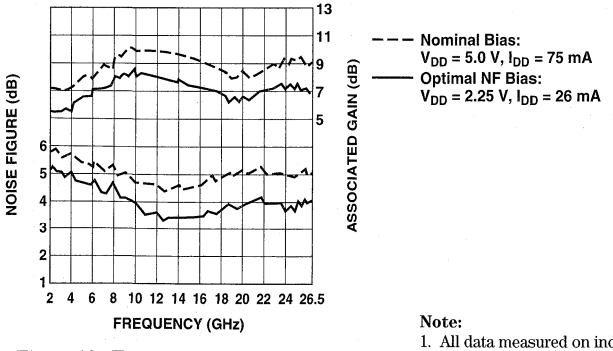


Figure 10. Typical Noise Figure Performance.

Note:

1. All data measured on individual devices mounted in an HP83040 Series Modular Microcircuit Package @ T_A = 25°C (except where noted).

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

HEWLETT® PACKARD

2 – 26.5 Medium Power Amplifier

Technical Data

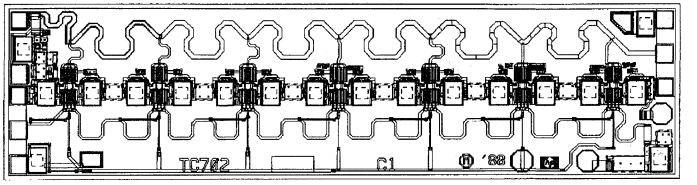
HMMC-5027

Features

- **Wide-Frequency Range:** 2-26.5 GHz
- **Moderate Gain:** 7 dB
- **Gain Flatness:** 1 dB
- **Return Loss:**
  Input -13 dB
  Output -11 dB
- **Low-Frequency Operation Capability:** < 2 GHz
- **Gain Control:**
  30 dB Dynamic Range
- **Medium Power:**
  20 GHz: P_{-1dB}: 22 dBm
  P_{sat}: 24 dBm
  26.5 GHz: P_{-1dB}: 19 dBm
  P_{sat}: 21 dBm

Description

The HMMC-5027 is a broadband GaAs MMIC Traveling Wave Amplifier designed for medium output power and moderate gain over the full 2 to 26.5 GHz frequency range. Seven MESFET cascode stages provide a flat gain response, making the HMMC-5027 an ideal wideband power block. Optical lithography is used to produce gate lengths of ≈0.5 mm. The HMMC-5027 incorporates advanced MBE technology, Ti-Pt-Au gate metallization, silicon nitride passivation, and polyimide for scratch protection.



Chip Size: 2980 x 770 µm (117.3 x 30.3 mils)
Chip Size Tolerance: ±10 µm (±0.4 mils)
Chip Thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions: 75 x 75 µm (2.95 x 2.95 mils), or larger

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{DD}	Positive Drain Voltage	V		8.0
I_{DD}	Total Drain Current	mA		300
V_{G1}	First Gate Voltage	V	-5	0
I_{G1}	First Gate Current	mA	-1	+1
V_{G2}	Second Gate Voltage	V	-2.5	+5
I_{G2}	Second Gate Current	mA	-25	
P_{DC}	DC Power Dissipation	watts		2.4
P_{in}	CW Input Power	dBm		23
T_{ch}	Operating Channel Temp.	°C		+150
T_{case}	Operating Case Temp.	°C	-55	
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp. (for 60 seconds maximum)	°C		+300

Note:
1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A = 25°C except for T_{ch}, T_{STG}, and T_{max}.

HMMC-5027 DC Specifications/Physical Properties [1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current (V_{DD} = 8.0 V, V_{G1} = 0.0 V, V_{G2} = open circuit)	mA	200	300	500
V_p	First Gate Pinch-off Voltage (V_{DD} = 8.0 V, I_{DD} = 30 mA, V_{G2} = open circuit)	V	-2.2	-1.3	-.5
V_{G2}	Second Gate Self-Bias Voltage (V_{DD} = 8.0 V, V_{G1} = 0.0 V)	V		1.8 (0.27 x V_{DD})	
$I_{DSOFF}(V_{G1})$	First Gate Pinch-off Current (V_{DD} = 8.0 V, V_{G1} = -3.5 V, V_{G2} = open circuit)	mA		7	
$I_{DSOFF}(V_{G2})$	Second Gate Pinch-off Current (V_{DD} = 5.0 V, V_{G1} = 0.0 V, V_{G2} = -3.5 V)	mA		10	
$\theta_{ch\text{-}bs}$	Thermal Resistance ($T_{backside}$ = 25°C)	°C/W		28	

Note:

1. Measured in wafer form with T_{chuck} = 25°C. (Except $\theta_{ch\text{-}bs}$.)

HMMC-5027 RF Specifications[1],

T_{op} = 25°C, V_{D1} = V_{D2} = 5 V, V_{G1} = V_{G2}= Open, Z_O = 50 Ω, unless otherwise noted

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
BW	Guaranteed Bandwidth[2]	GHz	2		26.5
S_{21}	Small Signal Gain	dB	6	7	
ΔS_{21}	Small Signal Gain Flatness	dB		±0.8	
RL_{in}	Input Return Loss	dB		-13	-10
RL_{out}	Output Return Loss	dB		-11	-10
S_{12}	Reverse Isolation	dB		-28	-25
P_{-1dB}	Output Power @ 1dB Gain Compression	dBm	16.5	19	
P_{sat}	Saturated Output Power	dBm	18.5	21	
H_2	Second Harmonic Power Level ($2 < f_o < 20$) [$P_o(f_o)$ = 21 dBm or P_{-1dB}, whichever is less]	dBc		-21	-18
H_3	Third Harmonic Power Level ($2 < f_o < 20$) [$P_o(f_o)$ = 21 dBm or P_{-1dB}, whichever is less]	dBc		-32	-18
NF	Noise Figure	dB		11	

Notes:

1. Small-signal data measured in wafer form with T_{chuck} = 25°C. Large-signal data measured on individual devices mounted in an HP83040 Series Modular Microcircuit Package at T_A = 25°C.
2. Performance may be extended to lower frequencies through the use of appropriate off-chip circuitry. Upper corner frequency ~ 30 GHz.

HMMC-5027 Applications

The HMMC-5027 series of traveling wave amplifiers are designed for use as general purpose wideband power stages in communication systems and microwave instrumentation. They are ideally suited for broadband applications requiring a flat gain response and excellent port matches over a 2 to 26.5 GHz frequency range. Dynamic gain control and low-frequency extension capabilities are designed into these devices.

Biasing and Operation

These amplifiers are biased with a single positive drain supply (V_{DD}) and a single negative gate supply (V_{G1}). The recommended bias conditions for the HMMC-5027 are V_{DD} = 8.0 V, I_{DD} = 250 mA or I_{DSS}, whichever is less. To achieve this drain current level, V_{G1} is typically biased between 0 V and -0.6 V. No other bias supplies or connections to the device are required for 2 to 26.5 GHz operation. The gate voltage (V_{G1}) MUST be applied prior to the drain voltage (V_{DD}) during power up and removed after the drain voltage during power down. See Figure 3 for assembly information.

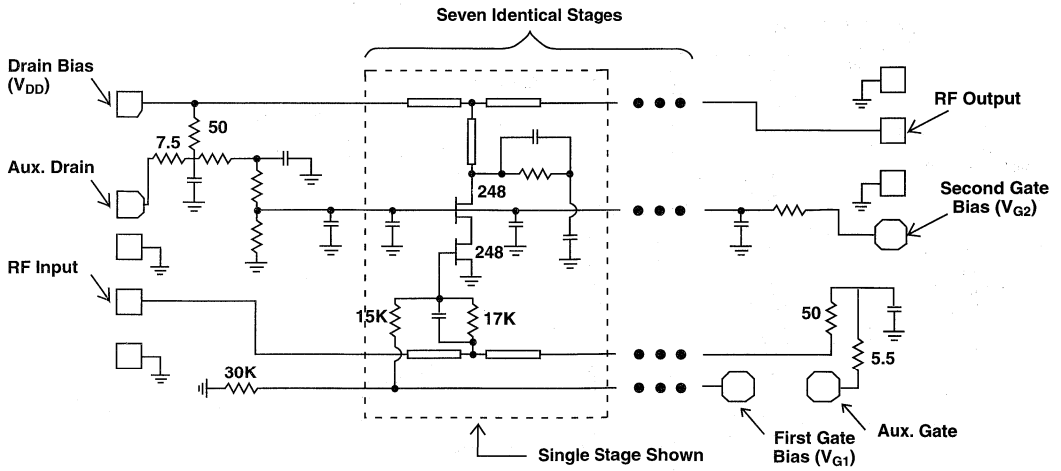
The auxiliary gate and drain contacts are used only for low-frequency performance extension below ≈ 1.0 GHz. When used, these contacts must be AC coupled only. (Do not attempt to apply bias to these pads.) The second gate (V_{G2}) can be used to obtain 30 dB (typical) dynamic gain control. For normal operation, no external bias is required on this contact and its self-bias potential is between +1.5 and +2.5 volts. Applying an external bias between its open circuit potential and -2.5 volts will adjust the gain while maintaining a good input/output port match.

Assembly Techniques

Solder die-attach using a fluxless AuSu solder preform is the recommended assembly method. Gold thermosonic wedge bonding with 0.7 mil diameter Au wire is recommended for all bonds. Tool force should be 22 ± 1 gram, stage temperature should be 150 ± 2°C, and ultrasonic power and duration should be 64 ± 1 dB and 76 ± 8 msec, respectively. The bonding pad and chip backside metallization is gold.

For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.



Notes:
FET gate periphery in microns.
All resistors in ohms. (Ω),
(or in K-ohms, where indicated)

Figure 1. HMMC-5027 Schematic.

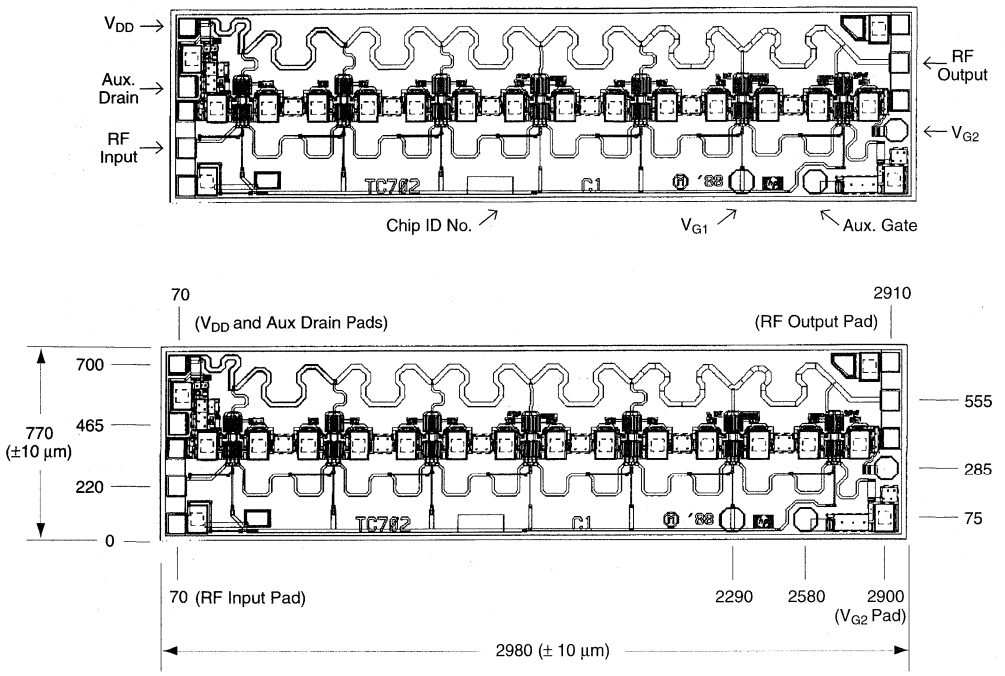


Figure 2. HMMC-5027 Bonding Pad Locations.

Notes:
All dimensions in microns.
Rectangular Pad Dim: 75 x 75 µm.
Octagonal Pad Dim: 90 µm dia.
All other dimensions ±5 µm (unless otherwise noted).
Chip thickness: 127 ± 15 µm.

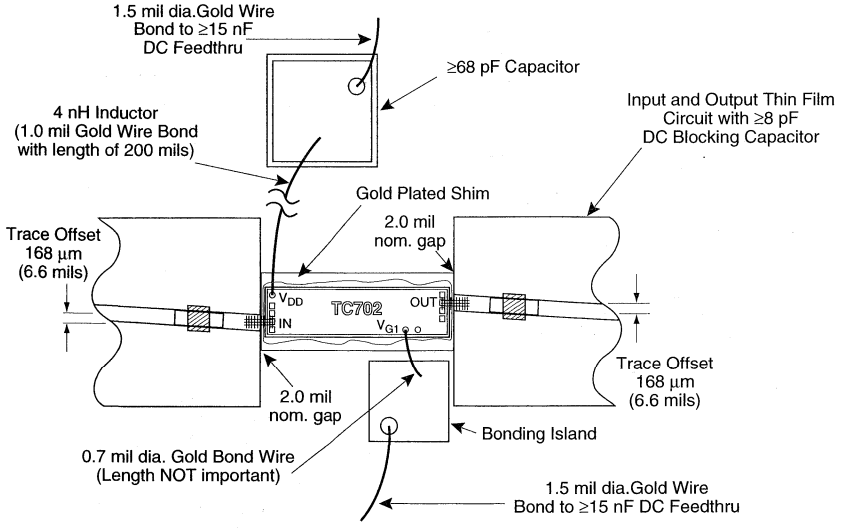


Figure 3. HMMC-5027 Assembly Diagram.

Note:
Total offset between RF input and RF output pad is 335 µm (13.2 mils).

HMMC-5027 Typical Performance

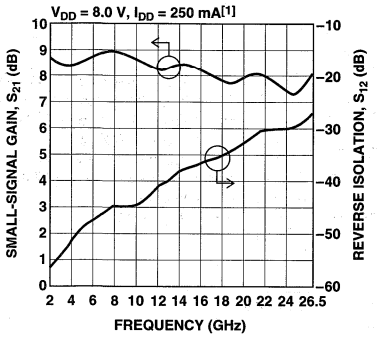


Figure 4. Typical Gain and Reverse Isolation vs. Frequency.

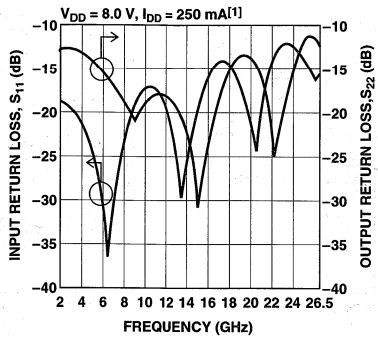


Figure 5. Typical Input and Output Return Loss vs. Frequency.

Typical Scattering Parameters[1],

(T_{chuck} = 25°C, V_{DD} = 8.0 V, I_{DD} = 250 mA or I_{DSS}, whichever is less, $Z_{in} = Z_o = 50\ \Omega$

Freq.	S_{11}			S_{21}			S_{12}			S_{22}		
GHz	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
2.0	-18.7	0.116	-139.5	-57.7	0.0013	-165.2	8.7	2.717	116.6	-13.0	0.223	173.5
3.0	-20.1	0.099	-159.0	-54.9	0.0018	144.2	8.4	2.635	94.8	-13.0	0.224	150.0
4.0	-21.5	0.084	-175.7	-52.0	0.0025	154.0	8.3	2.612	72.0	-13.5	0.212	127.1
5.0	-24.6	0.059	167.8	-49.9	0.0032	111.3	8.4	2.634	48.2	-14.0	0.200	101.6
6.0	-32.0	0.025	167.4	-48.2	0.0039	91.3	8.6	2.699	23.3	-15.3	0.171	71.7
7.0	-30.8	0.029	-94.8	-46.9	0.0045	74.9	8.8	2.763	-3.5	-16.9	0.143	39.5
8.0	-22.7	0.073	-103.2	-45.5	0.0053	21.0	8.8	2.768	-30.9	-18.4	0.120	-2.2
9.0	-18.9	0.114	-121.5	-45.2	0.0055	10.3	8.8	2.744	-58.9	-21.3	0.086	-46.9
10.0	-17.2	0.137	-142.6	-44.7	0.0058	-15.5	8.5	2.673	-85.9	-18.9	0.114	-90.7
11.0	-17.4	0.135	-163.9	-43.5	0.0067	-33.4	8.3	2.608	-112.5	-17.9	0.127	-129.6
12.0	-19.3	0.108	175.6	-41.5	0.0084	-45.4	8.2	2.564	-138.5	-18.2	0.123	-162.6
13.0	-25.6	0.052	170.3	-40.6	0.0093	-75.8	8.2	2.578	-164.9	-19.3	0.108	163.4
14.0	-27.0	0.045	-113.0	-38.6	0.0118	-95.9	8.3	2.610	167.1	-22.1	0.078	126.5
15.0	-19.2	0.109	-111.0	-37.8	0.0129	-124.7	8.3	2.605	138.4	-31.2	0.028	56.7
16.0	-15.6	0.167	-127.9	-37.1	0.0139	-149.1	8.2	2.574	108.8	-23.5	0.067	-33.3
17.0	-14.3	0.193	-148.4	-36.3	0.0153	-174.5	8.0	2.510	79.7	-18.1	0.124	-80.7
18.0	-14.8	0.182	-166.6	-35.8	0.0163	164.1	7.8	2.444	50.9	-15.2	0.174	-115.2
19.0	-17.1	0.140	-179.3	-34.7	0.0185	141.5	7.7	2.418	22.1	-13.7	0.207	-147.6
20.0	-21.4	0.086	-166.2	-32.9	0.0227	112.6	7.8	2.466	-7.5	-13.9	0.202	177.9
21.0	-18.4	0.121	-129.5	-31.6	0.0262	80.7	8.1	2.527	-39.9	-16.8	0.145	136.7
22.0	-13.8	0.205	-137.2	-30.9	0.0285	42.7	8.0	2.512	-74.0	-25.3	0.054	66.9
23.0	-12.1	0.247	-152.7	-30.6	0.0296	13.3	7.6	2.395	-108.4	-19.8	0.102	-56.2
24.0	-12.3	0.244	-169.8	-30.3	0.0304	-15.5	7.4	2.344	-142.5	-13.7	0.207	-103.5
25.0	-14.7	0.184	-175.8	-29.7	0.0329	-44.9	7.3	2.315	-175.6	-11.3	0.272	-136.7
26.0	-16.7	0.146	-149.3	-28.5	0.0375	-78.1	7.9	2.469	148.1	-11.7	0.259	-171.3
26.5	-14.1	0.197	-141.6	-28.0	0.0399	-98.5	8.0	2.503	126.9	-13.0	0.223	172.3

Note:

1. Data obtained from on-wafer measurements.

HMMC-5027 Typical Performance

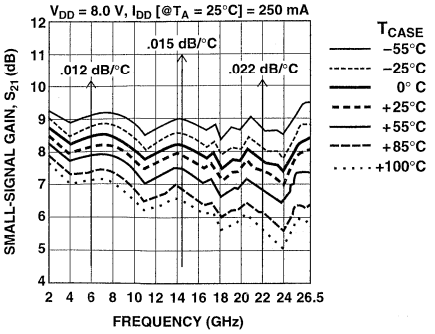


Figure 6. Typical Small-Signal Gain vs. Temperature.

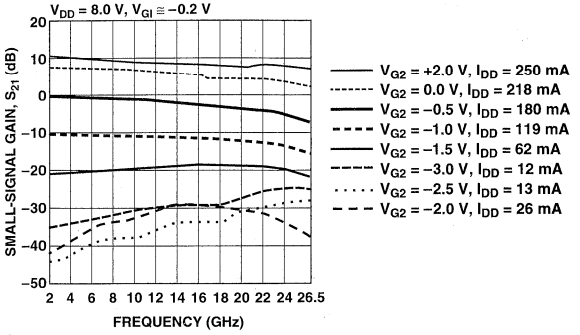


Figure 7. Typical Gain vs. Second Gate Control Voltage.

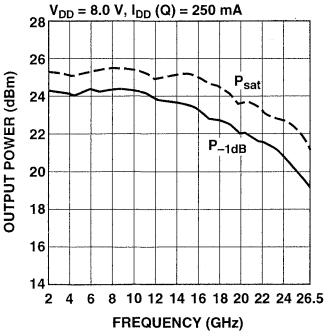


Figure 8. Typical 1 dB Gain Compression and Saturated Output Power vs. Frequency.

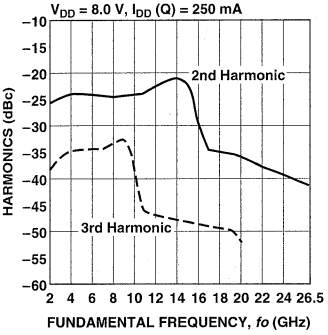


Figure 9. Typical Second and Third Harmonic vs. Fundamental Frequency at P_{OUT} = +21 dBm.

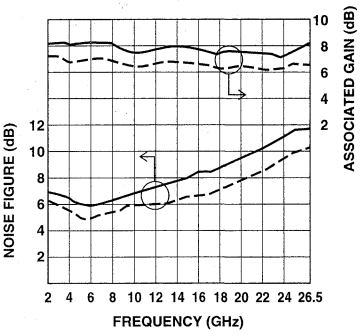


Figure 10. Typical Noise Figure Performance.

Note:

1. All data measured on individual devices mounted in an HP83040 Series Modular Microcircuit Package @ T_A = 25°C (except where noted).

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

38 GHz LNA

Technical Data

HMMC-5038

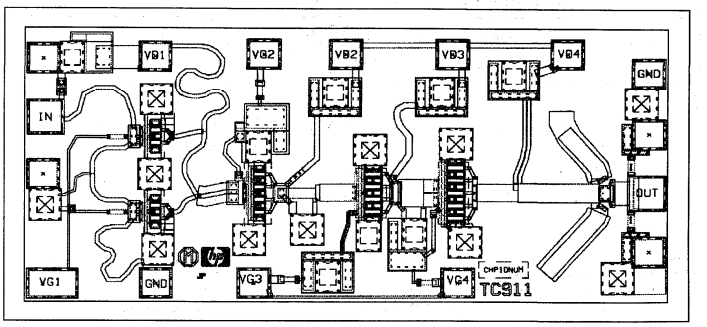
Features

- **Low Noise Figure:** 4.8 dB
- **Frequency Range:** 37 – 40 GHz
- **High Gain (Adjustable):** 3 V, 120 mA @ 23 dB Gain 3 V, 80 mA @ 20 dB Gain
- **50 Ω Input/Output Matching**

Description

The HMMC-5038 MMIC is a high-gain low-noise amplifier (LNA) designed for communication receivers that operate from 37 GHz to 40 GHz. The gain of this four stage LNA can be adjusted by altering the gate bias of the output two, or three, stages while maintaining optimum noise figure bias for the input stage(s). Large FETs provide high power handing capability to avoid power compression. The backside of the chip is both RF and DC ground. This helps simplify the assembly process and reduce assembly related performance variations and costs.

The HMMC-5038 is fabricated using a PHEMT integrated circuit structure that provides good noise and gain performance.



Chip Size:	1630 x 760 µm (64.2 x 29.9 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	80 x 80 µm (3.1 x 3.1 mils)

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
$V_{D1, 2-3-4}$	Drain Supply Voltages	V		5
$I_{G1, 2-3-4}$	Gate Supply Voltages	V	-3.0	0
I_{DD}	Total Drain Current	mA		300
P_{in}	RF Input Power	dBm		15
T_{ch}	Channel Temperature[2]	°C		+160
T_A	Backside Ambient Temp.	°C	-55	+125
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp.	°C		+310

Note:

1. Absolute maximum ratings for continuous operation unless otherwise noted.
2. Refer to DC Specifications/Physical Properties table for derating information.

DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
$V_{D1, 2-3-4}$	Low Noise Drain Supply Operating Voltages	V	2	3	5
I_{D1}	First Stage Drain Supply Current (V_{DD} = 3 V, V_{G1} = -0.8 V)	mA		22	
I_{D2-3-4}	Drain Supply Current for Stages 2, 3, and 4 Combined (V_{DD} = 3 V, V_{GG} = -0.8 V)	mA		98	
$V_{G1, 2, 3-4}$	Gate Supply Operating Voltages (I_{DD} = 120 mA)	V		-0.8	
V_p	Pinch-off Voltage (V_{DD} = 3 V, $I_{DD} \leq$ 10 mA)	V	-2	-1.2	-0.8
θ_{ch-bs}	Thermal Resistance[2] (Channel-to-Backside @ T_{ch} = 160°C)	°C/W		62	
T_{ch}	Channel Temperature[3] (T_A = 125°C, MTTF > 10^6 hrs, V_{DD} = 3 V, I_{DD} = 120 mA)	°C		150	

Notes:
1. Backside ambient operating temperature T_A = 25°C unless otherwise noted.
2. Thermal resistance (°C/Watt) at a channel temperature T (°C) can be *estimated* using the equation: $\theta(T) \cong 62 \times [T(°C) + 273] / [160°C + 273]$.
3. Derate MTTF by a factor of two for every 8°C above T_{ch}.

RF Specifications, T_A = 25°C, V_{DD} = 3 V, I_{DD} = 120 mA, Z_o = 50 Ω

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
BW	Operating Bandwidth	GHz	37		40
S_{21}	Small Signal Gain[1]	dB	20	23	
ΔS_{21}	Small Signal Gain Flatness	dB		±0.5	
$(RL_{in})_{MIN}$	Minimum Input Return Loss w/o external capacitive matching[2]	dB	8	12	
$(RL_{out})_{MIN}$	Minimum Output Return Loss	dB	12	18	
S_{12}	Reverse Isolation	dB		50	
P_{-1dB}	Output Power @ 1dB Gain Compression	dBm		12	
NF	Noise Figure[3]	dB		4.8	

Notes:
1. Gain may be reduced by biasing for lower I_{DD}. Increasing I_{DD} will increase Gain.
2. Minimum input return may be improved by approximately 3 dB by including a small capacitive (~30 fF) stub on the input transmission line.
3. Noise Figure may be further reduced by optimizing DC bias conditions.

Applications

The HMMC-5038 low noise amplifier (LNA) is designed for use in digital radio communication systems and point-to-multipoint links that operate within the 37 GHz to 40 GHz frequency band. High gain and low noise temperature make it ideally suited as a front-end gain stage in the receiver. The MMIC solution is a cost effective alternative to hybrid assemblies.

Biasing and Operation

The recommended DC bias condition is with all drains connected to single 3 volt supply and all gates connected to an adjustable negative voltage supply as shown in Figure 1(a). The gate voltage is adjusted for a total drain supply current of typically 120 mA. Reducing the current in stages 3 and 4 will reduce the overall gain. The gain can be adjusted further by altering the current through stage 2 with little affect on noise figure. Optimum noise figure is realized with V_{D1}= 3 to 4 volts and I_{D1} = 20 to 25 mA.

The second, third, and fourth stage DC drain bias lines are connected internally and therefore require only a single bond wire. An additional bond wire is needed for the first stage DC drain bias, V_{D1}.

The third and fourth stage DC gate bias lines are connected internally. A total of three DC gate bond wires are required: One for V_{G1}, one for V_{G2}, and one for the V_{G3}-to-V_{G4} connection as shown in Figure 1.

A DC blocking capacitor is needed in the RF input transmission line only if there is DC voltage present. The RF output is AC-coupled.

Optimum input match is achieved when an optional capacitive (~30 fF) stub is included on the input transmission line. This capacitance compliments the bond wire inductance to complete the input matching network. No ground wires are needed because ground connections are made with plated through-holes to the backside of the device.

Assembly Techniques

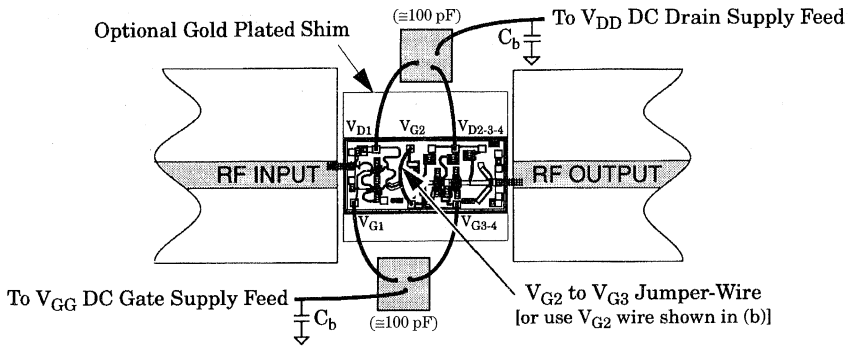
A conductive epoxy such as ABLEBOND® 71-1LM1 or ABLEBOND® 84-1LM1 is the recommended assembly method provided the Absolute Maximum Thermal Ratings are not exceeded. Solder die attach using a fluxless gold-tin (AuSn) solder preform may also be used. The device should be attached to an electrically conductive surface to complete the DC and RF ground paths. The backside metallization on the device is gold.

It is recommended that the RF input and RF output connections be made using either 500 line/inch (or equivalent) gold wire mesh, or dual 0.7 mil diameter gold wire. The RF wires should be kept as short as possible to minimize inductance. The bias supply can be 0.7 mil diameter gold wires.

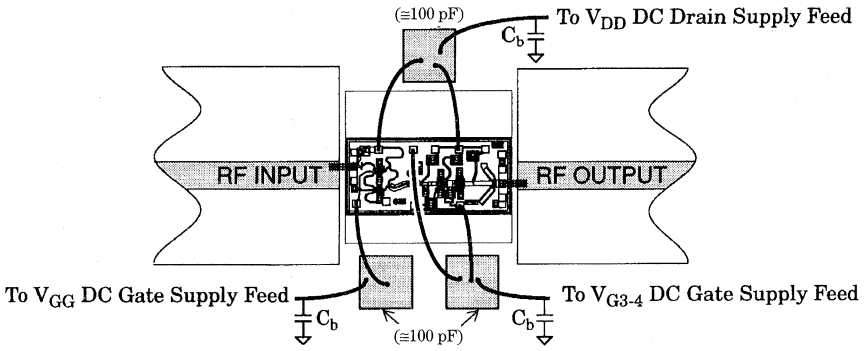
Thermosonic wedge is the preferred method for wire bonding to the gold bond pads. Mesh wires can be attached using a 2 mil round tacking tool and a tool force of approximately 22 grams with an ultrasonic power of roughly 55 dB for a duration of 76 ± 8 msec. A guided-wedge at an ultrasonic power level of 64 dB can be used for the 0.7 mil wire. The recommended wire bond stage temperature is 150 ± 2°C.

For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.



(a) Single drain-supply and single gate-supply assembly.



(b) Separate first-stage gate bias supply.

This diagram shows an optional variation to the V_{G2} jumper-wire bonding scheme presented in (a).

Figure 1. HMMC-5038 Common Assembly Diagrams.
(Note: To assure stable operation, bias supply feeds should be bypassed to ground with a capacitor, C_b > 100 nF typical.)

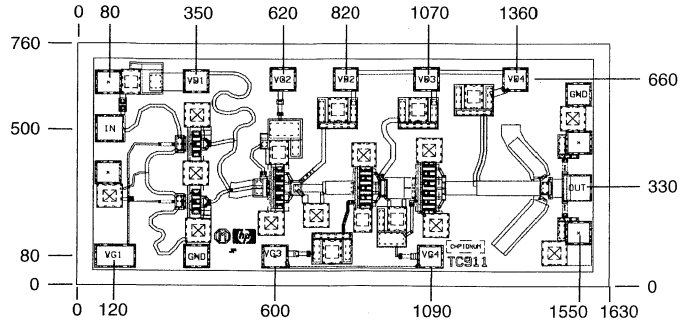


Figure 2. HMMC-5038 Bonding Pad Locations. (Dimensions in micrometers)

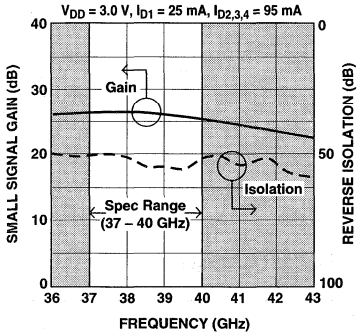


Figure 3. Gain and Isolation vs. Frequency.

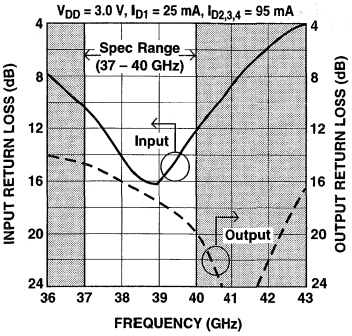


Figure 4. Input and Output Return Loss vs. Frequency.

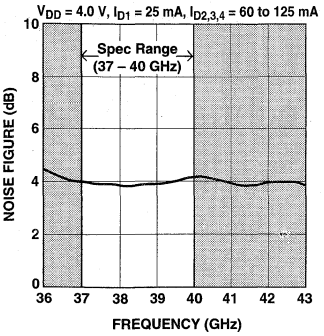


Figure 5. Noise Figure vs. Frequency.

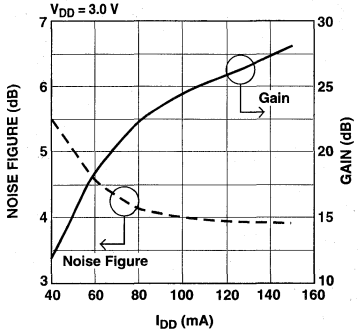


Figure 6. 38 GHz Noise Figure and Gain vs. I_{DD}.

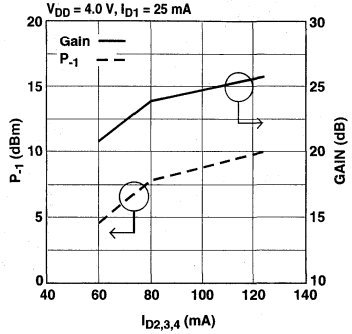


Figure 7. 38 GHz Gain and Power Performance vs. $I_{D2,3,4}$.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

HEWLETT® PACKARD

20–40 GHz Amplifier

Technical Data

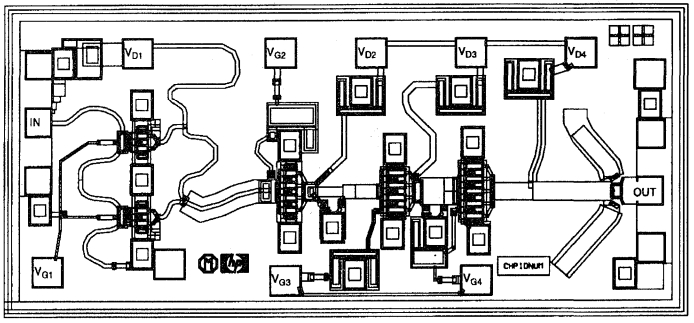
HMMC-5040

Features

- **Large Bandwidth:** 20 - 44 GHz Typical 21 - 40 GHz Specified
- **High Gain:** 22 dB Typical
- **Saturated Output Power:** 21 dBm Typical
- **Supply Bias:** ≤ 4.5 volts @ ≤ 300 mA

Description

The HMMC-5040 is a high-gain broadband MMIC amplifier designed for both military applications and commercial communication systems. This four stage amplifier has input and output matching circuitry for use in 50 ohm environments. It is fabricated using a PHEMT integrated circuit structure that provides exceptional broadband performance. The backside of the chip is both RF and DC ground. This helps simplify the assembly process and reduces assembly related performance variations and costs. This MMIC is a cost effective alternative to hybrid (discrete-FET) amplifiers that require complex tuning and assembly processes.



Chip Size:	1720 x 760 µm (67.7 x 29.9 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	80 x 80 µm (3.1 x 3.1 mils)

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
$V_{D1, 2-3-4}$	Drain Supply Voltages	V		5
$V_{G1, 2-3-4}$	Gate Supply Voltages	V	-3.0	0.5
I_{DD}	Total Drain Current	mA		400
P_{in}	RF Input Power	dBm		21
T_{ch}	Channel Temperature[2]	°C		+160
T_A	Backside Ambient Temp.	°C	-55	+75
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp.	°C		+300

Note:

1. Absolute maximum ratings for continuous operation unless otherwise noted.
2. Refer to DC Specifications/Physical Properties table for derating information.

HMMC-5040 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
$V_{D1, 2-3-4}$	Drain Supply Operating Voltages	V	2	4.5	5
I_{D1}	First Stage Drain Supply Current (V_{DD} = 4.5 V, V_{G1} = -0.6 V)	mA		55	
I_{D2-3-4}	Total Drain Supply Current for Stages 2, 3, and 4 (V_{DD} = 4.5 V, V_{GG} = -0.6 V)	mA		24.5	
$V_{G1, 2, 3-4}$	Gate Supply Operating Voltages (I_{DD} = 300 mA)	V		-0.6	
V_p	Pinch-off Voltage (V_{DD} = 4.5 V, $I_{DD} \leq$ 10 mA)	V	-2	-1.2	-0.8
θ_{ch-bs}	Thermal Resistance[2] (Channel-to-Backside @ T_{ch} = 160°C)	°C/W		62	
T_{ch}	Channel Temperature[3] (T_A = 125°C, MTTF > 10^6 hrs, V_{DD} = 4.5 V, I_{DD} = 300 mA)	°C		160	

Notes:
1. Backside ambient operating temperature T_A = 25°C unless otherwise noted.
2. Thermal resistance (°C/Watt) at a channel temperature T (°C) can be *estimated* using the equation: $\theta(T) \cong 62 \times [T(°C) + 273] / [160°C + 273]$.
3. Derate MTTF by a factor of two for every 8°C above T_{ch}.

HMMC-5040 RF Specifications, T_A = 25°C, V_{DD} = 4.5 V, I_{DD} = 300 mA, Z_o = 50 Ω

Symbol	Parameters/Conditions		Broadband Specifications			Narrow Band Performance		
		Units	Min.	Typ.	Max.	Typical		
BW	Operating Bandwidth	GHz	21	20–44	40	21–24	27–29	37–40
S_{21}	Small Signal Gain	dB	20	22		25	23	22
ΔS_{21}	Small Signal Gain Flatness	dB		±1.5		±1	±0.75	±0.3
$(RL_{in})_{MIN}$	Minimum Input Return Loss	dB	8	10		9	10	14
$(RL_{out})_{MIN}$	Minimum Output Return Loss	dB	8	10		10	11	12
S_{12}	Reverse Isolation	dB		54		54	54	54
P_{-1dB}	Output Power (@ 1dB Gain Compression)	dBm		18		18	18	18
P_{sat}	Saturated Output Power @ 3 dB Gain Compression	dBm	20	21		21	21	21

HMMC-5040 Applications

The HMMC-5040 broadband amplifier is designed for both military (35 GHz) applications and wireless communication systems that operate at 23, 28, and 38 GHz. It is also suitable for use as a frequency multiplier due to excellent below-band input return loss and high gain.

Biasing and Operation

The recommended DC bias condition is with all drains connected to single 4.5 volt (or less) supply and all gates connected to an adjustable negative voltage supply as shown in Figure 12a. The gate voltage is adjusted for a total drain supply current of typically up to 300 mA. Figures 4, 5, 8, and 9 can be used to help estimate the minimum drain voltage and current necessary for a given RF gain and output power.

The second, third, and fourth stage DC drain bias lines are connected internally (Figure 1) and therefore require only a single bond wire. An additional bond wire is needed for the first stage DC drain bias, V_{D1}.

Only the third and fourth stage DC gate bias lines are connected internally. A total of three DC gate bond wires are required: one for V_{G1}, one for V_{G2}, and one for the V_{G3}-to-V_{G4} connection. The RF input has matching circuitry that creates a 50 ohm DC and RF path to ground. A DC blocking capacitor should be used in the RF input transmission line. Any DC voltage applied to the RF input must be maintained below 1 volt. The RF output is AC-coupled.

No ground wires are needed since ground connections are made with plated through-holes to the backside of the device.

The HMMC-5040 can also be used to double, triple, or quadruple the frequency of input signals. Many bias schemes may be used to generate and amplify desired harmonics within the device. The information given here is intended to be used by the customer as a starting point for such applications. Optimum conversion efficiency is obtained with approximately 14 dBm input drive level.

As a doubler, the device can multiply an input signal in the 10-20 GHz frequency range up to 20-40 GHz with conversion gain for output frequencies exceeding 30 GHz. Similarly, 5-10 GHz signals can be quadrupled to 20-40 GHz with some conversion loss. Frequency doubling or quadrupling is accomplished by operating the first gain stage at pinch-off ($V_{G1} = V_P \cong -1.2$ volts). Stages 2, 3, and 4 are biased for normal amplification. The assembly diagram shown in Figure 12b can be used.

To operate the device as a frequency *tripler* the drain voltage can be reduced to approximately 2.5 volts and the gate voltage can be set at about -0.4 volts or adjusted to minimize second harmonics if needed. Either of Figures 12a or Figure 12b can be used.

Contact your local HP sales representative for additional information concerning multiplier performance and operating conditions.

Assembly Techniques

Solder die attach using a fluxless gold-tin (AuSn) solder preform is the recommended assembly method. A conductive epoxy such as ABLEBOND® 71-1LM1 or ABLEBOND® 36-2 may also be used for die attaching provided the Absolute Maximum Ratings are not exceeded. The device should be attached to an electrically conductive surface to complete the DC and RF ground paths. The backside metallization on the device is gold.

It is recommended that the RF input and output connections be made using either 500 lines/inch (or equivalent) gold wire mesh. The RF connections should be kept as short as possible to minimize inductance. The DC bias supply wires can be 0.7 mil diameter gold.

Thermosonic wedge is the preferred method for wire bonding to the gold bond pads. Mesh wires can be attached using a 2 mil round tacking tool and a tool force of approximately 22 grams with an ultrasonic power of roughly 55 dB for a duration of 76 ± 8 msec. A guided-wedge at an ultrasonic power level of 64 dB can be used for the 0.7 mil wire. The recommended wire bond stage temperature is 150 ± 2°C.

For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

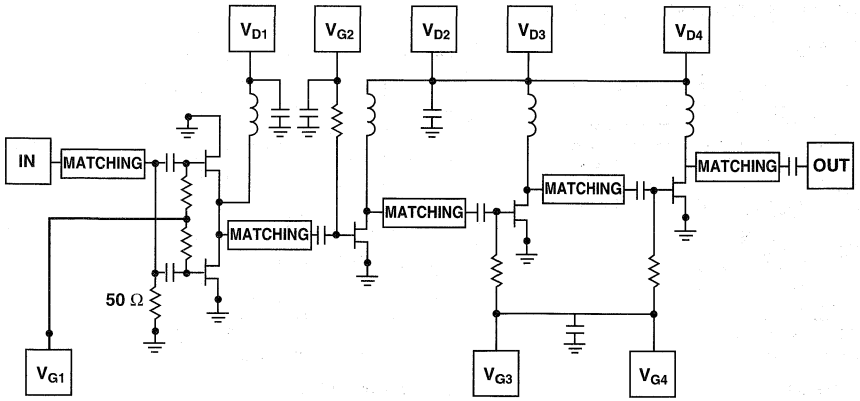


Figure 1. HMMC-5040 Simplified Schematic Diagram.

HMMC-5040 Typical Performance

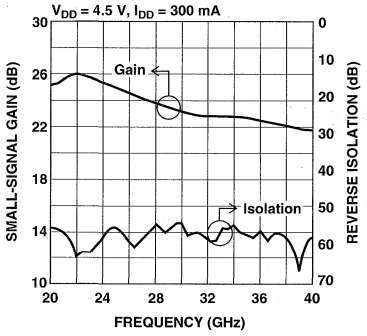


Figure 2. Typical Gain and Isolation vs. Frequency.[1]

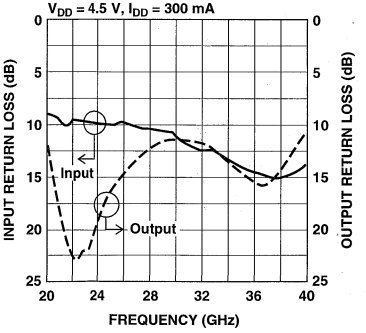


Figure 3. Typical Input and Output Return Loss vs. Frequency.[1]

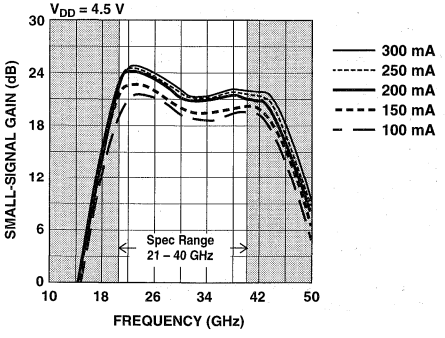


Figure 4. Broadband Gain as a Function of Drain Current vs. Frequency with V_{DD} = 4.5 V.[1]

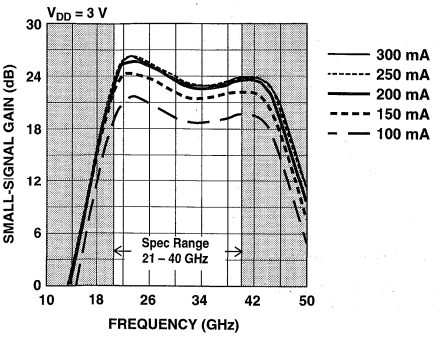


Figure 5. Broadband Gain as a Function of Drain Current vs Frequency with V_{DD} = 3 V.[1]

Note:
1. Wafer-probed measurements

HMMC-5040 Typical Performance, continued

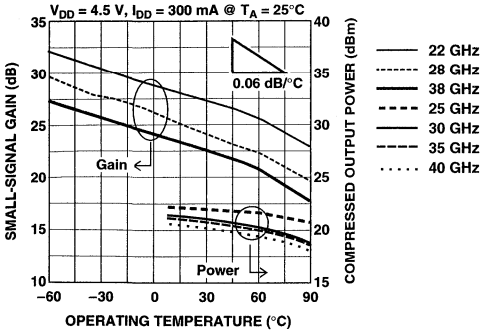


Figure 6. Small-Signal Gain[3] and Compressed Power[1] vs. Temperature.

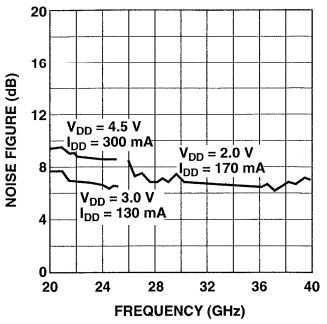


Figure 7. Noise Figure vs. Frequency.

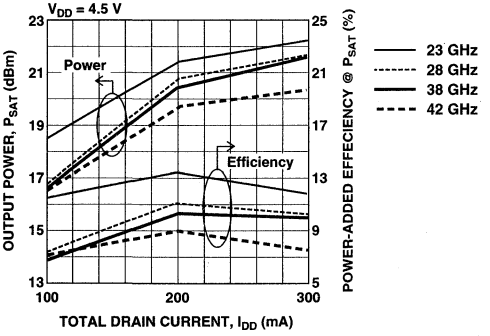


Figure 8. Output Power[1] and Efficiency vs. Drain Current with V_{DD} = 4.5 V.

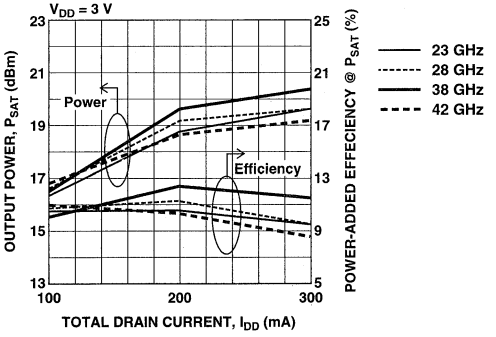


Figure 9. Output Power[1] and Efficiency vs. Drain Current with V_{DD} = 3 V.

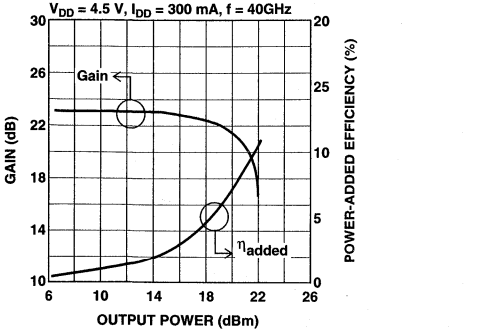


Figure 10. Gain Compression and Efficiency Characteristics.[2]

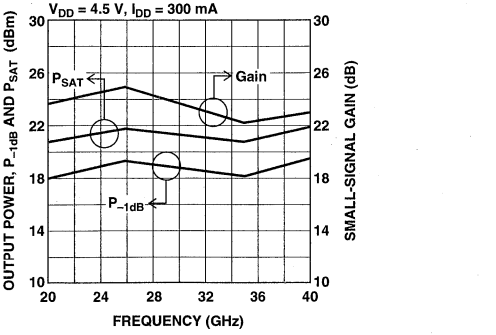


Figure 11. Output Power and Gain vs. Frequency Characteristics.[2]

Notes:
1. Output power into 50 Ω with 2 dBm input power. Wafer-probed measurements.
2. Wafer-probed measurements.
3. Measurements taken on a device mounted in a connectorized package calibrated at the connector terminals.

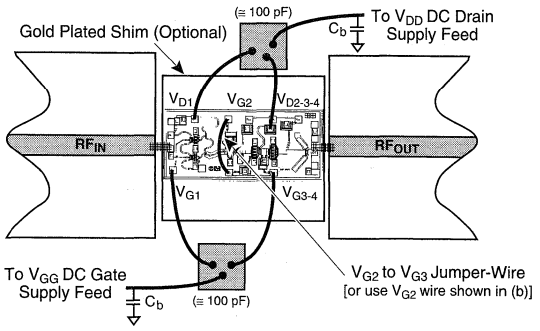


Figure 12a. Single drain and single gate supply assembly for tripler and standard amplifier applications.

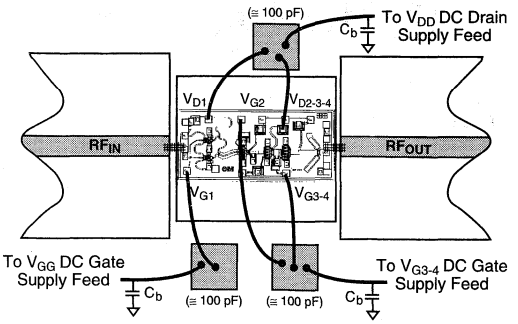


Figure 12b. Separate first-stage gate bias supply for any multiplier or amplifier application. This diagram shows an optional variation to the V_{G2} jumper-wire bonding scheme presented in (a).

Figure 12. HMMC-5040 Common Assembly Diagrams.
(Note: To assure stable operation, bias supply feeds should be bypassed to ground with a capacitor, C_b > 100 nF typical.)

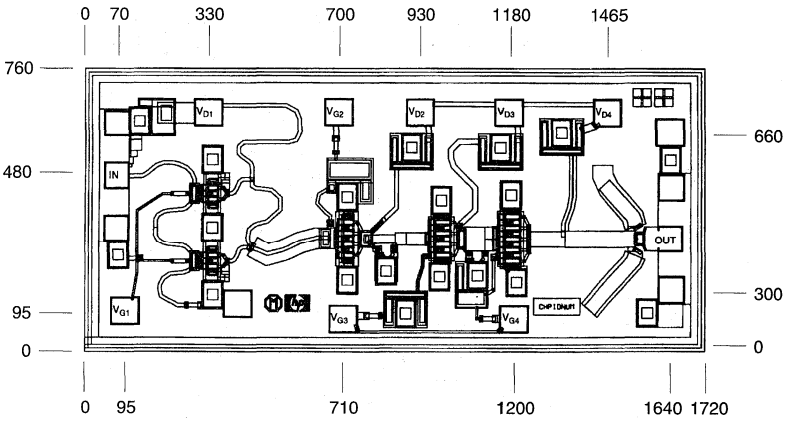


Figure 13. HMMC-5040 Bonding Pad Locations. (Dimensions in micrometers)

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

HEWLETT® PACKARD

6–20 GHz Amplifier

Technical Data

HMMC-5618

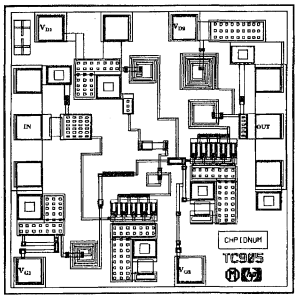
Features

- **High Efficiency:** 11% @ P_{-1dB} Typical
- **Output Power, P_{-1dB}:** 18 dBm Typical
- **High Gain:** 14 dB Typical
- **Flat Gain Response:** ±0.5 dB Typical
- **Low Input/Output VSWR:** <1.7:1 Typical
- **Single Supply Bias:** 5 volts (@ 115 mA Typical) with Optional Gate Bias

Description

The HMMC-5618 6–20 GHz MMIC is an efficient two-stage amplifier that is designed to be used as a cascadable intermediate gain block for EW applications. In communication systems, it can be used as an amplifier for a local oscillator, or as a transmit amplifier. It is fabricated using a PHEMT integrated circuit structure that provides exceptional efficiency and flat gain performance. During typical operation, with a single 5-volt DC power supply, each gain stage is biased for Class-A operation for optimal power output with minimal distortion. The RF input and RF output has matching circuitry for use in 50 ohm environments.

The backside of the chip is both RF and DC ground. This helps simplify the assembly process and reduces assembly related performance variations and costs. The MMIC is a cost effective alternative to hybrid (discrete-FET) amplifiers that require complex tuning and assembly processes.



Chip Size:	920 x 920 µm (36.2 x 36.2 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	80 x 80 µm (3.2 x 3.2 mils)

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{D1}, V_{D2}	Drain Supply Voltage	V		5.5
V_{G1}	Optional Gate Supply Voltage	V	-5	+1
V_{G2}	Optional Gate Supply Voltage	V	-10	+1
I_{D1}	Drain Supply Current	mA		70
I_{D2}	Drain Supply Current	mA		84
P_{in}	RF Input Power[2]	dBm		20
T_{ch}	Channel Temp.[3]	°C		+160
T_A	Backside Ambient Temp.	°C	-55	+100
T_{STG}	Storage Temperature	°C	-65	+150
T_{max}	Maximum Assembly Temp.	°C		+300

Notes:

1. Absolute maximum ratings for continuous operation unless otherwise noted.
2. Operating at this power level for extended (continuous) periods is not recommended.
3. Refer to *DC Specifications/Physical Properties* table for derating information.

HMMC-5618 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
V_{D1}, V_{D2}	Drain Supply Voltage	V	3.0	5.0	5.5
I_{D1}	Stage-One Drain Supply Current (V_{D1} = 5 V, V_{G1} = Open or Ground)	mA		50	
I_{D2}	Stage-Two Drain Supply Current (V_{D2} = 5 V, V_{G2} = Open or Ground)	mA		65	
$I_{D1} + I_{D2}$	Total Drain Supply Current ($V_{D1} = V_{D2}$ = 5 V, $V_{G1} = V_{G2}$ = Open or Ground)	mA		115	140
V_{P1}	Optional Input-Stage Gate Supply Pinch-off Voltage (V_{D1} = 5 V, I_{D1} < 3 mA: Input Stage OFF[2])	V	-4	-2.8	
I_{G1}	Gate Supply Current (Input Stage OFF[2])	mA		0.9	
V_{P2}	Optional Input-Stage Gate Supply Pinch-off Voltage (V_{D2} = 5 V, I_{D2} < 3.6 mA: Output Stage OFF[2])	V	-7.5	-5.3	
I_{G2}	Gate Supply Current (Output Stage OFF[2]) (V_{D2} = 5 V, V_{G2} = Open or Ground)	mA		1.7	
$\theta_{ch\text{-}bs}$	Thermal Resistance[3] (Channel-to-Backside at T_{ch} = 150°C)	°C/Watt		87	
T_{ch}	Channel Temperature[4] (T_A = 100°C, MTTF = 10^6 hrs, $V_{D1} = V_{D2}$ = 5 V, $V_{G1} = V_{G2}$ = Open)	°C		150	

Notes:
1. Backside ambient operating temperature T_A = 25°C unless otherwise noted.
2. The specified FET stage is in the OFF state when biased with a gate voltage level that is sufficient to pinch off the drain current.
3. Thermal resistance (in °C/Watt) at a channel temperature T (°C) can be estimated using his equation: $\theta(T) \cong 87 \times [T(°C)+273] / [150°C+273]$.
4. Derate MTTF by a factor of two for every 8°C above T_{ch}.

HMMC-5618 RF Specifications, T_A = 25°C, $V_{D1} = V_{D2}$ = 5 V, $V_{G1} = V_{G2}$ = Open or Ground, Z_O = 50 Ω

Symbol	Parameters and Test Conditions	Units	Typ.	6–18 GHz		5.9–20 GHz	
				Min.	Max.	Min.	Max.
Gain	Small Signal Gain	dB	14	12		11.5	
Δ Gain	Gain Flatness	dB	±0.5				
$\Delta S_{21}/\Delta T$	Temperature Coefficient of Gain	dB/°C	-0.025				
$(RL_{in})_{MIN}$	Minimum Input Return Loss	dB	12	10		9	
$(RL_{out})_{MIN}$	Minimum Output Return Loss	dB	12	10		10	
Isolation	Reverse Isolation	dB	40				
P_{-1dB}	Output Power @ 1 dB Gain Compression	dBm	18	17		17	
P_{sat}	Saturated Output Power (P_{in} = 10 dBm)	dBm	20	18.5		18.5	
NF	Noise Figure	dB	5.5		7		7

HMMC-5618 Applications

The HMMC-5618 is a GaAs MMIC amplifier designed for optimum Class-A efficiency and flat gain performance from 6 GHz to 20 GHz. It has applications as a cascadable gain stage for EW amplifiers, buffer stages, LO drives, phased-array radar, and transmitter amplifiers used in commercial communication systems. The MMIC solution is a cost effective alternative to hybrid assemblies.

Biasing and Operation

The MMIC amplifier is normally biased with a single positive drain supply connected to both V_{D1} and V_{D2} bond pads as shown in Figure 8a. The recommended drain supply voltage is 3 to 5 volts. If desired, the first stage drain bonding pad can be biased separately to provide a small amount of gain slope control or bandwidth extension as demonstrated in Figure 2.

No ground wires are required because all ground connections are made with plated through-holes to the backside of the device.

Gate bias pads (V_{G1} and V_{G2}) are also provided to allow adjustments in gain, RF output power, and DC power dissipation, if necessary. No connection to the gate pads is needed for single drain-bias operation. However, for custom applications, the DC current flowing through the input and/or output gain stage may be adjusted by applying a voltage to the gate bias pad(s) as shown in Figure 8b. A negative gate-pad voltage will decrease the drain current. The gate-pad voltage is approximately zero volts during operation with no DC gate supply. Refer to the Absolute Maximum Ratings table for allowed DC and thermal conditions.

Assembly Techniques

Solder die attach using a fluxless gold-tin (AuSn) solder preform is the recommended assembly method. A conductive epoxy such as ABLEBOND® 71-1LM1 or ABLEBOND® 36-2 may also be used for die attaching provided the Maximum Thermal Ratings are not exceeded. The device should be attached to an electrically conductive surface to complete the DC and RF ground paths. The backside metallization on the device is gold.

It is recommended that the RF input, RF output, and DC supply connections be made using 0.7 mil diameter gold wire. The device has been designed so that optimum performance is realized when the RF input and RF output bond-wire inductance is approximately 0.2 nH as demonstrated in Figures 4, 6, and 7. Therefore, mesh or multiple-wire bonds are not necessary. It is, however, recommended that the RF wires be as short as possible to minimize assembly related performance variations.

Thermosonic wedge is the preferred method for wire bonding to the gold bond pads. Wires can be attached using a guided-wedge at an ultrasonic power level of roughly 64 dB for a duration of 76 ±8 msec with a stage temperature of 150 ± 2°C.

For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

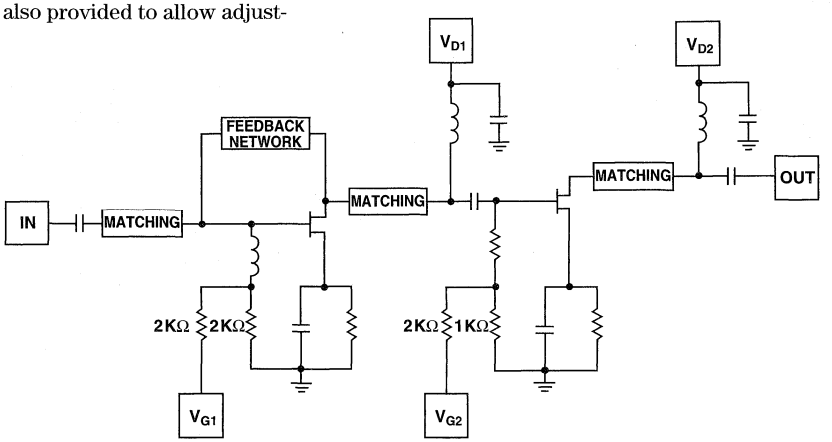


Figure 1. HMMC-5618 Simplified Schematic.

HMMC-5618 Typical Scattering Parameters[1],

($T_A = 25°C, V_{D1} = V_{D2} = 5.0\,V, V_{G1} = V_{G2} = Open, Z_o = 50\,\Omega$

Freq.	S_{11}			S_{21}			S_{12}			S_{22}		
GHz	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
2.0	-4.8	0.574	-140.8	-71.2	0.000	-73.5	-43.0	0.0070	117.3	-0.9	0.901	-75.4
2.5	-5.6	0.526	-166.9	-74.4	0.000	-12.0	-25.3	0.0544	-113.7	-1.6	0.835	-99.7
3.0	-6.0	0.501	166.4	-73.6	0.000	-41.3	-8.0	0.3981	-124.1	-3.3	0.687	-127.0
3.5	-6.2	0.492	136.2	-55.9	0.002	-51.8	2.9	1.4008	-159.1	-6.1	0.498	-156.7
4.0	-6.7	0.461	99.3	-49.4	0.003	-94.9	10.4	3.3208	154.4	-10.3	0.305	171.1
4.5	-8.8	0.363	60.6	-45.5	0.005	-140.6	14.2	5.1331	104.5	-16.7	0.147	133.8
5.0	-11.9	0.255	30.7	-43.8	0.006	-179.4	15.4	5.9052	62.9	-23.2	0.069	76.1
5.5	-14.4	0.190	10.9	-43.8	0.006	152.8	15.6	6.0539	31.6	-22.0	0.079	21.3
6.0	-15.8	0.163	-3.8	-43.4	0.007	132.6	15.6	6.0319	6.8	-18.9	0.114	-5.5
6.5	-16.4	0.152	-16.2	-43.4	0.007	116.8	15.6	6.0062	-14.1	-16.8	0.144	-19.6
7.0	-16.3	0.153	-27.4	-43.1	0.007	101.8	15.5	5.9669	-32.7	-15.4	0.171	-30.5
7.5	-16.0	0.159	-38.0	-43.0	0.007	87.6	15.5	5.9318	-49.7	-14.3	0.193	-39.4
8.0	-15.4	0.171	-48.2	-42.8	0.007	79.1	15.4	5.8635	-65.4	-13.5	0.212	-47.1
8.5	-14.9	0.180	-58.5	-42.7	0.007	68.9	15.4	5.8567	-80.0	-12.9	0.227	-54.4
9.0	-14.5	0.189	-67.5	-42.5	0.008	58.9	15.3	5.8232	-94.2	-12.5	0.237	-61.4
9.5	-14.1	0.198	-75.8	-42.3	0.008	50.2	15.2	5.7757	-107.8	-12.2	0.246	-67.8
10.0	-13.7	0.206	-83.6	-42.0	0.008	41.0	15.2	5.7385	-121.0	-12.0	0.252	-73.9
10.5	-13.4	0.214	-91.2	-42.0	0.008	33.7	15.1	5.7043	-133.8	-11.9	0.254	-79.6
11.0	-13.2	0.219	-98.3	-42.0	0.008	27.5	15.1	5.6618	-146.2	-11.9	0.253	-85.2
11.5	-13.0	0.223	-105.1	-41.7	0.008	19.8	15.0	5.6180	-158.4	-12.0	0.250	-90.0
12.0	-13.0	0.224	-111.4	-41.3	0.009	13.9	14.9	5.5801	-170.4	-12.2	0.245	-94.3
12.5	-13.0	0.224	-117.5	-40.9	0.009	6.2	14.9	5.5525	177.7	-12.5	0.238	-98.2
13.0	-13.1	0.221	-123.2	-40.8	0.009	1.0	14.9	5.5276	166.0	-12.8	0.230	-101.6
13.5	-13.3	0.217	-128.7	-40.5	0.009	-6.7	14.8	5.5138	154.2	-13.1	0.221	-104.3
14.0	-13.5	0.210	-134.1	-40.2	0.010	-12.5	14.8	5.5069	142.3	-13.5	0.211	-106.2
14.5	-13.9	0.201	-138.9	-40.0	0.010	-17.5	14.8	5.4997	130.5	-13.9	0.201	-107.1
15.0	-14.5	0.188	-143.4	-39.2	0.011	-25.3	14.8	5.5050	118.6	-14.4	0.191	-106.8
15.5	-15.2	0.174	-147.2	-39.1	0.011	-31.8	14.8	5.5089	106.3	-14.7	0.184	-105.4
16.0	-16.2	0.155	-150.0	-38.6	0.012	-38.9	14.8	5.5103	93.8	-14.9	0.180	-103.4
16.5	-17.5	0.133	-150.7	-38.4	0.012	-45.8	14.8	5.5013	80.9	-14.9	0.180	-100.3
17.0	-19.2	0.110	-147.8	-37.8	0.013	-52.1	14.8	5.4892	67.9	-14.6	0.186	-97.4
17.5	-21.1	0.088	-138.0	-37.3	0.014	-60.7	14.7	5.4475	54.4	-14.3	0.194	-95.6
18.0	-22.1	0.079	-117.7	-36.7	0.015	-69.6	14.7	5.4016	40.5	-13.7	0.206	-95.1
18.5	-20.7	0.092	-96.6	-35.9	0.016	-74.8	14.5	5.3231	26.1	-13.3	0.217	-96.0
19.0	-18.2	0.123	-83.9	-35.4	0.017	-85.0	14.3	5.2168	11.2	-13.0	0.224	-98.0
19.5	-15.4	0.169	-80.3	-35.0	0.018	-95.7	14.0	5.0371	-4.3	-12.9	0.226	-99.4
20.0	-13.0	0.224	-81.8	-34.8	0.018	-105.6	13.7	4.8240	-19.9	-13.0	0.225	-100.9
20.5	-11.1	0.278	-85.7	-34.7	0.018	-114.9	13.2	4.5580	-36.4	-13.3	0.217	-99.8
21.0	-9.6	0.332	-91.2	-34.2	0.020	-126.3	12.5	4.2135	-52.5	-13.8	0.205	-97.5
21.5	-8.3	0.384	-97.7	-34.3	0.019	-137.2	11.7	3.8489	-68.9	-14.0	0.199	-90.2
22.0	-7.3	0.432	-284.7	-34.2	0.020	-328.3	10.8	3.4671	-85.5	-13.4	0.214	-80.1

Note:

1. Data obtained from on-wafer measurements.

HMMC-5618 Typical Performance

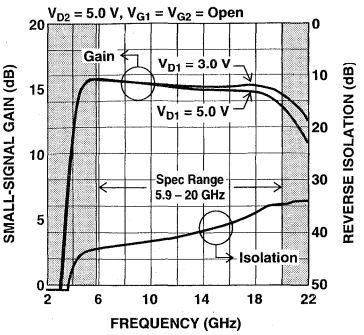


Figure 2. Gain and Isolation vs. Frequency.[1]

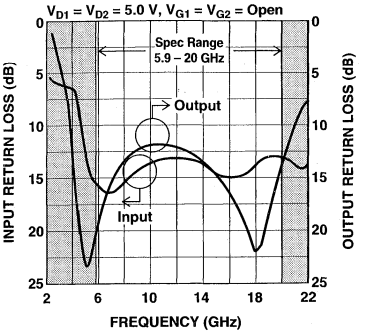


Figure 3. Input and Output Return Loss vs. Frequency.[1]

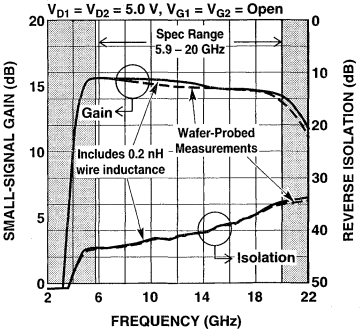


Figure 4. Effects of Input/Output Bond Wire Inductance on Gain and Isolation.[2]

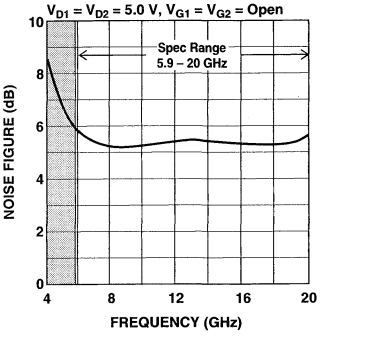


Figure 5. Noise Figure vs. Frequency.[1]

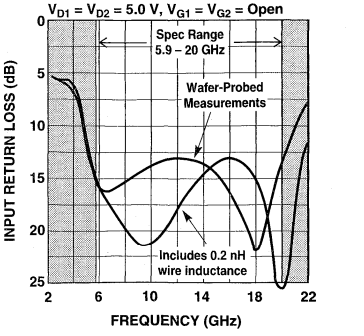


Figure 6. Effects of Input/ Output Bond Wire Inductance on Input Return Loss.[2]

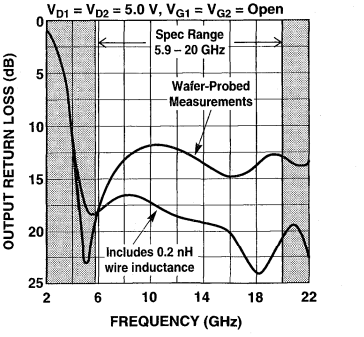


Figure 7. Effects of Input/Output Bond Wire Inductance on Output Return Loss.[2]

Notes:

1. Wafer-probed measurements.
2. Effect of 0.2 nH inductance in the RF input and RF output bond wires is modeled from measured wafer-probe tests calibrated at the pads of the MMIC device.

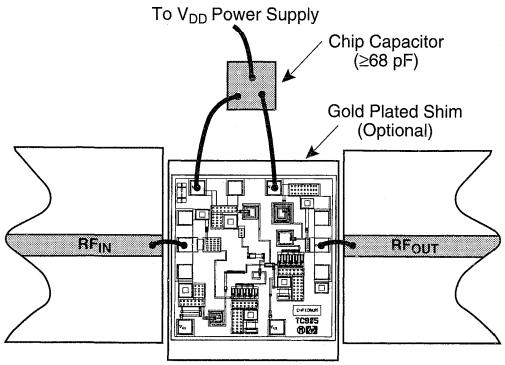


Figure 8a. Assembly for single drain-bias operation.

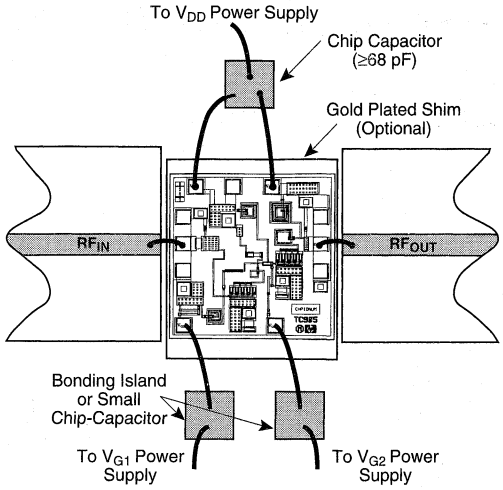


Figure 8b. Assembly with gate bias connections.

Figure 8. HMMC-5618 Assembly Diagrams.

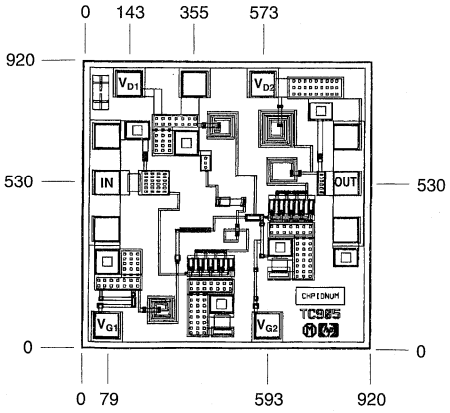


Figure 9. HMMC-5618 Bonding Pad Positions. (Dimensions are in micrometers.)

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

HEWLETT® PACKARD

6–20 GHz High-Gain Amplifier

Technical Data

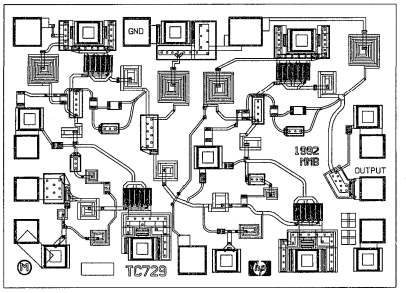
HMMC-5620

Features

- **Wide-Frequency Range:** 6–20 GHz
- **High Gain:** 17 dB
- **Gain Flatness:** ±1.0 dB
- **Return Loss:**
  Input -15 dB
  Output -15 dB
- **Single Bias Supply Operation**
- **Low DC Power Dissipation:** P_{DC} ~ 0.5 Watts
- **Medium Power:**
  20 GHz: P_{-1dB}: 12 dBm
  P_{sat}: 13 dBm

Description

The HMMC-5620 is a wideband GaAs MMIC Amplifier designed for medium output power and high gain over the 6 to 20 GHz frequency range. Four MESFET cascade stages provide high gain, while the single bias supply offers ease of use. E-Beam lithography is used to produce gate lengths of ≈ 0.3 µm. The HMMC-5620 incorporates advanced MBE technology, Ti-Pt-Au gate metallization, silicon nitride passivation, and polyimide for scratch protection.



Chip Size:	1410 x 1010 µm (55.5 x 39.7 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	80 x 80 µm (2.95 x 2.95 mils), or larger

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{DD}	Positive Drain Voltage	V		7.5
I_{DD}	Total Drain Current	mA		135
P_{DC}	DC Power Dissipation	watts		1.0
P_{in}	CW Input Power	dBm		20
T_{ch}	Operating Channel Temp.	°C		+160
T_{case}	Operating Case Temp.	°C	-55	
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp. (for 60 seconds maximum)	°C		+300

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A = 25°C except for T_{ch}, T_{STG}, and T_{max}.

HMMC-5620 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{DD}	Drain Current (V_{DD} = +5.0 V)	mA	70	100	135
I_{DD}	Drain Current (V_{DD} = +7.0 V)	mA		105	
$\theta_{ch\text{-}bs}$	Thermal Resistance ($T_{backside}$ = 25°C)	°C/W		70	

Note:

1. Measured in wafer form with T_{chuck} = 25°C. (Except $\theta_{ch\text{-}bs}$).

HMMC-5620 RF Specifications/Physical Properties

V_{DD} = 5.0 V, $I_{DD}(Q)$ = 100 mA, Z_{in} = Z_o = 50 Ω[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
BW	Guaranteed Bandwidth	GHz	6		20
S_{21}	Small Signal Gain	dB	15	17	21
ΔS_{21}	Small Signal Gain Flatness	dB		±1.0	±1.25
RL_{in}	Input Return Loss	dB		-15	-10
RL_{out}	Output Return Loss	dB		-15	-10
S_{12}	Reverse Isolation	dB		-55	
P_{-1dB}	Output Power @ 1 dB Gain Compression	dBm		12	
P_{sat}	Saturated Output Power	dBm		13	
H_2	Second Harmonic Power Level ($6 < f_o < 20$) $P_o(f_o)$ = 10 dBm	dBc		-30	
H_3	Third Harmonic Power Level ($6 < f_o < 20$) $P_o(f_o)$ = 10 dBm	dBc		-40	
NF	Noise Figure	dB		9.0	

Note:

1. Small-signal data measured in wafer form with T_{chuck} = 25°C. Large-signal data measured on individual devices mounted in an HP83040 Series Modular Microcircuit Package at T_A = 25°C.

HMMC-5620 Applications

The HMMC-5620 amplifier is designed for use as a general purpose wideband, high gain stage in communication systems and microwave instrumentation. It is ideally suited for broadband applications requiring high gain and excellent port matches over a 6 to 20 GHz frequency range. Both RF input and output ports are AC-coupled on chip.

Biasing and Operation

This amplifier is biased with a single positive drain supply (V_{DD}). The recommended bias for the HMMC-5620 is V_{DD} = 5.0 V, which results in I_{DD} = 100 mA (Typ.). No other bias supplies or connections to the device are required for 6 to 20 GHz operation. See Figure 3 for assembly information.

Assembly Techniques

Solder die-attach using a fluxless AuSu solder preform is the recommended assembly method. Gold thermosonic wedge bonding with 0.7 or 1.0 mil diameter Au wire is recommended for D.C. bonds. For RF bonds, MWTC recommends low inductance mesh interconnections for best return loss performance. Tool force should be 22 ± 1 gram, stage temperature should be 150 ± 2°C, and ultrasonic power and duration should be 64 ± 1 dB and 76 ± 8 msec, respectively. The bonding pad and chip backside metallization is gold.

For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

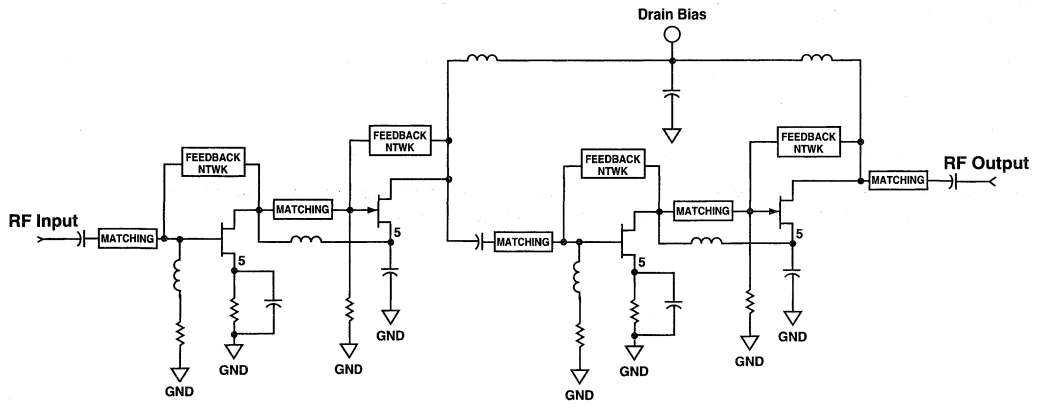


Figure 1. HMMC-5620 Schematic.

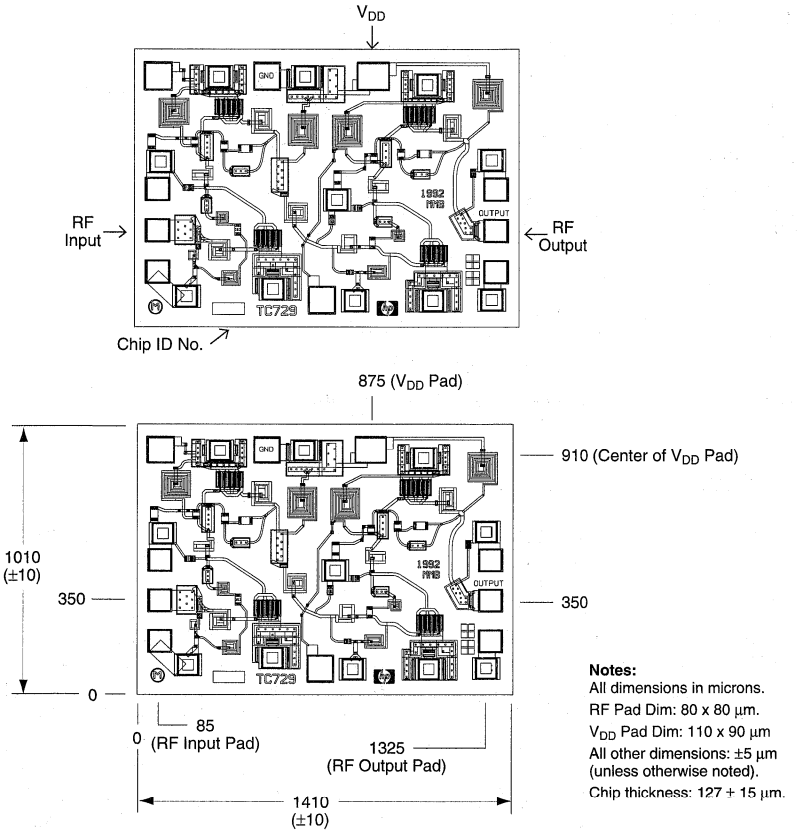


Figure 2. HMMC-5620 Bonding Pad Locations.

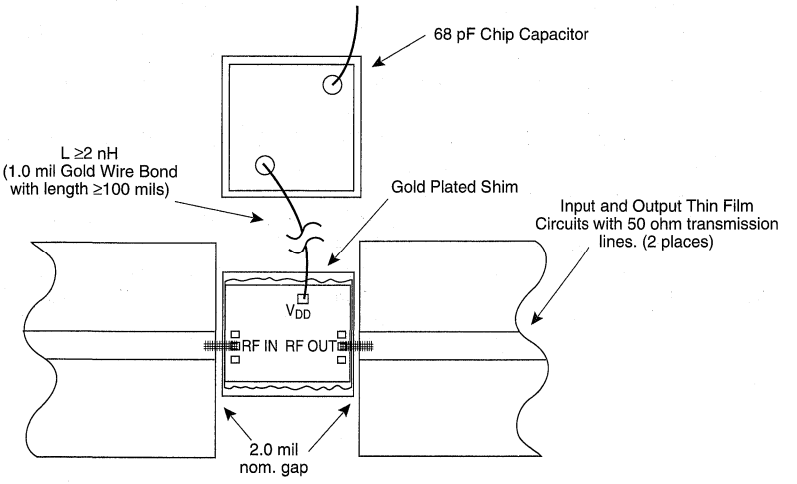


Figure 3. HMMC-5620 Assembly Diagram. (For 6.0 – 20.0 GHz Operation)

HMMC-5620 Typical Performance

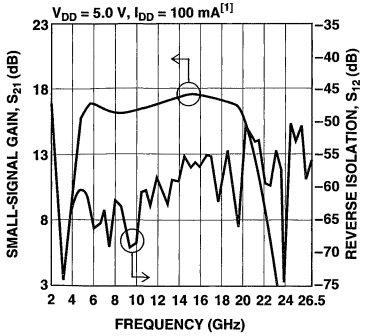


Figure 4. Typical Gain and Reverse Isolation vs. Frequency.

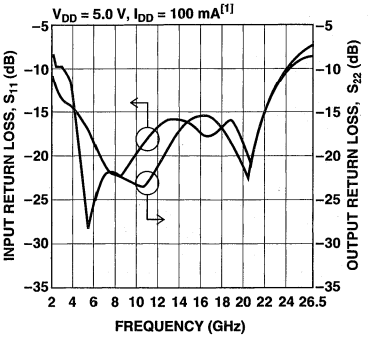


Figure 5. Typical Input and Output Return Loss vs. Frequency.

Typical Scattering Parameters[1], (T_{chuck} = 25°C, V_{DD} = 5.0 V, I_{DD} = 100 mA, Z_{in} = Z_o = 50 Ω)

Freq.	S_{11}			S_{21}			S_{12}			S_{22}		
GHz	dB	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.
2.0	-10.7	0.292	-100.3	-46.1	0.0049	-174.7	-6.2	0.491	-52.2	-8.1	0.395	-152.2
3.0	-13.5	0.212	-117.5	-74.1	0.0002	114.0	3.5	1.489	-170.0	-10.1	0.311	-171.5
4.0	-14.6	0.186	-136.6	-63.1	0.0007	-122.1	13.0	4.486	82.2	-12.7	0.232	136.5
5.0	-15.8	0.162	-168.9	-60.4	0.0010	-161.8	16.0	6.310	-26.5	-21.7	0.082	61.5
6.0	-18.4	0.120	157.5	-66.5	0.0005	162.7	16.7	6.839	-116.8	-25.7	0.052	-86.6
7.0	-20.9	0.090	123.0	-62.7	0.0007	-175.3	16.3	6.531	173.2	-22.1	0.079	-131.4
8.0	-22.2	0.078	83.1	-61.3	0.0009	-178.0	16.0	6.310	114.2	-21.7	0.082	-150.6
9.0	-21.9	0.080	41.3	-66.5	0.0005	-62.4	16.0	6.310	60.2	-22.5	0.075	-156.7
10.0	-20.2	0.097	6.6	-68.1	0.0004	-159.3	16.1	6.383	9.0	-23.2	0.070	-152.9
11.0	-18.4	0.120	-21.0	-60.0	0.0010	-113.5	16.3	6.531	-40.7	-23.4	0.067	-143.0
12.0	-16.7	0.146	-46.4	-58.3	0.0012	-112.2	16.6	6.761	-89.9	-21.5	0.084	-136.8
13.0	-15.8	0.161	-70.0	-62.7	0.0007	-130.0	17.0	7.079	-139.4	-19.1	0.111	-133.7
14.0	-15.8	0.163	-90.0	-59.3	0.0011	-161.1	17.3	7.328	170.1	-17.2	0.137	-143.0
15.0	-16.4	0.151	-105.6	-57.5	0.0013	173.9	17.4	7.413	118.6	-16.0	0.159	-152.8
16.0	-17.5	0.134	-115.4	-57.1	0.0014	-165.9	17.5	7.499	66.0	-15.5	0.168	-167.9
17.0	-17.7	0.130	-114.1	-55.6	0.0017	175.5	17.3	7.328	12.3	-15.5	0.167	-179.7
18.0	-16.8	0.145	-118.4	-62.3	0.0008	98.2	17.0	7.079	-43.1	-16.5	0.149	162.9
19.0	-16.1	0.156	-131.6	-59.7	0.0010	112.8	16.7	6.839	-101.9	-17.7	0.130	145.2
20.0	-18.5	0.119	-143.8	-52.5	0.0024	72.9	16.0	6.310	-168.5	-20.8	0.091	93.0
21.0	-19.9	0.101	-108.1	-53.2	0.0022	-7.1	15.3	5.842	119.8	-20.4	0.096	-4.3
22.0	-14.2	0.195	-107.7	-59.3	0.0011	-8.0	10.7	3.414	54.2	-14.9	0.179	-63.6
23.0	-11.6	0.263	-125.6	-54.0	0.0020	-54.4	5.4	1.857	-0.4	-12.0	0.250	-93.3
24.0	-10.3	0.306	-142.2	-75.8	0.0002	-158.2	0.3	1.034	-47.5	-10.3	0.306	-110.4
25.0	-9.6	0.330	-157.2	-53.5	0.0021	-165.8	-4.5	0.595	-90.5	-9.0	0.353	-124.2
26.0	-9.2	0.347	-169.9	-59.0	0.0011	-137.5	-9.0	0.355	-131.1	-7.9	0.402	-134.3
26.5	-9.1	0.349	-357.4	-54.9	0.0018	78.2	-11.2	0.275	-511.3	-7.4	0.426	-140.2

Note:

1. Data obtained from on-wafer measurements.

HMMC-5620 Typical Performance

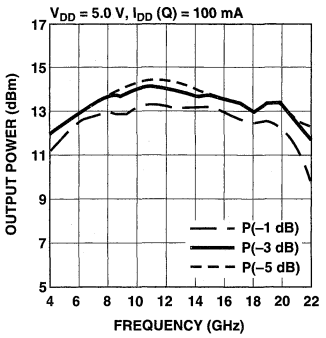


Figure 6. Typical Output Power vs. Frequency (with 5 V bias.)

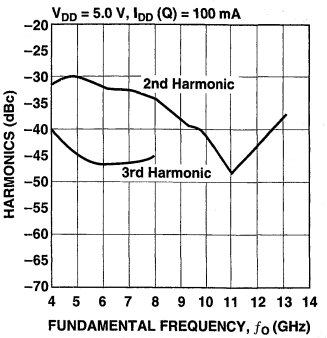


Figure 7. Typical Second and Third Harmonics vs. Fundamental Frequency at P_{OUT} = 10 dBm.

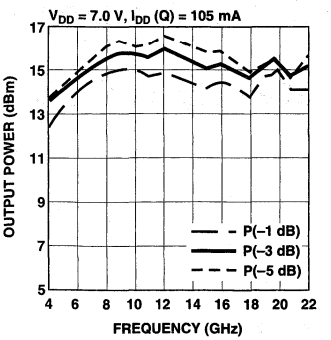


Figure 8. Typical Output Power vs. Frequency (with 7 V bias).

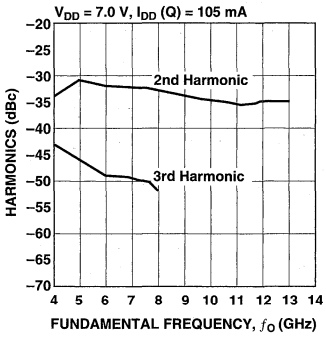


Figure 9. Typical Second and Third Harmonics vs. Fundamental Frequency at P_{OUT} = 10 dBm.

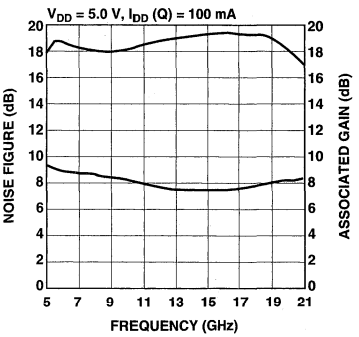


Figure 10. Typical Noise Figure Performance vs. Frequency.

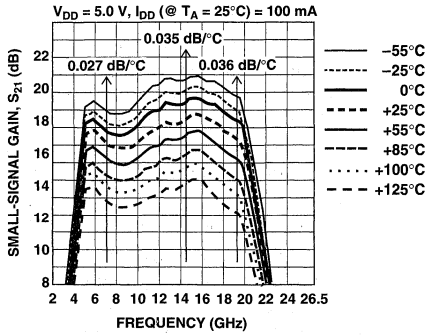


Figure 11. Typical Small-Signal Gain vs. Temperature.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

HEWLETT® PACKARD

Silicon Bipolar RFIC 900 MHz Driver Amplifier

Technical Data

HPMX-3002

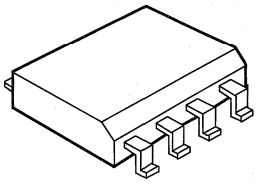
Features

- **RFIC Medium Power Amplifier**
- **150-960 MHz Operating Range**
- **+22 dBm Typ. P_{1dB}, +23 dBm Typ. P_{sat} @ 900 MHz**
- **50 dB Typ. Power Control Range**
- **6 V, 160 mA Operation**
- **S0-8 Surface Mount Package with Improved Heatsinking**

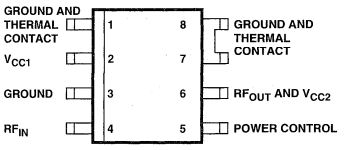
Applications

- **Driver Amplifier for GSM Cellular Handsets**
- **Driver or Output Stage for 900 MHz ISM Band Transmitters**
- **Driver or Output Stage for Transmitters Operating in the 150-960 MHz Range**

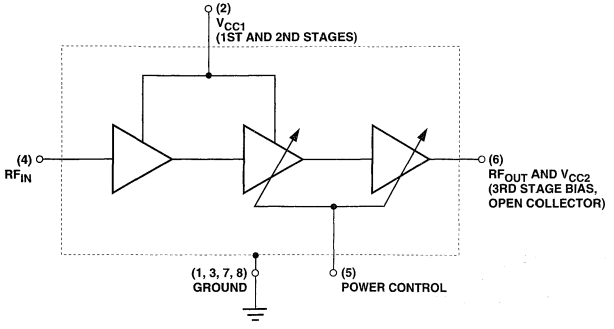
Plastic S0-8 Package



Pin Configuration



Functional Block Diagram



Description

Hewlett-Packard's HPMX-3002 is a silicon microwave monolithic integrated circuit driver amplifier housed in a S0-8 surface mount plastic package. It operates over the 150 - 960 MHz frequency range, and at 900 MHz it produces +23 dBm of saturated output power, has 30 dB of small signal gain and a 50 dB power control range. The amplifier has a well-matched input, and an open collector output which provides good linearity and efficiency and is easy to externally match to 50 Ω for optimal power output.

This device is well suited as a driver amplifier for European GSM (Global System for Mobile communications) portable and mobile telephone systems, or as the output stage for other low cost applications such as 900 MHz ISM band spread-spectrum.

The HPMX-3002 is fabricated with Hewlett-Packard's 15 GHz f_t ISOSAT-II process, which combines stepper lithography, ion implantation, self-alignment techniques, and gold metallization to produce RFICs with superior performance, uniformity and reliability .

HPMX-3002 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
P_{diss}	Power Dissipation[2,3]	mW	1400
P_{in}	Input Power	dBm	+5
V_{CC}[1]	Supply Voltage	V	8
V_{CC}[2]	Supply Voltage, 3rd Stage	V	12
V_{cont}	Control Voltage	V	5
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperatuere	°C	-65 to 150

Thermal Resistance[2]:
Θ_{jc} = 66°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_c = 25 °C (T_c is defined to be the temperature at the ends of pin 7 where it contacts the circuit board).
3. Derate at 15.2 mW/°C for T_C > 58°C.

HPMX-3002 Guaranteed Electrical Parameters, T_C = 37°C, Z_O = 50 Ω

V_{CC1} = 4.5 V, V_{CC2} = 6 V, P_{IN} = -6 dBm @ 900 MHz, output matched for maximum power
I_{CC1} = 65 mA nom., I_{CC2} = 95 mA nom. set by V_{cont} (pin 5) = 2.2 V (unless otherwise noted).

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
P_{out}	Output Power	P_{IN} = -6 dBm, f = 900 MHz	dBm	22	23	
PCR	Power Control Range	f = 900 MHz, V_{cont} = 0 to 2.2 V	dBm	40	50	
I_{CC1}	Driver Stages Current	V_{CC1} = 4.5 V	mA		65	75
I_{CC2}	Output Stage Current	V_{CC2} = 6 V	mA		95	120

HPMX-3002 Summary Characterization Information, T_C = 37°C, Z_O = 50 Ω

V_{CC1} = 4.5 V, V_{CC2} = 6 V, P_{in} = -6 dBm @ 900 MHz, output matched for maximum power
I_{CC1} = 65 mA nom., I_{CC2} = 95 mA nom. set by V_{cont} (pin 5) = 2.2 V (unless otherwise noted).

Symbol	Parameters and Test Conditions		Units	Typ.
P_{1dB}	Output Power at 1 dB Gain Compression	P_{IN} set for P_{out} = P 1 dB, f = 900 MHz	dBm	22
G_{ss}	Small Signal Gain	f = 900 MHz, P_{in} = -18 dBm	dB	32
IP_3	Third Order Intercept Point	f_1 = 900 MHz, f_2 = 901 MHz P_{out} per tone = 12 dBm	dBm	29
IP_5	Fifth Order Intercept Point	f_1 = 900 MHz, f_2 = 901 MHz P_{out} per tone = 12 dBm	dBm	24
NF	Noise Figure		dB	9.5
$VSWR_{in}$	Input Voltage Standing Wave Ratio		-	1.5:1
I_{cont}	Control Current	V_{cont} = 0 to 2.2V	mA	2.5

HPMX-3002 Pin Description

Ground (pins 1,3,7,8):
This RFIC is ground sensitive. A short path to ground with minimal parasitics must be provided on all ground leads to prevent stability problems. The PC board should be 0.032" or less in thickness. Multiple vias should be placed near the ground leads. Failure to properly ground this device can lead to positive return gain and possible stability problems. We suggest performing a stability analysis using the device s parameters and a description of the inductance of your ground path. A recommended board layout is shown on the final page of this data sheet. Pins 7 and 8 also provide the primary thermal path for heatsinking the device.

V_{CC1} (pin 2):
This pin provides the DC bias for the amplifier driver stages, and has an operating range of 4.5 to 6 V (5 V nominal). It should be bypassed close to RFIC body using a 1000 pF capacitor.

RF_{in} (pin 4):
The impedance of this RFIC is well matched to 50 Ω from 100 MHz to 1100 MHz. Normally, no additional impedance matching is required. S-parameters are provided should the designer need to "fine tune" the input match. Pin 4 must be AC coupled to generator (1000 pF typ. blocking capacitor). The nominal drive level is -6 dBm, and under normal operating conditions should not exceed 0 dBm.

Control (pin 5):
Applying a DC voltage to this pin adjusts the gain of the last 2 stages of the RFIC over a 50 dB range. Pin 5 has an operational range of 0 to 2.5 V. The power control function is designed for operation in the 800 - 1000 MHz frequency range, and decreases in adjustment capability at lower frequencies – refer to the performance graphs (figure 3).

RF_{out} and V_{CC2} (Pin 6):
Pin 6 connects to the open collector of the output stage. A power match is required at this pin. The typical match for operation between 800 and 1000 MHz consists of a shunt L (8 nH typ.) and a series C (27 pF typ.), with the series C also serving as the blocking capacitor. The s parameter data should be used to generate matches for other frequency bands.

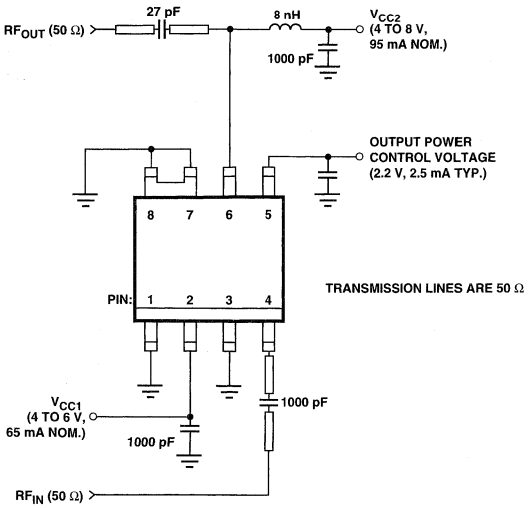


Figure 1. HPMX-3002 Typical 900 MHz Amplifier Use.

HPMX-3002 Typical Performance, T_C = 37°C, Z_O = 50 Ω

P_{in} = -6 dBm @ 900 MHz, V_{CC1} = 4.5 V, V_{CC2} = 6 V, $V_{control}$ = 2.2 V, I_{CC1} = 66 mA, I_{CC2} = 95 mA nom.
Output matched for max. P_{out} @ 900 MHz (unless otherwise noted)

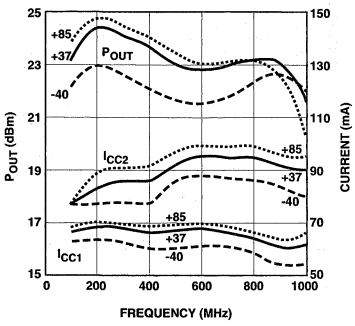


Figure 2. HPMX-3002 Output Power and Current vs. Frequency and Temperature.

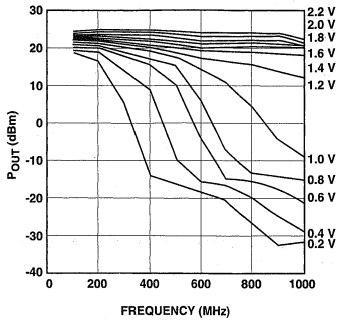


Figure 3. HPMX-3002 Output Power vs. Frequency and Control Voltage.

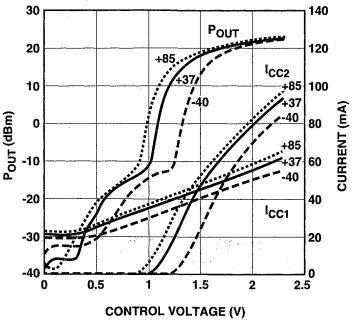


Figure 4. HPMX-3002 Output Power and Current vs. Control Voltage and Temperature.

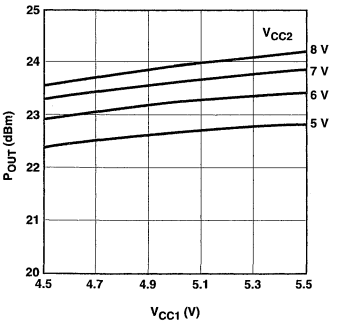


Figure 5. HPMX-3002 Output Power vs. Supply Voltage.

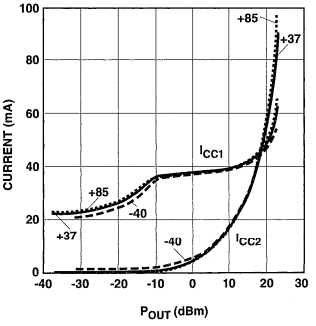


Figure 6. HPMX-3002 Current vs. Output Power and Temperature.

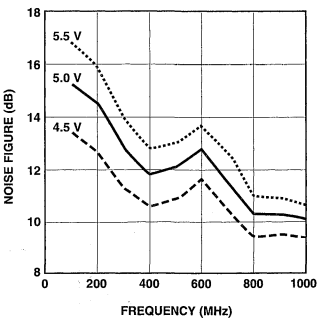


Figure 7. HPMX-3002 Noise Figure vs. Frequency and V_{CC1}.

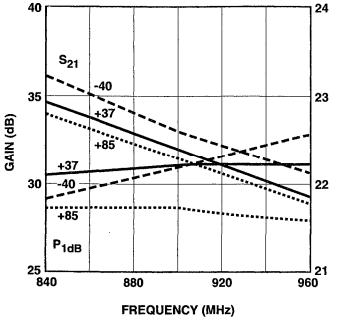


Figure 8. HPMX-3002 one dB Compressed Power and Small Signal Gain vs. Frequency and Temperature.

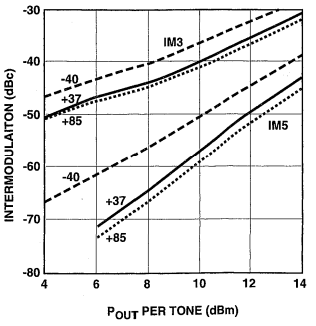


Figure 9. HPMX-3002 Intermodulation Distortion vs. Output Power and Temperature with $V_{control}$ = 2.0 V.

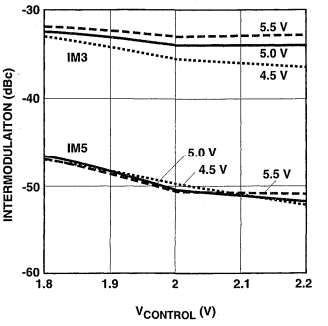


Figure 10. HPMX-3002 Intermodulation Distortion vs. Control Voltage and V_{CC1} for P_{out} per tone = 12 dBm.

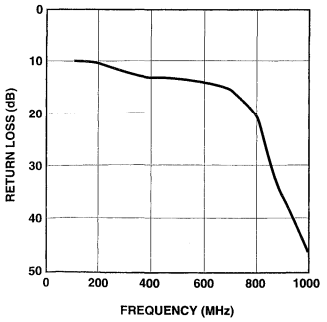


Figure 11. HPMX-3002 Input Return Loss vs. Frequency.

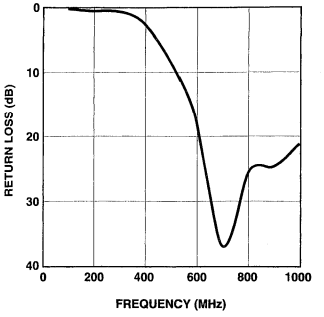


Figure 12. HPMX-3002 Output Return Loss vs. Frequency.

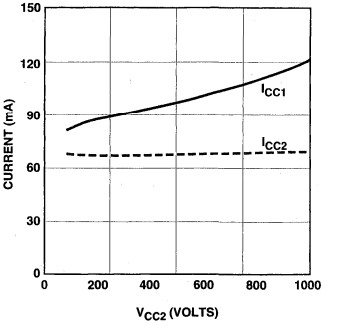


Figure 13. HPMX-3002 Stage Current vs. Supply Voltage with V_{CC1} = 4.5 V.

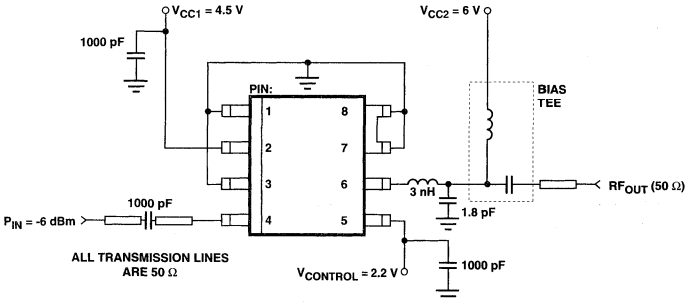


Figure 14. HPMX-3002 Test Circuit Configuration.

HPMX-3002 Typical Scattering Parameters, $T_C = 37°C$, $Z_O = 50\ \Omega$ $V_{control} = 1.6\ V$

$V_{CC1} = 4.5\ V$, $V_{CC2} = 6\ V$

Freq	S_{11}		S_{21}			S_{12}			S_{22}		k
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.10	0.33	151	42.89	139.44	-138	-60.00	0.001	143	0.91	-25	0.77
0.20	0.34	92	44.16	161.44	143	-53.98	0.002	152	0.75	-53	0.82
0.30	0.31	51	42.95	140.50	98	-53.98	0.002	146	0.65	-67	1.10
0.40	0.31	18	42.06	126.79	63	-47.96	0.004	148	0.65	-76	0.77
0.50	0.29	-14	41.91	124.61	29	-44.44	0.006	141	0.73	-89	0.65
0.60	0.23	-52	42.12	127.67	-10	-40.92	0.009	143	0.85	-107	0.62
0.70	0.09	-117	41.62	120.47	-60	-38.42	0.012	138	0.88	-136	0.73
0.80	0.06	66	38.19	81.23	-106	-37.08	0.014	135	0.65	-162	0.84
0.90	0.16	42	34.23	51.44	-144	-35.92	0.016	131	0.41	-179	0.94
1.00	0.19	11	29.87	31.15	-169	-33.98	0.020	130	0.31	-170	1.04
1.10	0.21	6	26.42	20.93	-165	-32.40	0.024	127	0.25	-164	1.14

HPMX-3002 Typical Scattering Parameters, $T_C = 37°C$, $Z_O = 50\ \Omega$ $V_{control} = 2.0\ V$

$V_{CC1} = 4.5\ V$, $V_{CC2} = 6\ V$

Freq	S_{11}		S_{21}			S_{12}			S_{22}		k
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.10	0.33	143	45.90	197.18	-158	-60.00	0.001	153	0.85	-31	0.85
0.20	0.31	83	45.15	180.94	128	-60.00	0.001	99	0.63	-56	1.78
0.30	0.28	43	43.46	148.88	88	-53.98	0.002	142	0.56	-65	1.26
0.40	0.27	11	42.43	132.22	55	47.96	0.004	138	0.60	-74	0.87
0.50	0.25	-21	42.15	128.14	22	-44.44	0.006	147	0.70	-88	0.67
0.60	0.19	-63	42.13	127.82	-17	-41.94	0.008	143	0.80	-108	0.61
0.70	0.05	-144	41.26	115.62	-64	-39.17	0.011	135	0.81	-138	0.73
0.80	0.09	61	37.86	78.15	-107	-37.72	0.013	135	0.59	-161	0.86
0.90	0.17	38	34.07	50.54	-144	-35.92	0.016	131	0.39	-178	0.95
1.00	0.19	12	29.89	31.23	-168	-33.98	0.020	132	0.30	-169	1.04
1.10	0.21	6	26.54	21.22	166	-32.40	0.024	127	0.24	-164	1.14

HPMX-3002 Typical Scattering Parameters, $T_C = 37°C$, $Z_O = 50\,\Omega$ $V_{control} = 2.2\,V$

$V_{CC1} = 4.5\,V$, $V_{CC2} = 6\,V$

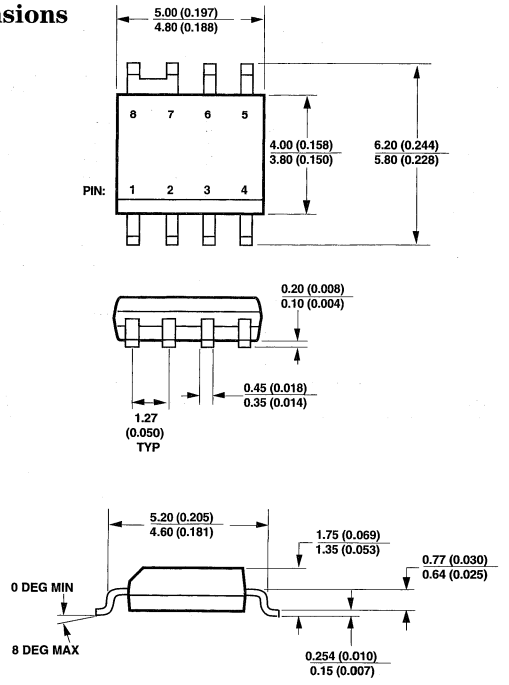
Freq	S_{11}		S_{21}			S_{12}			S_{22}		k
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.10	0.26	122	46.64	214.70	160	-60.00	0.001	111	0.58	-30	1.70
0.20	0.18	67	43.80	154.92	99	-60.00	0.001	133	0.49	-33	2.53
0.30	0.15	30	41.76	122.46	65	-53.98	0.002	139	0.52	-40	1.64
0.40	0.12	-1	40.36	104.17	38	-50.46	0.003	149	0.59	-52	1.22
0.50	0.08	-30	39.64	95.89	6	-44.44	0.006	148	0.66	-68	0.79
0.60	0.02	-112	39.17	90.91	-29	-41.94	0.008	142	0.71	-89	0.70
0.70	0.13	92	38.03	79.70	-71	-40.00	0.010	137	0.65	-114	0.75
0.80	0.19	51	35.15	57.23	-109	-37.72	0.013	135	0.50	-131	0.88
0.90	0.23	34	32.04	39.99	-142	-35.92	0.016	134	0.34	-143	0.99
1.00	0.24	11	28.44	26.42	-168	-34.43	0.019	132	0.29	-139	1.11
1.10	0.24	4	25.49	18.82	166	-32.77	0.023	129	0.34	-137	1.15

Part Number Ordering Information

Part Number	Option	No. of Devices	Container
HPMX-3002	-	100	Tube
HPMX-3002	#T10	1000	Reel

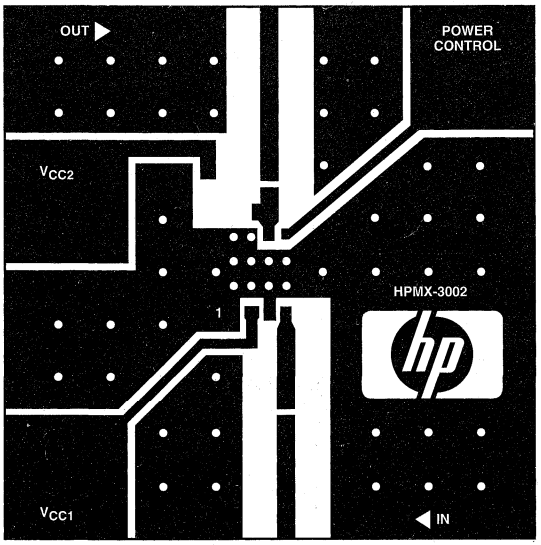
Package Dimensions

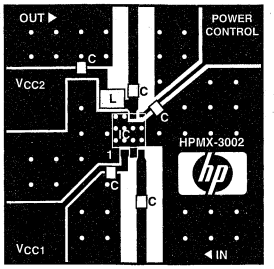
S0-8 Package



NOTE: DIMENSIONS ARE IN MILLIMETERS (INCHES).

HPMX-3002 Test Board Layout





Finished board size: 1.5" x 1.5" x 1/32"
Material: 1/32" epoxy/fiberglass, 1 oz. copper, both sides, tin/lead coating, both sides.
Note: "." marks indicate drilling locations for plated-through via holes to the groundplane on the bottom side of the board.
Board layed out for coil-craft #AO3T 8 nH spring-coil inductor.

HEWLETT® PACKARD

Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

INA-01100

Features

- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure:** 1.7 dB Typical at 100 MHz
- **High Gain:** 32.5 dB Typical at 100 MHz
- **3 dB Bandwidth:** DC to 500 MHz
- **Unconditionally Stable (k>1)**

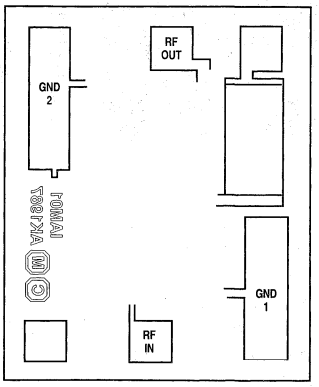
Description

The INA-01100 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier chip. It is designed for narrow or wide bandwidth industrial and military applications that require high gain and low noise IF or RF amplification.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1]

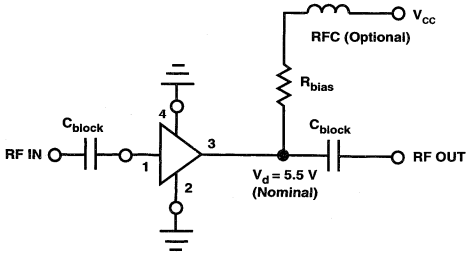
Chip Outline[1]



Note:

1. See Application Note, "A005: Transistor Chip Use" for additional information.

Typical Biasing Configuration



INA-01100 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance:
θ_{jc} = 60°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 16.7 mW/°C for T_{MS} > 176°C.

INA-01100 Electrical Specifications[1,3], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 100 MHz	dB		32.5	
ΔG_P	Gain Flatness	f = 10 to 250 MHz	dB		±0.5	
$f_{3\ dB}$	3 dB Bandwidth		MHz		500	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 10 to 250 MHz	dB		39	
VSWR	Input VSWR	f = 10 to 250 MHz			1.6:1	
	Output VSWR	f = 10 to 250 MHz			1.5:1	
NF	50 Ω Noise Figure	f = 100 MHz	dB		1.7	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 100 MHz	dBm		11	
IP_3	Third Order Intercept Point	f = 100 MHz	dBm		23	
t_D	Group Delay	f = 100 MHz	psec		200	
V_d	Device Voltage		V	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

Notes:
1. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
3. The values are the achievable performance for the INA-01100 mounted in a 70 mil stripline package.

INA-01100 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, V_{CC} = 35 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	0.09	–16	32.7	43.4	–1	–38.5	.012	–1	.18	1	1.17
0.05	0.10	–27	32.7	43.1	–10	–38.6	.012	15	.19	5	1.18
0.10	0.11	–5	32.4	41.9	–20	–38.4	.012	–8	.20	10	1.17
0.20	0.14	–80	31.6	38.0	–37	–38.6	.012	4	.24	14	1.22
0.30	0.18	–98	30.5	33.7	–52	–38.8	.011	–10	.27	15	1.31
0.40	0.20	–110	29.4	29.6	–65	–39.6	.011	2	.30	10	1.51
0.50	0.22	–115	28.4	26.2	–75	–38.6	.012	–12	.32	6	1.48
0.60	0.24	–120	27.4	23.4	–84	–39.1	.011	–7	.34	1	1.67
0.80	0.27	–124	25.7	19.3	–100	–38.3	.012	–6	.36	–11	1.76
1.00	0.30	–127	24.3	16.3	–115	–36.1	.016	–5	.36	–22	1.58
1.5	0.44	165	21.8	12.37	–179	–33.6	.020	42	.19	–69	1.75
2.0	0.44	154	17.9	7.88	146	–33.0	.022	42	.13	–106	2.42
2.5	0.46	148	14.6	5.36	121	–30.6	.029	36	.12	–151	2.63
3.0	0.48	139	11.4	3.71	96	–30.0	.032	45	.10	159	3.31

Note:
1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section of the *Communications Components Designer's* Catalog.

INA-01100 Typical Performance, T_A = 25°C

(unless otherwise noted: The values are the achievable performance for the INA-01100 mounted in a 70 mil stripline package.)

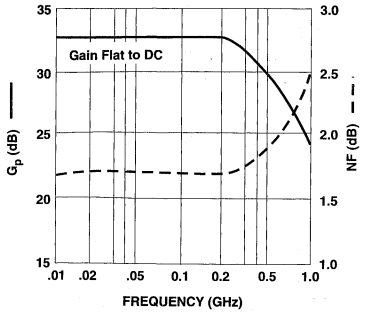


Figure 1. Typical Gain and Noise Figure vs. Frequency, T_A = 25°C, I_d = 35 mA

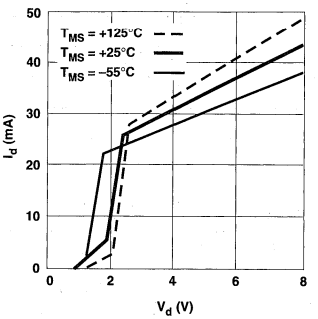


Figure 2. Device Current vs. Voltage.

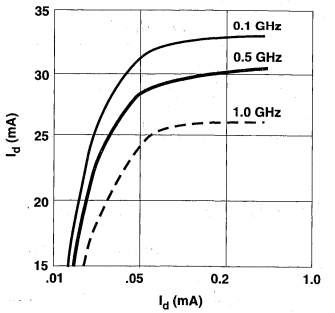


Figure 3. Power Gain vs. Current.

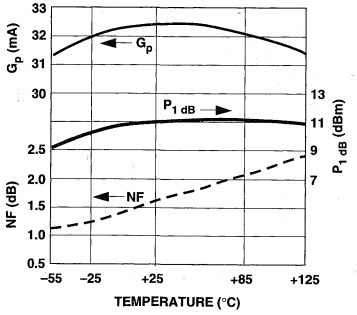


Figure 4. Output Power and 1 dB Gain Compression, NF and Power Gain vs. Case Temperature. f = 0.1 GHz, I_d = 35 mA.

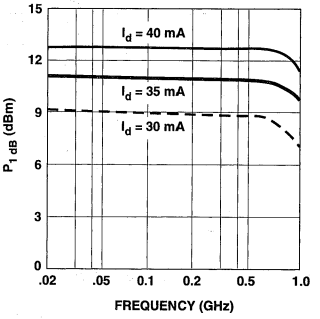


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

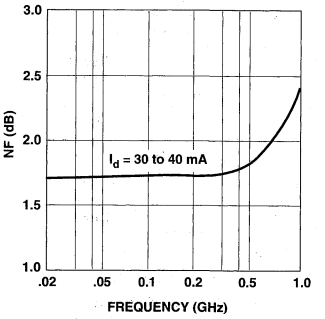
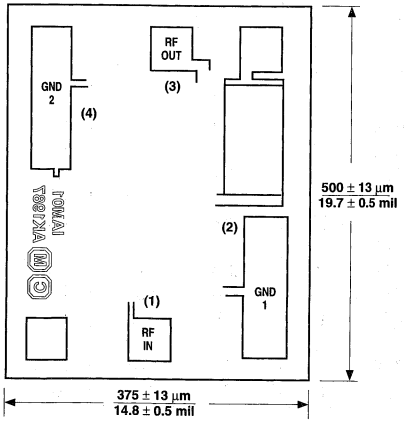


Figure 6. Noise Figure vs. Frequency.

INA-01100 Chip Dimensions



Chip thickness is 140 µm/5.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side. Note: Ground Bonding is Critical. Refer to Application Bulletin, "AB-0007: INA Bonding Configuration".

HEWLETT® PACKARD

Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

INA-01170

Features

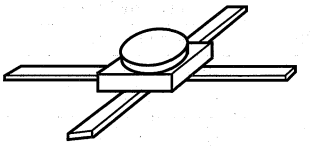
- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure:** 1.7 dB Typical at 100 MHz
- **High Gain:** 32.5 dB Typical at 100 MHz
- **3 dB Bandwidth:** DC to 500 MHz
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-Ceramic Surface Mount Package**

Description

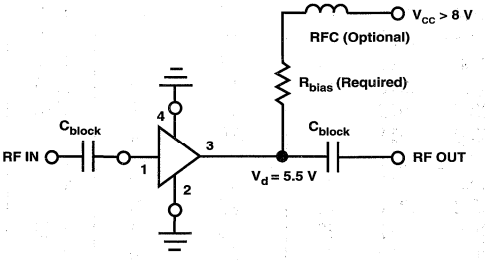
The INA-01170 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in a hermetic, high reliability package. It is designed for narrow or wide bandwidth industrial and military applications that require high gain and low noise IF or RF amplification.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

70 mil Package



Typical Biasing Configuration



INA-01170 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 140°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.1 mW/°C for T_C > 144°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

INA-01170 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 100 MHz	dB	30	32.5	35
ΔG_P	Gain Flatness	f = 10 to 250 MHz	dB		±0.5	
$f_{3\,dB}$	3 dB Bandwidth[2]		MHz		500	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 10 to 250 MHz	dB		39	
VSWR	Input VSWR	f = 10 to 250 MHz			1.6:1	
	Output VSWR	f = 10 to 250 MHz			1.5:1	
NF	50 Ω Noise Figure	f = 100 MHz	dB		2.0	2.5
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 100 MHz	dBm		11	
IP_3	Third Order Intercept Point	f = 100 MHz	dBm		23	
t_D	Group Delay	f = 100 MHz	psec		200	
V_d	Device Voltage		V	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

Notes:
1. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz Gain (G_P).

INA-01170 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	.09	–20	32.8	43.65	–2	–38.4	.012	–5	.17	–1	1.17
0.05	.10	–39	32.8	43.51	–9	–38.3	.012	17	.18	0	1.17
0.10	.13	–65	32.6	42.82	–18	–38.3	.012	–4	.18	1	1.17
0.15	.17	–83	32.4	41.71	–26	–38.4	.012	17	.19	2	1.18
0.20	.21	–96	32.1	40.41	–35	–38.6	.012	12	.19	3	1.18
0.25	.25	–107	31.8	38.93	–43	–39.0	.011	26	.19	4	1.26
0.30	.28	–115	31.5	37.38	–50	–39.0	.011	3	.20	5	1.26
0.40	.33	–130	30.7	34.19	–65	–39.3	.011	21	.21	3	1.31
0.50	.37	–140	29.9	31.13	–78	–39.2	.011	11	.22	0	1.35
0.60	.40	–150	29.0	28.30	–90	–38.9	.011	22	.23	–5	1.43
0.80	.43	–164	27.4	23.48	–112	–38.5	.012	30	.24	–19	1.52
1.0	.44	–176	25.8	19.45	–132	–36.5	.015	32	.23	–32	1.49
1.5	.44	165	21.8	12.37	–179	–33.6	.020	42	.19	–69	1.75
2.0	.44	154	17.9	7.88	146	–33.0	.022	42	.13	–106	2.42
2.5	.46	148	14.6	5.36	121	–30.6	.029	36	.12	–151	2.63
3.0	.48	139	11.4	3.71	96	–30.0	.032	45	.10	159	3.31

INA-01170 Typical Performance, T_A = 25°C

(unless otherwise noted)

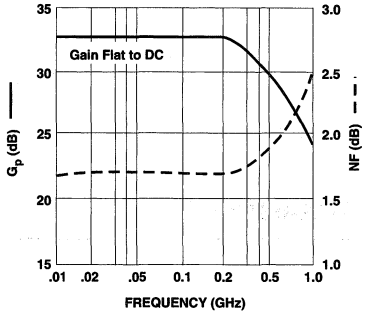


Figure 1. Typical Gain and Noise Figure vs. Frequency, T_A = 25°C, I_d = 35 mA.

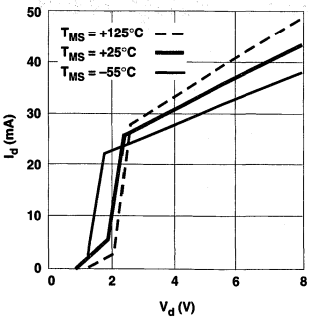


Figure 2. Device Current vs. Voltage.

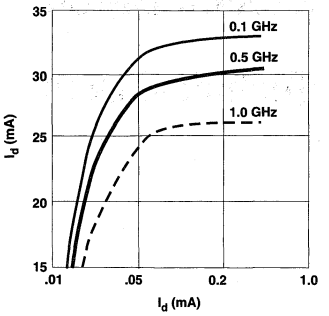


Figure 3. Power Gain vs. Current.

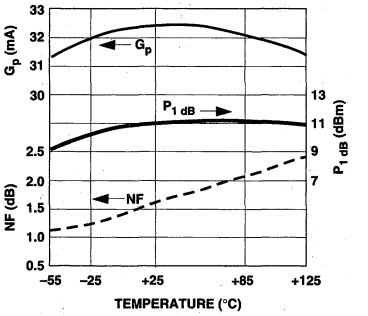


Figure 4. Output Power and 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.1 GHz, I_d = 35 mA.

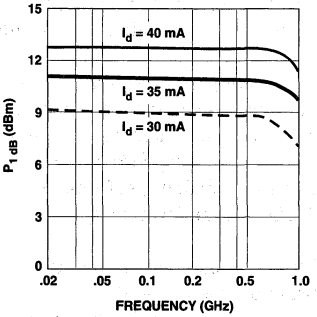


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

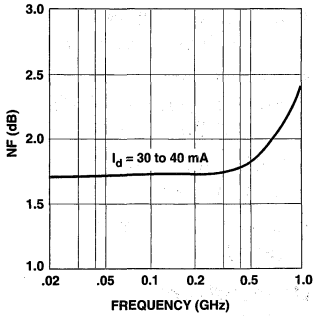
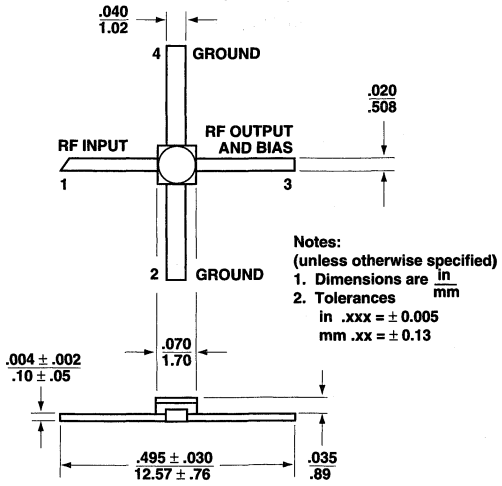


Figure 6. Noise Figure vs. Frequency.

70 mil Package Dimensions



HEWLETT® PACKARD

Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

INA-02100

Features

- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure:**
  2.0 dB Typical at 0.5 GHz
- **High Gain:**
  31.5 dB Typical at 0.5 GHz
  25.0 dB Typical at 1.5 GHz
- **3 dB Bandwidth:**
  DC to 1.0 GHz
- **Unconditionally Stable (k>1)**

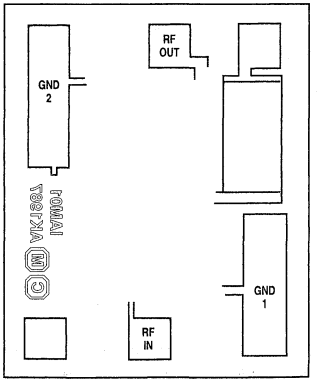
Description

The INA-02100 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier chip. It is designed for narrow or wide bandwidth industrial and military applications that require high gain and low noise IF or RF amplification.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1]

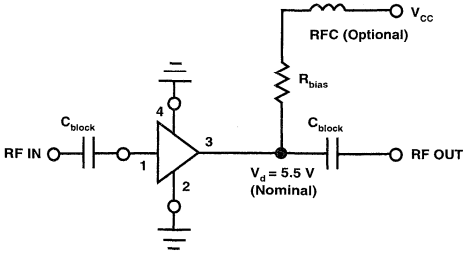
Chip Outline[1]



Notes:

1. See Application Note, "A005: Transistor Chip Use" for additional information.

Typical Biasing Configuration



INA-02100 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2]:
θ_{jc} = 60°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C
3. Derate at 16.7 mW/°C for T_{MS} > 176°C.

INA-02100 Electrical Specifications[1,3], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz	dB		31.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±1.5	
$f_{3\ dB}$	3 dB Bandwidth		GHz		1.0	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.01 to 1.0 GHz	dB		39	
VSWR	Input VSWR	f = 0.01 to 1.0 GHz			1.4:1	
	Output VSWR	f = 0.01 to 1.0 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.0	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		11	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		23	
t_D	Group Delay	f = 0.5 GHz	psec		350	
V_d	Device Voltage		V	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

Notes:
1. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
3. The values are the achievable performance for the INA-02100 mounted in a 70 mil stripline package.

INA-02100 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 5 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	0.06	–4	32.5	42.1	–2	–39.3	.011	14	.20	–1	1.27
0.05	0.05	–8	32.5	42.0	–8	–39.4	.011	12	.20	1	1.28
0.10	0.03	–46	32.3	41.3	–16	–37.9	.013	6	.20	–1	1.17
0.20	0.02	–52	31.8	39.0	–30	–39.2	.011	–4	.21	3	1.33
0.30	0.01	–46	31.1	36.2	–43	–38.8	.011	–12	.22	4	1.36
0.40	0.02	–44	30.4	33.3	–55	–40.4	.010	–2	.24	2	1.63
0.50	0.03	–35	29.7	30.7	–65	–39.3	.011	–17	.26	–1	1.56
0.60	0.06	–29	29.0	28.4	–74	–39.5	.011	–5	.28	–4	1.67
0.80	0.10	–41	27.9	24.8	–92	–38.1	.012	–9	.32	–14	1.58
1.00	0.17	–60	26.9	22.0	–108	–36.4	.015	–19	.34	–26	1.41
1.20	0.24	–73	26.0	19.9	–124	–35.5	.017	–16	.36	–40	1.32
1.40	0.30	–89	25.1	18.0	–141	–34.1	.020	–16	.38	–60	1.17
1.60	0.37	–103	24.1	16.0	–157	–32.6	.023	–30	.32	–91	1.19
1.80	0.42	–116	22.9	14.0	–174	–33.1	.022	–28	.26	–111	1.29
2.00	0.46	–128	21.5	12.0	171	–31.4	.027	–31	.22	–122	1.25
2.50	0.50	–146	18.3	8.2	142	–29.3	.034	–44	.19	–148	1.34
3.00	0.51	–162	14.6	5.4	116	–28.5	.038	–47	.15	178	1.83

Note:
1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section of the *Communications Components Designer's* Catalog.

INA-02100 Typical Performance, T_A = 25°C

(Unless otherwise noted: The values are the achievable performance for the INA-02100 mounted in a 70 mil stripline package.)

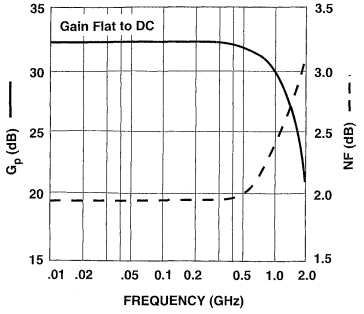


Figure 1. Typical Gain and Noise Figure vs. Frequency, T_A = 25°C, I_d = 35 mA.

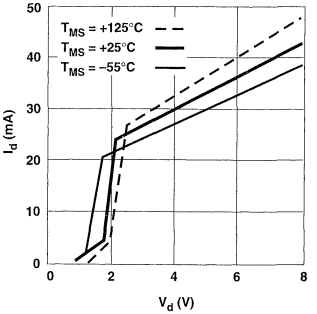


Figure 2. Device Current vs. Voltage.

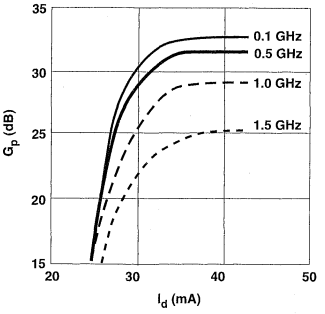


Figure 3. Power Gain vs. Current.

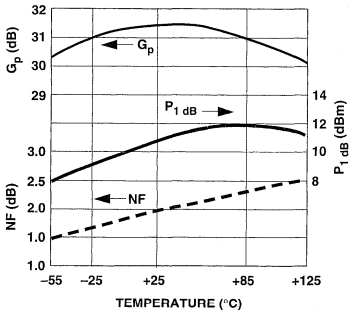


Figure 4. Output Power and 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.1 GHz, I_d = 35 mA.

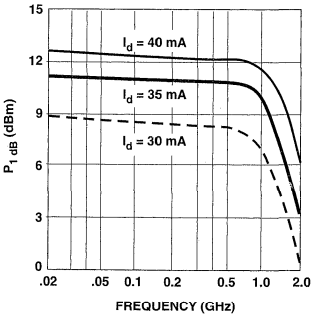


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

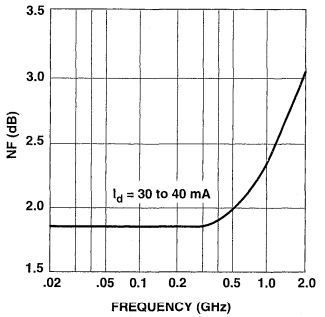
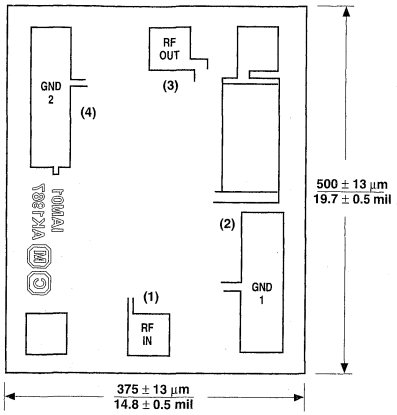


Figure 6. Noise Figure vs. Frequency.

INA-02100 Chip Dimensions



Chip thickness is 140 µm/5.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side. Note: Ground Bonding is Critical. Refer to Application Bulletin, "AB-0007: INA Bonding Configuration".

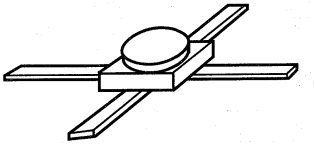
HEWLETT® PACKARD

Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

INA-02170

70 mil Package



Features

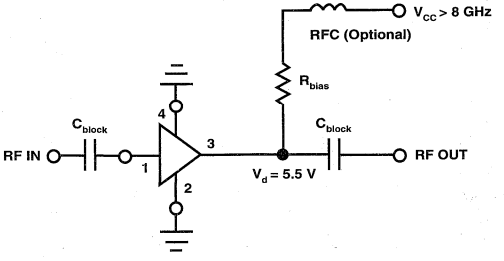
- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure:**
  2.0 dB Typical at 0.5 GHz
- **High Gain:**
  31.5 dB Typical at 0.5 GHz
  25.0 dB Typical at 1.5 GHz
- **3 dB Bandwidth:**
  DC to 1.0 GHz
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-Ceramic Surface Mount Package**

Description

The INA-02170 is a low noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in a hermetic, high reliability package. It is designed for narrow or wide bandwidth industrial and military applications that require high gain and low noise IF or RF amplification.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Typical Biasing Configuration



5965-9674E

INA-02170 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 140°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.1 mW/°C for T_C > 144°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

INA-02170 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz	dB	29.0	31.5	34.0
ΔG_P	Gain Flatness	f = 0.01 to 1.0 GHz	dB		±1.5	
$f_{3\,dB}$	3 dB Bandwidth[2]		GIIz		1.0	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.01 to 1.0 GHz	dB		39	
VSWR	Input VSWR	f = 0.01 to 1.0 GHz			1.4:1	
	Output VSWR	f = 0.01 to 1.0 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.0	2.5
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		11	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		23	
t_D	Group Delay	f = 0.5 GHz	psec		350	
V_d	Device Voltage		V	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

Notes:
1. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz Gain (G_P).

INA-02170 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	.05	–8	32.5	42.32	–2	–39.2	.011	14	.19	–1	1.26
0.05	.05	–31	32.5	42.32	–7	–38.9	.011	14	.19	–5	1.26
0.10	.06	–85	32.5	42.05	–14	–38.0	.013	10	.19	–10	1.15
0.20	.09	–110	32.3	41.06	–27	–38.8	.011	5	.18	–16	1.29
0.30	.12	–129	32.0	39.82	–40	–38.8	.011	1	.17	–21	1.32
0.40	.15	–140	31.7	38.43	–53	–40.2	.010	19	.16	–25	1.45
0.50	.17	–151	31.4	37.08	–65	–40.0	.010	8	.16	–27	1.48
0.60	.17	–159	31.0	35.49	–77	–39.6	.011	23	.16	–30	1.43
0.80	.18	–174	30.2	32.45	–101	–38.2	.012	23	.16	–40	1.43
1.00	.19	179	29.2	28.70	–126	–38.2	.012	17	.16	–53	1.55
1.20	.19	173	27.8	24.51	–149	–37.5	.013	27	.15	–71	1.66
1.40	.20	166	26.1	20.18	–171	–36.2	.015	35	.14	–102	1.73
1.60	.21	162	24.2	16.26	170	–36.3	.015	34	.12	–172	2.07
1.80	.22	159	22.3	13.02	153	–34.1	.020	46	.10	144	1.94
2.00	.23	155	20.4	10.45	139	–33.0	.022	37	.07	117	2.17
2.50	.25	150	16.7	6.82	112	–33.3	.022	32	.05	95	3.19
3.00	.29	144	13.1	4.51	87	–31.8	.026	32	.04	78	3.96

INA-02170 Typical Performance, T_A = 25°C

(unless otherwise noted)

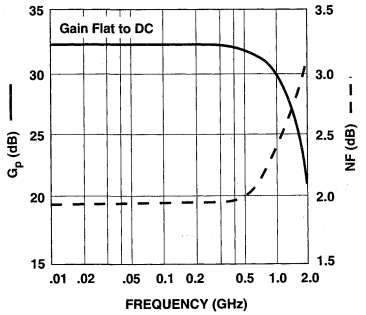


Figure 1. Typical Gain and Noise Figure vs. Frequency, T_A = 25°C, I_d = 35 mA.

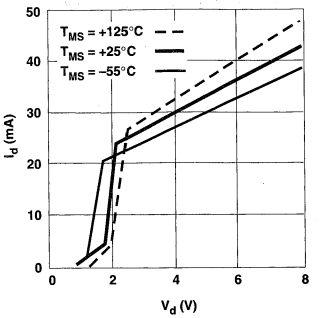


Figure 2. Device Current vs. Voltage.

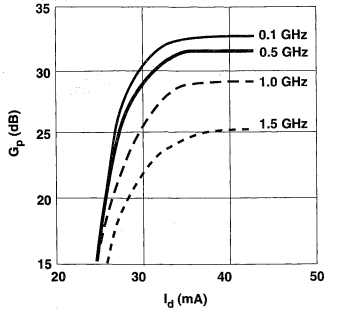


Figure 3. Power Gain vs. Current.

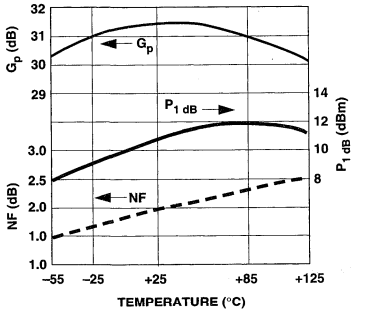


Figure 4. Output Power and 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.1 GHz, I_d = 35 mA.

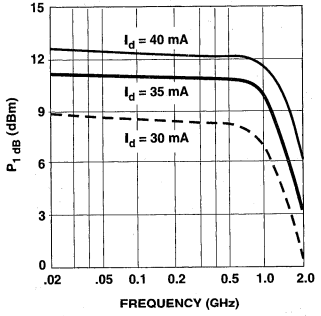


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

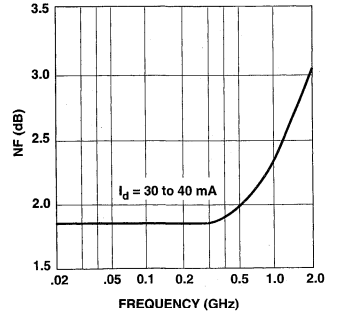
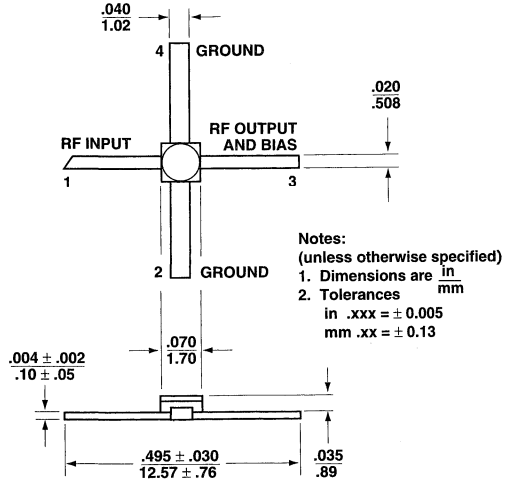


Figure 6. Noise Figure vs. Frequency.

70 mil Package Dimensions



HEWLETT® PACKARD

Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

INA-02184
INA-02186

Features

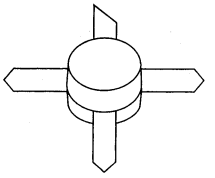
- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure:**
  2.0 dB Typical at 0.5 GHz
- **High Gain:**
  31 dB Typical at 0.5 GHz
  26 dB Typical at 1.5 GHz
- **3 dB Bandwidth:**
  DC to 0.8 GHz
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

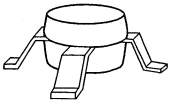
The INA-02184 and INA-02186 are low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifiers housed in low cost plastic packages. They are designed for narrow or wide bandwidth commercial applications that require high gain and low noise IF or RF amplification.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

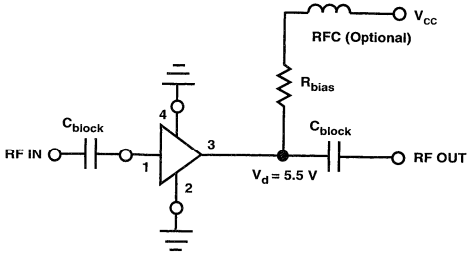
Package 84



Package 86



Typical Biasing Configuration



INA-02184, -02186 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3,4]	400 mW
RF Input Power	+13 dBm
Junction Temperature	+150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2]:
θ_{jc} = 90°C/W — INA-02184
θ_{jc} = 100°C/W — INA-02186

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 11.1 mW/°C for T_C > 144°C for INA-02184.
4. Derate at 10 mW/°C for T_C > 110°C for INA-02186.

INA-02184, -02186 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	INA-02184 Min.	INA-02184 Typ.	INA-02184 Max.	INA-02186 Min.	INA-02186 Typ.	INA-02186 Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz	dB	29.0	31.0		29.0	31.0	
ΔG_P	Gain Flatness	f = 0.01 to 1.0 GHz	dB		±2.0			±2.0	
$f_{3\ dB}$	3 dB Bandwidth[2]		GHz		0.8			0.8	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.01 to 1.0 GHz	dB		39			39	
VSWR	Input VSWR (Max over Freq. Range)	f = 0.01 to 1.0 GHz			1.5			2.0	
	Output VSWR (Max over Freq. Range)	f = 0.01 to 1.0 GHz			1.7			1.7	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.0			2.0	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		11			11	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		23			23	
t_D	Group Delay	f = 0.5 GHz	psec		330			350	
V_d	Device Voltage		V	4.0	5.5	7.0	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10			+10	

Notes:
1. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz Gain (G_P).

INA-02184, -02186 Part Number Ordering Information

Part Number	No. of Devices	Container
INA-02184-TR1	1000	7" Reel
INA-02184-BLK	100	Antistatic Bag
INA-02186-TR1	1000	7" Reel
INA-02186-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

INA-02184, -02186 Typical Performance, T_A = 25°C

(unless otherwise noted)

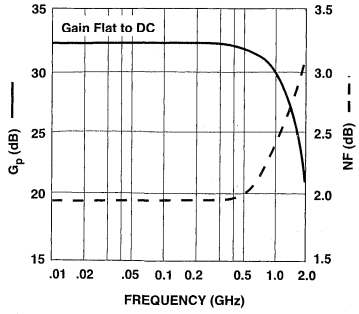


Figure 1. Typical Gain and Noise Figure vs. Frequency, T_A = 25°C, I_d = 35 mA.

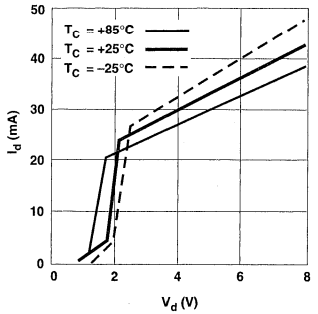


Figure 2. Device Current vs. Voltage.

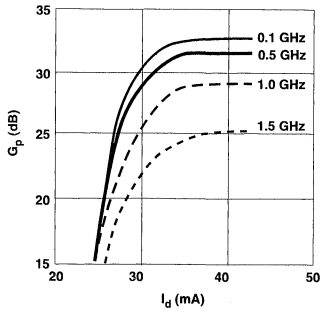


Figure 3. Power Gain vs. Current.

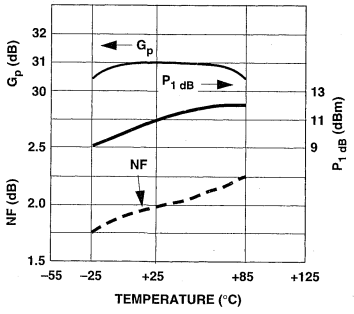


Figure 4. Output Power and 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 35 mA.

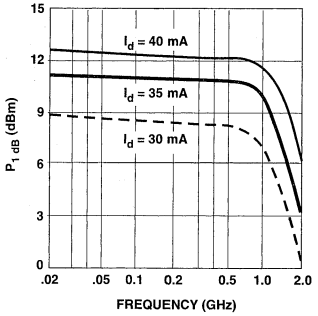


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

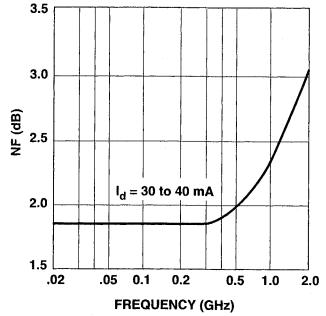


Figure 6. Noise Figure vs. Frequency.

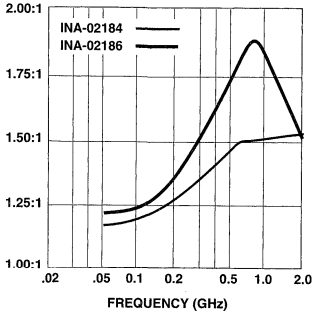


Figure 7. Input VSWR vs. Frequency, I_d = 35 mA.

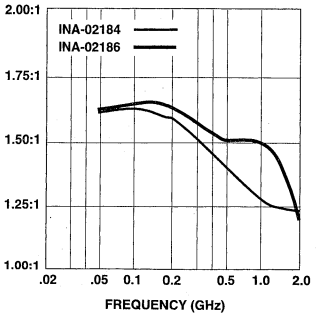


Figure 8. Output VSWR vs. Frequency, I_d = 35 mA.

Typical INA-02184 Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	.09	–176	31.9	39.33	–1	–40.0	.010	1	.25	–1	1.40
0.05	.09	–171	31.9	39.24	–6	–41.9	.008	–12	.25	–4	1.66
0.10	.10	–163	31.8	39.07	–13	–40.9	.009	1	.25	–8	1.52
0.20	.13	–159	31.7	38.30	–26	–40.0	.010	15	.23	–13	1.44
0.30	.15	–161	31.4	37.30	–39	–38.4	.012	16	.22	–17	1.29
0.40	.18	–168	31.2	36.42	–51	–39.2	.011	32	.21	–15	1.39
0.50	.19	–175	31.0	35.40	–63	–40.0	.010	34	.21	–16	1.52
0.60	.20	179	30.7	34.20	–75	–37.1	.014	35	.21	–17	1.24
0.80	.19	166	29.9	31.21	–101	–38.4	.012	38	.24	–26	1.44
1.00	.17	159	28.4	26.36	–126	–36.5	.015	53	.24	–41	1.40
1.20	.15	159	26.8	21.89	–149	–34.0	.020	56	.22	–60	1.31
1.40	.15	163	24.8	17.36	–169	–33.2	.022	62	.18	–78	1.50
1.60	.16	168	22.6	13.59	175	–31.4	.027	67	.14	–93	1.50
1.80	.18	168	20.7	10.86	161	–31.1	.028	61	.11	–108	1.74
2.00	.19	165	18.8	8.71	149	–30.2	.031	64	.08	–125	1.92
2.50	.23	159	14.9	5.56	127	–29.1	.035	56	.05	–167	2.54
3.00	.27	150	11.5	3.76	106	–27.1	.044	65	.04	156	2.89
3.50	.30	143	8.8	2.74	89	–26.0	.050	57	.04	137	3.39
4.00	.33	133	6.6	2.14	73	–25.0	.056	62	.05	137	3.78

Typical INA-02186 Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	.09	–178	31.5	37.38	–1	–40.0	.010	1	.24	–1	1.46
0.05	.09	–172	31.5	37.55	–6	–37.7	.013	11	.24	–5	1.22
0.10	.11	–160	31.5	37.46	–13	–39.2	.011	8	.23	–9	1.37
0.20	.14	–153	31.4	37.04	–25	–40.9	.009	15	.22	–17	1.60
0.30	.18	–156	31.3	36.62	–37	–38.4	.012	1	.21	–25	1.30
0.40	.22	–161	31.2	36.20	–49	–37.7	.013	28	.19	–30	1.25
0.50	.25	–169	31.1	35.70	–61	–39.2	.011	42	.18	–35	1.40
0.60	.28	–177	30.9	34.94	–74	–38.4	.012	44	.16	–39	1.33
0.80	.31	165	30.2	32.34	–101	–36.5	.015	52	.15	–47	1.20
1.00	.30	148	28.8	27.64	–129	–34.4	.019	57	.12	–59	1.15
1.20	.27	135	27.0	22.26	–153	–32.4	.024	62	.09	–70	1.15
1.40	.24	129	24.7	17.22	–173	–31.1	.028	61	.07	–80	1.23
1.60	.21	128	22.5	13.27	170	–31.4	.027	62	.04	–82	1.52
1.80	.20	129	20.4	10.42	156	–29.1	.035	61	.02	–83	1.50
2.00	.20	131	18.4	8.34	144	–29.1	.035	63	.01	–20	1.79
2.50	.23	133	14.5	5.29	123	–27.1	.044	59	.02	30	2.15
3.00	.27	130	11.2	3.61	103	–25.7	.052	63	.02	27	2.56
3.50	.31	124	8.3	2.60	86	–24.4	.060	64	.02	34	2.97
4.00	.34	118	6.1	2.02	70	–23.4	.068	58	.01	30	3.28

Emitter Inductance and Performance

As a direct result of their circuit topology, the performance of INA MMICs is extremely sensitive to groundpath ("emitter") inductance. The two stage design creates the possibility of a feedback loop being formed through the ground returns of the stages. If the path to ground provided by the external circuit is "long" (high in impedance) compared to the path back through the ground return of the other stage, then instability can occur (see Fig. 1). This phenomena can show up as a "peaking" in the gain versus frequency response (perhaps creating a negative gain slope amplifier), an increase in input VSWR, or even as return gain (a reflection coefficient greater than unity) at the input of the MMIC.

The "bottomline" is that ***excellent grounding is critical*** when using INA MMICs. The use of plated through holes or equivalent minimal path ground returns ***at the device*** is essential. An appropriate layout is shown in Figure 2. A corollary is that designs should be done on the thinnest practical substrate. The parasitic inductance of a pair of via holes passing through 0.032" thick P.C. board is approximately 0.1 nH, while that of a pair of via holes passing through 0.062" thick board is close to 0.5 nH. HP does not recommend using INA family MMICs on boards thicker than 32 mils.

These stability effects are entirely predictable. A circuit simulation using the data sheet S-parameters and including a description of the ground return path (via model or equivalent "emitter" inductance) will give an accurate picture of the performance that can be expected. Device characterizations are made with the ground leads of the MMIC directly contacting a solid copper block (system ground) at a distance of 2 to 4 mils from the body of the package. Thus the information in the data sheet is a true description of the performance capability of the MMIC, and contains minimal contributions from fixturing.

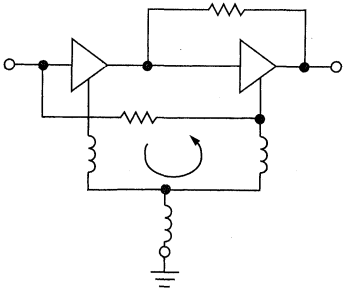


Figure 1. INA Potential Ground Loop.

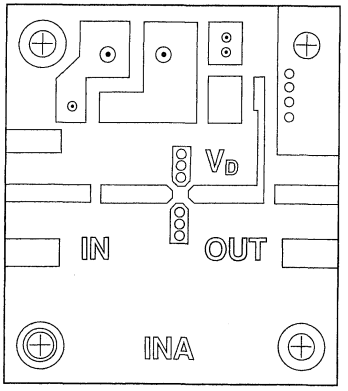
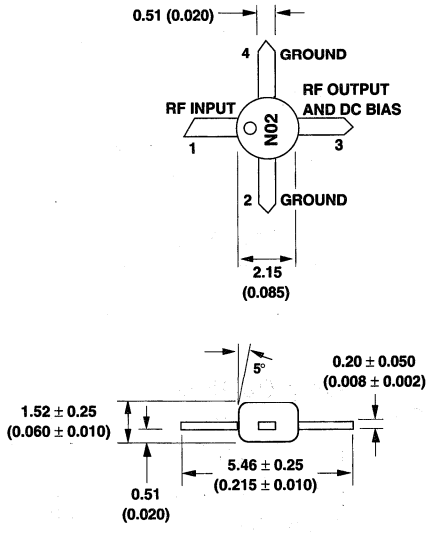


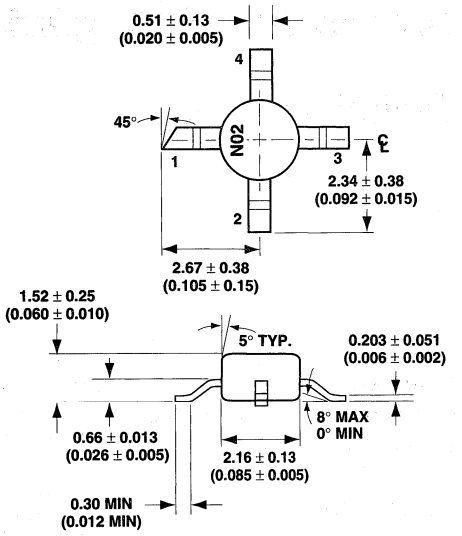
Figure 2. INA Circuit Board 2x Actual Size.

Package 84 Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Package 86 Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

INA-03100

Features

- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure:** 2.5 dB Typical at 1.5 GHz
- **High Gain:** 26.0 dB Typical at 2.8 GHz
- **3 dB Bandwidth:** DC to 2.8 GHz
- **Unconditionally Stable (k>1)**
- **Low Power Consumption**

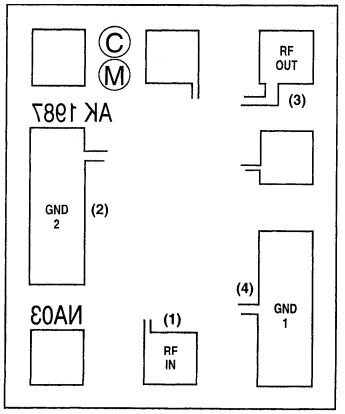
Description

The INA-03100 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier chip. It is designed for narrow or wide bandwidth commercial, industrial and military applications that require high gain and low noise IF or RF amplification with minimum power consumption.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1]

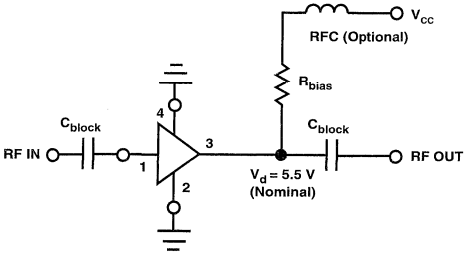
Chip Outline[1]



Note:

1. See Application Note, "A005: Transistor Chip Use" for additional information.

Typical Biasing Configuration



INA-03100 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2]:
θ_{jc} = 70°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 14.3 mW/°C for T_{MS} > 186°C.

INA-03100 Electrical Specifications[1,3], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 12 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.5 GHz	dB		26.0	
ΔG_P	Gain Flatness	f = 0.01 to 2.0 GHz	dB		±0.5	
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.8	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.01 to 2.0 GHz	dB		37	
VSWR	Input VSWR	f = 0.01 to 2.0 GHz			2.0[5]	
	Output VSWR	f = 0.01 to 2.0 GHz			3.0[5]	
NF	50 Ω Noise Figure	f = 1.5 GHz	dB		2.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.5 GHz	dBm		1.0	
IP_3	Third Order Intercept Point	f = 1.5 GHz	dBm		10	
t_D	Group Delay	f = 1.5 GHz	psec		200	
V_d	Device Voltage	f = 1.5 GHz	V	3.5	4.5	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+5	

Notes:
1. The recommended operating current range for this device is 8 to 20 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
3. The values are the achievable performance for the INA-03100 mounted in a 70 mil stripline package.

INA-03100 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 12 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.05	0.35	176	26.6	21.4	–4	–36.0	.016	8	.56	–1	1.25
0.10	0.35	172	26.6	21.3	–8	–36.5	.015	–4	.56	–3	1.30
0.20	0.33	165	26.4	21.0	–15	–36.4	.015	–5	.56	–4	1.30
0.40	0.31	150	26.1	20.1	–29	–36.0	.016	–13	.54	–7	1.33
0.60	0.27	137	25.6	19.0	–42	–37.6	.013	–14	.54	–8	1.58
0.80	0.23	125	25.0	17.8	–53	–36.1	.016	–13	.53	–9	1.49
1.00	0.19	113	24.5	16.7	–63	–35.1	.018	–16	.53	–10	1.43
1.20	0.16	99	24.0	15.9	–72	–36.9	.014	–21	.54	–12	1.72
1.40	0.13	76	23.8	15.4	–81	–36.4	.015	–12	.55	–15	1.65
1.60	0.12	51	23.6	15.2	–88	–35.6	.017	–11	.56	–17	1.54
1.80	0.13	21	23.6	15.5	–97	–34.1	.020	–5	.58	–20	1.24
2.00	0.18	–5	23.8	15.5	–106	–34.3	.019	–13	.60	–25	1.18
2.50	0.40	–52	24.7	17.2	–132	–30.2	.031	–9	.67	–38	0.53
3.00	0.81	–86	25.6	19.1	–167	–27.0	.045	–12	.70	–64	0.03

Note:
1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section of the *Avantek Microwave Semiconductors* databook.

INA-03100 Typical Performance, T_A = 25°C

(unless otherwise noted: The values are the achievable performance for the INA-03100 mounted in a 70 mil stripline package.)

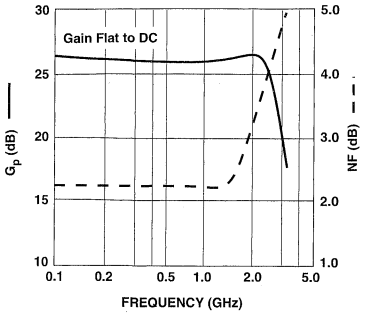


Figure 1. Typical Gain and Noise Figure vs. Frequency, T_A = 25°C, I_d = 12 mA.

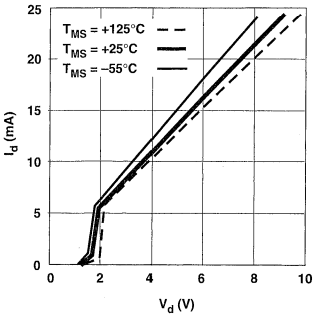


Figure 2. Device Current vs. Voltage.

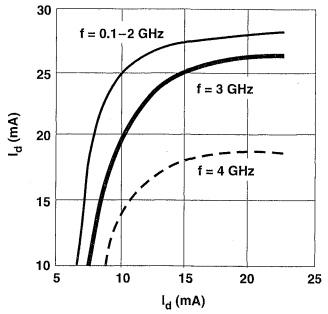


Figure 3. Power Gain vs. Current.

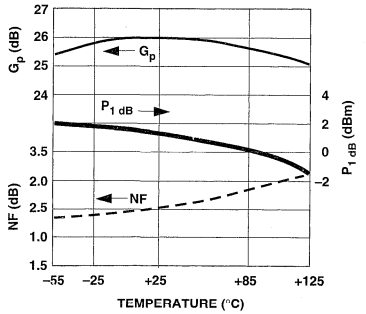


Figure 4. Output Power and 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.5 GHz, I_d = 12 mA.

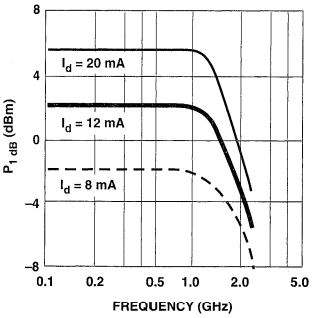


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

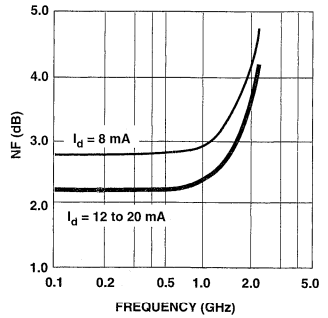
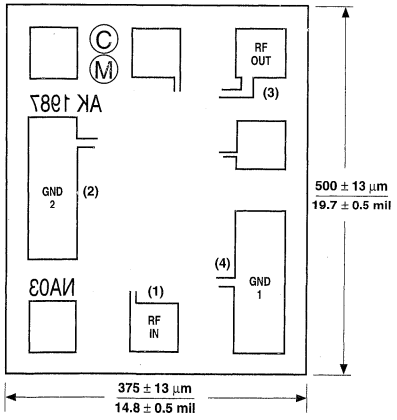


Figure 6. Noise Figure vs. Frequency.

INA-03100 Chip Dimensions



Chip thickness is 140 µm/5.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side. Note: Ground Bonding is Critical. Refer to Application Bulletin, "AB-0007: INA Bonding Configuration".

HEWLETT® PACKARD

Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

INA-03170

Features

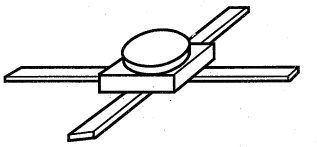
- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure:** 2.5 dB Typical at 1.5 GHz
- **High Gain:** 26.0 dB Typical at 1.5 GHz
- **3 dB Bandwidth:** DC to 2.8 GHz
- **Unconditionally Stable (k>1)**
- **Low Power Dissipation**
- **Hermetic Gold-Ceramic Surface Mount Package**

Description

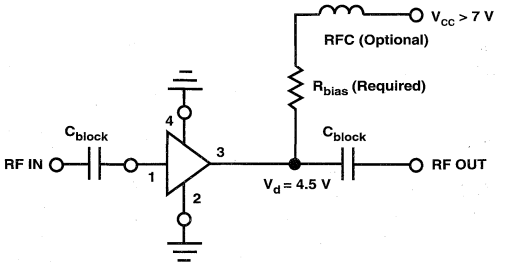
The INA-03170 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in a hermetic, high reliability package. It is designed for narrow or wide bandwidth commercial, industrial and military applications that require high gain and low noise IF or RF amplification with minimum power consumption.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

70 mil Package



Typical Biasing Configuration



5965-9677E

INA-03170 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	25 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 150°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.7 mW/°C for T_C > 170°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

INA-03170 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 12 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.5 GHz	dB	24.5	28.0	30.0
ΔG_P	Gain Flatness	f = 0.01 to 2.0 GHz	dB		±0.5	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.8	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.01 to 2.0 GHz	dB		37	
VSWR	Input VSWR	f = 0.01 to 2.0 GHz			2.0[3]	
	Output VSWR	f = 0.01 to 2.0 GHz			3.0[3]	
NF	50 Ω Noise Figure	f = 1.5 GHz	dB		2.5	3.0
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.5 GHz	dBm		1.0	
IP_3	Third Order Intercept Point	f = 1.5 GHz	dBm		10	
t_D	Group Delay	f = 1.5 GHz	psec		200	
V_d	Device Voltage	f = 1.5 GHz	V	4.0	5.3	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+5	

Notes:
1. The recommended operating current range for this device is 8 to 20 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz Gain (G_P).
3. VSWR can be improved by bypassing the bias directly to ground.

INA-03170 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 12 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.05	.35	178	26.6	21.48	–4	–35.9	.016	9	.56	–1	1.24
0.10	.35	176	26.6	21.42	–7	–36.5	.015	6	.56	–4	1.29
0.20	.34	172	26.6	21.37	–14	–36.5	.015	–1	.56	–7	1.30
0.40	.34	164	26.5	21.19	–28	–36.5	.015	–5	.54	–13	1.33
0.60	.33	158	26.4	20.91	–41	–38.4	.012	2	.53	–18	1.58
0.80	.32	152	26.3	20.69	–54	–37.1	.014	5	.51	–22	1.46
1.00	.32	147	26.2	20.48	–67	–36.5	.015	4	.50	–27	1.41
1.20	.32	141	26.2	20.40	–80	–39.2	.011	13	.49	–32	1.79
1.40	.31	133	26.3	20.73	–93	–37.7	.013	25	.48	–38	1.57
1.60	.31	125	26.5	21.15	–106	–37.1	.014	28	.47	–45	1.47
1.80	.30	117	26.8	21.84	–121	–35.4	.017	30	.46	–52	1.28
2.00	.27	106	26.9	22.20	–138	–37.1	.014	33	.42	–62	1.48
2.50	.15	94	26.6	21.48	–177	–35.4	.017	23	.31	–79	1.44
3.00	.16	159	23.7	15.32	133	–34.4	.019	42	.16	–72	1.78
3.50	.28	150	19.8	9.81	99	–35.4	.017	28	.19	–60	2.71

INA-03170 Typical Performance, T_A = 25°C

(unless otherwise noted)

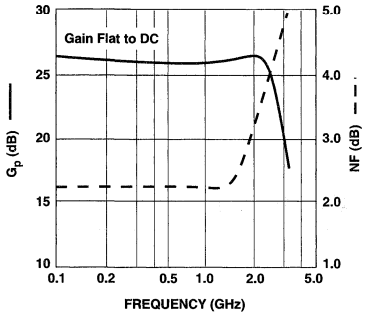


Figure 1. Typical Gain and Noise Figure vs. Frequency, T_A = 25°C, I_d = 12 mA.

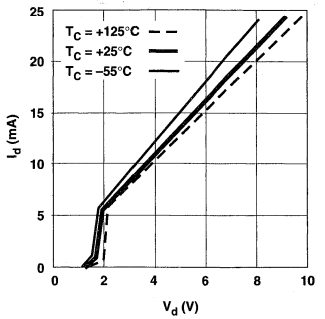


Figure 2. Device Current vs. Voltage.

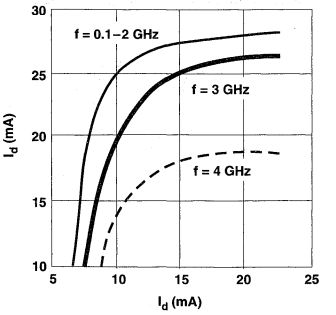


Figure 3. Power Gain vs. Current.

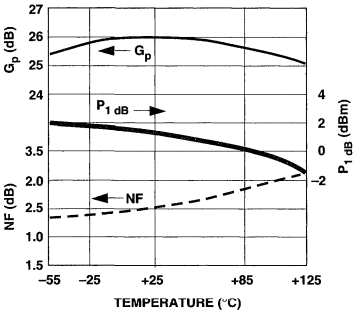


Figure 4. Output Power and 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.5 GHz, I_d = 12 mA.

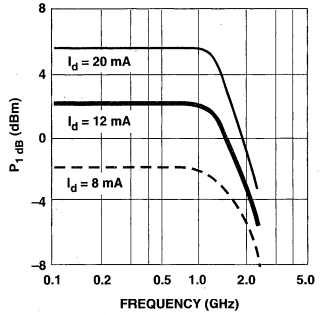


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

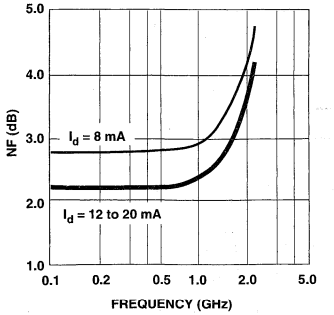
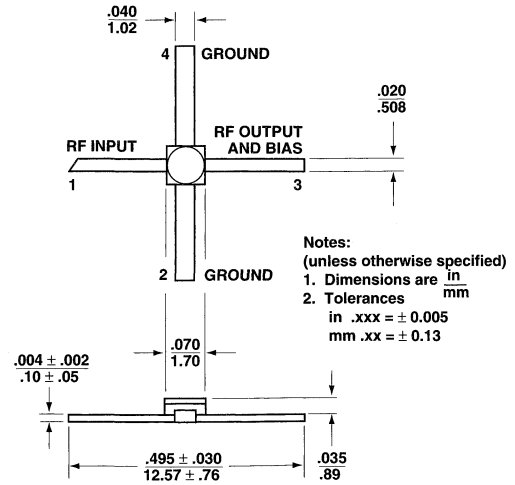


Figure 6. Noise Figure vs. Frequency.

70 mil Package Dimensions



HEWLETT® PACKARD

Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

INA-03184

Features

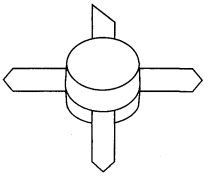
- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure:** 2.6 dB Typical at 1.5 GHz
- **High Gain:** 25 dB Typical at 1.5 GHz
- **3 dB Bandwidth:** DC to 2.5 GHz
- **Unconditionally Stable (k>1)**
- **Low Power Dissipation:** 10 mA Bias
- **Low Cost Plastic Package**

Description

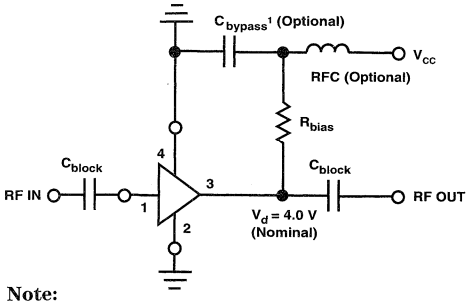
The INA-03184 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in a low cost surface mount plastic package. It is designed for narrow or wide bandwidth commercial and industrial applications that require high gain and low noise IF or RF amplification with minimum power consumption.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

84 Plastic Package



Typical Biasing Configuration



Note:

1. VSWR can be improved by bypassing a 100–120 Ω bias resistor directly to ground. See AN-S012: Low Noise Amplifiers.

INA-03184 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	25 mA
Power Dissipation[2]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance:
θ_{jc} = 100°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. Derate at 10 mW/°C for T_C > 130°C.

INA-03184 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 10 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.5 GHz	dB	23.0	25.0	
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.8	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.5	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 1.5 GHz	dB		35	
VSWR	Input VSWR	f = 0.01 to 2.0 GHz			2.0:1	
	Output VSWR	f = 0.01 to 2.0 GHz			3.0:1[3]	
NF	50 Ω Noise Figure	f = 1.5 GHz	dB		2.6	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.5 GHz	dBm		–2.0	
IP_3	Third Order Intercept Point	f = 1.5 GHz	dBm		7	
t_D	Group Delay	f = 1.5 GHz	psec		210	
V_d	Device Voltage		V	3.0	4.0	5.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+4	

Notes:
1. The recommended operating current range for this device is 8 to 18 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz Gain (G_P).
3. VSWR can be improved by bypassing a 100–200 Ω bias resistor directly to ground. See AN-S012: MagIC Low Noise Amplifiers.

INA-03184 Part Number Ordering Information

Part Number	No. of Devices	Container
INA-03184-TR1	1000	7" Reel
INA-03184-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

INA-03184 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 10 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.05	.32	179	25.6	19.14	–3	–37.1	.014	3	.55	0	1.48
0.10	.32	176	25.6	19.05	–7	–37.1	.014	4	.57	–3	1.45
0.20	.32	172	25.6	19.05	–14	–37.1	.014	6	.55	–5	1.48
0.40	.32	165	2.5	18.78	–29	–37.1	.014	10	.53	–11	1.53
0.60	.32	158	25.4	18.71	–43	–36.5	.015	11	.51	–14	1.49
0.80	.32	151	25.4	18.53	–57	–36.5	.015	13	.51	–17	1.50
1.00	.32	144	25.2	18.18	–72	–35.9	.016	21	.50	–20	1.46
1.20	.30	135	25.2	18.27	–86	–35.9	.016	25	.50	–23	1.46
1.40	.31	126	25.2	18.10	–102	–35.4	.017	30	.49	–29	1.42
1.60	.30	117	25.1	17.92	–117	–34.9	.018	38	.48	–34	1.38
1.80	.26	102	24.9	17.49	–135	–34.4	.019	44	.45	–41	1.39
2.00	.22	92	24.4	16.62	–153	–34.0	.020	49	.40	–50	1.44
2.50	.09	91	22.2	12.88	168	–33.6	.021	57	.26	–48	1.87
3.00	.14	160	18.9	8.79	134	–32.8	.023	65	.22	–33	2.40
3.50	.24	151	15.4	5.92	108	–32.0	.025	69	.26	–33	3.01
4.00	.29	139	12.4	4.18	87	–30.8	.029	81	.28	–43	3.52

Note:

1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

INA-03184 Typical Performance, T_A = 25°C

(unless otherwise noted)

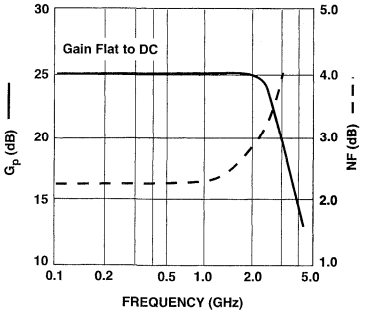


Figure 1. Typical Gain and Noise Figure vs. Frequency, T_A = 25°C, I_d = 10 mA.

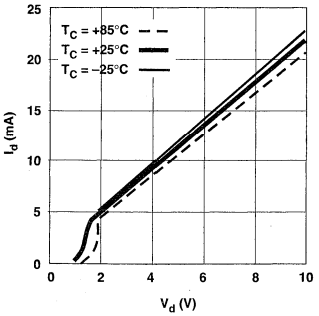


Figure 2. Device Current vs. Voltage.

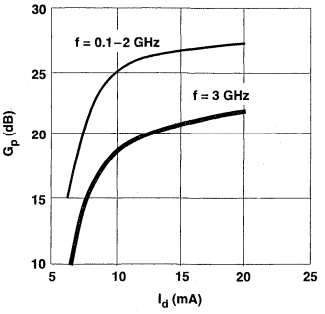


Figure 3. Power Gain vs. Current.

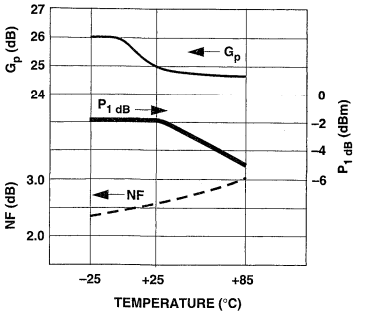


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.5 GHz, I_d = 10 mA.

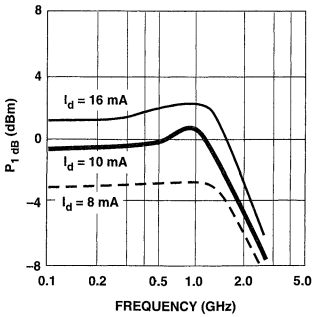


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

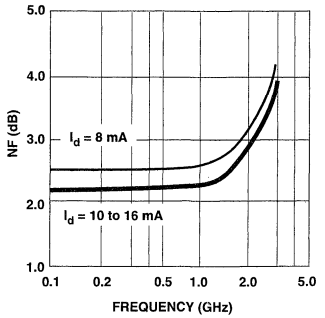
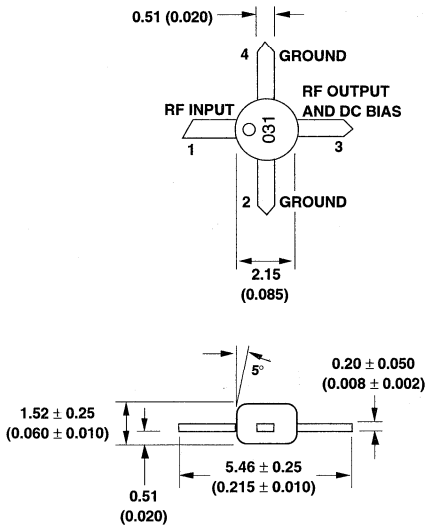


Figure 6. Noise Figure vs. Frequency.

84 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

INA-10386

Features

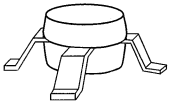
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 1.8 GHz
- **26 dB Typical Gain at 1.5 GHz**
- **10 dBm Typical P_{1dB} at 1.5 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**

Description

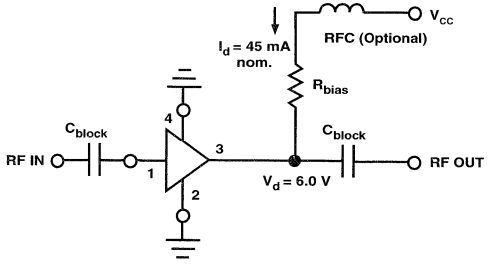
The INA-10386 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in a low cost surface mount plastic package. It is designed for narrow or wide bandwidth commercial and industrial applications that require high gain and moderate power.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

86 Plastic Package



Typical Biasing Configuration



INA-10386 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance:
θ_{jc} = 100°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 10 mW/°C for T_C > 75°C.

INA-10386 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 6V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.5 GHz	dB	23.0	26.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.5 GHz	dB		±1.0	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		1.8	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 2.0 GHz	dB		30	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 2.0 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 1.5 GHz	dB		3.8	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.5 GHz	dBm		10	
IP_3	Third Order Intercept Point	f = 1.5 GHz	dBm		23	
t_D	Group Delay	f = 1.5 GHz	psec		250	
I_d	Device Current		mA	35	45	55
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

Notes:
1. The recommended operating current range for this device is 40 to 60 mA. Typical performance as a function of current is on the following page.

INA-10386 Part Number Ordering Information

Part Number	No. of Devices	Container
INA-10386-TR1	1000	7" Reel
INA-10386-BLK	100	Antistatic Bag

INA-10386 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, V_d = 6 V)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.05	.12	–9	26.6	21.4	–4	–35.2	.017	1	.11	–3	1.51
0.10	.11	–17	26.7	21.6	–8	–35.6	.017	3	.12	–10	1.50
0.50	.13	–79	26.7	21.6	–38	–35.7	.016	10	.07	–40	1.59
1.00	.17	–137	26.8	21.9	–80	–34.1	.020	43	.03	18	1.33
1.50	.21	171	26.0	20.0	–126	–33.1	.023	53	.07	32	1.26
2.00	.21	127	23.6	15.1	–168	–29.9	.032	55	.07	9	1.23
2.50	.19	106	21.7	12.2	159	–28.4	.038	58	.04	42	1.27
3.00	.14	86	19.2	9.1	127	–26.7	.048	55	.05	56	1.37
3.50	.07	85	16.8	6.9	97	–24.8	.058	50	.06	47	1.44
4.00	.08	148	14.2	5.1	70	–24.7	.058	51	.04	40	1.82

INA-10386 Typical Performance, T_A = 25°C

(unless otherwise noted)

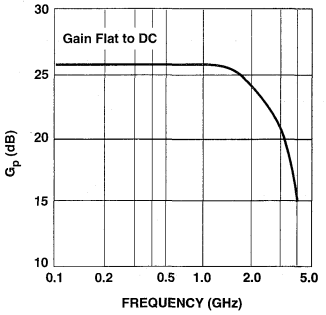


Figure 1. Typical Gain and Noise Figure vs. Frequency, T_A = 25°C, V_d = 6 V.

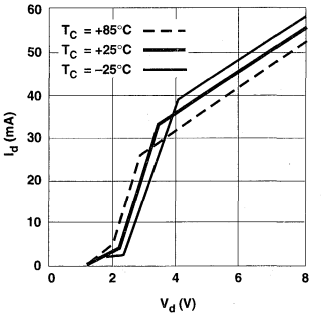


Figure 2. Device Current vs. Voltage.

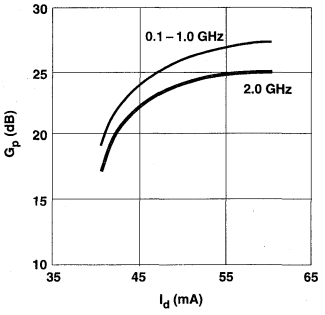


Figure 3. Power Gain vs. Current.

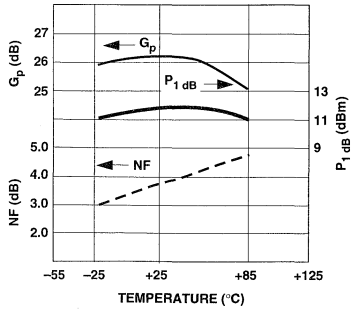


Figure 4. Output Power and 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.5 GHz, V_d = 6 V.

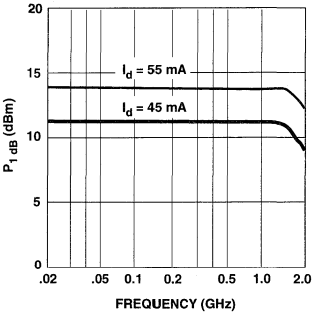


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

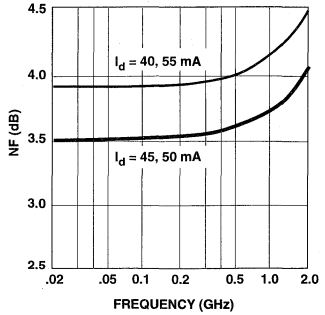
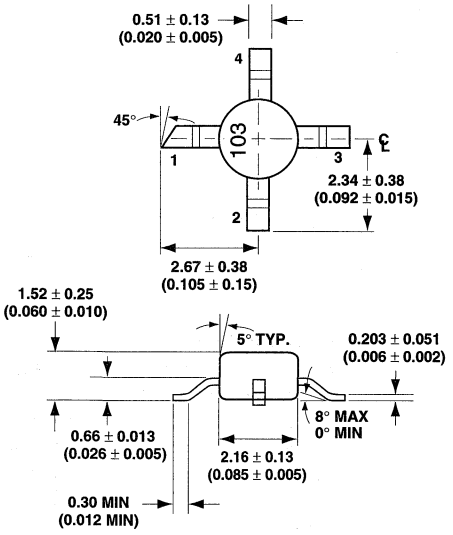


Figure 6. Noise Figure vs. Frequency.

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

1.5 GHz Low Noise Self-Biased Transistor Amplifier

Technical Data

INA-12063

Features

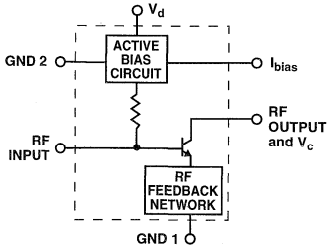
- **Integrated, Active Bias Circuit**
- **Single Positive Supply Voltage (1.5 – 5V)**
- **Current Adjustable, 1 to 10mA**
- **2 dB Noise Figure at 900 MHz**
- **16 dB Gain at 900 MHz**
  25 dB Gain at 100 MHz

Applications

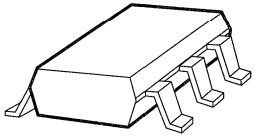
- **Amplifier Applications for Cellular, Cordless, Special Mobile Radio, PCS, ISM, and Wireless LAN Applications**

Equivalent Circuit

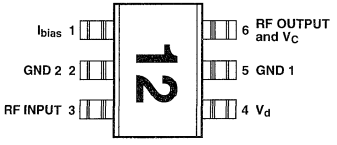
(Simplified)



Surface Mount Package SOT-363 (SC-70)



Pin Connections and Package Marking



Note:
Package marking provides orientation and identification.

Description

Hewlett-Packard's INA-12063 is a Silicon monolithic self-biased transistor amplifier that offers excellent gain and noise figure for applications to 1.5 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

The INA-12063 is a unique RFIC that combines the performance flexibility of a discrete transistor with the simplicity of using an integrated circuit. Using a patented bias circuit, the performance and operating current of the INA-12063 can be adjusted over the 1 to 10 mA range.

The INA-12063 is fabricated using HP's 30 GHz f_{MAX} ISOSAT™ Silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metalization, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity, and reliability.

INA-12063 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Supply Voltage, to Ground	V	7
V_c	Collector Voltage	V	7
I_c	Collector Current	mA	15
P_{in}	CW RF Input Power	dBm	13
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{j\text{-}c} = 170°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

Electrical Specifications, $T_C = 25°C$, $V_d = 3$ V, unless noted

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.	Std.Dev.[3]
G_P	Power Gain ($\|S_{21}\|^2$)	f = 900 MHz[1] f = 250 MHz[2]	dB	14.5	16 19		0.36
NF	Noise Figure	f = 900 MHz[1] f = 250 MHz[2]	dB		2.0 5.0	2.6	0.2
P_{1dB}	Output Power at 1 dB Gain Compression	f = 900 MHz[1] f = 250 MHz[2]	dBm		0 -7		
IP_3	Third Order Intercept Point	f = 900 MHz[1] f = 250 MHz[2]	dBm		15 2		
I_{dd}	Device Current[4]	900 MHz LNA[1] 250 MHz IF Amp[2]	mA		5 1.5	7	0.6

Notes:
1. See Test Circuit in Figure 32.
2. See Test Circuit in Figure 33.
3. Standard deviation number is based on measurement of at least 500 parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.
4. I_{dd} is the total current into Pins 1, 4, and 6 of the device, i.e. $I_{dd} = I_c + I_{bias} + I_d$.

INA-12063 Typical Performance, 900 MHz LNA (900 MHz Test Circuit, see Figure 32)

T_C = 25°C, Z_O = 50 Ω, V_d = 3 V, I_C = 5 mA, unless noted

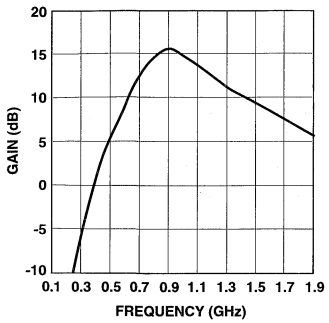


Figure 1. Gain vs. Frequency.

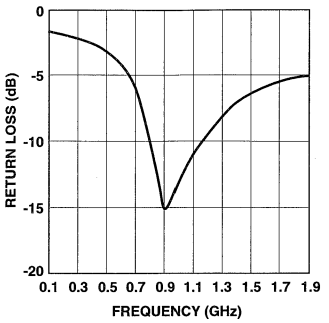


Figure 2. Input Return Loss vs. Frequency.

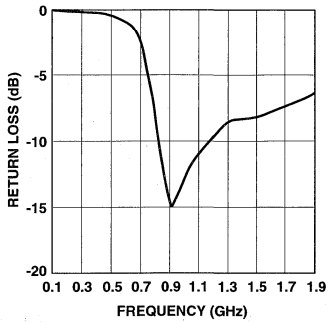


Figure 3. Output Return Loss vs. Frequency.

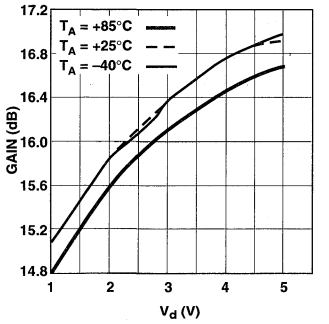


Figure 4. Gain at 900 MHz vs. Voltage and Temperature.

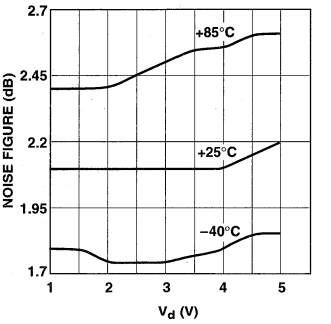


Figure 5. Noise Figure at 900 MHz vs. Voltage and Temperature.

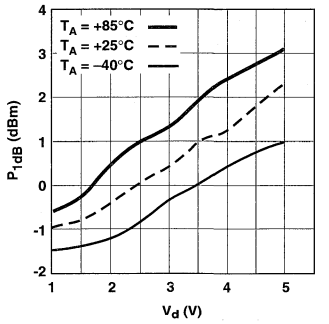


Figure 6. Output P_{1dB} at 900 MHz vs. Voltage and Temperature.

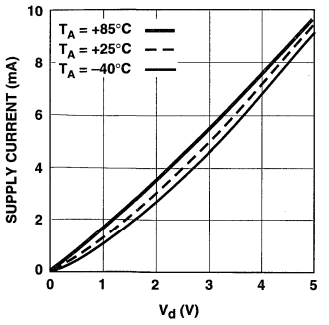


Figure 7. Supply Current vs. Voltage and Temperature.

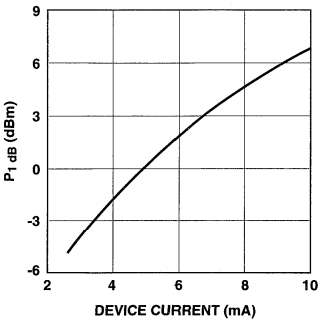


Figure 8. Output $P_{1\,dB}$ at 900 MHz vs. Device Current for V_d = 3 V.

INA-12063 Typical Scattering Parameters[1], I_C = 1.5 mA

T_C = 25°C, Z_O = 50 Ω, V_d = 3.0 V

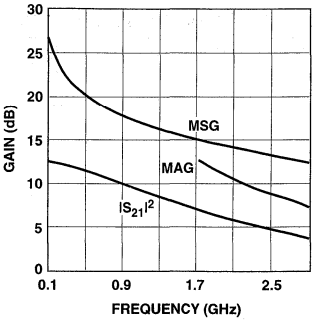
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	0.93	-8	12.6	4.26	172	-42.2	0.01	86	0.99	-3
0.2	0.92	-16	12.5	4.20	164	-36.2	0.02	79	0.99	-7
0.3	0.90	-24	12.3	4.11	157	-32.8	0.02	73	0.98	-10
0.4	0.89	-32	12.0	4.00	149	-30.5	0.03	69	0.96	-13
0.5	0.83	-38	11.7	3.83	141	-29.1	0.04	64	0.94	-16
0.6	0.79	-45	11.3	3.69	135	-27.9	0.04	60	0.93	-19
0.7	0.75	-52	10.9	3.49	128	-26.8	0.05	56	0.91	-21
0.8	0.72	-58	10.4	3.32	122	-26.1	0.05	53	0.89	-23
0.9	0.69	-64	10.1	3.18	116	-25.5	0.05	50	0.87	-26
1.0	0.65	-69	9.6	3.03	111	-24.9	0.06	47	0.86	-28
1.1	0.61	-74	9.2	2.89	106	-24.5	0.06	45	0.84	-30
1.2	0.59	-80	8.7	2.72	102	-24.2	0.06	43	0.83	-32
1.3	0.55	-84	8.4	2.64	97	-23.9	0.06	41	0.82	-34
1.4	0.52	-89	8.1	2.54	92	-23.6	0.07	40	0.81	-35
1.5	0.49	-94	7.7	2.43	88	-23.3	0.07	38	0.80	-37
1.6	0.47	-98	7.3	2.33	84	-23.2	0.07	36	0.79	-39
1.7	0.44	-103	7.0	2.23	80	-22.9	0.07	35	0.78	-40
1.8	0.42	-107	6.6	2.15	77	-22.9	0.07	35	0.77	-42
1.9	0.40	-112	6.4	2.08	73	-22.5	0.07	34	0.77	-44
2.0	0.38	-116	6.0	1.99	69	-22.3	0.08	33	0.76	-45
2.1	0.36	-120	5.7	1.93	66	-22.1	0.08	32	0.75	-47
2.2	0.34	-124	5.3	1.83	63	-22.0	0.08	29	0.74	-49
2.3	0.31	-129	5.2	1.82	59	-21.9	0.08	30	0.74	-51
2.4	0.31	-133	4.7	1.72	57	-22.0	0.08	29	0.73	-52
2.5	0.29	-137	4.6	1.70	54	-21.7	0.08	31	0.73	-54
2.6	0.28	-144	4.3	1.65	50	-21.4	0.08	30	0.73	-56
2.7	0.27	-149	4.1	1.60	47	-21.0	0.09	29	0.72	-58
2.8	0.25	-154	3.7	1.54	44	-20.7	0.09	27	0.71	-60
2.9	0.23	-156	3.5	1.50	41	-20.9	0.09	24	0.70	-61
3.0	0.24	-162	3.5	1.49	39	-21.0	0.09	28	0.71	-63

Note:

1. Reference plane per Figure 31 in Applications Information section.

Typical Noise Parameters @ 900 MHz, I_C = 1.5 mA

Fmin (dB)	Γ_{opt} Mag.	Γ_{opt} Ang.	R_N (Ω)
1.4	0.6	36	23



INA-12063 Typical Scattering Parameters[1], I_C = 2.5 mA

T_C = 25°C, Z_O = 50 Ω, V_d = 3.0 V

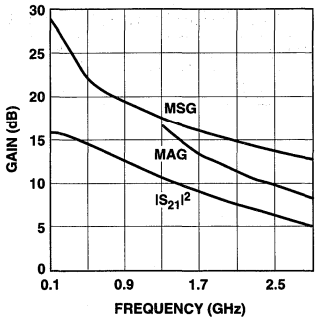
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	0.90	-10	16.0	6.33	171	-42.2	0.01	87	0.99	-4
0.2	0.88	-18	15.8	6.19	161	-36.2	0.02	79	0.98	-8
0.3	0.85	-27	15.5	5.98	153	-33.2	0.02	73	0.96	-11
0.4	0.82	-35	15.2	5.74	144	-31.1	0.03	68	0.94	-15
0.5	0.76	-42	14.6	5.37	135	-29.6	0.03	62	0.91	-18
0.6	0.71	-49	14.1	5.07	128	-28.4	0.04	59	0.90	-20
0.7	0.67	-56	13.5	4.73	122	-27.5	0.04	55	0.87	-23
0.8	0.62	-62	12.9	4.43	116	-26.6	0.05	53	0.85	-25
0.9	0.59	-67	12.4	4.18	110	-26.1	0.05	51	0.83	-27
1.0	0.54	-72	11.9	3.93	104	-25.6	0.05	49	0.82	-29
1.1	0.51	-76	11.4	3.71	100	-25.1	0.06	48	0.80	-30
1.2	0.49	-81	10.8	3.47	95	-24.8	0.06	46	0.79	-32
1.3	0.45	-84	10.4	3.31	91	-24.5	0.06	44	0.77	-34
1.4	0.42	-89	10.0	3.15	87	-24.1	0.06	44	0.76	-35
1.5	0.39	-93	9.5	2.98	83	-23.6	0.07	42	0.76	-37
1.6	0.37	-96	9.1	2.84	79	-23.5	0.07	41	0.74	-39
1.7	0.35	-100	8.7	2.72	76	-23.3	0.07	40	0.73	-40
1.8	0.33	-104	8.3	2.60	72	-23.0	0.07	41	0.73	-42
1.9	0.31	-108	8.0	2.51	69	-22.5	0.07	40	0.72	-43
2.0	0.29	-112	7.6	2.40	66	-22.2	0.08	40	0.72	-45
2.1	0.27	-115	7.3	2.31	62	-22.0	0.08	38	0.72	-47
2.2	0.25	-119	6.8	2.20	59	-21.8	0.08	36	0.71	-49
2.3	0.24	-122	6.6	2.15	56	-21.6	0.08	36	0.70	-50
2.4	0.23	-126	6.2	2.05	54	-21.7	0.08	36	0.69	-52
2.5	0.22	-131	6.1	2.01	51	-21.2	0.09	38	0.69	-53
2.6	0.20	-136	5.8	1.95	48	-20.7	0.09	36	0.69	-55
2.7	0.19	-142	5.5	1.89	45	-20.4	0.10	35	0.68	-57
2.8	0.18	-145	5.2	1.81	42	-20.0	0.10	32	0.68	-60
2.9	0.16	-146	4.9	1.75	39	-20.2	0.10	29	0.66	-60
3.0	0.17	-153	4.8	1.75	37	-20.1	0.10	32	0.68	-62

Note:

1. Reference plane per Figure 31 in Applications Information section.

Typical Noise Parameters @ 900 MHz, I_C = 2.5 mA

Fmin (dB)	Γ_{opt} Mag.	Γ_{opt} Ang.	R_N (Ω)
1.5	0.54	36	20



INA-12063 Typical Scattering Parameters[1], I_C = 5 mA

T_C = 25°C, Z_O = 50 Ω, V_d = 3.0 V

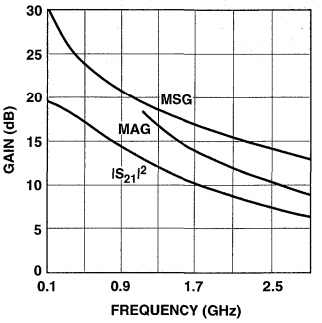
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	0.86	-11	19.6	9.56	168	-42.2	0.01	79	0.98	-5
0.2	0.82	-22	19.3	9.18	157	-36.8	0.01	73	0.96	-10
0.3	0.78	-31	18.7	8.65	146	-33.8	0.02	71	0.93	-13
0.4	0.73	-40	18.1	8.07	137	-31.7	0.03	68	0.90	-17
0.5	0.65	-46	17.3	7.34	128	-30.4	0.03	62	0.86	-20
0.6	0.59	-53	16.6	6.75	120	-28.7	0.04	61	0.85	-22
0.7	0.55	-59	15.8	6.18	114	-28.0	0.04	59	0.82	-24
0.8	0.50	-64	15.1	5.68	108	-27.2	0.04	56	0.80	-26
0.9	0.46	-68	14.4	5.26	103	-26.9	0.04	55	0.78	-27
1.0	0.43	-72	13.8	4.88	97	-26.3	0.05	52	0.77	-29
1.1	0.40	-76	13.2	4.55	93	-25.8	0.05	52	0.74	-30
1.2	0.37	-79	12.6	4.24	89	-25.3	0.05	52	0.74	-32
1.3	0.35	-81	12.0	3.99	85	-24.8	0.06	51	0.72	-34
1.4	0.33	-85	11.5	3.76	81	-24.3	0.06	50	0.72	-35
1.5	0.30	-87	11.0	3.55	78	-23.9	0.06	48	0.71	-36
1.6	0.28	-90	10.5	3.37	75	-23.5	0.07	48	0.70	-38
1.7	0.27	-94	10.1	3.21	71	-23.2	0.07	47	0.69	-39
1.8	0.25	-95	9.7	3.05	68	-22.9	0.07	48	0.69	-41
1.9	0.23	-99	9.3	2.93	64	-22.2	0.08	46	0.69	-42
2.0	0.22	-101	9.0	2.81	61	-22.0	0.08	45	0.68	-44
2.1	0.20	-104	8.5	2.67	58	-21.6	0.08	43	0.67	-45
2.2	0.18	-104	8.1	2.55	56	-21.3	0.09	41	0.67	-48
2.3	0.17	-107	7.8	2.47	53	-21.1	0.09	41	0.66	-50
2.4	0.17	-109	7.5	2.37	51	-20.8	0.09	41	0.66	-51
2.5	0.15	-114	7.3	2.31	48	-20.5	0.09	42	0.65	-53
2.6	0.14	-118	7.0	2.24	45	-20.0	0.10	40	0.66	-55
2.7	0.13	-123	6.7	2.17	42	-19.6	0.11	39	0.64	-56
2.8	0.12	-125	6.4	2.08	39	-19.3	0.11	36	0.63	-59
2.9	0.11	-126	6.1	2.02	37	-19.3	0.11	33	0.62	-59
3.0	0.11	-133	6.0	2.00	35	-19.3	0.11	35	0.64	-61

Note:

1. Reference plane per Figure 31 in Applications Information section.

Typical Noise Parameters @ 900 MHz, I_C = 5 mA

Fmin (dB)	Γ_{opt} Mag.	Γ_{opt} Ang.	R_N (Ω)
1.8	0.41	38	16



INA-12063 Typical Scattering Parameters[1], I_C = 8 mA

T_C = 25°C, Z_O = 50 Ω, V_d = 3.0 V

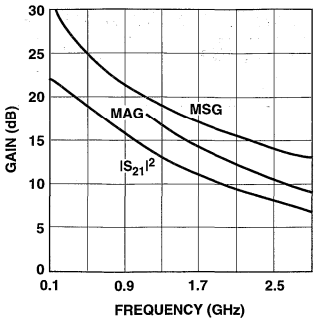
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	0.80	-13	22.3	12.97	166	-41.9	0.01	73	0.98	-5
0.2	0.76	-24	21.7	12.17	152	-37.4	0.01	72	0.94	-11
0.3	0.69	-35	20.9	11.10	141	-33.9	0.02	75	0.90	-15
0.4	0.63	-44	20.1	10.06	130	-32.2	0.02	69	0.86	-18
0.5	0.55	-49	19.0	8.89	121	-30.6	0.03	64	0.83	-21
0.6	0.50	-55	18.1	8.00	114	-29.6	0.03	64	0.80	-23
0.7	0.45	-59	17.1	7.20	107	-28.9	0.04	59	0.77	-24
0.8	0.41	-64	16.3	6.56	102	-28.0	0.04	59	0.76	-25
0.9	0.37	-67	15.6	6.02	97	-26.9	0.05	58	0.73	-26
1.0	0.34	-69	14.9	5.53	92	-26.5	0.05	58	0.71	-29
1.1	0.32	-72	14.1	5.08	88	-25.9	0.05	57	0.71	-30
1.2	0.30	-76	13.5	4.72	84	-25.4	0.05	56	0.70	-31
1.3	0.28	-76	12.9	4.40	81	-24.7	0.06	55	0.69	-33
1.4	0.26	-79	12.4	4.18	77	-24.1	0.06	53	0.68	-34
1.5	0.24	-82	11.7	3.86	74	-23.5	0.07	53	0.67	-36
1.6	0.23	-81	11.4	3.71	71	-23.4	0.07	52	0.65	-38
1.7	0.21	-84	10.8	3.48	68	-22.8	0.07	52	0.66	-39
1.8	0.20	-85	10.5	3.34	65	-22.7	0.07	51	0.66	-41
1.9	0.19	-89	9.9	3.14	62	-22.0	0.08	50	0.67	-42
2.0	0.17	-88	9.6	3.01	59	-21.5	0.08	48	0.66	-44
2.1	0.17	-91	9.2	2.89	56	-21.2	0.09	47	0.64	-45
2.2	0.15	-91	8.8	2.77	53	-21.0	0.09	44	0.63	-47
2.3	0.14	-93	8.6	2.68	51	-20.6	0.09	43	0.64	-49
2.4	0.14	-94	8.3	2.59	48	-20.4	0.09	43	0.64	-49
2.5	0.13	-98	8.0	2.51	47	-19.9	0.10	43	0.63	-51
2.6	0.12	-102	7.7	2.42	43	-19.5	0.11	42	0.61	-53
2.7	0.11	-103	7.3	2.32	40	-19.0	0.11	41	0.61	-56
2.8	0.10	-107	7.1	2.25	37	-18.6	0.12	38	0.61	-58
2.9	0.10	-101	6.7	2.17	36	-18.7	0.12	34	0.58	-60
3.0	0.09	-110	6.8	2.18	34	-18.7	0.12	35	0.61	-60

Note:

1. Reference plane per Figure 31 in Applications Information section.

Typical Noise Parameters @ 900 MHz, I_C = 8 mA

Fmin (dB)	Γ_{opt} Mag.	Γ_{opt} Ang.	R_N (Ω)
2.0	0.30	41	15



INA-12063 Applications Information

Introduction

The INA-12063 is a unique RFIC configuration that combines the performance flexibility of a discrete transistor with the simplicity of using an integrated circuit.

The INA-12063 is an integrated circuit that combines three functions: (1) a silicon bipolar RF transistor, (2) an RF feedback network, and (3) a patented[1] bias regulation circuit. A simplified schematic diagram of the INA-12063 is shown in Figure 9. The result is a versatile gain stage that can be operated from a single +1.5 to +5 volt power supply with the device current set by the user.

The INA-12063 is designed for use in battery powered equipment demanding high performance with low supply voltages and minimal current drain. Typical applications for the INA-12063 include low noise RF amplifiers, IF amplifiers, gain and buffer stages through 2 GHz. The INA-12063 is an excellent choice for use in cellular and cordless telephones, PCS, W/LAN's, RF modems and other commercial wireless equipment.

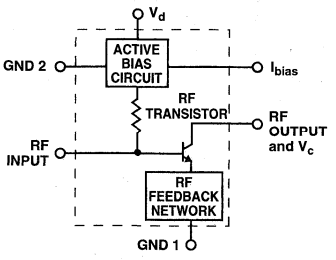


Figure 9. INA-12063 Schematic.

Description

The *active bias circuit* solves three problems normally encountered with traditional approaches for biasing discrete transistors. First, as an active bias circuit, the emitter of the RF transistor is DC grounded. This permits the collector current to be controlled without the need for resistors and/or bypass capacitors in the emitter that may degrade RF performance.

Second, the internal bias circuit greatly simplifies the design tasks commonly associated with biasing transistors, such as accurately regulating the collector current, allowing for variations in h_{FE}, making a non-intrusive DC connection to the base of the transistor, and stabilizing current over temperature.

And, third, the integrated bias circuit eliminates the cost, parts count, and associated PCB space required for as many as 8 additional DC components.

The integrated bias control circuit is very easy to use. For most applications, the collector current for the RF transistor can be set with a single resistor.

The geometry of the integrated *RF transistor* is designed to provide an excellent balance between low noise figure, high gain, and good dynamic range while retaining practical impedance matching levels. The operating current is typically in the 1 to 10 mA range.

The *integrated RF feedback* contains an inductive element in the emitter circuit of the RF transistor. This series feedback configuration is of the type often implemented in discrete transistor designs for the purpose of improving stability and bringing the optimum noise match at the input of the transistor closer to 50 Ω. The result is that for many applications, a simple, series inductor is often all that is needed to adequately match the input of the INA-12063 to 50 Ω.

In contrast to amplifiers that use resistive feedback to achieve broadband 50 Ω input and output matches, the INA-12063 leaves the designer with the flexibility of optimizing performance for a particular frequency band. For example, frequency selective input and output impedance matching circuits can be used to tune for optimum NF, maximum output power, low input VSWR, or to tailor the passband response to eliminate undesirable gain responses.

Setting the Bias Current

The integrated, active bias circuit is a 10:1 current mirror. The current mirror forces the collector current in the RF transistor to be approximately 10 times the current supplied to the I_{bias} pin.

In normal use, a voltage between +1.5 and +5 volts, is applied to both the V_d and V_c terminals of the INA-12063. Although normally connected to the same supply voltage, it is not necessary that both V_d and V_c be at the same voltage.

The collector current of the RF transistor is then set by injecting a small control current into the I_{bias} pin that is approximately 1/10 of the desired collector current.

[1] U.S. Patent Number 5436595

While there are any number of means of supplying the I_{bias} control current, the simplest way is to merely place a resistor between the V_d and I_{bias} terminals, shown as "R_{bias}" in Figure 10. R_{bias} will be sufficiently high to act as a current source. The value for R_{bias} is calculated as follows:

$$R_{bias} = 10 \left(\frac{V_d - 0.8}{I_c} \right) \quad (1)$$

where V_d is the device voltage, I_c is the desired collector current, and R_{bias} is the value of the bias determining resistor. For example, for a desired collector current of 1.5 mA and a power supply of 2.7 volts, the value of R_{bias} would be 12.7 KΩ.

Power Down

A power-down function for the INA-12063 can be conveniently implemented by switching the I_{bias} current. This method has the advantage of switching only a very small current since I_{bias} is typically only a fraction of a mA.

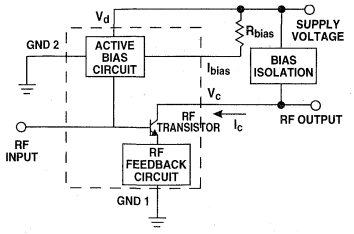


Figure 10. Single-Resistor Bias Circuit.

Amplifier Application Guidelines

This section describes the general approach for designing amplifiers using the INA-12063. This is a generic design approach and is applicable for most low noise RF or IF amplifiers or for general purpose gain and buffer stages.

The following "10-step" program is suggested as the design sequence:

1. Determine performance goals.
2. Select the bias condition.
3. Choose PCB material.
4. Check stability.
5. Determine required DC connections.
6. Design the input impedance matching network.
7. Design the output impedance matching network.
8. Layout the printed circuit board.
9. Computer optimization and performance verification.
10. Fabricate, assemble, and test.

Each of these steps in the design sequence will now be discussed in the following sections.

Step 1. Establish Performance Goals

The first step in the design of an INA-12063 amplifier stage is to establish performance goals. It may be necessary to consider performance tradeoffs between some amplifier parameters, such as Noise Figure, Input VSWR, Gain, Output Power, Output VSWR, Stability, and DC power consumption.

Some of these parameters are counterposed, for example, increased output power requires greater DC power consumption. The tradeoff decisions may require consideration of the choice of DC bias which is discussed in the next section. The final design will often be a balance between system-critical performance and those parameters of lesser significance.

Step 2. Choose Bias Conditions

The second step of the design process is to choose the bias conditions, i.e., the RF transistor operating voltage (V_c) and current (I_c). The bias conditions are chosen at this step in the design sequence since many of the RF design characteristics (e.g., S-parameters and noise parameters) are dependent on current and/or voltage.

The choice of bias *voltage* is often preemptive as it is normally fixed by available system resources, such as a battery voltage or system power supply. The INA-12063 will operate from supply voltages from 1.5 to 5 volts, with +3 volts considered to be the typical operating voltage.

Although noise figure and gain are somewhat insensitive to device voltage as an independent variable, some increase in output power can be realized with higher device voltages.

The bias *current* has the greatest effect on RF performance and the following tradeoffs should be considered:

Noise Figure increases with device current. The data in the Typical Noise Parameter tables shows an increase in F_{min} of from 1.4 dB at 1.5 mA of bias current to 2.0 dB at 8 mA.

Gain – Transducer gain, $|S_{21}|^2$, increases significantly in proportion to device current.

Output Power – One of the benefits of increased device current is greater output power. A typical increase in current from 1.5 to 8 mA results in a corre-

sponding increase in P_{1dB} of -5.2 dBm to +4.6 dBm. The data sheet curve in Figure 8 characterizes the P_{1dB} - I_C tradeoff.

Impedance Match – While it is not a parameter per se, the degree of difficulty of impedance match may also be a consideration in the selection of bias current. Generally, the higher the device current, the less "severe" the impedance match, i.e., Γ_{opt}, Γ_{ms}, Γ_{ml} are all closer to 50 Ω.

Step 3. Selection of PCB Material

If the selection of PCB material has not been preordained by other factors (e.g., system standards) then it should be chosen at this stage of the design process. The printed circuit board material is chosen at this step since it will have an effect on the next step of the stability analysis and on the subsequent design of the impedance matching networks.

Key factors to consider in the selection of board material are dielectric constant, RF loss characteristics, board thickness, and cost.

The dielectric constant and board thickness together contribute to the physical geometry of the circuit, an important consideration for miniaturization. Higher dielectric constant material enables the construction of more compact circuits since the physical dimensions of transmission lines are smaller.

In addition to transmission line widths, PCB board thickness also influences the quality of ground vias. Ground vias in excessively thick PCBs result in high inductance paths to ground. For some active devices, poor grounding can result in performance degradation or reduced stability.

Dielectric loss is not a significant factor for the moderate frequency ranges over which the INA-12063 is normally used. Low loss, low dielectric constant "microwave" type materials are usually reserved for applications demanding the very lowest noise figures (minimum circuit loss) and/or for frequencies above 2 GHz.

An overall good choice for most low cost wireless applications using devices such as the INA-12063 is a fiberglass-epoxy material such as FR-4 or G-10 with a thickness in the range of 0.020 to 0.031 inches.

Step 4. Stability Analysis

A stability analysis is the next step in the design process. The purpose of this step is to examine the circuit's tendency to oscillate. A linear CAD program, such as Hewlett-Packard's *Touchstone* should be used to calculate the stability factor, K, and stability measure, B1. The factors K and B1 are both derived from the S-parameters for the INA-12063 at the previously established bias voltage and current. The conditions for unconditional stability are:

$$K > 1 \text{ and } B1 > 0$$

While a simple analysis based only on the S-parameters is often adequate at this point, a slightly more rigorous analysis is recommended that includes the parasitic elements in the device's path to ground. At this stage in the design, a reasonable estimation (guess) of this electrical path and the construction of the ground vias are adequate. For the INA-12063, bear in mind that Pin 5 of the package is the critical connection for "RF" grounding. A typical RF path to ground consists of a short length of transmission line terminated in one or more ground vias. (The length of the PCB pad between the INA-12063 ground pin and the ground should be modeled as a microstripline ("MLIN" in *Touchstone*), and the plated through ground holes as "VIA" elements.)

When evaluating stability, it is a good practice to calculate K and B1 over the full frequency range for which S-parameters are available. The reason for this is that even though K and B1 may indicate stability over the frequency band of interest, the possibility exists for a circuit to oscillate at frequencies that are far outside of the band of interest.

While unconditional stability requires a positive, non-zero value of B1, most of the following stability analysis will focus on the K factor since the value of K indicates the degree of stability. What should the minimum value of K be to ensure stability? While K=1.001 is stable, some margin is prudent to allow for component tolerances, temperature effects, and manufacturing variations. Typical rules of thumb suggest that K should be at least 1.2 to 1.5.

There are three possible cases resulting from the CAD analysis:

- *Case 1* – K>1 over the entire frequency range.
- *Case 2* – K>1 within the band of interest and K<1 for some frequencies outside of the band of interest.
- *Case 3* – K<1 within the band of interest.

If the CAD analysis indicates there is a potential instability issue ($K < 1$ and/or $B1 \leq 0$ for any frequency) as in Case 2 or Case 3 above, then some stability countermeasures will be needed.

There are four basic techniques for handling potential instability:

(a) Live with it. If the source and load impedances that will be presented to the amplifier are well defined, the finesse approach of using stability circles may be used. Stability circles (calculated by a program such as *Touchstone*) are plotted on a Smith chart and define regions of loads that could cause a circuit to oscillate. An amplifier is safe from oscillation if the expected amplifier terminations lie well outside of the unstable regions on both the input and output impedance planes. Since the possibility of oscillation could exist at any frequency for which the INA-12063 has gain, stability circles must be checked at frequencies over a wide frequency range when this method is used.

(b) Resistive feedback. The use of resistive feedback is often used to create stable, wideband, amplifiers. While effective in stabilizing active devices, this method will not be considered here since a significant penalty is often paid in degraded NF, less gain, and lowered output power performance.

(c) Lossless feedback. Reactive feedback elements can also be used to stabilize amplifiers. The INA-12063 already incorporates one type of reactive feedback in the emitter of the RF transistor, with a resulting improvement in stability. Further use of the lossless feedback technique is not suggested for most INA-12063 amplifier applications since this method adds considerable design complexity as well as additional parts count and board space to the circuit.

(d) Resistive loading. Resistive loading can be used at either the input or output of the INA-12063 to create an unconditionally stable amplifier. This is the brute-force method of ensuring stability. It is fairly fail-safe and is also the simplest to implement. The addition of a resistive element to either the amplifier input or output creates RF loss which manifests itself as lower gain plus either increased NF (if the resistance is added to the input) or lower output power (if the resistance is placed at the output.)

In keeping with the goals of low cost (i.e., circuit simplicity), the resistive loading method is the technique suggested for producing an unconditionally stable amplifier for most applications of the INA-12063.

The resistive loading can be applied in either series or shunt and can be added to either the input or output of the amplifier. The choice of series or shunt resistive load may be dictated by whether the real part of the output impedance of the amplifier device is greater or less than 50 Ω. The logical choice is to use a shunt resistor when the amplifier impedance is >50 Ω and a series resistor for the case of >50 Ω. This technique will bring the overall impedance closer to 50 Ω, thus simplifying the match. In some cases, excessive voltage drop across the stabilizing resistor due to the DC current into the device may preclude the use of the series configuration. Shunt resistance is usually the most straightforward solution to implement since it can be easily bypassed to ground with a capacitor without disturbing the bias.

For gain or buffer stages requiring maximum output power, the loading is applied to the amplifier input. If the performance goal is low noise figure, the resistive loading is implemented on the output side of the INA-12063 as shown in Figure 11.

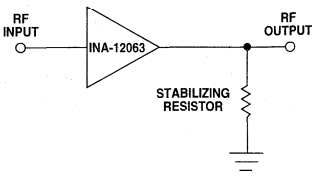


Figure 11. Shunt Stabilizing Resistor for LNA.

A simple manual optimization may be used to determine a starting value for the stabilizing resistor. By adding a shunt resistor to the output of the INA-12063 in the circuit file used in the previous stability analysis, K may be observed while adjusting the value of the resistor. The shunt resistor should be the highest value that will adequately stabilize the circuit.

The three possible cases resulting from the stability analysis will now be considered.

Case 1 (K>1 over the entire frequency range) is always the hoped for situation since it is the easiest to deal with. If K is greater than unity by a comfortable margin, then no further action is needed at this point.

Case 2 (K>1 within the band of interest; K<1 for some frequencies outside of the band of interest) is the next simplest case to handle. Since K>1 in the band of interest, little or no performance tradeoffs may be needed to make the amplifier unconditionally stable.

By using R-C or R-L combinations, frequency selective resistive loading can be applied only over the frequency range for which K < 1 in order to stabilize the amplifier without adversely affecting in-band performance.

Case 3 (K<1 in the band of interest) requires tradeoffs in NF or output power to achieve an unconditionally stable amplifier stage.

The INA-12063 typically falls into either Case 2 or Case 3, depending on the bias current, circuit grounding, and frequency band of interest.

In all cases, a final check of stability should be done in the analysis of the completed amplifier design. This is done as part of Step 9 in the design sequence.

Step 5. DC Connections

The DC connections to the INA-12063 are considerations in the next two steps in which the input and output impedance matching networks are chosen. The goal is economy of components by integrating as many of the DC connections into the matching circuits as practical. For example the use of a series C in an impedance matching network could double as a DC blocking capacitor. Or, a shunt L can be used to apply the required supply voltage to the output of the INA-12063.

One of the advantages of the active bias circuit in the INA-12063 is that there is no need for an external DC bias connection to the RF Input. If desired, the input may be connected directly to matching networks using a series capacitor as the first element.

Pins 4 and 6 are connected to the supply voltage and Pins 2 and 5 are DC grounded. Pins 1 and 4 should be bypassed to ground. A high value resistor from Pin 1 to Pin 6 is a simple and convenient method for setting the device operating current. Pin 3, has an internal voltage present and is normally connected to a DC blocking capacitor. The only DC connection which could affect RF performance is that of applying the supply voltage to the RF Output pin.

Step 6. Designing the Input Match

The input impedance match is generally designed to achieve either of two goals, either lowest noise figure or maximum power transfer. The maximum power transfer match provides maximum gain and corresponds to minimum VSWR. In some cases, noise circles in combination with constant gain circles are used to design an intermediate match point to achieve a compromise in performance between low noise figure and low input VSWR.

If the design goal is to obtain lowest NF, the input of the INA-12063 is matched to the conjugate of Γ_{opt}. Γ_{opt} is the reflection coefficient of the source termination that results in F_{min}, the lowest possible device noise figure. Γ_{opt} design data are found in the tables of Typical Noise Parameters. Alternatively Γ_{opt} can be calculated using the same CAD circuit file used in the stability analysis in Step 4 above. This method is slightly more accurate since it takes the feedback effects of device grounding and stabilization components into account.

If the design goal is to obtain maximum power transfer (maximum gain/minimum input VSWR), then the input of the INA-12063 is matched to Γ_{ms}. Γ_{ms} is the source impedance resulting from the simultaneous conjugate match of the input and output of the device. Since Γ_{ms} is only defined for devices/circuits with K > 1, the CAD circuit file from design Step 4, including any stabilizing resistors, is used to calculate Γ_{ms}.

For most communication systems operating over relatively small bandwidths, a single frequency match approach is usually adequate. As a general rule, the selection of high pass networks for the input (and output) matching circuits is desirable to reduce excess gain at low frequencies.

As a final note in the choice of the input matching structure, the use of a series C element is possible at the input of the INA-12063 since the internal bias circuit obviates the need for an external DC connection to the input.

The choice of using either lumped element or distributed (transmission line) matching elements is mainly dictated by size and frequency constraints as well as by cost considerations. While distributed elements are "free" since they are etched onto the PCB, they usually use more board space than an equivalent lumped element (chip) component.

Before proceeding to the next step, circuit stability and out-of-band gain should be re-checked.

Step 7. Designing the Output Match

The output of the INA-12063 is normally matched for maximum power transfer (maximum gain and lowest output VSWR.) Maximum power transfer occurs when the output is matched to the conjugate of Γ_{ml}. Γ_{ml} is computed from the same CAD circuit file as used for determining Γ_{ms} in the design of the input matching network in the previous step. A typical LNA is matched for Γ_{opt} at the input and Γ_{ml} at the output.

Note: The small signal match for maximum power transfer should not be confused with matching the output of the INA-12063 for the *highest* output power. As output power is increased, the device becomes nonlinear resulting in a shift away from the Γ_{ml} match. While various load pull types of measurements exist to determine the optimum impedance match for maximum output power under nonlinear conditions, these tests are fairly tedious and an empirical tuning approach is often more expedient to arrive at a solution. The Γ_{ml} match may be used as a starting point in tuning for maximum output power.

The same comments regarding single frequency match, high pass networks, and lumped vs. distributed elements referred to in the input matching step above are applicable to the output matching circuit.

Once again, out-of-band gain and stability should be checked.

Step 8. RF Layout

Up to this point, we have completed the RF electrical design, the choice of circuit board material, and the DC circuit. The next step is to lay out the printed circuit board. While the layout is not critical, some precautions should be considered.

A recommended PCB pad layout for the miniature SOT-363 (SC-70) package used by the INA-12063 is shown in Figure 12 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the INA-12063. The layout is shown with a footprint of a SOT-363 package superimposed on the PCB pads for reference.

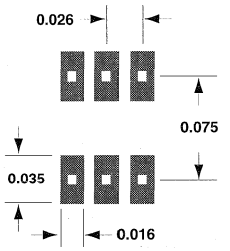


Figure 12. PCB Pad Layout for INA-12063 Package (dimensions in inches).

Starting with the package pad layout in Figure 12, an RF layout similar to the one in Figure 13 is suggested as a starting point for the INA-12063 amplifier.

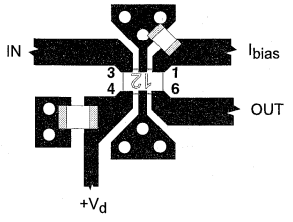


Figure 13. RF Layout.

This layout shows the direct grounding of Pin 5 (the device RF ground) which should be connected to ground through as short a path as practical, unless additional shunt feedback is desired. Capacitive bypasses should be placed on the DC connections at Pins 1 and 4 to prevent possible feedback and/or oscillation in the active bias circuit. Multiple vias are used to ensure good RF grounding.

It is recommended that the PCB pads for the two ground pins *not* be connected together. Each ground pin should have its own separate path to ground, otherwise, unintentional feedback could lead to potential instability in the RF transistor or internal bias circuit.

Step 9. Final CAD Analysis and Optimization

Following the completion of the amplifier electrical design and layout, it is advisable to do a final CAD analysis and circuit optimization. The analysis at this point will take into account such things as component parasitics (e.g., series L in chip caps), actual transmission line dimensions and interconnections, effects of ground vias, etc.

The circuit should be analyzed over the full range of the provided S-parameters to re-verify amplifier stability and ensure well-behaved out-of-band performance. With the full circuit parasitics and losses taken into account, it may be necessary to adjust the value of the shunt stabilizing resistor.

The results of this final analysis and optimization are then used to make final adjustments to component values and the PCB layout as

well as to ensure that the performance goals in Step 1 will be met.

Step 10. Build and Test
The final step is to fabricate circuit boards and assemble amplifiers for testing and verification of performance. Some adjustment in component values and transmission lines may be done at this step to allow for imperfections in the computer simulation. This completes the amplifier design.

900 MHz LNA Design Example
As an application example, the design of a low noise amplifier stage for 900 MHz using the INA-12063 will be described. This amplifier design would be representative for use in many low-cost, battery power receiver applications such as LNAs for cellular telephones or 900 MHz ISM/spread spectrum systems.

This example will follow the above design sequence.

1. Performance goals. As a receiver front end stage, the primary design goals for this example amplifier are: (1) noise figure less than 2 dB, and, (2) a input 3rd order intercept (IP_3) point of at least -10 dBm. Secondary goals are low output VSWR and minimum DC current drain. The resulting input VSWR and stage gain will be accepted. Low cost is always a design goal.

Results of this step:

Constrain:

NF ≤ 2 dB
Input IP_3 ≥ -10 dBm
Low cost

Optimize:

Minimize output VSWR
Minimize DC power

Accept:

Gain
Input VSWR

2. Select bias conditions. For this example, the supply voltage is constrained by an assumed battery supply of 3 volts, leaving device current as the only remaining bias variable. The current is selected based on output power which is driven by the IP_3 requirement. The table of Electrical Specifications provides a starting point. Using the typical gain of 16 dB and a difference of 15 dB between the output IP_3 and P_{1dB}, the design goal of an input 3rd order intercept point of -10 dBm is translated to a 1-dB compressed output power requirement of -9 dBm. Figure 8 indicates a current of 2.5 mA will meet this P_{1dB} requirement with adequate design margin.

Results of this step:

Bias: 3 volts, 2.5 mA

3. Choose PCB material. FR-4 with a thickness of 0.031 inches is chosen as the printed circuit board material. FR-4 meets the requirement of low cost while providing acceptable low loss performance at 900 MHz.

A thickness of 0.031 inches is suitable for the miniaturization of microstriplines and thin enough to allow for low inductance ground vias. With a relative dielectric constant (ε_r) of 4.8, the width of a 50 Ω microstripline on 0.031 inch FR-4 is 0.056 inches, which is a convenient size for mounting chip components.

Results of this step:

PCB Material: 0.031-inch FR-4

4. Evaluate stability. Stability factor is calculated from the set of S-parameters closest to the chosen bias condition, which in this example is 3 volts and 2.5 mA. For the required accuracy in the stability analysis, a short length of transmission line (0.030-inch long, 0.015-inch wide) is added to connect the RF ground pin (Pin 5) of the INA-12063 to a 0.025-inch diameter ground via.

Hewlett-Packard's *Touchstone* CAD program was used to calculate the stability factor (K), stability measure (B1), and gain over the full S-parameter frequency range of 0.1 to 3.1 GHz. The results show a value of K<1 at 900 MHz, corresponding the "Case 3" situation described in the stability discussion in design Step 4 above. To preserve NF, the stabilizing resistor, R1, shown in Figure 14, was added from the output of the INA-12063 to ground. Since the real part of the output impedance of the INA-12 is >50 Ω, a resistor in the shunt configuration is used to move the overall impedance closer to 50 Ω.

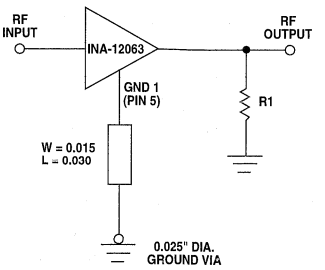


Figure 14. Stabilizing Resistor on Output.

The *Touchstone* circuit file for this step is shown in Figure 15.

```
DIM
  FREQ GHZ
  RES  OH
  LNG  IN
CKT
  MSUB ER=4.8 H=0.031
       T=0.001 RHO=1 RGH=0
  S2P  1  2  3  TYP25B.S2P
  MLIN 3  4  W=0.015 L=0.030
  VIA  4  0  D1=0.025
       D2=0.025 H=0.031
       T=0.001
  RES  2  0  R=600  ! R1
  DEF2P  1  2  INA12
TERM
   Z0 = 50
OUT
  INA12   K
  INA12   B1
  INA12   DB[S21]
  INA12   DB[GMAX]
!  INA12   MAG[GMN]
!  INA12   ANG[GMN]
!  INA12   MAG[GM2]
!  INA12   ANG[GM2]
FREQ
  SWEEP  0.1  3.1   0.1
```

Figure 15. CAD File for Stability Analysis and Conjugate Match.

The value of the shunt resistor, R1, is varied while observing the resulting K. While a 600 Ω resistor is found to stabilize the circuit at 900 MHz (K=1.46), there still exists a possibility of oscillation at 100 MHz with the worst case value of K = 0.72. There are two options at this point: (a) lower the value of the shunt resistor, which trades additional stability for circuit gain and output power, or (b) use a frequency selective circuit to resistive load the device only at lower frequencies.

In the interest of circuit simplicity (meeting the objective of low cost) the shunt resistor value was lowered to 290 Ω. This value resulted in a K > 1 over the full frequency range at a trade-off in gain of 1.7 dB. (The stability measure criteria, B1 > 0, was also verified.)

Results of this step:

A 290 Ω shunt resistor was added to the output of the INA-12063 for stability.

5. Allow for DC connections. The required DC connections to be made to this example amplifier are: +3 volts to the RF Output and V_d terminals (Pins 4 & 6), a suitable bias current into I_{bias} (Pin 1), and Pins 2 and 5 to ground. The RF Input (Pin 3) and RF Output should have blocking capacitors if the amplifier is to be cascaded with stages that do not have a DC open circuit.

To set the INA-12063 operating current to 2.5 mA, a 9.1 KΩ resistor will be connected between the +3 volt supply and the I_{bias} pin. The DC schematic for the LNA is shown in Figure 16.

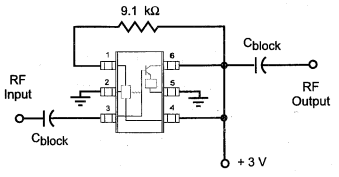


Figure 16. 900 MHz LNA DC Schematic.

Results of this step:

The DC connections were identified and will be considered in choosing the input & output matching circuits.

6. Design of the input impedance matching network. Commensurate with the primary design objective of low noise figure, the 50 Ω input to the amplifier stage will be matched to the conjugate of Γ_{opt}. The value of Γ_{opt}, 0.53 ∠+36°, is found in the table of Typical Noise Parameters for a bias current of 2.5 mA. (Alternatively, a slightly more accurate Γ_{opt} could also have been calculated using the CAD circuit file in Figure 15, which includes the RF ground parasitics and stabilizing resistor.) The conjugate of Γ_{opt}, 0.53 ∠–36°, is plotted on the Smith chart as Point A in Figure 17. Since Point A is not sufficiently close to the R=1 or G=1 circles on the Smith chart, a single series or shunt element will not provide an exact match. (For less critical NF performance, a simple series inductor would be adequate for the input match.) A two-element matching network will therefore be required.

Impedances in this region of the Smith chart can be matched to 50 Ω by either of two possible L-C combinations, either a shunt C-series L or a shunt L-series C. Normally, the shunt L-series C would be a good choice since its high pass filter characteristic would help roll off excess low end gain. However, a DC blocking capacitor would be required between the INA-12063 and the matching network. Placing extraneous components within matching network is usually not recommended. The shunt C-series L network is therefore chosen as the input matching topology.

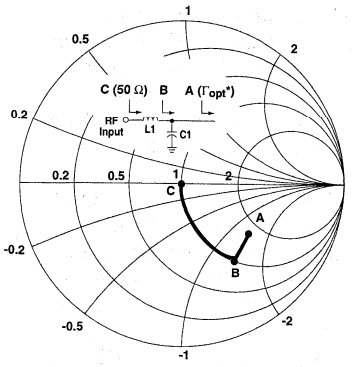


Figure 17. Input Impedance Match.

As shown in Figure 17, a shunt capacitor of 0.59 pF will move Γ_{opt} * at Point A to a position on the unit conductance circle (G=1) at Point B. A 11.2 nH series inductor then completes the match to 50 Ω by moving the impedance at Point B to the center of the chart.

The value of the shunt capacitor is small enough that a short length of open-circuit transmission line could be used in place of the lumped element capacitor. This saves the expense of a chip component with the tradeoff of a small amount of additional circuit board space. A 0.20-inch length of open-circuit 50 Ω line is one choice that would be equivalent to the 0.59 pF shunt capacitor. The input matching circuit is shown in Figure 19.

Results of this step:

The input circuit is:

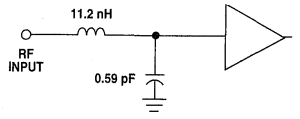


Figure 18. Input Circuit.

7. Design of the output impedance matching network. Using the circuit file from step 4 (Figure 15), *Touchstone* was used to calculate the load impedance Γ_{ml} (0.62 ∠+35°) of the INA-12063 to achieve maximum power transfer. The conjugate of Γ_{ml}, Γ_{ml}* (0.62 ∠-35°), is plotted as Point A on the Smith chart in Figure 19.

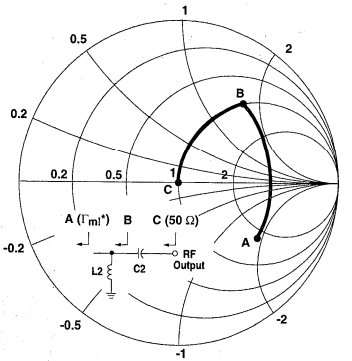


Figure 19. Output Impedance Match.

The two possible L-C networks that can be used to match Γ_{ml}* to 50 Ω are either a shunt C-series L or a shunt L-series C circuit. By choosing the shunt L-series C circuit, two of the DC considerations from Step 5 can be satisfied: the shunt L can be bypassed and used to apply the +3 volt supply to the RF output terminal, and the series C will serve double duty as the DC blocking capacitor.

Referring again to Figure 19, a shunt inductance of 10.8 nH moves Γ_{ml}* at Point A to Point B which is on the G1 circle of the Smith chart. The addition of 1.9 pF of series capacitance completes the impedance transformation to Point C at the center of the chart. The output matching circuit is shown in Figure 20.

Results of this step:

The output circuit is:

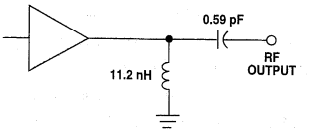


Figure 20. Output Circuit.

The circuit values from this step and from Step 6 will be used as a starting point to be refined in Step 9 when the circuit is expanded to take practical interconnections and parasitics into account.

8. PCB Layout. The results of the preceding steps and the PCB layout guidelines in design Step 8 were used to draft the circuit board layout shown in Figure 21. Since parasitic effects are minimal, the current source resistor, R2, can be conveniently placed directly from the RF output to the I_{bias} connection. A bypass capacitor is added to the shunt stabilizing resistor, R1 and matching inductor, L2, on the output. A DC blocking capacitor, C1, is included at the input to complete the amplifier.

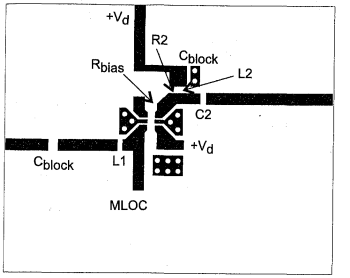


Figure 21. PCB Layout of 900 MHz LNA.

Results of this step:

PCB layout completed.

9. Final CAD simulation and optimization. With reference to Figure 21 the CAD circuit file from step 4 is embellished to include the effects of component mounting pads, lengths of transmission lines used to interconnect components, ground vias, bypass and blocking capacitors, etc. (Since 900 MHz is a fairly moderate frequency, extremely fine detail is not required.)

Using the previous element values for the matching circuits as a starting point, *Touchstone* was used to optimize the circuit for noise figure and output match, which were the primary design goals from Step 1. The input and output matching elements were used as variables for the optimization. Following the optimization, the value of the stabilizing resistor, R1, was also reviewed and it was found that an increase to 330 Ω was sufficient to make K>1 over the entire frequency range of the S-parameters. The *Touchstone* circuit file for the complete amplifier is shown in Appendix A and the simulation results in Appendix B.

The schematic for the complete INA-12063 amplifier circuit is shown in Figure 22.

A final simulation using optimized component values predicted performance of the amplifier at 900 MHz to be:

NF = 1.6 dB
Gain = 13.4 dB
MAG = 14.1 dB
Input RL = 8.4 dB
Output RL = 31 dB

Results of this step:

Optimization of circuit and verification of performance goals.

10. Assemble and test. A circuit based on the PCB layout was assembled using components with standard values that were closest to those resulting from the circuit optimization.

The test results compared well with the computer simulations from the previous step. For this particular circuit, it was determined experimentally that less shunt capacitance was required at the input than predicted by the CAD analysis. As a result, the shunt, open circuit stub near Pin 3 was shortened to tune the circuit for minimum noise figure. The final LNA is shown in Figure 23.

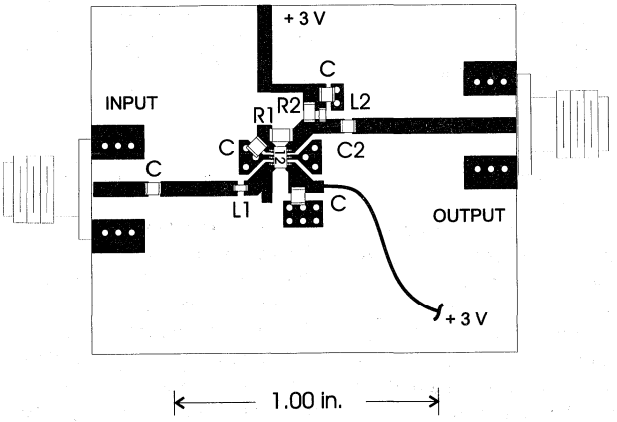


Figure 23. Completed 900 MHz LNA.

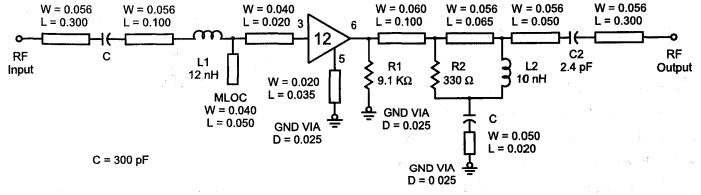


Figure 22. 900 MHz Amplifier Schematic.

Actual, measured test results are shown in Figures 24 through 28. Output power for 1 dB of gain compression (P_{1dB}) at 900 MHz was measured as -4.6 dBm.

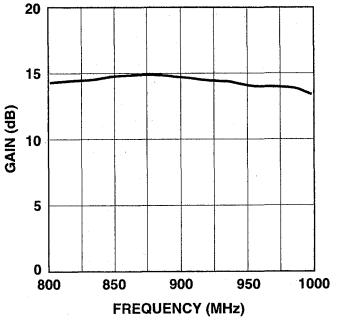


Figure 24. Measured Gain of Example 900 MHz LNA.

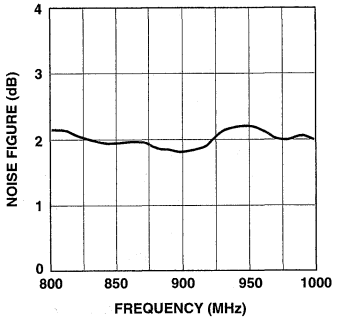


Figure 25. Measured Noise Figure of Example 900 MHz LNA.

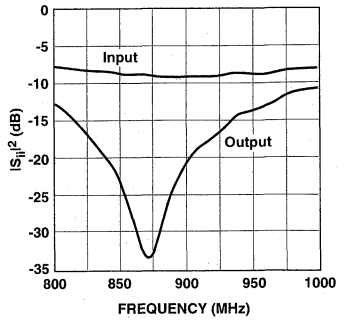


Figure 26. Measured Input and Output Return Loss of Example 900 MHz LNA.

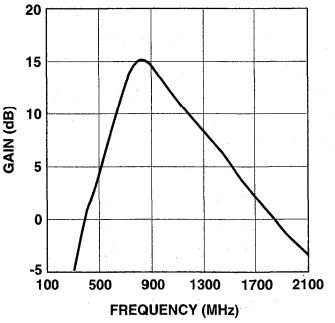


Figure 27. Measured Gain of Example 900 MHz LNA for Extended Frequency.

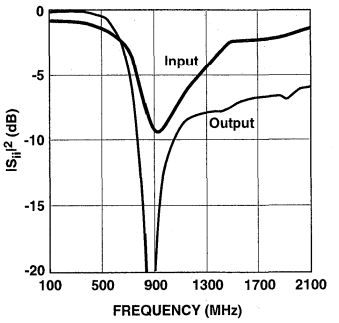


Figure 28. Measured Input and Output Return Loss of Example 900 MHz LNA for Extended Frequency.

Results of this step:
A prototype circuit was built and performance goals verified by measurement. The following 900 MHz data was measured on the example LNA:

NF = 1.9 dB
Gain = 14.7 dB
P_{1dB} (output) = -4.6 dBm
Input Return Loss = 9.6 dB
(Input VSWR = 2.0 : 1)
Output Return Loss = 20.4 dB
(Output VSWR = 1.2 : 1)
DC Power = 8 mW
(3 volts, 2.55 mA)

Hints and Troubleshooting

• Oscillation

Even though a design may be unconditionally stable (K > 1 and B1 > 0) over its full frequency range, other possibilities exist that may cause an amplifier circuit to oscillate. One thing to look for, is oscillation in bias circuits. It is important to capacitively bypass the connections to active bias circuits to ensure stable operation. In multistage circuits, feedback through bias lines can also lead to oscillation.

Components of insufficient quality for the frequency range of the amplifier can sometimes lead to instability. Also, component values that are chosen to be much higher in value than is appropriate for the application can present a problem. In both of these cases, the components may have reactive parasitics that make their impedances very different than expected. Chip capacitors may have excessive inductance, or chip inductors can exhibit resonances at unexpected frequencies.

In systems with high gain cascades, another possible feedback path that could lead to oscillation is radiation. Feedback via radiation is most frequently encountered in situations where a large cavity housing is used in combination with multiple gain stages. One solution to minimizing radiation feedback is to design the housing so that it is well below its equivalent waveguide cutoff frequency. Another solution is to use shielding to partition the gain.

• A Note on Supply Line Bypassing

When multiple bypass capacitors are used throughout the power supply lines in a wireless system, consideration should be given to potential resonances. It is important to ensure that the capacitors, when combined with additional parasitic L's and C's on the circuit board, do not form resonant circuits. The addition of a small value resistor in the bias supply line between bypass capacitors will often "de-Q" the bias circuit and eliminate resonance effects.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-363 package, will reach solder reflow temperatures faster than those with a greater mass.

The INA-12063 is has been qualified to the time-temperature profile shown in Figure 29. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235°C.

These parameters are typical for a surface mount assembly process for the INA-12063. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

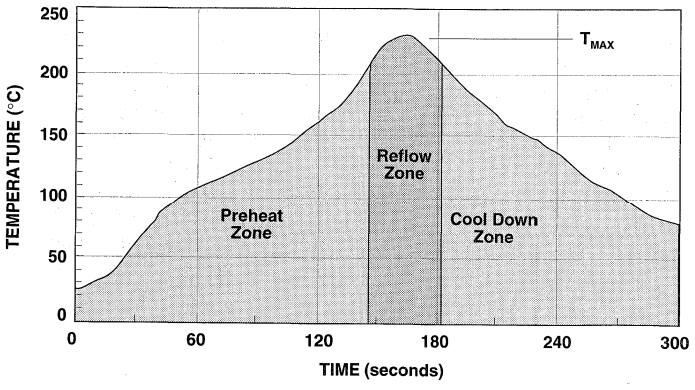


Figure 29. Surface Mount Assembly Profile.

Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either minimum or maximum, "typical," or standard deviations.

The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on of a minimum of 500 parts taken from 3 non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard bell curve.

Parameters considered to be the most important to system performance are bounded by *minimum* or *maximum* values. For the INA-12063, these parameters are: Power Gain ($|S_{21}|^2$), Noise Figure (NF), and Device Current. Each of these guaranteed parameters is 100% tested.

Values for most of the parameters in the table of Electrical Specifications that are described by *typical* data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as S-parameters or Noise Parameters and the performance curves, the data represents a nominal part taken from the center of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate circuit using the INA-12063, but to also optimize and evaluate trade-offs that affect a complete wireless system, the *standard deviation* (σ) is provided for many of the Electrical Specifications parameters (at 25°C) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean. Referring to Figure 30 for example, the probability of a parameter being between $\pm 1\sigma$ is 68.3%; between $\pm 2\sigma$ is 95.4%; and between $\pm 3\sigma$ is 99.7%.

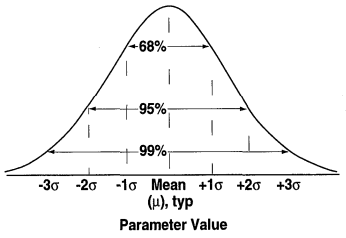


Figure 30. Normal Distribution.

Phase Reference Planes

The positions of the reference planes used to specify S-parameters and Noise Parameters for the INA-12063 are shown in Figure 31. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

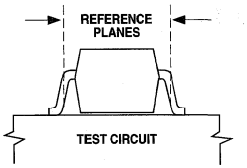


Figure 31. Phase Reference Planes.

Test Circuits

The test circuit shown in Figure 32 is used for 100% testing of the guaranteed RF and DC parameters that are shown in the Table of Electrical Specifications.

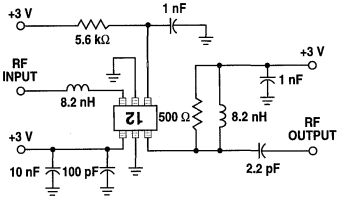


Figure 32. 900 MHz Test Circuit.

The test circuits in Figures 32 and 33 were used to generate the characterization data and performance curves for 900 MHz and 250 MHz.

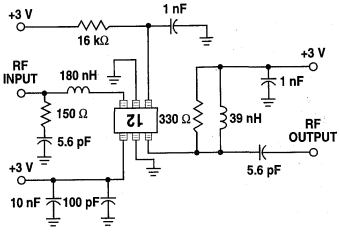


Figure 33. 250 MHz Test Circuit.

Electrostatic Sensitivity

RFICs are electrostatic discharge (ESD) sensitive devices. Although the INA-12063 is robust in design, permanent damage may occur to these devices if they are subjected to high energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without detection and may result in degradation in performance, reliability, or failure.

Electronic devices may be subjected to ESD damage in any of the following areas:

- Storage and handling
- Inspection and testing
- Assembly
- In-circuit use

The INA-12063 is a ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, testing, assembling, and using these devices to avoid damage.

The in-use aspect of potential ESD damage is sometimes overlooked. One such example of possible damage is in the use of an ESD sensitive device as the front-end LNA stage in personal communication equipment, such as cellular telephones, PCS, or RF modems.

The input to receiver LNAs are frequently connected to external antennas that are subject to human contact and exposure to other potentially damaging levels of ESD. If this type of condition exists, some type of circuit protection may be needed. One simple method of preventing ESD damage is to add a DC return path (e.g., a shunt inductor) to the input of the receiver. This type of protection may be integrated into other parts of the receiver front end, such as in a T/R switch, filter, or the input matching network to the LNA.

Appendix A - *Touchstone* Circuit File.

```
! Hewlett-Packard CMCD
!  Bob Myers       20 Sept 1996
!
! HP Touchstone circuit file
! INA-12063 Single Stage LNA
!     fc = 900 MHz, Vc = 3.0 V, Ic = 2.5 mA
!     Input Matched for NF

DIM
   FREQ GHZ
   RES  OH
   CAP  PF
   IND  NH
   LNG  IN
   ANG  DEG

VAR
! Input match
   L1#  0   12.6477      20
   A1#  0    0.201808     0.4              ! Length of MLOC
!  C1#  0    0.636904    10
! Output match
   L2#  0    9.25249     20
   C2#  0    2.56665     10

CKT
   MSUB   ER=4.8  H=0.031  T=0.001  RHO=1  RGH=0
   MLIN   1    2    W=0.056  L=0.300
   CAP    2    3    C=300           ! Input DC block
   MLIN   3    4    W=0.056  L=0.100
   IND    4    5    L^L1            ! L1 in Input match
   MLOC   5       W=0.04  L^A1      ! Z1 in Input match
!  CAP    5    0    C^C1            ! Alternate shunt C
   MLIN   5    6    W=0.04   L=0.020
   S2P    6    7    8     C:\SPARA\A120633B.S2P
   RES    7    0    R=9100          ! R1 bias resistor
   MLIN   8    9    W=0.020  L=0.035       ! Z2 in RF ground
   VIA    9    0    D1=0.025  D2=0.025  H=0.031  T=0.0015  W=0.04
   MLIN   7    10   W=0.06   L=0.100
   RES    10   12   R=330           ! R2 Stabilizing R
   MLIN   10   11   W=0.056  L=0.065
   IND    11   12   L^L2            ! L2 in Output match
   MLIN   11   15   W=0.056  L=0.050
   CAP    12   13   C=300           ! Bypass C
   MLIN   13   14   W=0.050  L=0.020
   VIA    14   0    D1=0.025  D2=0.025  H=0.031  T=0.001  W=0.04
   CAP    15   16   C^C2            ! C2 in Output match
   MLIN   16   17   W=0.056  L=0.300
   DEF2P  1    17   INA12

TERM
   Z0 = 50

OUT
   INA12   NF         GR3
   INA12   DB[S21]    GR1
   INA12   DB[S11]    GR2
   INA12   DB[S22]    GR2
   INA12   DB[GMAX]   GR1
```

```
   INA12   K                ! Stability factor (K > 1)
   INA12   B1               ! Stability Measure (B1 > 0)

FREQ
   SWEEP  0.1  3.1   0.02

GRID
   FREQ  0.8   1.0   0.05
!  FREQ  0.1   3.1   0.1
   GR1   0    20     5              ! Gain
   GR2   0   -40     10             ! Return loss
   GR3   0     4     1              ! NF

OPT
   FREQ   0.85   0.95
   INA12  NF<1.6      5
   INA12  DB[S22]<-20 1
```

Appendix B – *Touchstone* Output File.

FREQ GHZ	NF INA12	DB[S21] INA12	DB[S11] INA12	DB[S22] INA12	DB[GMAX] INA12	K INA12	B1 INA12
0.1	11.178	-43.253	-0.913	0.000	5.717	109.193	0.000
0.2	9.706	-13.998	-1.070	-0.005	22.248	1.404	0.002
0.3	8.725	-4.922	-1.429	-0.027	22.535	1.094	0.010
0.4	7.627	1.602	-1.843	-0.111	21.559	1.071	0.036
0.5	6.366	6.760	-2.947	-0.418	18.878	1.295	0.108
0.6	4.929	11.048	-4.674	-1.404	17.490	1.414	0.287
0.7	3.388	13.713	-7.101	-4.424	16.155	1.569	0.634
0.8	2.048	14.210	-8.450	-11.782	15.081	1.656	0.957
0.9	1.588	13.289	-7.910	-35.279	14.143	1.813	1.104
1.0	2.490	11.823	-6.677	-14.634	13.285	1.926	1.161
1.1	4.284	10.309	-5.483	-11.002	12.521	2.018	1.198
1.2	6.292	8.776	-4.459	-8.998	11.836	2.122	1.223
1.3	8.193	7.440	-3.727	-7.952	11.221	2.230	1.237
1.4	9.918	6.113	-3.076	-7.141	10.708	2.259	1.248
1.5	11.469	4.870	-2.611	-6.578	10.169	2.287	1.249
1.6	12.868	3.720	-2.221	-6.221	9.663	2.369	1.256
1.7	14.146	2.647	-1.900	-5.875	9.243	2.416	1.254
1.8	15.317	1.637	-1.646	-5.602	8.885	2.370	1.252
1.9	16.402	0.728	-1.440	-5.414	8.558	2.317	1.252
2.0	17.415	-0.174	-1.265	-5.222	8.233	2.288	1.247
2.1	18.367	-1.007	-1.124	-5.024	7.924	2.279	1.236
2.2	19.264	-1.850	-1.011	-4.905	7.498	2.344	1.231
2.3	20.112	-2.453	-0.912	-4.871	7.307	2.285	1.237
2.4	20.927	-3.275	-0.815	-4.736	7.002	2.299	1.229
2.5	21.700	-3.842	-0.737	-4.665	6.926	2.116	1.228
2.6	22.446	-4.446	-0.672	-4.546	6.747	2.039	1.217
2.7	23.162	-5.015	-0.615	-4.528	6.521	1.978	1.220
2.8	23.861	-5.656	-0.566	-4.345	6.252	1.975	1.195
2.9	24.530	-6.216	-0.523	-4.338	5.870	2.103	1.198
3.0	25.179	-6.619	-0.475	-4.171	6.107	1.889	1.177
3.1	25.811	-7.041	-0.442	-4.077	6.024	1.760	1.164

Results of computer simulation of optimized 900 MHz LNA.

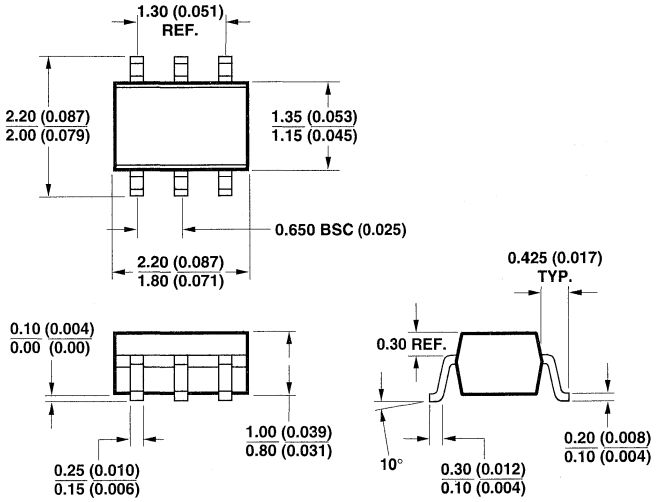
[1] U.S. Patent Number 5436595

INA-12063 Part Number Ordering Information

Part Number	Devices per Container	Container
INA-12063-TR1	3000	7" reel
INA-12063-BLK	100	tape strip in antistatic bag

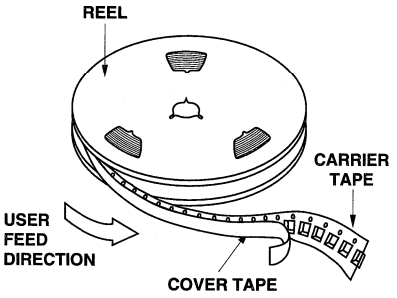
Package Dimensions

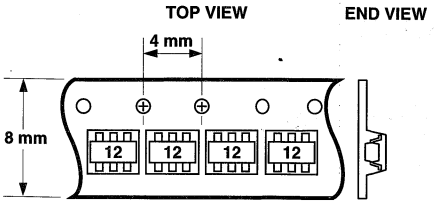
Outline 63 (SOT-363/SC-70)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

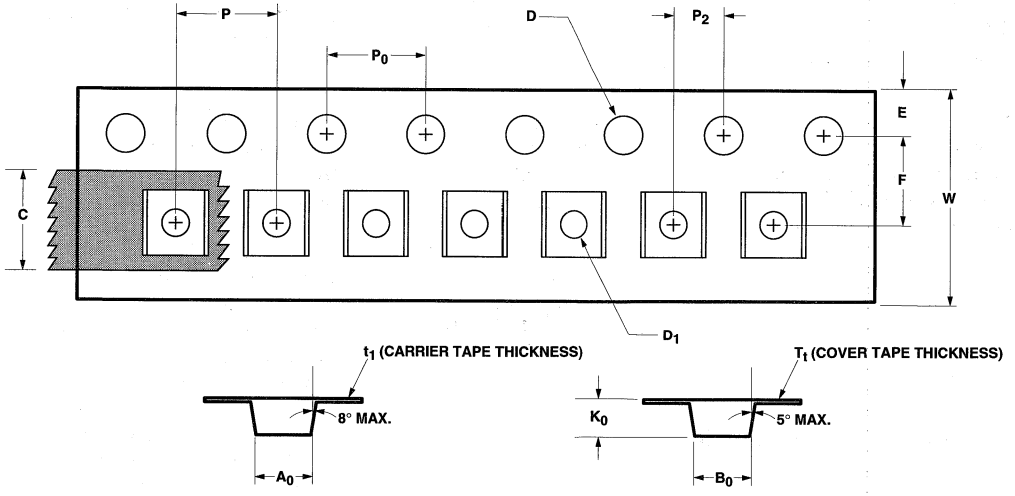
Device Orientation





Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

1 GHz Low Noise Silicon MMIC Amplifier

Technical Data

INA-30311

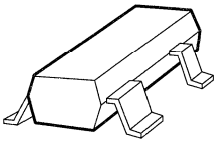
Features

- **Internally Biased, Single 3 V Supply (6 mA)**
- **3.5 dB NF**
- **13 dB Gain**
- **Unconditionally Stable**

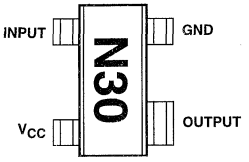
Applications

- **LNA or IF Amplifier for Cellular, Cordless, Special Mobile Radio, PCS, ISM, and Wireless LAN Applications**

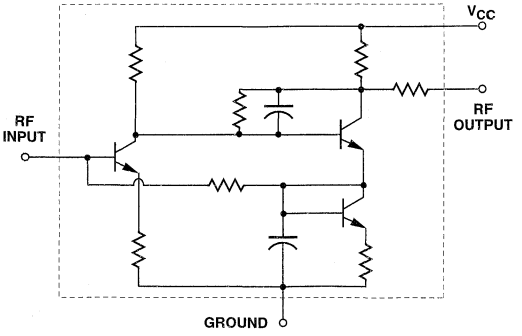
SOT-143 Surface Mount Package



Pin Connections and Package Marking



Equivalent Circuit (Simplified)



Description

Hewlett-Packard's INA-30311 is a Silicon monolithic amplifier for applications to 1.0 GHz. Packaged in a miniature SOT-143 package, it requires very little board space.

The INA-30311 uses an internally biased topology which eliminates the need for external components and provides decreased sensitivity to ground inductance.

The INA-30311 is designed with an output impedance that varies from near 200 Ω at low frequencies to near 50 Ω at higher frequencies. This provides a matching advantage for IF circuits, as well as improved power efficiency, making it suitable for battery powered designs.

The INA-30311 is fabricated using HP's 30 GHz f_{MAX} ISOSAT™ Silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metallization, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity, and reliability.

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{CC}	Device Voltage, to ground	V	12
P_{in}	CW RF Input Power	dBm	+13
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{j-c} = 550°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

INA-30311 Electrical Specifications[3], $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 3$ V

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G_p	Power Gain ($\|S_{21}\|^2$)	f = 900 MHz	dB	11	13	
NF	Noise Figure	f = 900 MHz	dB		3.5	
P_{1dB}	Output Power at 1 dB Gain Compression	f = 900 MHz	dBm		-11	
IP_3	Third Order Intercept Point	f = 900 MHz	dBm		-2	
VSWR	Input VSWR	f = 900 MHz			1.7	
I_{cc}	Device Current		mA		6.3	7.5
t_d	Group Delay	f = 900 MHz	ps		325	

INA-30311 Typical Scattering Parameters[3], $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 3$ V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	Factor
0.05	0.09	-1	16.12	6.40	-6	-38.1	0.012	2	0.57	-1	4.35
0.10	0.09	-2	16.11	6.39	-12	-38.2	0.012	4	0.56	-3	4.43
0.20	0.10	-6	16.12	6.40	-25	-38.4	0.012	8	0.56	-7	4.41
0.30	0.13	-16	16.14	6.41	-38	-38.9	0.011	13	0.55	-11	4.83
0.40	0.16	-29	16.07	6.36	-52	-39.4	0.011	19	0.54	-14	4.88
0.50	0.18	-42	15.90	6.24	-66	-40.1	0.010	27	0.52	-18	5.60
0.60	0.21	-59	15.56	6.00	-81	-40.7	0.009	40	0.50	-20	6.58
0.70	0.22	-75	15.04	5.65	-95	-40.7	0.009	57	0.47	-23	7.26
0.80	0.24	-92	14.34	5.21	-109	-39.6	0.011	74	0.46	-24	6.49
0.90	0.25	-107	13.44	4.70	-122	-37.6	0.013	86	0.44	-24	6.23
1.00	0.26	-122	12.53	4.23	-135	-35.5	0.017	94	0.43	-25	5.35
1.20	0.27	-144	10.50	3.35	-155	-32.3	0.024	100	0.42	-26	4.83
1.40	0.27	-162	8.50	2.66	-173	-29.6	0.033	101	0.42	-27	4.43
1.60	0.27	-177	6.69	2.16	172	-27.5	0.042	100	0.42	-28	4.31
1.80	0.27	173	5.01	1.78	159	-25.7	0.052	99	0.42	-30	4.22
2.00	0.27	163	3.58	1.51	147	-24.1	0.062	97	0.42	-32	4.17
2.20	0.27	156	2.35	1.31	136	-22.5	0.075	95	0.42	-35	3.97
2.40	0.26	150	1.21	1.15	126	-21.4	0.085	92	0.41	-37	4.04
2.50	0.26	147	0.75	1.09	122	-20.9	0.091	91	0.41	-39	3.99

Note:
3. Reference plane per Figure 9 in Applications Information section.

INA-30311 Typical Performance, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 3\ V$

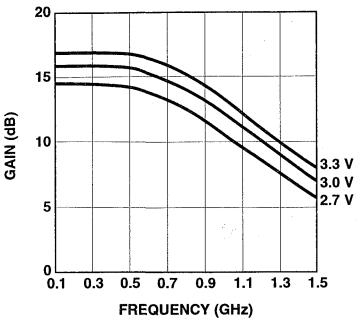


Figure 1. Power Gain vs. Frequency and Voltage.

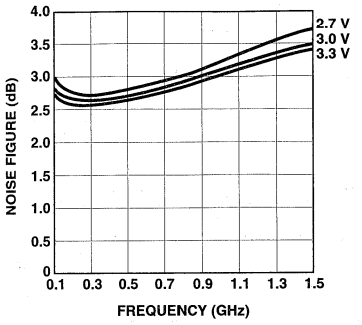


Figure 2. Noise Figure vs. Frequency and Voltage.

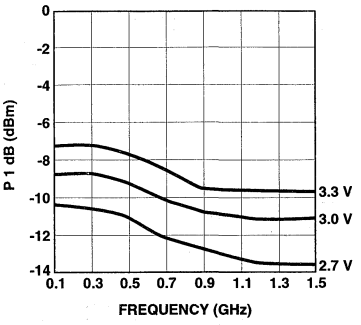


Figure 3. Output Power for 1 dB Gain Compression vs. Frequency and Voltage.

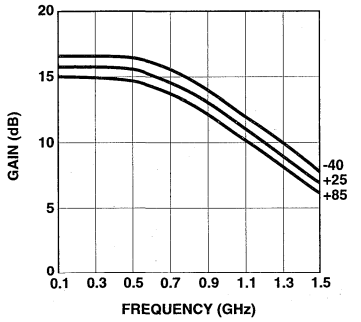


Figure 4. Gain vs. Frequency and Temperature.

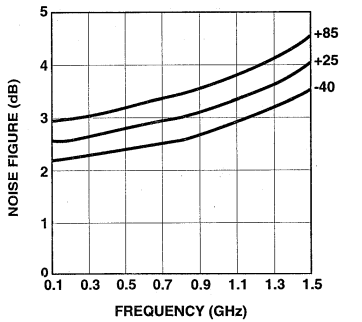


Figure 5. Noise Figure vs. Frequency and Temperature.

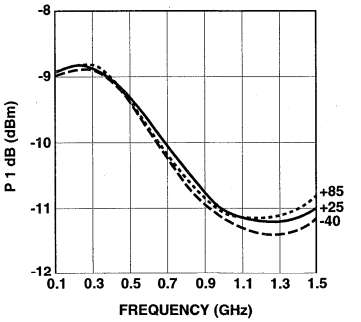


Figure 6. Output Power for 1 dB Gain Compression vs. Frequency and Temperature.

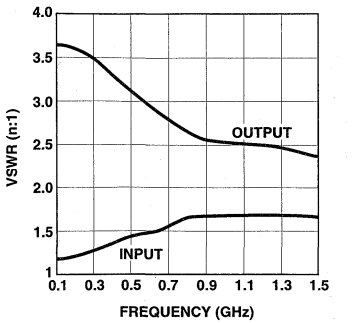


Figure 7. Input and Output VSWR vs. Frequency.

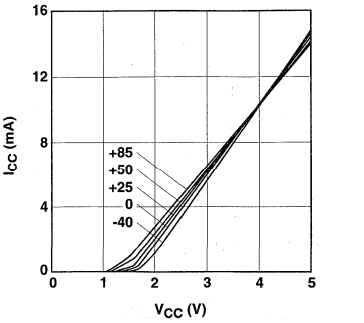


Figure 8. Supply Current vs. Voltage and Temperature.

INA-30311 Applications Information

Introduction

The INA-30311 is a silicon RF integrated circuit that provides an easy-to-use solution for low noise or multi-purpose gain block applications up to 1000 MHz. This two-stage amplifier design uses resistive feedback to provide flat gain over a wide frequency range. This device is assembled in a miniature, surface mount package and is intended for use in low cost wireless communication products.

A unique feature of the INA-30311 is that it is designed with a 50 Ω input impedance and an output impedance that approaches 200 Ω at lower frequencies. This impedance converting feature is very useful for applications such as receiver IF circuits in which the INA-30311 is followed by high input impedance devices like signal processing circuits, filters, or mixed signal ICs.

In addition to simplifying the match to higher impedance devices, a key benefit of the higher output impedance feature is an improvement in power efficiency.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters are shown in Figure 9. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

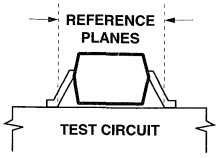


Figure 9. Reference Planes.

Biasing

The INA-30311 is a voltage biased device and operates from a single +3 volt power supply. With a current drain of 6 mA, this amplifier is suitable for use in battery powered applications. All bias circuitry is fully integrated into the IC eliminating the need for external DC components. RF performance is very stable for 3-volt battery supplies that may range from 2.7 to 3.3 volts, depending on battery "freshness" or state of charge in the case of rechargeable batteries.

While the INA-30311 was designed for use in +3 volt battery powered applications, the internal bias regulation circuitry allows it to be used with any power supply voltage from +2.7 to +5 volts.

Typical Configurations

The way in which the INA-30311 is used depends on the particular application and operating frequency.

- For receiver IF amplifier applications up to several hundred MHz, the relatively higher output impedance level of the INA-30311 may be used to advantage when interfacing directly with devices having higher than 50 Ω input impedances, such as certain signal processing or mixed signal ICs. This application is shown in Figure 10.

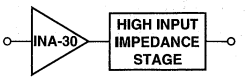


Figure 10. INA-30311 Driving a High Input Impedance Stage.

- A second implementation, shown in Figure 11, uses a simple reactive network at the amplifier's output to match the output impedance to 50 Ω.

This matched output arrangement will provide an additional 0.9 dB of gain and output power at 900 MHz when driving into a 50 Ω stage.

- The third way to use the INA-30311 is to simply cascade several INA-30311's with 50 Ω stages and neglect the effects of the output mismatch.

The 50 Ω cascade without impedance matching, shown in Figure 12, trades off the improvement in stage gain and output power for a more simplified interstage circuit and reduced circuit board space.

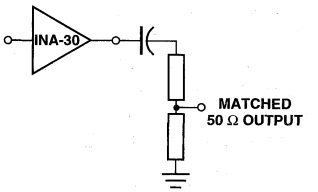


Figure 11. Impedance Matched Output.

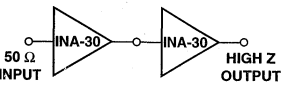


Figure 12. Simple Cascade without Impedance Matching.

Operating Details

The basic application of the INA-30311 is shown in Figure 13. DC blocking capacitors should be placed in series with the RF Input and RF Output to isolate adjoining circuits from the internal bias voltages that are present at these terminals. The values of the blocking capacitors are determined by the lowest frequency of operation for a particular application. The capacitor's reactances are chosen to be 5% or less of the amplifier's input or output impedance at the lowest operating frequency. For example, an amplifier to be used in an application covering the 902 to 928 MHz band would require an input blocking capacitor of at least 70 pF, which is 2.5 Ω of reactance, or 5% of 50 Ω at 902 MHz.

The V_{CC} connection to the amplifier must be RF bypassed by placing a capacitor to ground directly at the bias pin of the package. Like the DC blocking capacitors, the value of the V_{CC} bypass capacitor is determined by the lowest operating frequency for the amplifier. This value is typically the same as that of the DC blocking capacitors. If long bias lines are used to the amplifier to the V_{CC} supply, additional bypass capacitors may be needed to prevent resonances that would otherwise result in undesirable gain responses. A well-bypassed V_{CC} line is also desirable to prevent possible oscillations that may occur due to feedback through the bias line from other stages in a cascade.

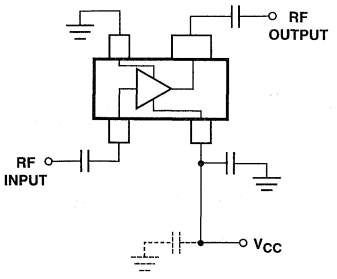


Figure 13. Basic Amplifier Application.

Adequate grounding is needed to obtain maximum performance. The ground pin of the INA-30311 should be connected to directly to RF ground by using plated through holes (vias) near the package terminals.

FR-4 or G-10 PCB material is a good choice for most low cost wireless applications. Typical board thickness is 0.025 or 0.031 inches. The width of 50 Ω microstriplines in these PCB thicknesses is also convenient for mounting chip components such as the series DC blocking capacitors.

50 Ω Example

The demonstration circuit in Figure 14 shows the INA-30311 used without output impedance matching and is an example of the cascade depicted in Figure 12. This layout illustrates the simplest implementation of the INA-30311 by using 50 Ω microstriplines with DC blocking capacitors for both the input and output. The V_{CC} supply connection is RF bypassed very close to the lead of the RFIC. Provision is also made for an additional bypass capacitor on the V_{CC} line near the edge of the PCB.

900 MHz Matched Example

This section describes a demonstration circuit for 900 MHz that is based on the matched output configuration shown in Figure 11.

The output VSWR of the INA-30311 is approximately 2.6:1 at 900 MHz and results in a 0.9 dB mismatch loss when used in a 50 Ω system. The use of a simple impedance matching circuit at the output will increase both gain and output power by 0.9 dB. The noise figure of the amplifier remains the same and does not depend on whether or not the output is matched.

There are many circuit topologies that may be used to match the output impedance of the INA-30311 to a 50 Ω load. The example presented in Figure 15 is designed to match the amplifier's output for frequencies near 900 MHz.

This circuit is representative for applications in the 800 MHz cellular or 900 MHz unregulated frequency bands. This example uses a series capacitor to resonate with a shunt, high impedance transmission line. The transmission line is tapped at a 50 Ω level for the output. This circuit provides the desired impedance transformation with a minimum of components, using only one chip capacitor that also doubles as the output DC block.

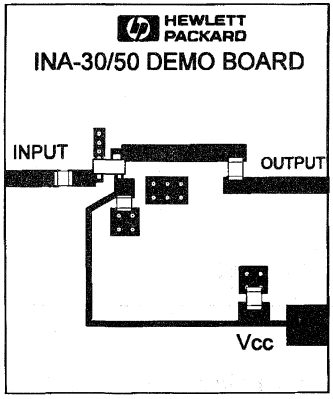


Figure 14. 50 Ω Input/Output Example.

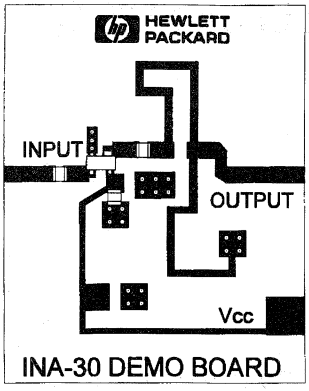
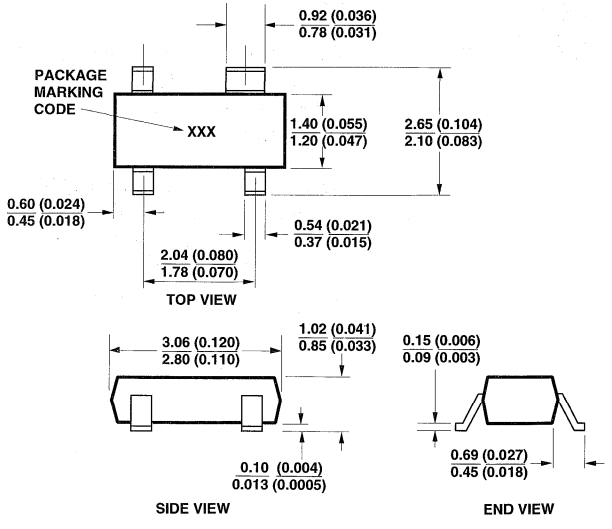


Figure 15. Matched Output Example.

INA-30311 Part Number Ordering Information

Part Number	Devices per Container	Container
INA-30311-TR1	3,000	7" reel
INA-30311-BLK	100	Antistatic bag

Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

1 GHz Low Noise Silicon MMIC Amplifier

Technical Data

INA-50311

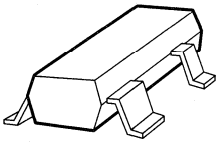
Features

- **Internally Biased, Single 5 V Supply (17 mA)**
- **19 dB Gain**
- **3.6 dB NF**
- **Unconditionally Stable**

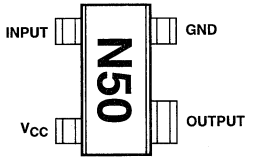
Applications

- **Amplifier for Cellular, Cordless, Special Mobile Radio, PCS, ISM, Wireless LAN, and TV Tuner Applications**

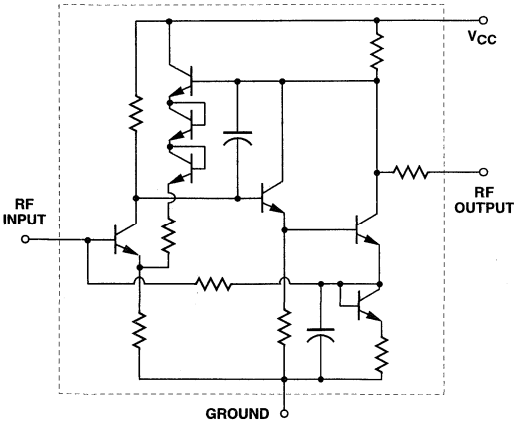
SOT-143 Surface Mount Package



Pin Connections and Package Marking



Equivalent Circuit (Simplified)



Description

Hewlett-Packard's INA-50311 is a Silicon monolithic amplifier that offers excellent gain and noise figure for applications to 1.0 GHz. Packaged in a miniature SOT-143 package, it requires very little board space.

The INA-50311 uses a topology which is internally biased, eliminating the need for external components and providing decreased sensitivity to ground inductance.

The INA-50311 is fabricated using HP's 30 GHz f_{MAX} ISOSAT™ Silicon bipolar process which uses nitride self-alignment sub-micrometer lithography, trench isolation, ion implantation, gold metallization, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity, and reliability.

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{CC}	Device Voltage, to ground	V	12
P_{in}	CW RF Input Power	dBm	+13
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{jc} = 550°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

INA-50311 Electrical Specifications[3], $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 5\ V$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G_p	Power Gain ($\|S_{21}\|^2$)	f = 900 MHz	dB	16.5	19	
NF	Noise Figure	f = 900 MHz	dB		3.6	
P_{1dB}	Output Power at 1 dB Gain Compression	f = 900 MHz	dBm		0	
IP_3	Third Order Intercept Point	f = 900 MHz	dBm		+10	
VSWR	Input VSWR	f = 900 MHz			1.5	
	Output VSWR	f = 900 MHz			1.2	
I_{cc}	Device Current		mA		17	22
ι_d	Group Delay	f = 900 MHz	ps		320	

INA-50311 Typical Scattering Parameters[3], $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 5\ V$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	Factor
0.05	0.12	-2	22.2	12.82	-6	-31.9	0.025	5	0.08	-11	1.68
0.10	0.12	-5	22.2	12.81	-12	-31.7	0.026	9	0.07	-24	1.63
0.20	0.12	-10	22.1	12.80	-24	-31.4	0.027	16	0.07	-44	1.59
0.30	0.14	-16	22.1	12.68	-36	-31.1	0.028	23	0.08	-62	1.55
0.40	0.15	-25	21.9	12.45	-49	-30.6	0.030	30	0.09	-78	1.48
0.50	0.16	-32	21.7	12.12	-61	-30.0	0.032	36	0.09	-94	1.44
0.60	0.17	-45	21.3	11.65	-74	-29.3	0.034	42	0.10	-107	1.42
0.70	0.18	-57	20.9	11.04	-87	-28.5	0.038	47	0.11	-120	1.36
0.80	0.19	-71	20.3	10.35	-99	-27.7	0.041	51	0.11	-131	1.35
0.90	0.19	-84	19.6	9.57	-111	-26.9	0.045	54	0.11	-141	1.34
1.00	0.20	-98	18.9	8.78	-122	-26.0	0.050	56	0.11	-149	1.32
1.20	0.21	-122	17.2	7.28	-143	-24.3	0.061	59	0.11	-163	1.31
1.40	0.21	-143	15.5	5.97	-161	-22.8	0.072	60	0.11	-172	1.33
1.60	0.21	-162	13.8	4.92	-176	-21.5	0.084	60	0.10	-179	1.37
1.80	0.22	-177	12.2	4.08	169	-20.4	0.095	58	0.10	175	1.42
2.00	0.22	170	10.7	3.43	157	-19.5	0.106	55	0.10	172	1.49
2.20	0.21	158	9.3	2.92	145	18.5	0.119	54	0.10	166	1.55
2.40	0.20	149	8.1	2.53	134	-17.9	0.127	50	0.11	163	1.65
2.50	0.20	146	7.5	2.37	129	-17.7	0.131	49	0.12	160	1.69

Note:
3. Reference plane per Figure 9 in Applications Information section.

INA-50311 Typical Performance, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 5\ V$

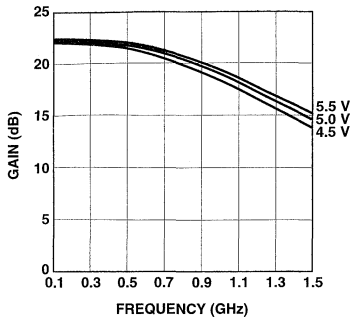


Figure 1. Power Gain vs. Frequency and Voltage.

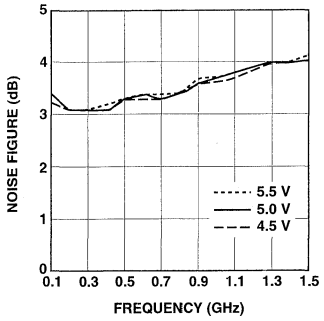


Figure 2. Noise Figure vs. Frequency and Voltage.

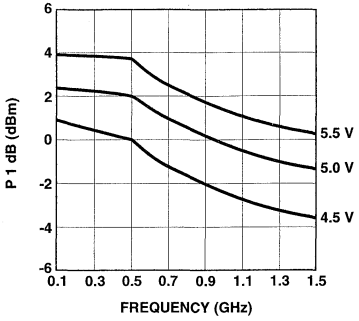


Figure 3. Output Power for 1 dB Gain Compression vs. Frequency and Voltage.

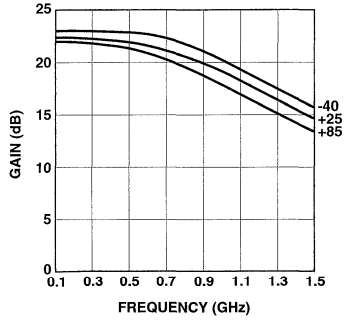


Figure 4. Gain vs. Frequency and Temperature.

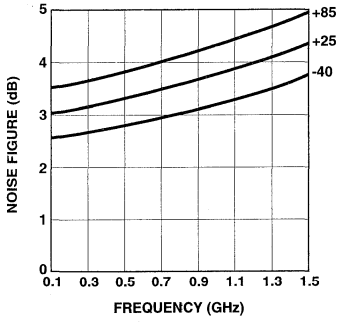


Figure 5. Noise Figure vs. Frequency and Temperature.

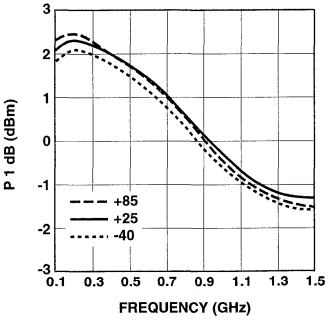


Figure 6. Output Power for 1 dB Gain Compression vs. Frequency and Temperature.

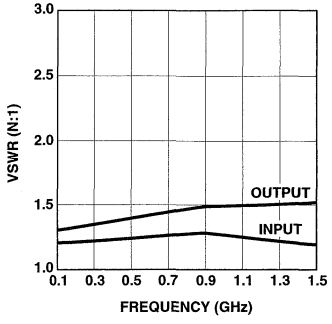


Figure 7. Input and Output VSWR vs. Frequency.

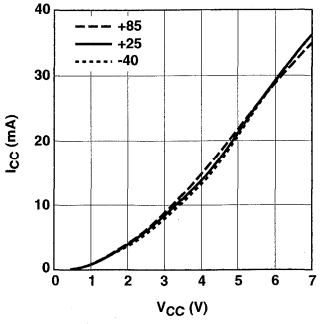


Figure 8. Supply Current vs. Voltage and Temperature.

INA-50311 Applications Information

Introduction

INA-50311 is a silicon RF integrated circuit amplifier with a 50 Ω input and output. The INA-50311 uses resistive feedback to provide flat gain for low noise or multi-purpose gain block applications up to 1000 MHz.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters are shown in Figure 9. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

Biasing

The INA-50311 is a voltage biased device and operates from a single +5 volt power supply with a current drain of only 17 mA. All bias circuitry is fully integrated into the IC eliminating the need for external DC components. The supply voltage for the INA-50311 is fed in through a separate V_{CC} pin of the device and does not require RF isolation from the input or output signal connections.

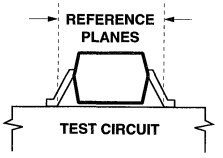


Figure 9. Reference Planes.

Operating Details

The INA-50311 is very easy to use. The basic application of the INA-50311 is shown in Figure 10.

DC blocking capacitors are placed in series with the RF Input and RF Output to isolate adjacent circuits from the internal bias voltages that are present at these terminals. The values of the blocking capacitors are determined by the lowest operating frequency. The values for the blocking capacitors are chosen such that their reactances are small relative to 50 Ω. As an example, use of the INA-50311 for an application covering the 902 to 928 MHz band would require blocking capacitors of at least 70 pF.

The V_{CC} connection to the amplifier must be RF bypassed by placing a capacitor to ground directly at the bias pin of the package. Like the DC blocking capacitors, the value of the V_{CC} bypass capacitor is determined by the lowest operating frequency for the amplifier. This value may typically be the same as that of the DC blocking capacitors. If long bias lines are used to connect the amplifier to the V_{CC} supply, additional bypass capacitors may be needed to prevent resonances that would otherwise result in undesirable gain responses. A well-bypassed V_{CC} line is also desirable to prevent possible oscillations that may occur due to feedback through the bias line from other stages in a cascade.

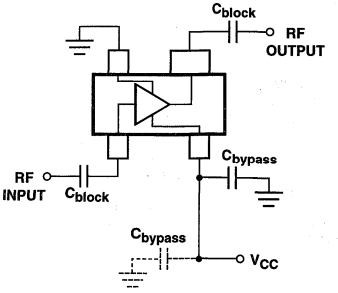


Figure 10. Basic Amplifier Application.

Adequate grounding is needed to obtain maximum performance. The ground pin of the INA-50311 should be connected directly to RF ground by using plated through holes (vias) near the package terminals.

FR-4 or G-10 PCB material is a good choice for most low cost wireless applications. Typical board thickness is 0.025 or 0.031 inches. The width of 50 Ω microstriplines in these PCB thicknesses is also convenient for mounting chip components such as the series DC blocking capacitors.

Circuit Example

The amplifier example in Figure 11 shows a typical implementation of the INA-50311. The input and output connections are through 50 Ω microstriplines with DC blocking capacitors.

The V_{CC} supply connection is RF bypassed very close to the lead of the RFIC. Provision is also made for an additional bypass capacitor on the V_{CC} line near the edge of the PCB.

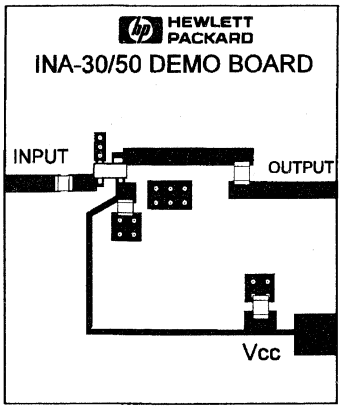
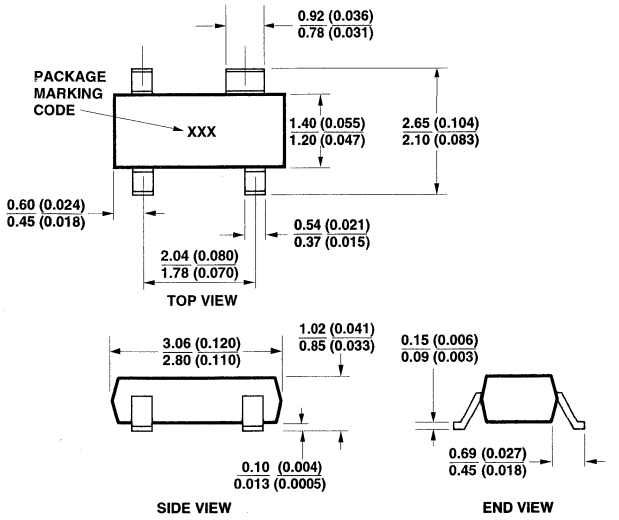


Figure 11. Application Example.

INA-50311 Part Number Ordering Information

Part Number	Devices per Container	Container
INA-50311-TR1	3,000	7" reel
INA-50311-BLK	100	Antistatic bag

Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

2.4 GHz Low Noise Silicon MMIC Amplifier

Technical Data

INA-51063

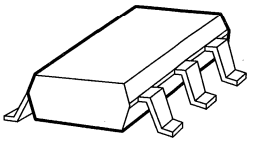
Features

- **Ultra-Miniature Package**
- **Internally Biased, Single 5 V Supply (12 mA)**
- **20.5 dB Gain**
- **3 dB NF**
- **Unconditionally Stable**

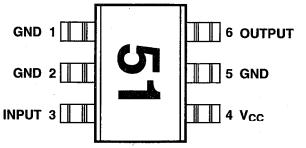
Applications

- **Amplifier for Cellular, Cordless, Special Mobile Radio, PCS, ISM, Wireless LAN, DBS, TVRO, and TV Tuner Applications**

Surface Mount SOT-363 (SC-70) Package



Pin Connections and Package Marking



Note: Package marking provides orientation and identification.

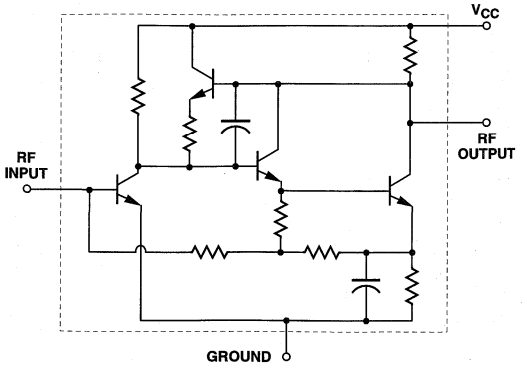
Description

Hewlett-Packard's INA-51063 is a Silicon monolithic amplifier that offers excellent gain and noise figure for applications to 2.4 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

The INA-51063 uses a topology which is internally biased, eliminating the need for external components and providing decreased sensitivity to ground inductance.

The INA-51063 is fabricated using HP's 30 GHz f_{MAX} ISOSAT™ Silicon bipolar process which uses nitride self-alignment sub-micrometer lithography, trench isolation, ion implantation, gold metallization, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity, and reliability.

Equivalent Circuit (Simplified)



5965-9680E

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{CC}	Supply Voltage, to ground	V	12
P_{in}	CW RF Input Power	dBm	+13
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{jc} = 200°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board)

INA-51063 Electrical Specifications[3], $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 5$ V

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G_p	Power Gain ($\|S_{21}\|^2$)	f = 1500 MHz	dB	18	20.5	
NF	Noise Figure	f = 1500 MHz	dB		3	
P_{1dB}	Output Power at 1 dB Gain Compression	f = 1500 MHz	dBm		-2.5	
IP_3	Third Order Intercept Point	f = 1500 MHz	dBm		+6	
VSWR	Input VSWR	f = 1500 MHz			1.3	
	Output VSWR	f = 1500 MHz			1.8	
I_{cc}	Device Current		mA		12	14
t_d	Group Delay	f = 1500 MHz	ps		240	

INA-51063 Typical Scattering Parameters[3], $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 5.0$ V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	Factor
0.05	0.17	177	20.8	10.94	-4	-30.9	0.029	-1	0.23	-5	1.65
0.10	0.17	175	20.8	10.95	-7	-30.8	0.029	-2	0.23	-8	1.65
0.20	0.16	170	20.8	10.94	-14	-30.9	0.028	-4	0.23	-16	1.70
0.30	0.16	166	20.7	10.89	-21	-31.0	0.028	-5	0.23	-25	1.70
0.40	0.14	162	20.8	10.94	-28	-31.2	0.028	-7	0.24	-33	1.69
0.50	0.13	159	20.8	10.96	-35	-31.3	0.027	-9	0.24	-43	1.74
0.60	0.12	158	20.8	11.00	-42	-31.5	0.027	-10	0.24	-52	1.74
0.70	0.10	158	20.9	11.06	-49	-31.6	0.026	-12	0.24	-61	1.79
0.80	0.08	164	20.9	11.06	-57	-31.9	0.026	-14	0.25	-69	1.78
0.90	0.07	172	20.9	11.10	-64	-32.1	0.025	-15	0.26	-77	1.83
1.00	0.07	-174	20.9	11.10	-72	-32.5	0.024	-17	0.26	-85	1.89
1.10	0.07	-156	20.9	11.14	-80	-32.7	0.023	-18	0.27	-94	1.95
1.20	0.08	-142	20.9	11.11	-88	-33.2	0.022	-21	0.27	-103	2.02
1.30	0.10	-135	20.9	11.08	-96	-33.5	0.021	-23	0.28	-113	2.10
1.40	0.12	-131	20.8	11.01	-105	-33.9	0.020	-25	0.28	-122	2.19
1.50	0.14	-131	20.7	10.88	-113	-34.6	0.019	-28	0.28	-131	2.31
1.60	0.17	-132	20.6	10.71	-122	-35.2	0.017	-30	0.28	-140	2.57
1.70	0.19	-134	20.4	10.45	-131	-36.0	0.016	-33	0.28	-150	2.77
1.80	0.22	-135	20.1	10.16	-139	-36.8	0.014	-36	0.27	-159	3.20
1.90	0.24	-139	19.8	9.78	-148	-37.8	0.013	-39	0.27	-168	3.53
2.00	0.26	-142	19.4	9.37	-157	-39.1	0.011	-42	0.25	-177	4.32
2.10	0.28	-145	19.0	8.90	-165	-40.6	0.009	-47	0.24	175	5.49
2.20	0.30	-148	18.5	8.42	-174	-42.2	0.008	-53	0.22	166	6.49
2.30	0.32	-151	18.0	7.96	179	-44.3	0.006	-63	0.21	158	9.03
2.40	0.33	-154	17.4	7.45	171	-46.7	0.005	-79	0.20	150	11.51
2.50	0.35	-157	16.9	6.98	164	-48.9	0.004	-108	0.18	143	15.20
3.00	0.41	-169	13.8	4.89	133	-39.0	0.011	163	0.10	115	7.64
3.50	0.45	-179	10.8	3.48	108	-31.9	0.025	146	0.03	123	4.61
4.00	0.50	172	8.3	2.59	88	-26.9	0.045	132	0.05	-132	3.29

Note:
3. Reference plane per Figure 9 in Applications Information section.

INA-51063 Typical Performance, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 5\ V$

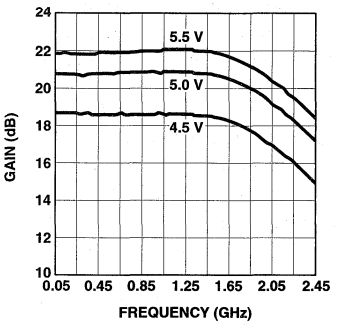


Figure 1. Gain vs. Frequency and Voltage.

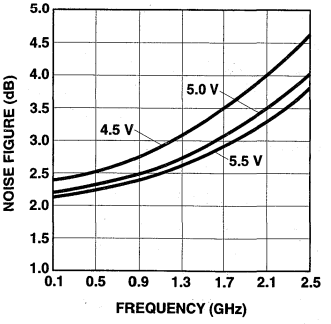


Figure 2. Noise Figure vs. Frequency and Voltage.

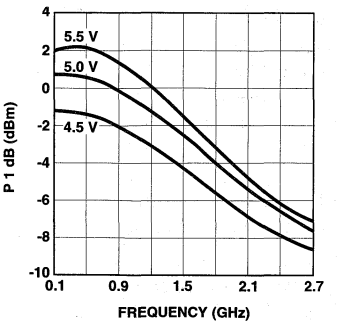


Figure 3. Output Power for 1 dB Gain Compression vs. Frequency and Voltage.

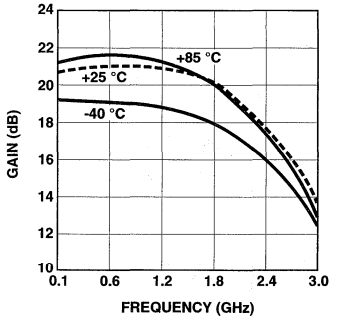


Figure 4. Gain vs. Frequency and Temperature.

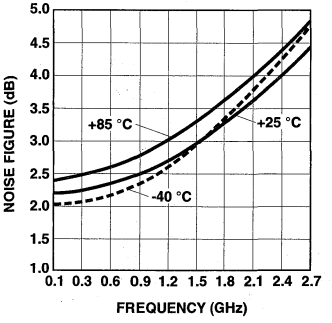


Figure 5. Noise Figure vs. Frequency and Temperature.

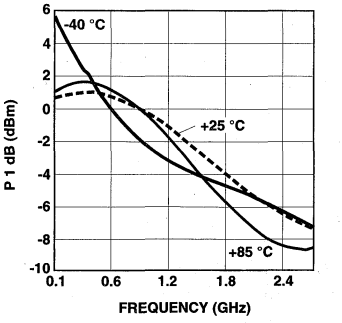


Figure 6. Output Power for 1 dB Gain Compression vs. Frequency and Temperature.

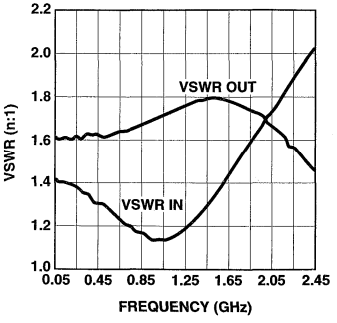


Figure 7. Input and Output VSWR vs. Frequency.

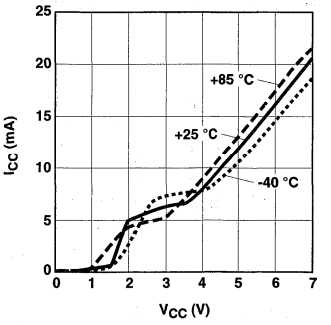


Figure 8. Supply Current vs. Voltage and Temperature.

INA-51063 Applications Information

Introduction

The INA-51063 is a silicon RFIC amplifier with a 50 Ω input and output. The INA-51063 is easy to use for low noise and multi-purpose gain block applications up to 2.4 GHz.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters are shown in Figure 9. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

Biasing

The INA-51063 is a voltage biased device and operates from a single +5 volt power supply with a typical current drain of only 12 mA. All bias regulation circuitry is integrated into the RFIC. The supply voltage for the INA-51063 is fed in through the separate V_{CC} pin of the device and does not require RF isolation from the input or output. No additional external DC components are needed.

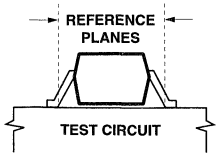


Figure 9. Reference Planes.

Operating Details

The INA-51063 is very easy to use. The basic application of the INA-51063 is shown in Figure 10.

DC blocking capacitors are placed in series with the RF Input and RF Output to isolate adjacent stages from the internal bias voltages that are present at these terminals. The values of the blocking capacitors are determined by the lowest operating frequency. The values for the blocking capacitors are chosen such that their reactances are small relative to 50 Ω. As an example, use of the INA-51063 for a 2.4 GHz application would require blocking capacitors of at least 33 pF.

The V_{CC} connection to the amplifier must be RF bypassed by placing a capacitor to ground directly at the bias pin of the package. Like the DC blocking capacitors, the value of the V_{CC} bypass capacitor is determined by the lowest operating frequency for the amplifier. This value may typically be the same as that of the DC blocking capacitors. If long bias lines are used to connect the amplifier to the V_{CC} supply, additional bypass capacitors may be needed to prevent resonances that would otherwise result in undesirable gain responses. A well-bypassed V_{CC} line is also desirable to prevent possible oscillations that may occur due to feedback through the bias line from other stages in a cascade.

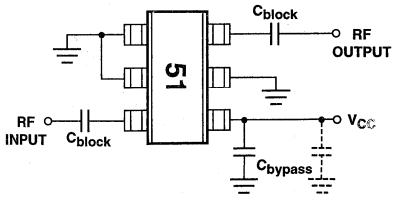


Figure 10. Basic Amplifier Application.

SOT-363 PCB Layout

The INA-51063 is packaged in the miniature SOT-363 (SC-70) surface mount package. A PCB pad layout for the SOT-363 package is shown in Figure 11 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the INA-51063. The layout is shown

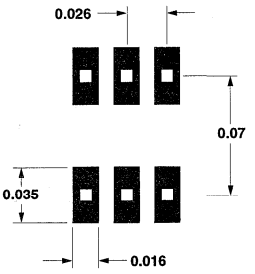


Figure 11. PCB Pad Layout (Dimensions in Inches).

with a nominal SOT-363 package footprint superimposed on the PCB pads.

RF Layout

The RF layout in Figure 12 is suggested as a starting point for designs using the INA-51063 amplifier. Adequate grounding is needed to obtain maximum performance and to reduce the possibility of potential instability. All three ground pins of the RFIC should be connected to RF ground by using plated through holes (vias) near the package terminals. The power supply connection to the amplifier must be RF bypassed by placing a capacitor directly to ground at the V_{CC} pin of the package.

It is recommended that the PCB traces for the ground pins NOT be connected together underneath the body of the package. PCB pads hidden under the package cannot be adequately inspected for SMT solder quality.

FR-4 or G-10 PCB material is a good choice for most low cost wireless applications. Typical board thickness is 0.025 or 0.031 inches. The width of 50 Ω microstriplines in these PCB thicknesses is also convenient for mounting chip components such as the series inductor at the input for impedance matching or for DC blocking capacitors. For noise figure sensitive applications, the use of PTFE/glass dielectric materials may be warranted to minimize transmission line losses at the amplifier input.

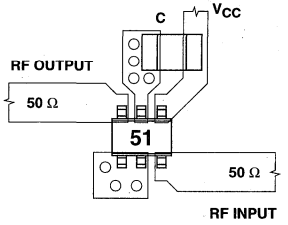


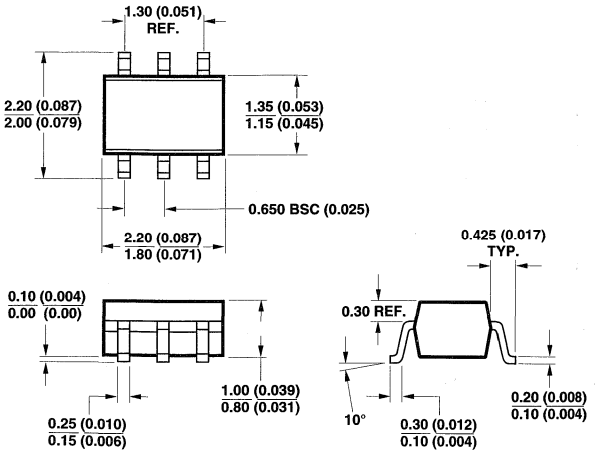
Figure 12. RF Layout.

INA-51063 Part Number Ordering Information

Part Number	Devices per Container	Container
INA-51063-TR1	3,000	7" reel
INA-51063-BLK	100	Antistatic bag

Package Dimensions

Outline 63 (SOT-363/SC-70)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

1.5 GHz Low Noise Silicon MMIC Amplifier

Technical Data

INA-52063

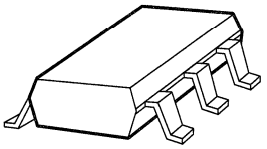
Features

- **Ultra-Miniature Package**
- **Single 5 V Supply (30 mA)**
- **22 dB Gain**
- **8 dBm P_{1dB}**
- **Unconditionally Stable**

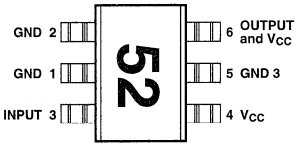
Applications

- **Amplifier for Cellular, Cordless, Special Mobile Radio, PCS, ISM, Wireless LAN, DBS, TVRO, and TV Tuner Applications**

Surface Mount SOT-363 (SC-70) Package



Pin Connections and Package Marking



Note: Package marking provides orientation and identification.

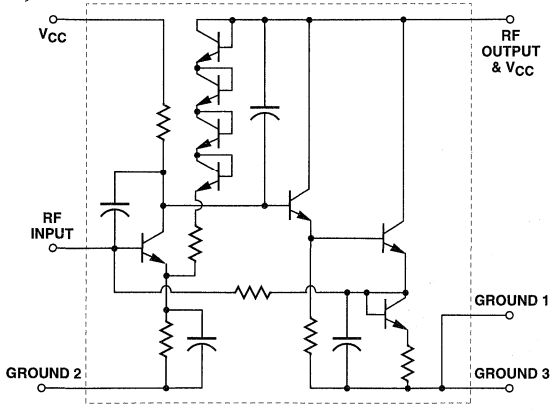
Description

Hewlett-Packard's INA-52063 is a Silicon monolithic amplifier that offers excellent gain and power output for applications to 1.5 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

The INA-52063 is fabricated using HP's 30 GHz f_{MAX} ISOSAT™ Silicon bipolar process which uses nitride self-alignment sub-micrometer lithography, trench isolation, ion implantation, gold metallization, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity, and reliability.

Equivalent Circuit

(Simplified)



Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{CC}	Supply Voltage, to Ground	V	12
P_{in}	CW RF Input Power	dBm	+13
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{j-c} = 170°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board)

INA-52063 Electrical Specifications, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 5$ V, unless noted

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G_p	Power Gain ($\|S_{21}\|^2$)	f = 900 MHz	dB	20	22	
NF	Noise Figure	f = 900 MHz	dB		4.0	
P_{1dB}	Output Power at 1 dB Gain Compression	f = 900 MHz	dBm		+8	
IP_3	Third Order Intercept Point	f = 900 MHz	dBm		+20	
IP_3	Third Order Intercept Point	f = 2100 MHz	dBm		+15	
VSWR	Input VSWR	f = 900 MHz			1.4	
	Output VSWR	f = 900 MHz			1.3	
I_{CC}	Device Current		mA		30	38
τ_d	Group Delay	f = 900 MHz	ps		238	

INA-52063 Typical Performance, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 5$ V, unless noted

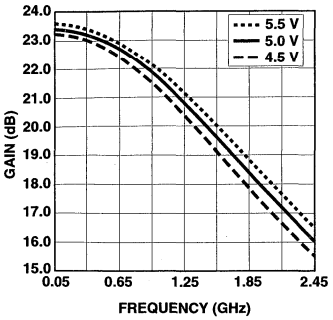


Figure 1. Gain vs. Frequency and Voltage.

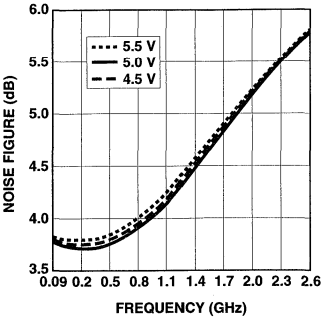


Figure 2. Noise Figure vs. Frequency and Voltage.

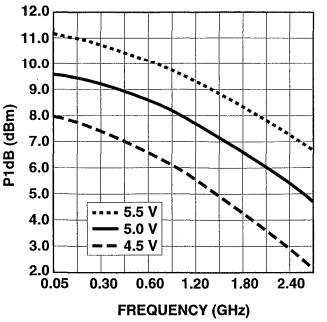


Figure 3. Output Power for 1 dB Gain Compression vs. Frequency and Voltage.

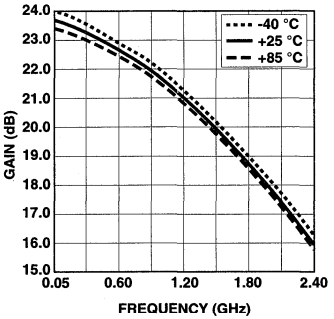


Figure 4. Gain vs. Frequency and Temperature.

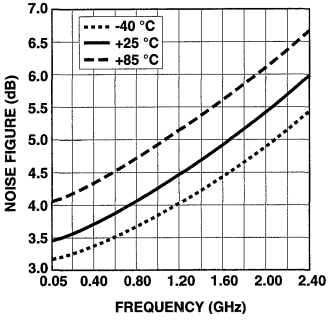


Figure 5. Noise Figure vs. Frequency and Temperature.

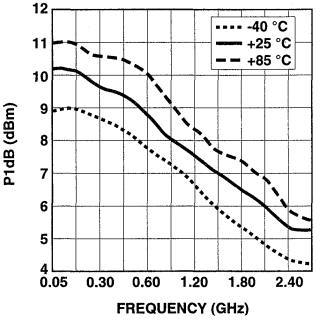


Figure 6. Output Power for 1 dB Gain Compression vs. Frequency and Temperature.

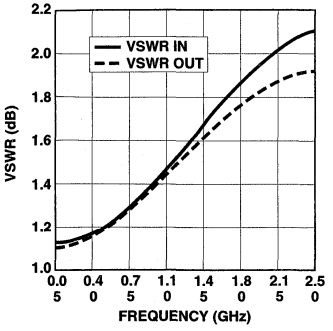


Figure 7. Input and Output VSWR vs. Frequency.

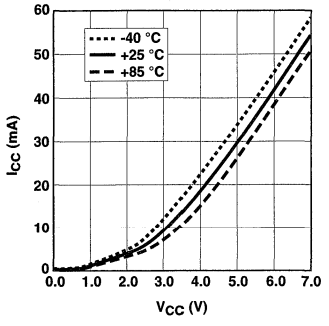


Figure 8. Supply Current vs. Voltage and Temperature.

INA-52063 Typical Scattering Parameters[3], T_C = 25°C, Z_O = 50 Ω, V_{CC} = 5.0 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	Factor
0.05	0.06	165	23.5	14.88	-5	-29.3	0.034	0	0.05	1	1.24
0.10	0.06	154	23.4	14.84	-9	-29.3	0.034	0	0.05	0	1.24
0.20	0.06	131	23.4	14.72	-19	-29.4	0.034	0	0.05	-1	1.25
0.30	0.07	104	23.3	14.57	-28	-29.5	0.034	1	0.06	-5	1.25
0.40	0.07	80	23.1	14.33	-37	-29.4	0.034	2	0.07	-10	1.26
0.50	0.09	66	23.0	14.08	-46	-29.4	0.034	3	0.08	-14	1.27
0.60	0.10	46	22.8	13.76	-55	-29.4	0.034	4	0.09	-21	1.28
0.70	0.12	30	22.6	13.41	-64	-29.3	0.034	5	0.11	-29	1.29
0.80	0.13	14	22.3	13.01	-73	-29.2	0.035	6	0.13	-37	1.28
0.90	0.15	0	22.0	12.59	-82	-29.0	0.036	6	0.14	-45	1.27
1.00	0.17	-12	21.7	12.14	-90	-28.8	0.036	7	0.16	-52	1.28
1.20	0.21	-33	21.0	11.22	-106	-28.4	0.038	7	0.20	-67	1.25
1.40	0.24	-50	20.2	10.28	-122	-28.1	0.040	6	0.23	-81	1.24
1.60	0.27	-66	19.4	9.38	-137	-27.7	0.041	4	0.25	-94	1.26
1.80	0.30	-80	18.6	8.55	-151	-27.5	0.042	2	0.27	-107	1.29
2.00	0.32	-93	17.8	7.80	-164	-27.4	0.043	-1	0.29	-118	1.33
2.20	0.33	-105	17.1	7.13	-177	-27.6	0.042	-5	0.30	-129	1.44
2.40	0.35	-117	16.3	6.52	170	-27.8	0.041	-8	0.31	-139	1.56
2.60	0.36	-128	15.5	5.98	159	-28.1	0.039	-12	0.32	-149	1.74
2.80	0.36	-139	14.8	5.52	147	-28.9	0.036	-15	0.33	-158	2.01
3.00	0.36	-149	14.1	5.08	136	-29.5	0.033	-16	0.33	-168	2.37

Note: 3. Reference plane per Figure 9 in Applications Information section.

INA-52063 Applications Information

Introduction

The INA-52063 is a silicon RFIC amplifier that is designed with an internal resistive feedback network to provide a 50 Ω input and 50 Ω output impedance. With a Third Order Intercept Point of +20 dBm and a low Noise Figure of 4 dB, the INA-52063 is especially useful for RF and IF amplifier applications requiring high dynamic ranges.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters for this device are shown in Figure 9. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

SOT-363 PCB Layout

The INA-52063 is packaged in the miniature SOT-363 (SC-70) surface mount package. A PCB pad layout for the SOT-363 package is shown in Figure 10 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding pad parasitics that could impair the high frequency performance of the INA-52063. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads for reference.

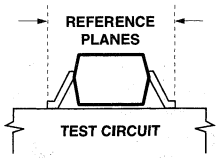


Figure 9. Phase Reference Planes.

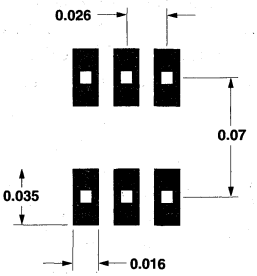


Figure 10. PCB Pad Layout (dimensions in inches).

Operating Details

The INA-52063 is a voltage biased device that operates from a +5 volt power supply with a typical current drain of 30 mA. All bias regulation circuitry is integrated into the RFIC.

Figure 11 shows a typical implementation of the INA-52063. The supply voltage for the INA-52063 must be applied to two terminals, the V_{CC} pin and the RF Output pin.

The V_{CC} connection to the amplifier is RF bypassed by placing a capacitor to ground near the V_{CC} pin of the amplifier package.

The power supply connection to the RF Output pin is achieved by means of a RF choke (inductor). The value of the RF choke must be large relative to 50 Ω in order to prevent loading of the RF Output.

The supply voltage end of the RF choke is bypassed to ground with a capacitor. If the physical layout permits, this can be the same bypass capacitor that is used at the V_{CC} terminal of the amplifier.

Blocking capacitors are normally placed in series with the RF Input and the RF Output to isolate the DC voltages on these pins from circuits adjacent to the amplifier. The values for the blocking and bypass capacitors are selected to provide a reactance at the lowest frequency of operation that is small relative to 50 Ω.

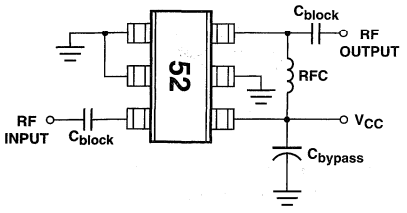


Figure 11. Basic Amplifier Application.

RF Layout

An example layout for an amplifier using the INA-52063 is shown in Figure 12.

This example uses a microstripline design (solid groundplane on the back side of the circuit board). The circuit board material is 0.031-inch thick FR-4. Plated through holes (vias) are used to bring the ground to the top side of the circuit where needed. Multiple vias are used to reduce the inductance of the path to ground.

Figure 13 shows an assembled amplifier. The +5 volt supply is fed directly into the V_{CC} pin of the INA-52063 and into the RF Output pin through the RF choke (RFC). Capacitor C3 provides RF bypassing for both the V_{CC} pin and the power supply end of the RFC.

Capacitor C4 is optional and may be used to add additional bypassing for the V_{CC} line. A well bypassed V_{CC} line is especially necessary in cascades of amplifier stages to prevent oscillation that may occur as a result of RF feedback through the power supply lines.

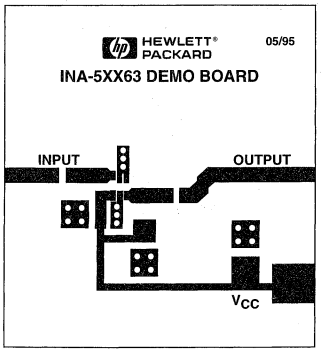


Figure 12. RF Layout.

For this demonstration circuit, the value chosen for the RF choke was 220 nH (Coilcraft 1008CS-221 or equivalent). All of the blocking and bypass capacitors are 1000 pF. These values provide excellent amplifier performance from under 50 MHz through 1 GHz. Larger values for the choke and capacitors can be used to extend the lower end of the bandwidth. Since the gain of the INA-52063 extends down to DC, the frequency response of the amplifier is limited only by the values of the capacitors and choke.

A convenient method for making RF connection to the demonstration board is to use a PCB mounting type of SMA connector (Johanson 142-0701-881, or equivalent). These connectors can be slipped over the edge of the PCB and the center conductors soldered to the input and output lines. The ground pins of the connectors are soldered to the ground plane on the backside of the board. The extra ground pins for the top of the board are not needed and are clipped off.

PCB Materials

Typical choices for PCB material for low cost wireless applications are FR-4 or G-10 with a thickness of 0.025 or 0.031 inches. A thickness of 0.062 inches is the maximum that is recommended for use with this particular device. The use of a thicker board material increases the inductance of the plated through vias used for RF grounding and may deteriorate circuit performance. Adequate grounding is needed not only to obtain maximum amplifier performance but also to reduce any possibility of instability.

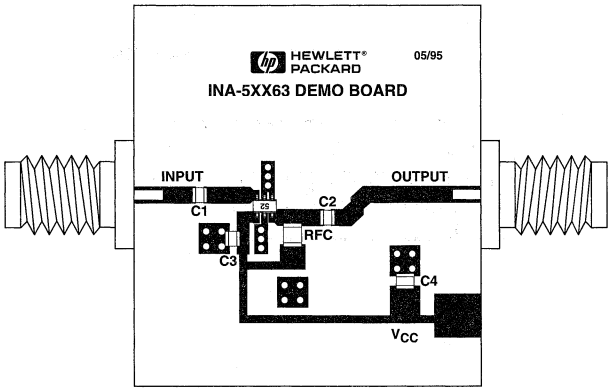
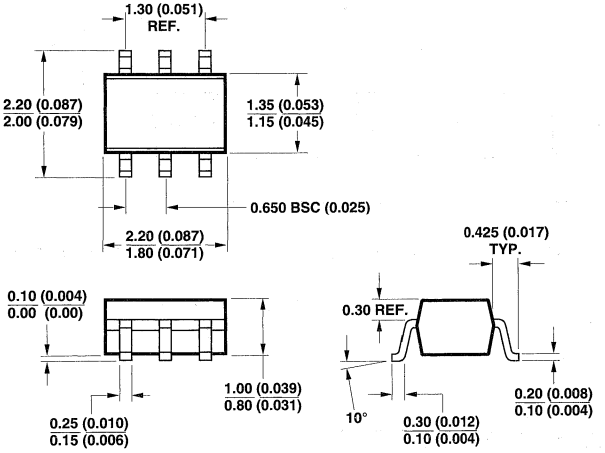


Figure 13. Assembled Amplifier.

Package Dimensions

Outline 63 (SOT-363/SC-70)

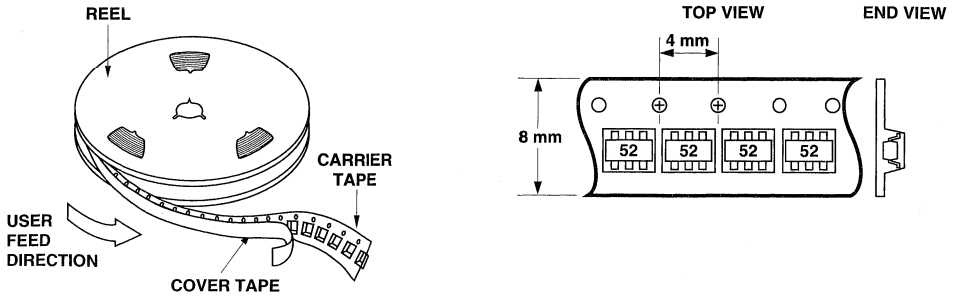


DIMENSIONS ARE IN MILLIMETERS (INCHES)

INA-52063 Part Number Ordering Information

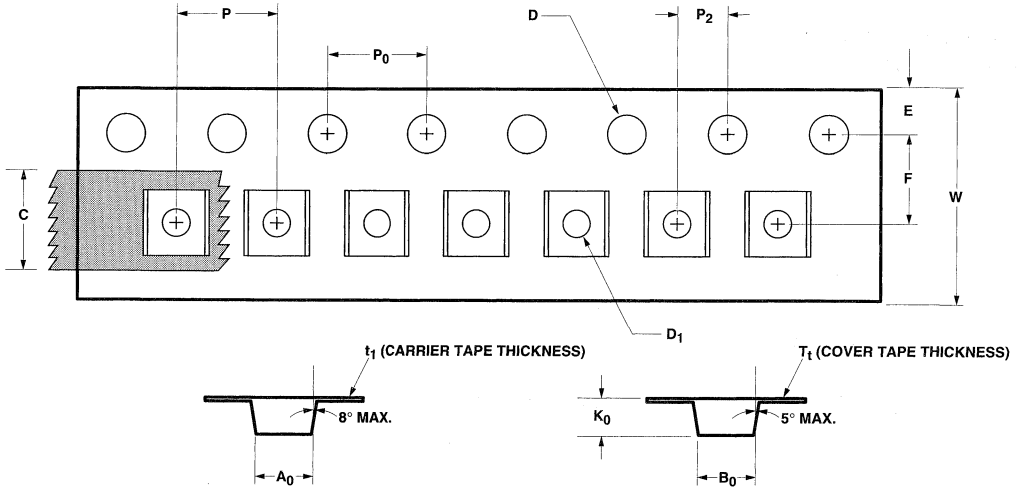
Part Number	Devices per Container	Container
INA-52063-TR1	3,000	7" reel
INA-52063-BLK	100	Antistatic bag

Device Orientation



Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

3.0 GHz Low Noise Silicon MMIC Amplifier

Technical Data

INA-54063

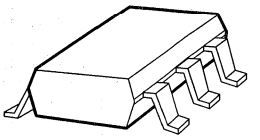
Features

- **Ultra-Miniature Package**
- **Single 5 V Supply (29 mA)**
- **21.5 dB Gain (1.9 GHz)**
- **8.0 dBm P_{1dB} (1.9 GHz)**
- **Positive Gain Slope**
- **Unconditionally Stable**

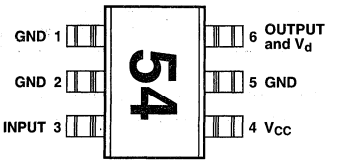
Applications

- **IF Amplifier for DBS Downconverter, Cellular, Cordless, Special Mobile Radio, PCS, ISM, and Wireless LAN Applications**

Surface Mount Package SOT-363 (SC-70)



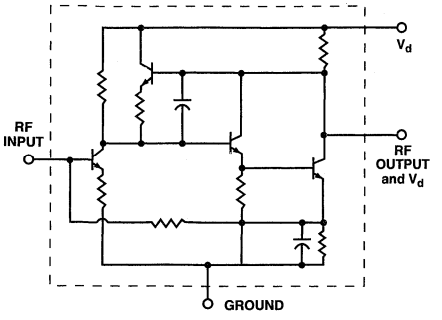
Pin Connections and Package Marking



Note:
Package marking provides orientation and identification.

Equivalent Circuit

(Simplified)



Description

Hewlett-Packard's INA-54063 is a Silicon monolithic amplifier that offers excellent gain and power output for applications to 3.0 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

With its wide bandwidth and high linearity, the INA-54063 is an excellent candidate for DBS IF applications. It also features a unique gain curve which increases over the range from 1 to 2 GHz. This gain slope compensates for the gain rolloff found in typical receiver systems.

The INA-54063 is fabricated using HP's 30 GHz f_{MAX} ISOSAT™ Silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metalization, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity, and reliability.

5965-5364E

INA-54063 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Supply Voltage, to Ground	V	12
P_{in}	CW RF Input Power	dBm	13
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{j-c} = 165°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

Electrical Specifications, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_d = 5$ V, unless noted

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.	Std. Dev.[1]
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1900 MHz	dB	19	21.5		0.7
NF	Noise Figure	f = 1900 MHz	dB		5.0		0.4
P_{1dB}	Output Power at 1 dB Gain Compression	f = 1900 MHz	dBm		8.0		
IP_3	Third Order Intercept Point	f = 1900 MHz f = 2150 MHz	dBm		17 15.7		
$VSWR_{in}$	Input VSWR	f = 1900 MHz			1.4		
$VSWR_{out}$	Output VSWR	f = 1900 MHz			2.4		
I_d	Device Current		mA		29	36	1.8
t_d	Group Delay	f = 1900 MHz	ps		272		

Note:
1. Standard deviation number is based on measurement of at least 500 parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.

INA-54063 Typical Performance

T_C = 25°C, Z_O = 50 Ω, V_d = 5 V, unless noted

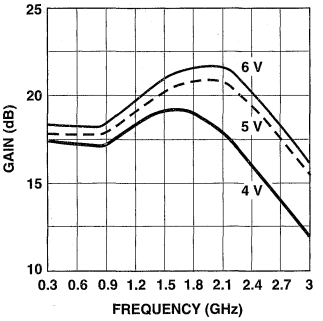


Figure 1. Gain vs. Frequency and Voltage.

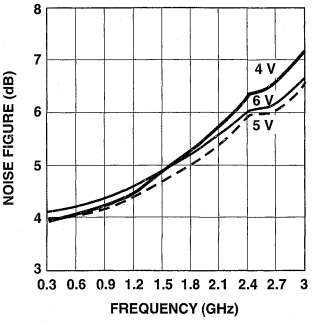


Figure 2. Noise Figure vs. Frequency and Voltage.

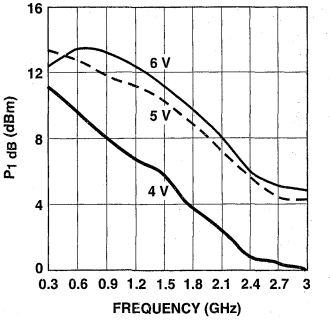


Figure 3. Output Power for 1 dB Gain Compression vs. Frequency and Voltage.

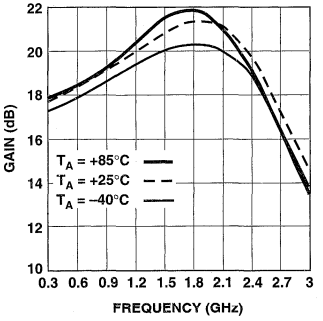


Figure 4. Gain vs. Frequency and Temperature.

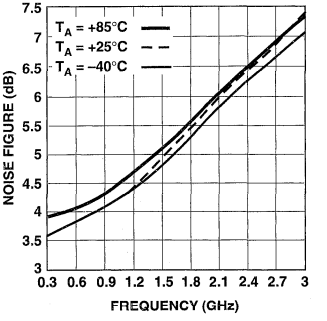


Figure 5. Noise Figure vs. Frequency and Temperature.

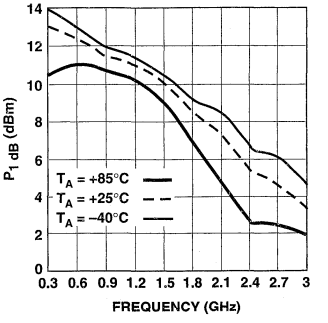


Figure 6. Output Power for P_{1dB} Gain Compression vs. Frequency and Temperature.

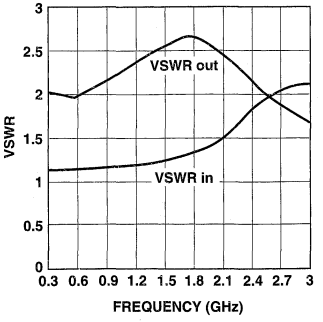


Figure 7. Input and Output VSWR vs. Frequency.

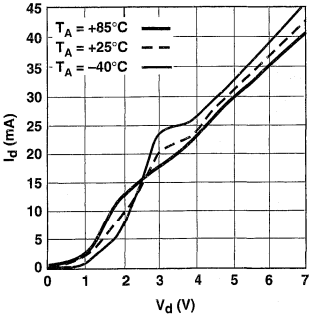


Figure 8. Supply Current vs. Voltage and Temperature.

INA-54063 Typical Scattering Parameters[1], T_C = 25°C, Z_O = 50 Ω, V_d = 5.0 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Factor
0.10	0.11	91	16.9	7.02	19	-27.7	0.04	21	0.47	75	1.50
0.20	0.09	64	17.6	7.56	2	-27.1	0.04	7	0.35	34	1.47
0.30	0.08	51	17.7	7.71	-7	-27.0	0.04	0	0.32	10	1.46
0.40	0.09	42	17.9	7.81	-14	-27.1	0.04	-5	0.31	-7	1.46
0.50	0.08	46	18.1	8.00	-21	-27.3	0.04	-9	0.30	-23	1.47
0.60	0.09	39	18.2	8.11	-27	-27.5	0.04	-12	0.30	-36	1.47
0.70	0.09	32	18.3	8.24	-33	-27.8	0.04	-15	0.31	-47	1.48
0.80	0.09	22	18.5	8.41	-39	-28.1	0.04	-17	0.33	-56	1.48
0.90	0.10	13	18.7	8.58	-45	-28.4	0.04	-19	0.34	-65	1.48
1.00	0.10	5	18.9	8.80	-51	-28.8	0.04	-21	0.35	-73	1.48
1.10	0.11	-3	19.1	9.05	-57	-29.2	0.03	-23	0.37	-80	1.48
1.20	0.11	-11	19.4	9.28	-64	-29.6	0.03	-25	0.38	-88	1.50
1.30	0.12	-20	19.6	9.58	-70	-30.1	0.03	-26	0.39	-94	1.50
1.40	0.12	-29	19.9	9.88	-78	-30.6	0.03	-27	0.40	-101	1.52
1.50	0.13	-36	20.2	10.19	-85	-31.1	0.03	-28	0.41	-108	1.54
1.60	0.14	-44	20.4	10.51	-93	-31.5	0.03	-29	0.41	-114	1.55
1.70	0.15	-53	20.7	10.86	-101	-32.0	0.03	-30	0.42	-120	1.57
1.80	0.16	-61	21.0	11.16	-111	-32.7	0.02	-31	0.42	-126	1.63
1.90	0.17	-68	21.1	11.36	-120	-33.5	0.02	-31	0.41	-132	1.74
2.00	0.20	-73	21.2	11.44	-130	-34.2	0.02	-29	0.40	-138	1.87
2.10	0.22	-80	21.2	11.43	-141	-34.9	0.02	-29	0.38	-144	2.04
2.20	0.24	-89	21.0	11.25	-152	-35.6	0.02	-28	0.37	-148	2.22
2.30	0.26	-99	20.7	10.86	-164	-36.0	0.02	-27	0.35	-151	2.41
2.40	0.27	-108	20.1	10.16	-175	-36.8	0.01	-26	0.34	-155	2.82
2.50	0.28	-112	19.5	9.39	175	-37.8	0.01	-24	0.32	-158	3.42
2.60	0.29	-117	18.6	8.55	166	-39.0	0.01	-23	0.31	-162	4.31
2.70	0.30	-124	17.8	7.79	157	-39.3	0.01	-15	0.29	-164	4.94
2.80	0.30	-130	16.9	7.03	150	-39.6	0.01	-16	0.28	-166	5.69
2.90	0.30	-133	16.1	6.35	144	-41.6	0.01	-15	0.26	-170	8.05
3.00	0.30	-136	15.3	5.83	138	-42.5	0.01	-5	0.25	-171	9.80
3.10	0.31	-138	14.6	5.35	132	-43.7	0.01	3	0.23	-173	12.33
3.20	0.31	-140	13.8	4.92	127	-45.4	0.01	13	0.22	-174	16.36
3.30	0.31	-142	13.2	4.57	121	-45.4	0.01	31	0.21	-174	17.56
3.40	0.31	-143	12.5	4.23	116	-45.7	0.01	47	0.20	-174	19.78
3.50	0.32	-145	11.9	3.93	111	-44.8	0.01	65	0.19	-174	19.14
3.60	0.32	-147	11.2	3.65	106	-43.4	0.01	75	0.19	-174	17.63
3.70	0.33	-148	10.6	3.38	101	-42.2	0.01	82	0.18	-174	16.53
3.80	0.34	-149	9.9	3.11	96	-41.1	0.01	88	0.18	-175	15.72
3.90	0.35	-152	9.1	2.84	92	-40.3	0.01	93	0.17	-175	15.60
4.00	0.35	-156	8.4	2.62	89	-39.3	0.01	99	0.16	-174	15.11
4.10	0.34	-159	7.8	2.46	85	-38.0	0.01	103	0.14	-171	14.09
4.20	0.33	-161	7.1	2.27	79	-37.6	0.01	104	0.13	-156	14.64
4.30	0.32	-161	5.6	1.91	75	-37.6	0.01	112	0.19	-135	17.07
4.40	0.33	-161	4.5	1.68	81	-35.8	0.02	127	0.31	-150	14.81
4.50	0.34	-162	4.8	1.73	82	-33.4	0.02	129	0.33	-170	10.72
4.60	0.35	-166	4.9	1.75	80	-31.7	0.03	128	0.32	180	8.78
4.70	0.35	-170	4.8	1.74	76	-30.4	0.03	126	0.30	173	7.69
4.80	0.33	-173	4.6	1.69	72	-29.3	0.03	124	0.30	167	7.09
4.90	0.34	-174	4.2	1.62	69	-28.2	0.04	123	0.29	164	6.57
5.00	0.34	-177	3.9	1.57	66	-27.2	0.04	122	0.29	160	6.04

Note 1: Reference plane per Figure 14 in Applications Information section.

INA-54063 Applications Information

Introduction

The INA-54063 is a silicon RFIC amplifier that is designed with an internal resistive feedback network to provide a 50 Ω input and near 75 Ω output impedance. With a 1-dB compressed Output Power of 8 dBm and Noise Figure of 5 dB, the INA-54063 is well suited for amplifier applications requiring high dynamic ranges.

A unique feature of the INA-54063 is a positive gain slope over the 1–2 GHz range that is useful in many satellite-based TV and datacom systems. When used for the IF amplifier, the up-slope in the gain of the INA-54063 is intended to compensate for the negative gain slope in many Low Noise Block downconverters (LNB) used in consumer and commercial TV delivery systems, such as DDS, DBS, and TVRO. The positive gain slope can also compensate for the high frequency attenuation characteristics of 75 Ω cables used to connect the outdoor LNBs to indoor set-top converters.

In addition to use in TV delivery systems, the INA-54063 will find many applications in 50 Ω input-50 Ω output gain and buffer stages in wireless communications systems.

Operating Details

The INA-54063 is a voltage biased device that operates from a +5 volt power supply with a typical current drain of 29 mA. All bias regulation circuitry is integrated into the RFIC. Figure 9 shows a typical implementation of the INA-54063. The supply voltage for the INA-54063 must be applied to two terminals, the V_{cc} pin and the RF Output pin.

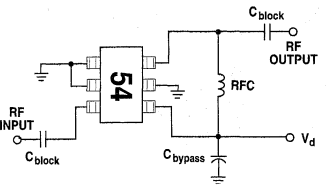


Figure 9. Basic Amplifier Application.

The V_d connection to the amplifier is RF bypassed by placing a capacitor to ground near the V_d pin of the amplifier package. The power supply connection to the RF Output pin is achieved by means of an RF choke (inductor). The value of the RF choke must be large relative to 50/75 Ω in order to prevent loading of the RF Output.

The supply voltage end of the RF choke is bypassed to ground with a capacitor. If the physical layout permits, this can be the same bypass capacitor that is used at the V_d terminal of the amplifier. Blocking capacitors are normally placed in series with the RF Input and the RF Output to isolate the DC voltages on these pins from circuits adjacent to the amplifier. The values for the blocking and bypass capacitors are selected to provide a reactance at the lowest frequency of operation that is small relative to 50 Ω.

Example Layout for 50 Ω Amplifier

An example layout for an amplifier using the INA-54063 with 50 Ω input and 50 Ω output is shown in Figure 10.

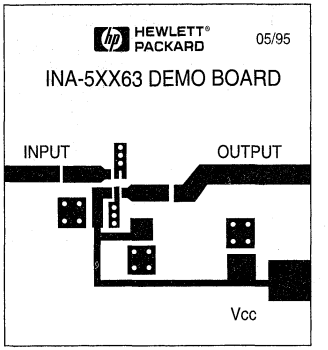


Figure 10. RF Layout for 50 Ω Input and Output.

This example uses a microstripline design (solid groundplane on the back side of the circuit board). The circuit board material is 0.031-inch thick FR-4. Plated through holes (vias) are used to bring the ground to the top side of the circuit where needed. Multiple vias are used to reduce the inductance of the path to ground.

Figure 11 shows an assembled amplifier. The +5 volt supply (V_{cc}) is fed directly into the V_d pin of the INA-54063 and into the RF Output pin through the RF choke (RFC). Capacitor C3 provides RF bypassing for both the V_d pin and the power supply end of the RFC.

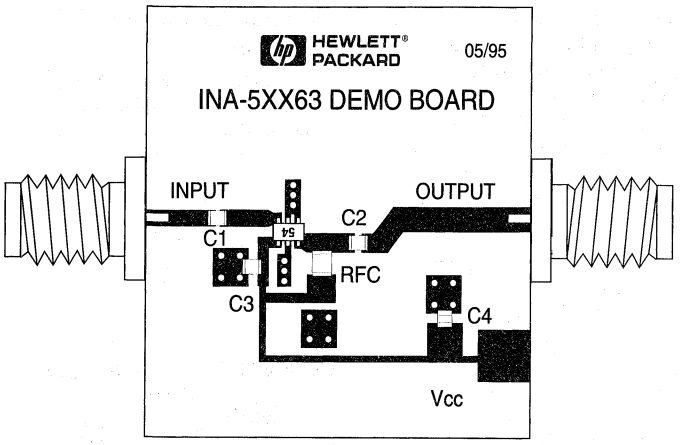


Figure 11. Assembled 50 Ω Amplifier.

Capacitor C4 is optional and may be used to add additional bypassing for the V_{cc} line. A well bypassed V_{cc} line is especially necessary in cascades of amplifier stages to prevent oscillation that may occur as a result of RF feedback through the power supply lines.

For this demonstration circuit, the value chosen for the RF choke was 220 nH (Coilcraft 1008CS-221 or equivalent). All of the blocking and bypass capacitors are 1000 pF. These values provide excellent amplifier performance from under 50 MHz through 2.5 GHz. Larger values for the choke and capacitors can be used to extend the lower end of the bandwidth. Since the gain of the INA-54063 extends down to DC, the frequency response of the amplifier is limited only by the values of the capacitors and choke.

A convenient method for making RF connection to the demonstration board is to use a PCB mounting type of SMA connector (Johanson 142-0701-881, or equivalent). These connectors can be slipped over the edge of the PCB and the center conductors soldered to the input and output lines. The ground pins of the connectors are soldered to the ground plane on the backside of the board. The extra ground pins for the top of the board are not needed and are clipped off.

The measured test results for the 50 Ω input/output example amplifier using the INA-54063 are shown in Figures 12 and 13.

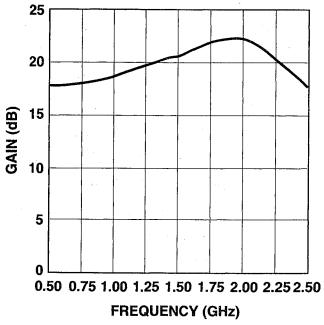


Figure 12. Measured Gain of 50 Ω Example Amplifier.

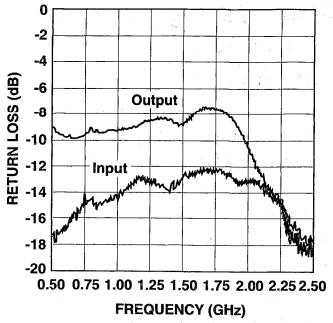


Figure 13. Measured Input and Output Return Loss for 50 Ω Example Amplifier.

PCB Materials

Typical choices for PCB material for low cost wireless applications are FR-4 or G-10 with a thickness of 0.025 or 0.031 inches. A thickness of 0.062 inches is the maximum that is recommended for use with this particular device. The use of a thicker board material increases the inductance of the plated through vias used for RF grounding and may deteriorate circuit performance. Adequate grounding is needed not only to obtain maximum amplifier performance but also to reduce any possibility of instability.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters for this device are shown in Figure 14. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

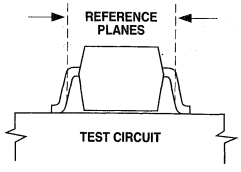


Figure 14. Phase Reference Planes.

SOT-363 PCB Layout

The INA-54063 is packaged in the miniature SOT-363 (SC-70) surface mount package. A PCB pad layout for the SOT-363 package is shown in Figure 15 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding pad parasitics that could impair the high frequency performance of the INA-54063. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads for reference.

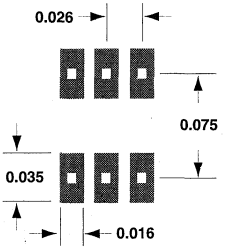


Figure 15. PCB Pad Layout for INA-54063 (dimensions in inches).

Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either "minimum or maximum," "typical," or "standard deviations." The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on of a minimum of 500 parts taken from 3 non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard "bell curve."

Parameters considered to be the most important to system performance are bounded by *minimum* or *maximum* values. For the INA-54063, these parameters are: Power Gain ($|S_{21}|^2$), Noise Figure (NF), and Device Current (I_d). Each of these guaranteed parameters is 100% tested.

Values for most of the parameters in the table of Electrical Specifications that are described by *typical* data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as S-parameters or Noise Parameters and the performance curves, the data represents a nominal part taken from the "center" of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate circuit using the INA-54063, but to also optimize and evaluate trade-offs that affect a complete wireless system, the *standard deviation* (σ) is provided for many of the Electrical Specifications parameters (at 25°C) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean.

Referring to Figure 16 for example, the probability of a parameter being between $\pm 1\sigma$ is 68.3%; between $\pm 2\sigma$ is 95.4%; and between $\pm 3\sigma$ is 99.7%.

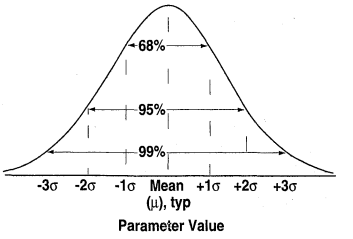


Figure 16. Normal Distribution.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-363 package, will reach solder reflow temperatures faster than those with a greater mass.

The INA-54063 is has been qualified to the time-temperature profile shown in Figure 17. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the

board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235°C.

These parameters are typical for a surface mount assembly process for the INA-54063. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

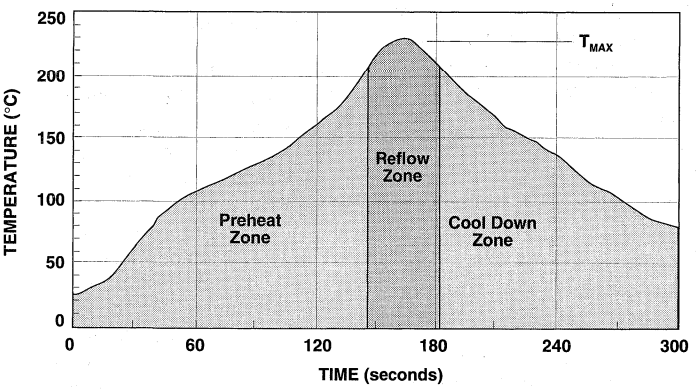


Figure 17. Surface Mount Assembly Profile.

Electrostatic Sensitivity

RFICs are electrostatic discharge (ESD) sensitive devices. Although the INA-54063 is robust in design, permanent damage may occur to these devices if they are subjected to high energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without detection and may result in degradation in performance, reliability, or failure. Electronic devices may be subjected to ESD damage in any of the following areas:

- Storage and handling
- Inspection and testing
- Assembly
- In-circuit use

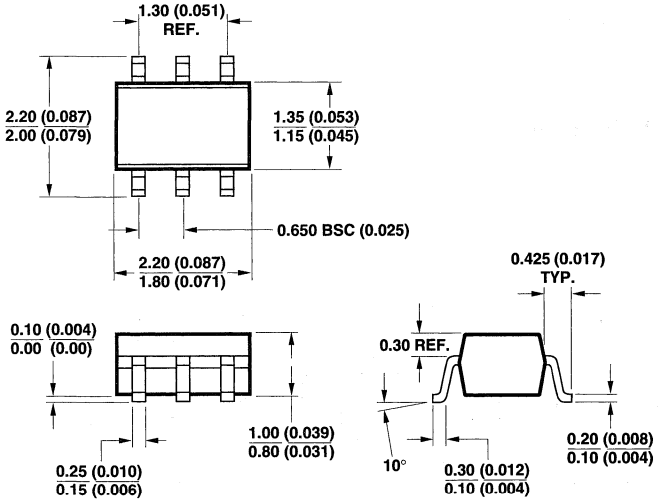
The INA-54063 is an ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, testing, assembling, and using these devices to avoid damage.

INA-54063 Part Number Ordering Information

Part Number	Devices per Container	Container
INA-54063-TR1	3000	7" reel
INA-54063-BLK	100	tape strip in antistatic bag

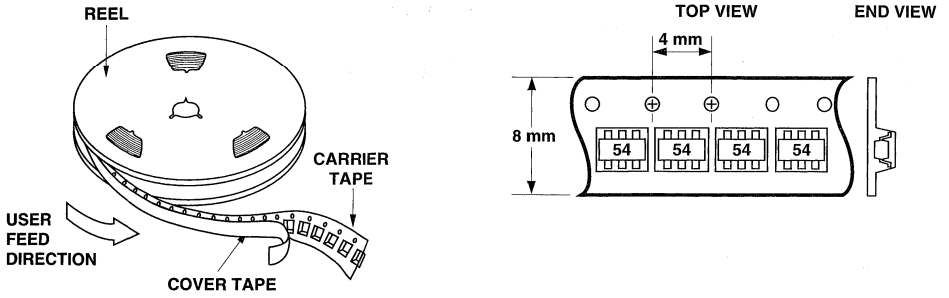
Package Dimensions

Outline 63 (SOT-363/SC-70)



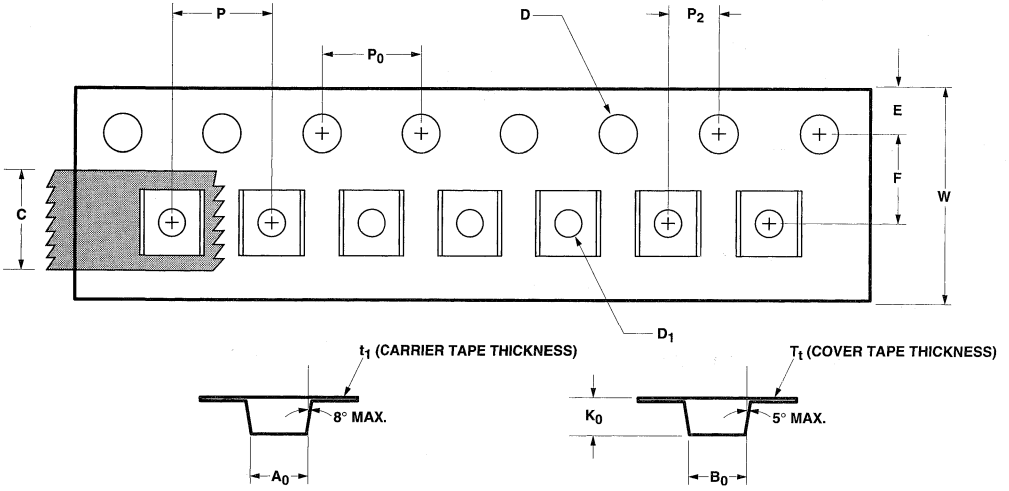
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Device Orientation



Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

Silicon Bipolar MMIC 1.5 GHz Variable Gain Amplifier

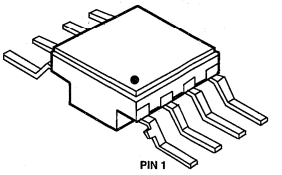
Technical Data

IVA-05128

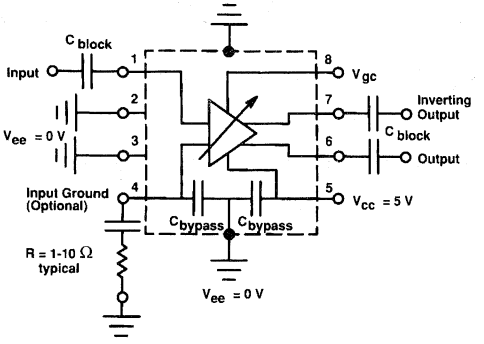
Features

- **50 MHz to 1.5 GHz Bandwidth**
- **Data Rates up to 2.0 Gbit/s**
- **High Gain:** 26 dB Typical
- **Wide Gain Control Range:** 30 dB Typical
- **Differential Output Capability**
- **Bias V_{CC} - V_{ee} = 5 V**
- **5 V TTL Compatible V_{gc} Control Voltage, I_{gc} < 3 mA**
- **Hermetic Ceramic Surface Mount Package**

28 Package



Typical Biasing Configuration and Functional Block Diagram



Description

The IVA-05128 is a variable gain amplifier housed in a miniature ceramic hermetic surface mount package. It is designed for narrow or wide bandwidth commercial, industrial and military applications that require high gain and wide gain control range. The amplifier can be used in a single-ended or differential output configuration. For low frequency applications (<50 MHz) a bypass capacitor and series resistor are connected to pin 4, the AC Input Ground lead.

Typical applications include variable gain amplification for fiberoptic systems at data rates in excess of the 1.24 Gb/s SONET standard, mobile radio and satellite receivers, millimeter wave receiver IF amplifiers and communications receivers.

The IVA series of variable gain amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process. This process uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

5965-9974E

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2,3]	600 mW
Input Power	+14 dBm
V_{gc} - V_{ee}	7 V
Junction Temperature	200°C
Storage Temperature	-65°C to 200°C

Thermal Resistance:[2,4]
θ_{jc} = 50°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 20 mW/°C for T_C >170°C.
4. See MEASUREMENTS section "Thermal Resistance" in Communications Components Catalog, for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: V_{CC} = 5 V, V_{ee} = 0 V, V_{gc} = 0 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain $\|S_{21}\|$[2]	f = 0.5 GHz	dB	20	26	
ΔG_P	Gain Flatness	f = 0.05 to 1.0 GHz	dB		±0.3	
f_{3dB}	3 dB Bandwidth[3]		GHz	1.0	1.5	
GCR	Gain Control Range[4]	f = 0.5 GHz, V_{gc} = 0 to 5 V	dB	25	30	
ISO	Reverse Isolation ($\|S_{12}\|$[2])	f = 0.5 GHz, V_{gc} = 0 to 5 V	dB		45	
VSWR	Input VSWR	f = 0.05 to 1.5 GHz, V_{gc} = 0 to 5 V			1.7:1	
	Output VSWR	f = 0.05 to 1.5 GHz, V_{gc} = 0 to 5 V			1.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		9	
P_{1dB}	Output Power at 1 dB Compression	f = 0.5 GHz	dBm		-2	
IP_3	Output Third Order Intercept Point	f = 0.5 GHz	dBm		8	
t_D	Group Delay	f = 0.5 GHz	psec		400	
I_{CC}	Supply Current		mA	25	35	45

Notes:
1. The recommended operating voltage range for this device is 4 to 6 V. Typical performance as a function of voltage is on the following page.
2. As measured using Input Pin 1 and Output Pin 6; with Output Pin 7 terminated into 50 ohms.
3. Referenced from 50 MHz Gain.
4. The recommended gain control range for these devices for dynamic control is 0 to 4.2 V. Operation at gain control settings above 4.2 V may result in gain increase rather than gain decrease.

IVA-05128 Typical Performance, T_A = 25°C, V_{CC} = 5 V, V_{ee} = 0 V

(unless otherwise noted)

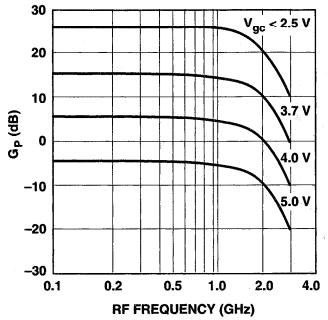


Figure 1. Typical Variable Gain vs. Frequency.

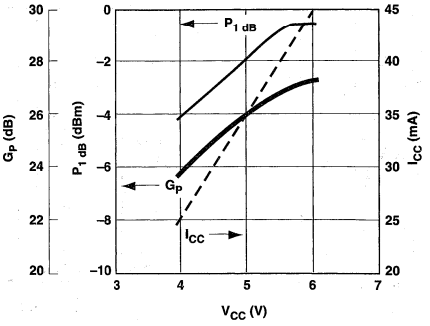


Figure 2. Power Gain and $P_{1\ dB}$ at 0.5 GHz and I_{CC} vs. Bias Voltage with V_{gc} = 0 V.

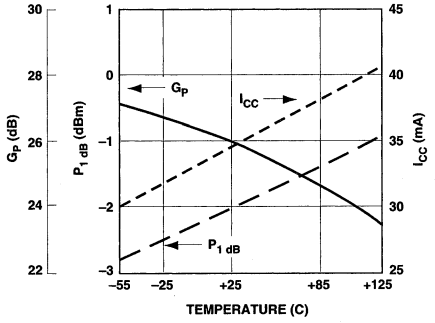


Figure 3. Power Gain and $P_{1\ dB}$ at 0.5 GHz and I_{CC} vs. Case Temperature with V_{gc} = 0 V.

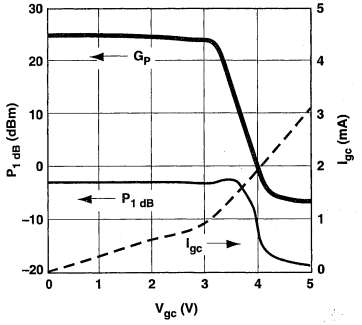


Figure 4. Power Gain and $P_{1\ dB}$ at 0.5 GHz and I_{gc} vs. Gain Control Voltage.

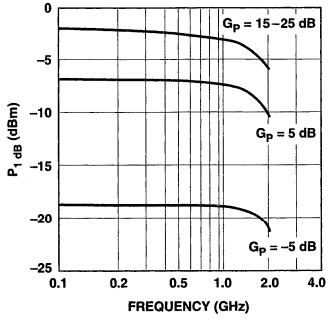


Figure 5. $P_{1\ dB}$ vs. Frequency.

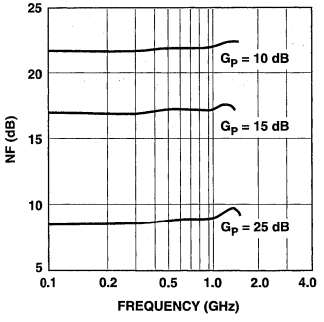


Figure 6. Noise Figure vs. Frequency.

IVA-05128 Typical Performance, T_A = 25°C, V_{CC} = 5 V, V_{ee} = 0 V, continued

(unless otherwise noted)

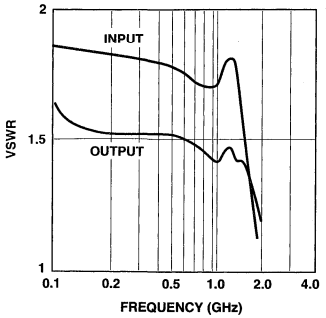


Figure 7. Input and Output VSWR vs. Frequency, V_{gc} = 0–5 V.

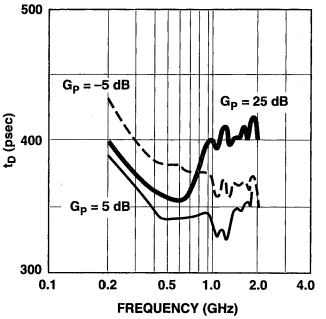
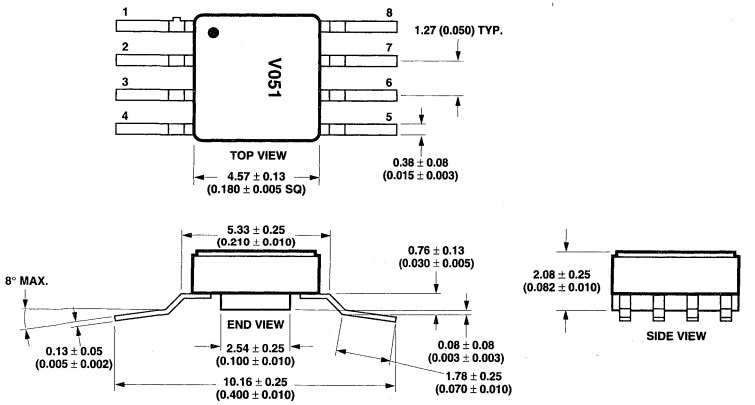


Figure 8. Group Delay vs. Frequency.

28 Package Outline



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Silicon Bipolar MMIC 1.5 GHz Variable Gain Amplifier

Technical Data

IVA-05208

Features

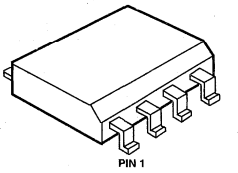
- **Differential Input and Output Capability**
- **DC to 1.5 GHz Bandwidth; 2.0 Gb/s Data Rates**
- **High Gain:** 30 dB Typical
- **Wide Gain Control Range:** 30 dB Typical
- **5 V Bias**
- **5 V V_{gc} Control Voltage, I_{gc} < 3 mA**
- **Fast Gain Control Response:** < 10 ns Typical
- **Low Cost Plastic Surface Mount Package**

Description

The IVA-05208 is a variable gain amplifier housed in a miniature low cost plastic surface mount package. This device can be used in any combination of single-ended or differential inputs or outputs (see Functional Block Diagram). The lowest frequency of operation is limited only by the values of user selected blocking and bypass capacitors.

Typical applications include variable gain amplification for fiber optic systems (e.g., SONET) with data rates up to 2.0 Gb/s, mobile radio and satellite receivers, millimeter wave receiver IF amplifiers and communication receivers.

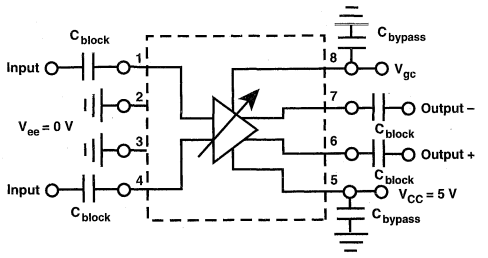
SO-8 Package



The IVA series of variable gain amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process. This process uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Typical Biasing Configuration and Functional Block Diagram

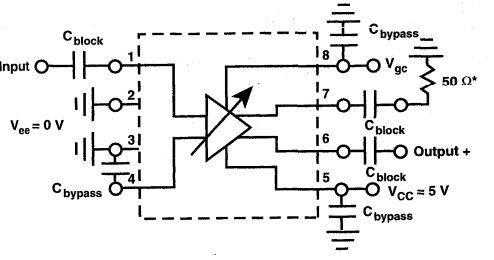
Differential Input/Differential Output



C_{bypass} = 1000 pF typical

Good grounding of Pins 2, 3 is critical for proper operation and good VSWR performance of this part.

Single Ended Input/Single Ended Output



* Optional: For Single-Ended Output operation, Pin 7 may be left unterminated (no C_{block} or 50 Ω)

5965-9682E

IVA-05208 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{CC}-V_{ee}	Device Voltage	V	8
	Power Dissipation[2,3]	mW	600
	Input Power	dBm	+14
V_{gc}-V_{ee}		V	7
T_J	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
θ_{jc} = 150°C/W

Notes:
1. Permanent damage may occur is any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.67 mW/°C for T_C > 60°C.

IVA-05208 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions:[2] V_{CC} = 5 V, V_{ee} = 0 V, V_{gc} = 0 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
Gp	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz	dB	25	30	
ΔGp	Gain Flatness	f = 0.05 to 1.0 GHz	dB		± 0.8	
f_{3dB}	3 dB Bandwidth[3]		GHz	1.2	1.8	
GCR	Gain Control Range[4]	f = 0.5 GHz V_{gc} = 0 to 5 V	dB	25	30	
ISO	Reverse Isolation ($\|S_{21}\|^2$)	f = 0.5 GHz V_{gc} = 0 to 5 V	dB		45	
VSWR	Input VSWR	f = 0.05 to 1.5 GHz V_{gc} = 0 to 5 V			2.0:1	
	Output VSWR	f = 0.05 to 1.5 GHz V_{gc} = 0 to 5 V			2.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		9	
P_{1dB}	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		-3	
V_{OUT}	Peak-to-Peak Single-Ended Output Voltage	f = 0.5 GHz	mVpp		450	
IP_3	Output Third Order Intercept Point	f = 0.5 GHz	dBm		7	
t_D	Group Delay	f = 0.5 GHz	psec		400	
I_{CC}	Supply Current		mA	25	35	50

Notes:
1. The recommended operating voltage range for this device is 4 to 6 V. Typical performance as a function of voltage is on the following page.
2. As measured using Input Pin 1 and Output Pin 6, with Output Pin 7 terminated into 50 ohms and Input Pin 4 at AC ground.
3. Referenced from 50 MHz Gain.
4. The recommended gain control range for these devices for dynamic control is 0 to 4.2 V. Operation at gain control settings above 4.2V may result in gain increase rather than gain decrease.

IVA-05208 Typical Performance, $T_A = 25°C$, $V_{CC} = 5$ V, $V_{ee} = 0$ V

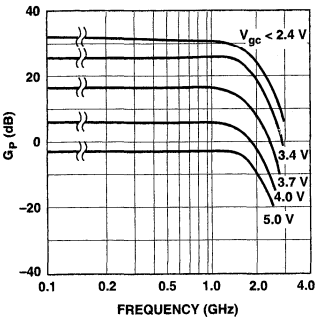


Figure 1. Typical Variable Gain vs. Frequency.

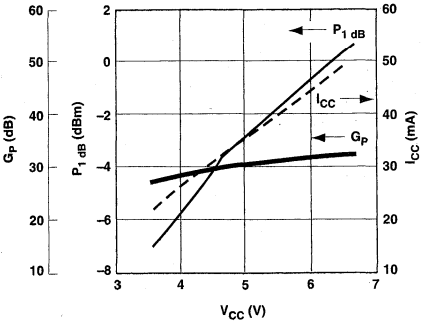


Figure 2. Power Gain and $P_{1\ dB}$ at 0.5 GHz and I_{CC} vs. Bias Voltage with $V_{gc} = 0$ V.

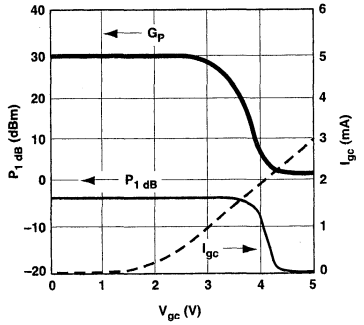


Figure 3. Power Gain and $P_{1\ dB}$ at 0.5 GHz and I_{gc} vs. Gain Control Voltage.

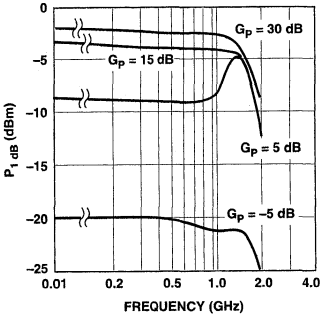


Figure 4. $P_{1\ dB}$ vs. Frequency.

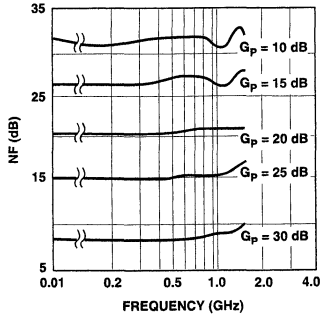


Figure 5. Noise Figure vs. Frequency.

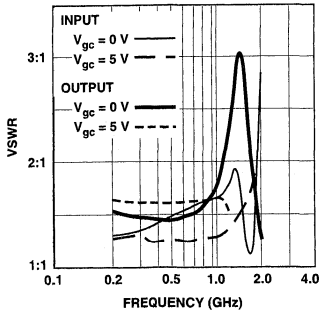


Figure 6. Input and Output VSWR vs. Frequency, V_{gc} = 0–5 V.

IVA-05208 Typical Performance, continued, $T_A = 25°C$, $V_{CC} = 5$ V, $V_{ee} = 0$ V

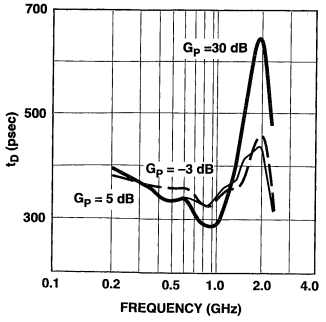


Figure 7. Group Delay vs. Frequency.

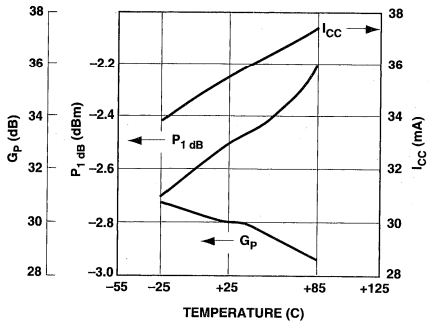
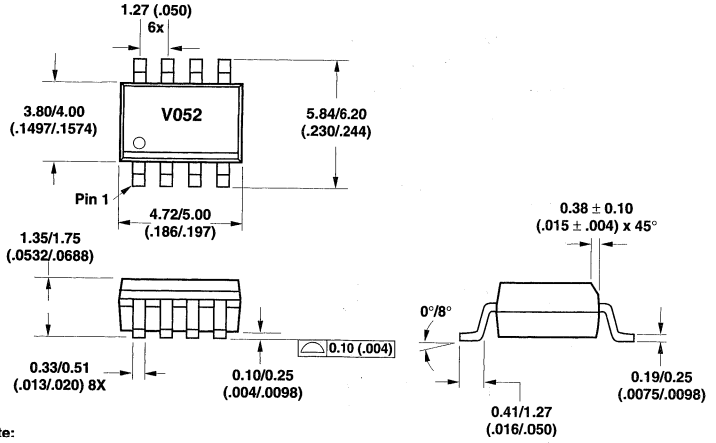


Figure 8. Power Gain and $P_{1\ dB}$ at 0.5 GHz and I_{CC} vs. Case Temperature with $V_{gc} = 0$ V.

IVA-05208 Part Number Ordering Information

Part Number	Number of Devices	Container
IVA-05208-TR1	1,000	7" Reel
IVA-05208-STR	10	Strip

SO-8 Package Dimensions



Note:
1. Dimensions are shown in millimeters (inches).

HEWLETT® PACKARD

Silicon Bipolar MMIC 1.5 GHz Variable Gain Amplifier Differential Option

Technical Data

IVA-05228

Features

- **Differential Input and Output Capability**
- **DC to 1.5 GHz Bandwidth; 2.0 Gb/s Data Rates**
- **High Gain:** 30 dB Typical
- **Wide Gain Control Range:** 30 dB Typical
- **5 V Bias**
- **5 V V_{gc} Control Voltage, I_{gc} < 3 mA**
- **Fast Gain Control Response:** < 10 ns Typical
- **Hermetic Ceramic Package**

Applications

- **LNA or Gain Stage for 2.4 GHz and 5.7 GHz ISM Bands**
- **Front End Amplifier for GPS Receivers**
- **LNA or Gain Stage for PCN and MMDS Applications**
- **C-Band Satellite Receivers**
- **Broadband Amplifier for Instrumentation**

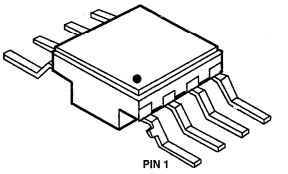
Description

The IVA-05228 is a variable gain amplifier housed in a miniature ceramic hermetic surface mount package. This device can be used in any combination of single-ended or differential inputs or outputs (see Functional Block Diagram). The lowest frequency of operation is limited only by the values of user selected blocking and bypass capacitors.

Typical applications include variable gain amplification for fiber optic systems (e.g., SONET) with data rates up to 2.0 Gb/s, mobile radio and satellite receivers, millimeter wave receiver IF amplifiers and communication receivers.

The IVA series of variable gain amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}

28 Package



ISOSAT™-I silicon bipolar process. This process uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{CC}-V_{ee}	Device Voltage	V	8
	Power Dissipation[2,3]	mW	600
	Input Power	dBm	+14
V_{gc}-V_{ee}		V	7
T_J	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to 200

Thermal Resistance: [2,4]
θ_{jc} = 50°C/W

Notes:
1. Permanent damage may occur is any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 20 mW/°C for T_C > 170°C.
4. See MEASUREMENTS section "Thermal Resistance" in Communications Components Catalog for more information.

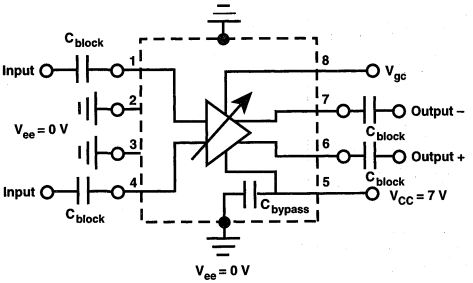
IVA-05228 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions:[2] V_{CC} = 5 V, V_{ee} = 0 V, V_{gc} = 0 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
Gp	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz	dB	25	30	
ΔGp	Gain Flatness	f = 0.05 to 1.0 GHz	dB		± 0.5	
f_{3dB}	3 dB Bandwidth[3]		GHz	1.0	1.5	
GCR	Gain Control Range[4]	f = 0.05 GHz V_{gc} = 0 to 5 V	dB	25	30	
ISO	Reverse Isolation ($\|S_{21}\|^2$)	f = 0.05 GHz V_{gc} = 0 to 5 V	dB	25	30	
VSWR	Input VSWR	f = 0.05 to 1.5 GHz V_{gc} = 0 to 5 V			1.7:1	
	Output VSWR	f = 0.05 to 1.5 GHz V_{gc} = 0 to 5 V			1.5:1	
NF_{50}	50 Ω Noise Figure	f = 0.5 GHz	dB		9	
P_{1dB}	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		-3	
V_{OUT}	Peak-to-Peak Single-Ended Output Voltage	f = 0.5 GHz	mVpp		450	
IP_3	Output Third Order Intercept Point	f = 0.5 GHz	dBm		7	
t_D	Group Delay	f = 0.5 GHz	psec		400	
I_{CC}	Supply Current		mA	25	35	45

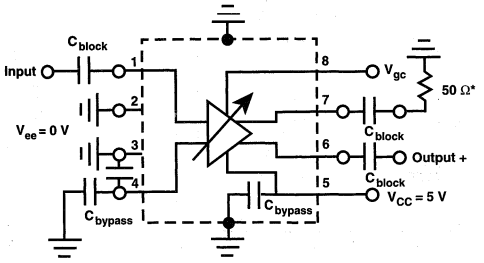
Notes:
1. The recommended operating voltage range for this device is 4 to 6 V. Typical performance as a function of voltage is on the following page.
2. As measured using Input Pin 1 and Output Pin 6, with Output Pin 7 terminated into 50 ohms and Input Pin 4 at AC ground.
3. Referenced from 50 MHz Gain.
4. The recommended gain control range for these devices for dynamic control is 0 to 4.2 V. Operation at gain control settings above 4.2V may result in gain increase rather than gain decrease.

Typical Biasing Configuration and Functional Block Diagram

Differential Input/Differential Output



Single Ended Input/Single Ended Output



* Optional: For Single-Ended Output operation, Pin 7 may be left unterminated (no C_{block} or 50 Ω)
C_{bypass} = 1000 pF typical
Good grounding of Pins 2, 3 is critical for proper operation and good VSWR performance of this part.

IVA-05228 Typical Performance, T_A = 25°C, V_{CC} = 5 V, V_{ee} = 0 V

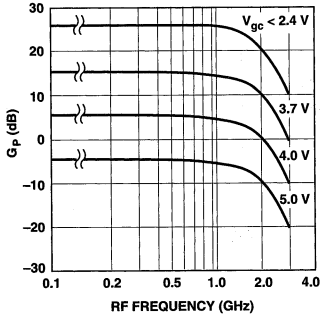


Figure 1. Typical Variable Gain vs. Frequency.

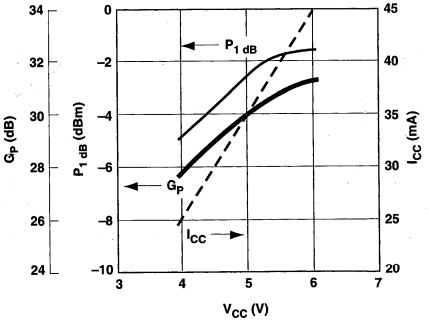


Figure 2. Power Gain and $P_{1\ dB}$ at 0.5 GHz and I_{CC} vs. Bias Voltage with V_{gc} = 0 V.

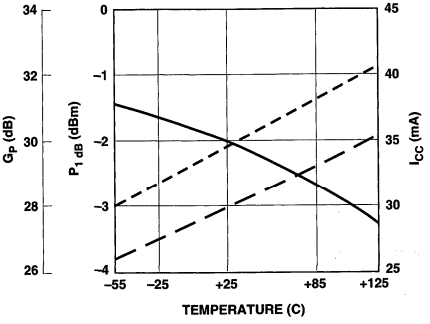


Figure 3. Power Gain and $P_{1\ dB}$ at 0.5 GHz and I_{CC} vs. Case Temperature with V_{gc} = 0 V.

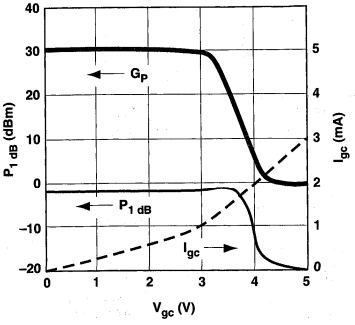


Figure 4. Power Gain and $P_{1\ dB}$ at 0.5 GHz and I_{gc} vs. Gain Control Voltage.

IVA-05228 Typical Performance, continued, $T_A = 25°C$, $V_{CC} = 5$ V, $V_{ee} = 0$ V

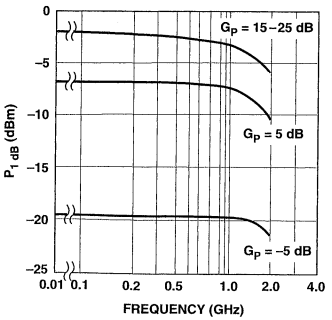


Figure 5. $P_{1\,dB}$ vs. Frequency.

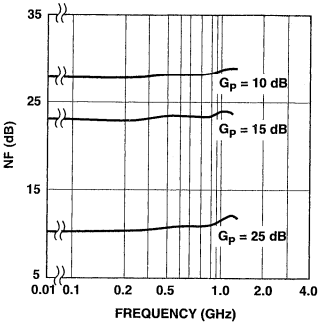


Figure 6. Noise Figure vs. Frequency.

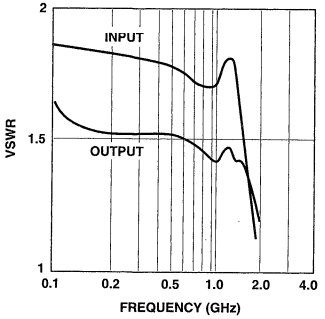


Figure 7. Input and Output VSWR vs. Frequency, V_{gc} = 0–5 V.

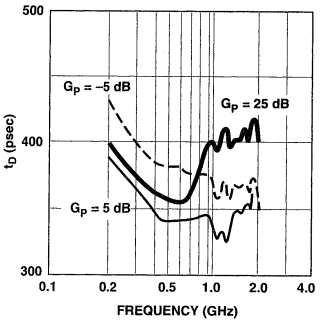
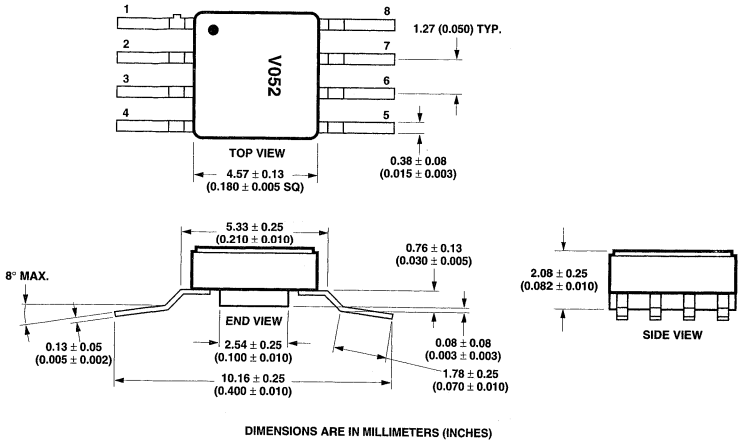


Figure 8. Group Delay vs. Frequency.

28 Package Outline



HEWLETT® PACKARD

Silicon Bipolar MMIC 2.5 GHz Variable Gain Amplifier

Technical Data

IVA-14208
IVA-14228

Features

- **Differential Input and Output Capability**
- **DC to 2.5 GHz Bandwidth; 3.4 Gbits/s Data Rates**
- **High Gain:** 24 dB Typical
- **Wide Gain Control Range:** 34 dB Typical
- **6 V Bias**
- **5 V V_{GC} Control Range, I_{GC} <3 mA**
- **Fast Gain Response:** <10 nsec Typical
- **IVA-14208:** Low Cost Plastic Surface Mount Package
- **IVA-14228:** Hermetic Ceramic Surface Mount Package

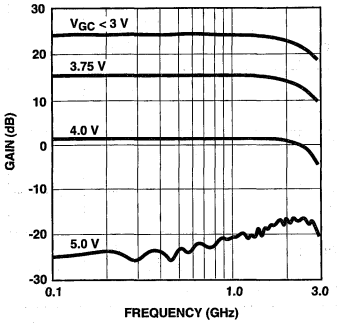


Figure 1. IVA-14228 Typical Variable Gain vs. Frequency and V_{GC} at V_{CC} = 6 V, T_{case} = 25°C.

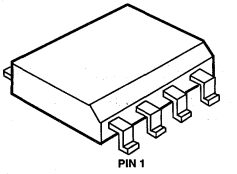
Description

The IVA-14 series MMICs are variable gain amplifiers. The IVA-14208 is housed in a miniature low cost plastic surface mount package. The IVA-14228 is housed in a miniature hermetic ceramic surface mount package. Both devices can be used in any combination of single-ended or differential inputs or outputs (see Functional Block Diagram). The lowest frequency of operation is limited only by the values of user selected blocking and bypass capacitors.

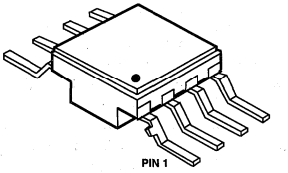
Typical applications include variable gain amplification or limiting for fiber optic systems (e.g. SONET) with data rates up to 3.4 Gbits/s, mobile radio and satellite receivers, millimeter wave receiver IF amplifiers and communications receivers.

The IVA series of variable gain amplifiers is fabricated using Hewlett-Packard's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-1 silicon bipolar process. This process uses nitride self-alignment, sub-micrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

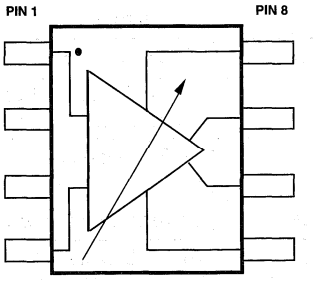
IVA-14208
Plastic SO-8 Package



IVA-14228
Ceramic '28' Package



Functional Block Diagram and Pin Configuration



PIN DESCRIPTION	
1. INPUT +	8. V_{GC}
2. V_{EE}, AC GROUND	7. OUTPUT +
3. V_{EE}, AC GROUND	6. OUTPUT –
4. INPUT –	5. V_{CC}

IVA-14228 PACKAGE BOTTOM IS V_{EE} AC GROUND.

IVA-14208, -14228 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	IVA-14208	IVA-14228
V_{CC}-V_{EE}	Device Voltage, T_{case} = 25°C	Volts	12	12
P_{in}	Input Power, T_{case} = 25°C	dBm	13	13
V_{GC}-V_{EE}	Control Voltage, T_{case} = 25°C	Volts	10	10
T_j	Junction Temperature+	°C	150	200
T_{stg}	Storage Temperature	°C	-65 to +150	-65 to +200
P_t	Total Device Dissipation	mW	1000[2]	1000[3]

Thermal Resistance:

IVA-14208 Thermal Resistance Junction to Case[4]: θ_{jc} = 68°C/W
IVA-14228 Thermal Resistance Junction to Case[4]: θ_{jc} = 63°C/W

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_{case} = 25°C. Derate at 14.7 mW/°C for T_{case} > 82°C.
3. T_{case} = 25°C. Derate at 15.9 mW/°C for T_{case} > 137°C.
4. T_j = 150°C.

IVA-14208, -14228 Guaranteed Electrical Specifications All measurements reflect single-ended (unbalanced) performance. T_{case} = 25°C. V_{CC} = 6 V, V_{EE} = 0 V, V_{GC} = 0 V, Z_L = 50 Ω

			IVA-14208			IVA-14228		
Symbol	Parameter	Units	Min.	Typ.	Max.	Min.	Typ.	Max.
GP	Power Gain ($\|S_{21}\|^2$), f = 1 GHz	dB	20	24		22	24	
ΔGP	Gain Flatness, f = 0.05 to 2 GHz	dB		±1.2			±0.7	
f_{3dB}	3 dB Bandwidth	GHz	2.0	2.5		2.2	2.5	
GCR	Gain Control Range[2], f = 1 GHz, V_{GC} = 0 to 5 V	dB	30	34		30	34	
ISO	Reverse Isolation ($\|S_{12}\|^2$), f = 1 GHz, V_{GC} = 0 to 5 V	dB		37			40	
VSWR	Input VSWR, f = 0.05 to 2.0 GHz, V_{GC} = 0 to 5 V			2:1			2:1	
	Output VSWR, f = 0.05 to 2.0 GHz, V_{GC} = 0 to 5 V			2:1			2.5:1	
NF	50 Ω Noise Figure, f = 1 GHz	dB		9.0			9.0	
P_{1dB}	Output Power at 1 dB Gain Compression f = 1 GHz	dBm		-2.0			-2.0	
V_{OUT}	Pk-Pk Single-ended Output Voltage, f = 1 GHz	mVpp		450			450	
IP_3	Third Order Intercept Point, f = 1 GHz	dBm		8			8	
t_D	Group Delay, f = 1 GHz	psec		450			450	
I_{cc}	Supply Current	mA	28	38	48	28	38	48

Notes:
1. The recommended operating voltage range for these devices is 5 to 8 V. Typical performance as a function of voltage is shown in the graphs on the following pages.
2. The recommended gain control range for these devices for dynamic control is 0 to 4.2 V. Operation at gain control settings above 4.2 V may result in gain control increase rather than gain decrease. See figures 4 and 19.

IVA-14228 Typical Performance Curves

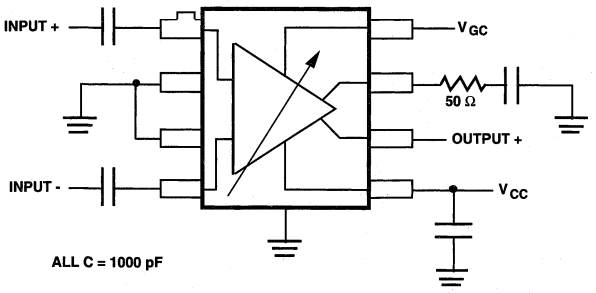


Figure 2. IVA-142X8 Connection Diagram Showing Balanced Inputs and Unbalanced Outputs. Inputs and Outputs May Be Either Balanced or Unbalanced.

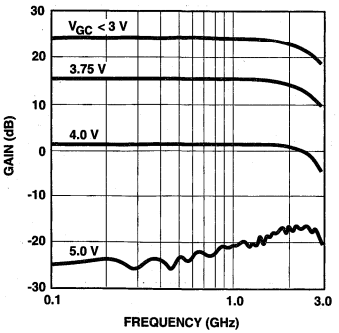


Figure 3. IVA-14228 Gain vs. Frequency and V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

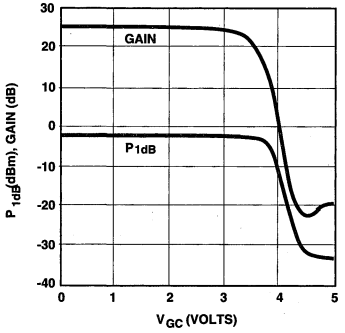


Figure 4. IVA-14228 P_{1dB} and Gain vs. V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

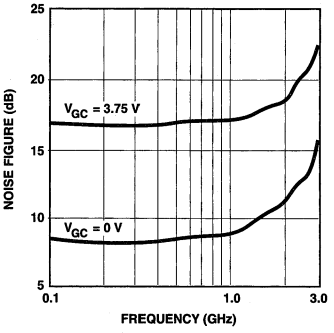


Figure 5. IVA-14228 Noise Figure vs. Frequency and V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

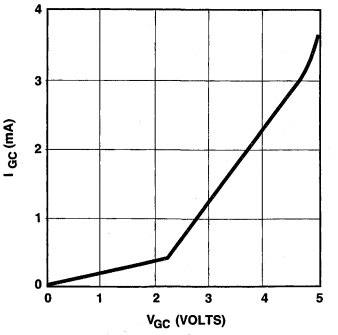


Figure 6. IVA-14228 I_{GC} vs. V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

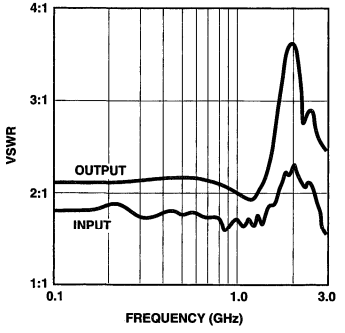


Figure 7. IVA-14228 VSWR vs. Frequency; V_{CC} = 6 V, V_{GC} = 0 V, T_{case} = 25°C.

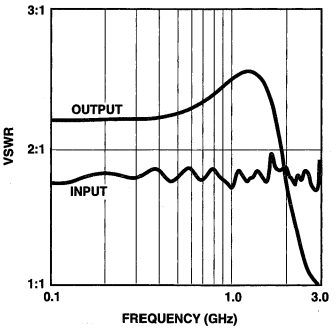


Figure 8. IVA-14228 VSWR vs. Frequency; V_{CC} = 6 V, V_{GC} = 5 V, T_{case} = 25°C.

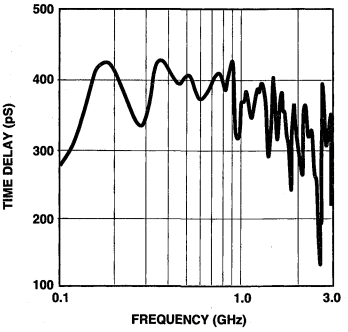


Figure 9. IVA-14228 Group Delay vs. Frequency; V_{GC} = 0 V, V_{CC} = 6 V, T_{case} = 25°C.

IVA-14228 Typical Performance Curves (cont.)

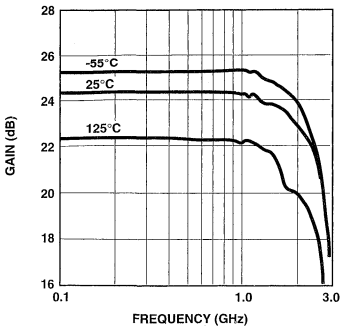


Figure 10. IVA-14228 Gain vs. Frequency and Temperature; V_{CC} = 6 V, V_{GC} = 0 V.

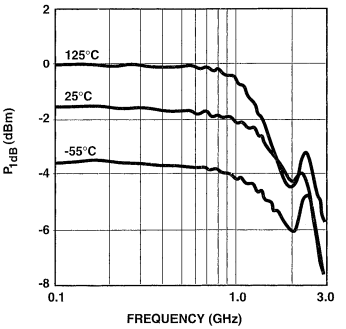


Figure 11: IVA-14228 P_{1dB} vs. Frequency and Temperature; V_{CC} = 6 V, V_{GC} = 0 V.

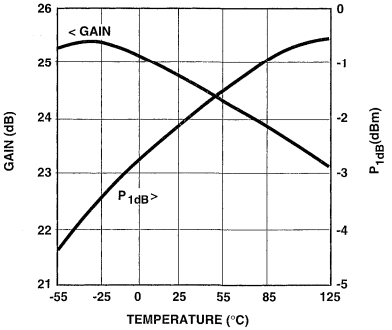


Figure 12. IVA-14228 Gain and P_{1dB} vs. Temperature; V_{CC} = 6 V, V_{GC} = 0 V, Frequency = 1 GHz.

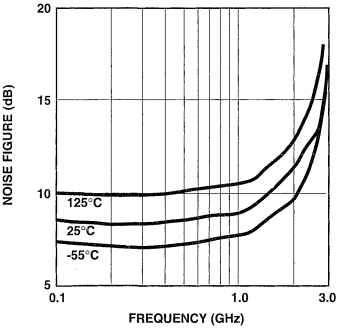


Figure 13. IVA-14228 Noise Figure vs. Frequency and Temperature; V_{CC} = 6 V, V_{GC} = 0 V.

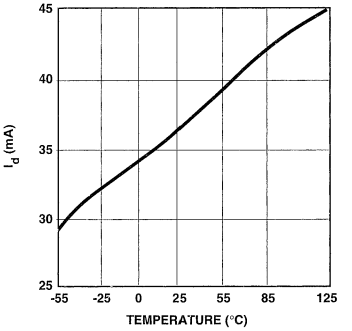


Figure 14. IVA-14228 I_{CC} vs. Temperature; V_{CC} = 6 V, V_{GC} = 0 V, Frequency = 1 GHz.

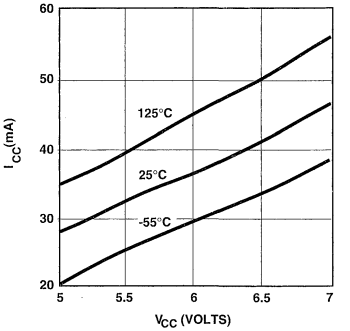


Figure 15. IVA-14228 I_{CC} vs. V_{CC} and Temperature; V_{GC} = 0 V.

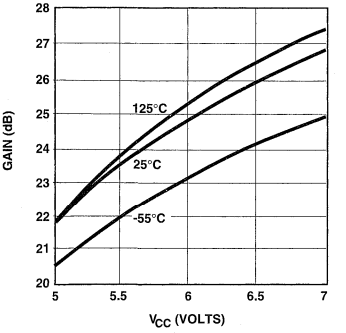


Figure 16. IVA-14228 Gain vs. V_{CC} and Temperature; V_{GC} = 0 V, Frequency = 1 GHz.

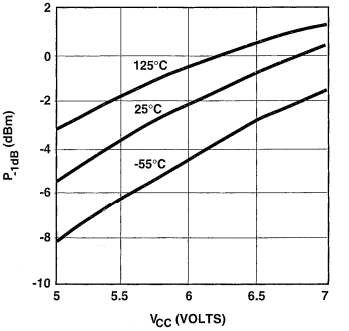


Figure 17. IVA-14228 P_{1dB} vs. V_{CC} and Temperature; V_{GC} = 0 V, Frequency = 1 GHz.

IVA-14208 Typical Performance Curves

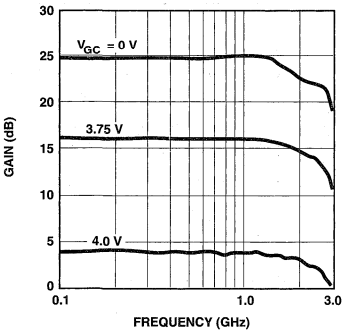


Figure 18. IVA-14208 Gain vs. Frequency and V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

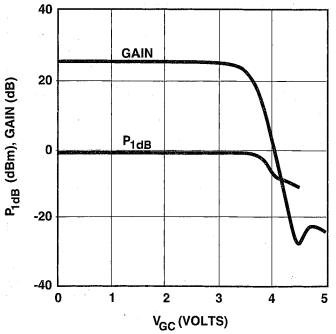


Figure 19. IVA-14208 Gain and P_{1dB} vs. V_{GC}; V_{CC} = 6 V, Frequency = 1 GHz, T_{case} = 25°C.

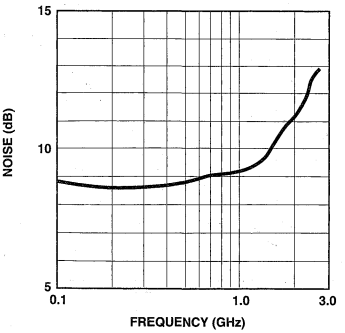


Figure 20. IVA-14208 Noise Figure vs. Frequency; V_{CC} = 6 V, V_{GC} = 0 V, T_{case} = 25°C.

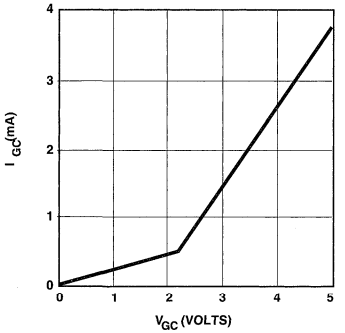


Figure 21. IVA-14208 I_{GC} vs. V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

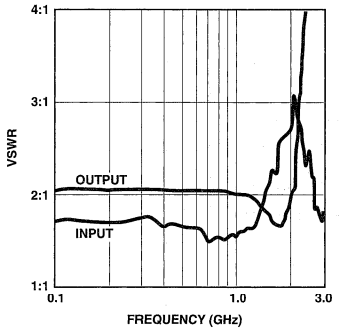


Figure 22. IVA-14208 VSWR vs. Frequency; V_{CC} = 6 V, V_{GC} = 0 V, T_{case} = 25°C.

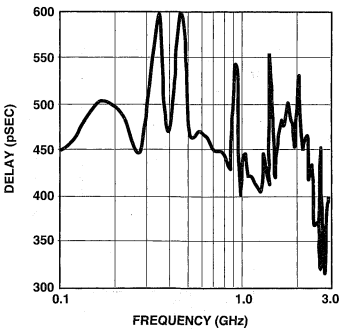


Figure 23. IVA-14208 Group Delay vs. Frequency; V_{CC} = 6 V, V_{GC} = 0 V, T_{case} = 25°C.

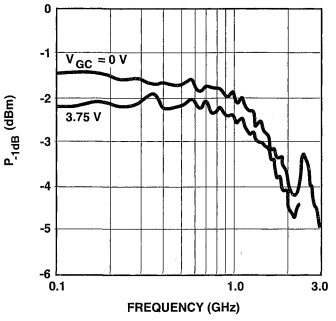


Figure 24. IVA-14208 P_{1dB} vs. Frequency and V_{GC}; V_{CC} = 6 V, Frequency = 1 GHz, T_{case} = 25°C.

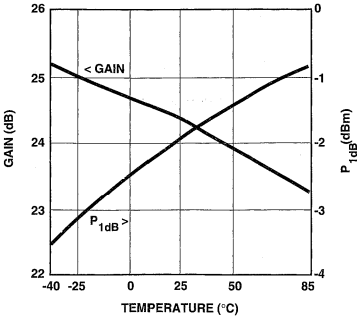


Figure 25. IVA-14208 Gain and P_{1dB} vs. Temperature; V_{CC} = 6 V, V_{GC} = 0 V, Frequency = 1 GHz.

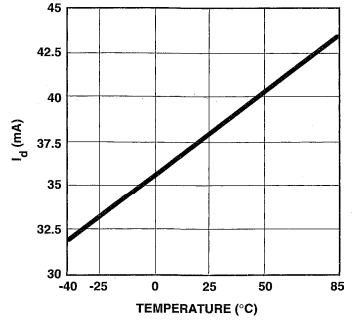


Figure 26. IVA-14208 I_{CC} vs. Temperature; V_{CC} = 6 V, V_{GC} = 0 V.

IVA-14208 Typical Performance Curves (cont.)

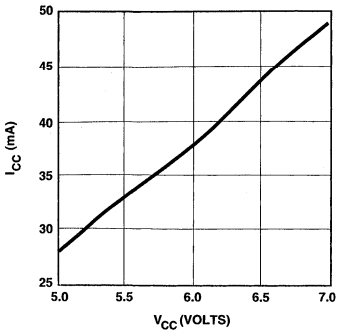


Figure 27. IVA-14208 I_{CC} vs. V_{CC}; V_{GC} = 0 V, T_{case} = 25°C.

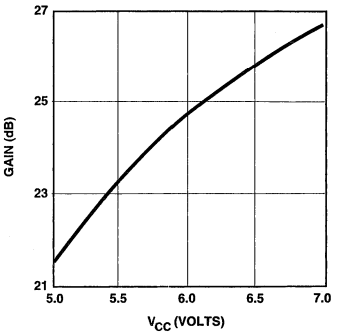


Figure 28. IVA-14208 Gain vs. V_{CC}; V_{GC} = 0 V, Frequency = 1 GHz, T_{case} = 25°C.

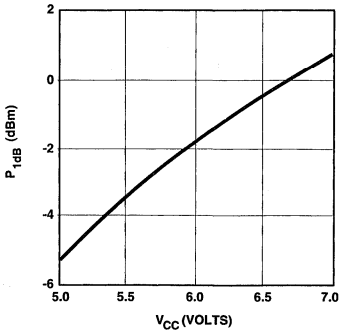


Figure 29. IVA-14208 P_{1dB} vs. V_{CC} ; V_{GC} = 0 V, Frequency = 1 GHz, T_{case} = 25°C.

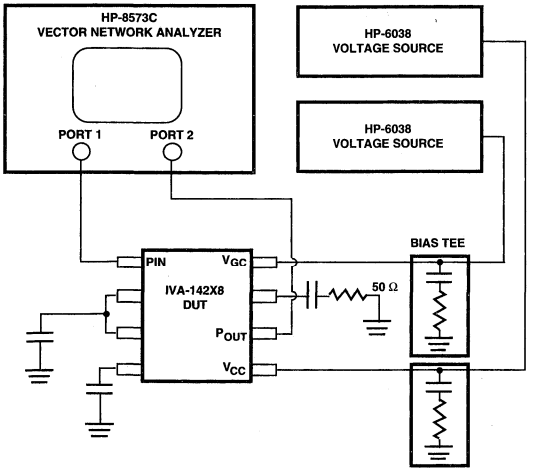
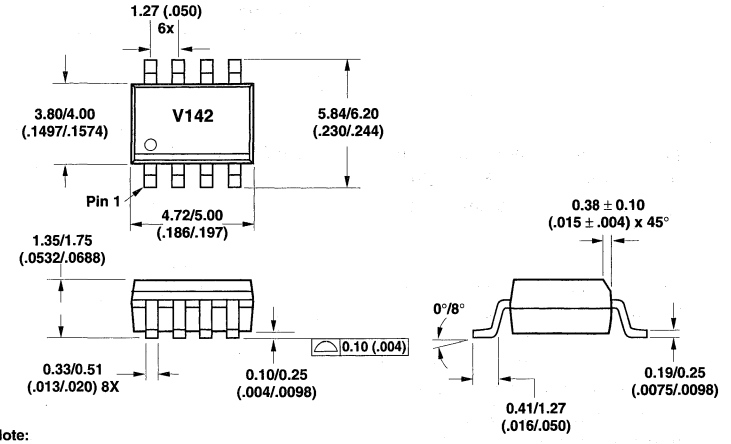


Figure 30. Test Equipment Setup for Measuring Performance of the IVA-142X8.

IVA-14208, -14228 Part Number Ordering Information

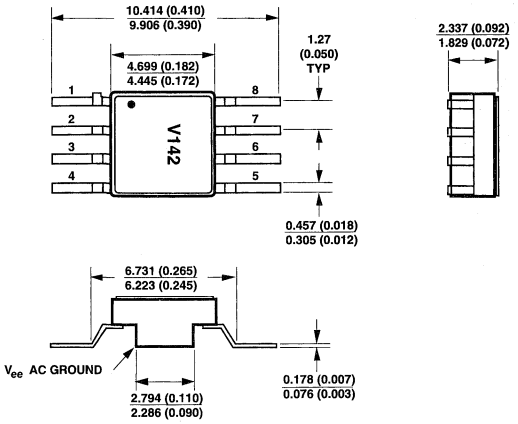
Part Number	Container Type	Qty. per Container
IVA-14208-STR	BIP Strip	1
IVA-14208-TR1	7" Reel	1000
IVA-14228-STR	BIP Strip	1

SO-8 Package Dimensions for IVA-14208



Note:
1. Dimensions are shown in millimeters (inches).

28 Package Dimensions for IVA-14228



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSIONS ARE IN INCHES.

HEWLETT® PACKARD

2 – 6 GHz Cascadable GaAs MMIC Amplifier

Technical Data

MGA-64135

Features

- **Cascadable 50 Ω Gain Block**
- **Broadband Performance: 2–6 GHz**
  12.0 dB Typical Gain
  ±0.8 dB Gain Flatness
  12.0 dBm $P_{1\ dB}$
- **Single Supply Bias**
- **Cost Effective Ceramic Microstrip Package**

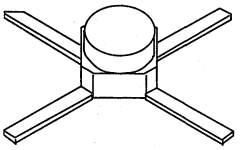
Description

The MGA-64135 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This device is designed for use as a general purpose 50 ohm gain block in the 2 to 6 GHz frequency range. Typical applications include narrow and broadband IF and RF amplifiers for commercial, industrial, and military requirements.

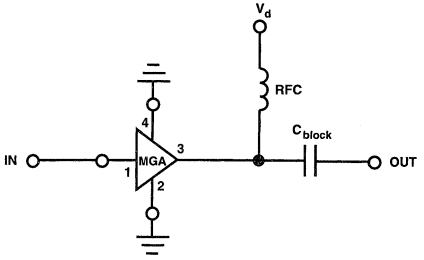
This MMIC is a cascade of two stages, each utilizing shunt feedback to establish a broadband impedance match. The source of each stage is AC grounded to allow biasing from a single positive power supply. The interstage blocking capacitor as well as a resistive "self-bias" network are included on chip.

The die is fabricated using HP's nominal .5 micron recessed Schottky-barrier-gate, gold metallization and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

35 Micro-X Package



Typical Biasing Configuration



MGA-64135 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Device Voltage	V	12
P_{diss}	Total Power Dissipation[2]	mW	650
P_{in}	CW RF Input Power	dBm	+13
T_{ch}	Channel Temperature	°C	175
T_{STG}	Storage Temperature[3]	°C	-65 to 175

Thermal Resistance:	θ_{jc} = 150°C/W[4]; T_{CH} = 150°C
Liquid Crystal Measurement:	1 μm Spot Size[5]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Derate linearly at 8.3 mW/°C for T_{CASE} > 103°C.
3. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
4. The thermal resistance value is based on measurements taken with the device soldered to a 25 mil Teflon PCB.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

MGA-64135 Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 10 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 2 to 6 GHz	dB	10.0	12.0	
ΔG_P	Gain Flatness	f = 2 to 6 GHz	dB		±1.20	
—	Gain Variation vs. Temperature T_{CASE} = –25°C to +85°C	f = 2 to 6 GHz	dB		±0.5	
VSWR	Input VSWR	f = 2 to 6 GHz			1.5:1	2.0:1
	Output VSWR	f = 2 to 6 GHz			1.4:1	2.0:1
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 2 to 6 GHz	dBm	10.0	12.0	
NF	50 Ω Noise Figure	f = 2 to 6 GHz	dB		7.5	
—	Reverse Isolation ($\|S_{21}\|^2$)	f = 2 to 6 GHz	dB		35	
I_d	Device Current		mA	35	50	65

MGA-64135 Typical Performance, T_A = 25°C

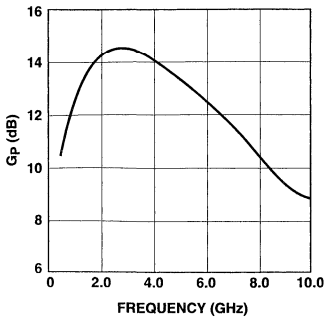


Figure 1. Power Gain vs. Frequency, V_d = 10 V.

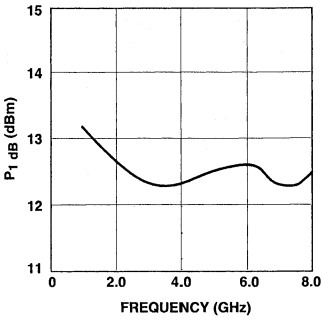


Figure 2. Output Power @ 1 dB Gain Compression vs. Frequency, V_d = 10 V.

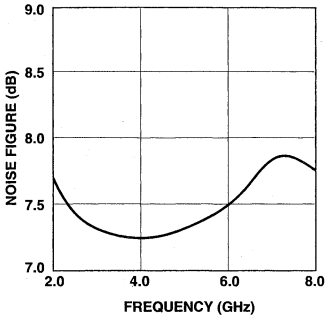


Figure 3. Noise Figure vs. Frequency, V_d = 10 V.

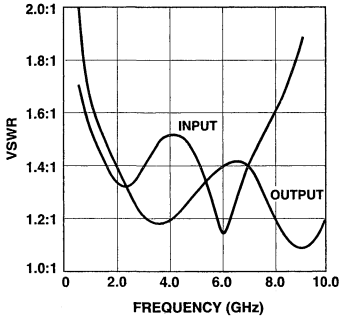
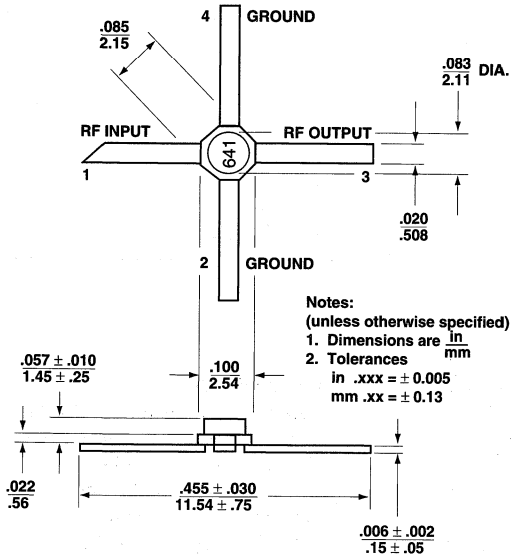


Figure 4. VSWR vs. Frequency, V_d = 10 V.

MGA-64135 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, V_d = 10 V)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.27	–38	10.6	3.38	174	–31.0	.028	–13	.38	–41
1.0	.18	–44	12.9	4.42	–9	–33.1	.022	–20	.26	–48
2.0	.14	–67	14.3	5.21	–54	–34.9	.018	–19	.16	–59
3.0	.17	–91	14.5	5.33	–93	–37.1	.014	–21	.11	–75
4.0	.20	–105	14.2	5.11	–131	–37.8	.013	–15	.11	–71
5.0	.18	–114	13.6	4.79	–167	–37.3	.014	–10	.14	–57
6.0	.07	–162	12.8	4.35	157	–38.5	.012	–1	.17	–41
7.0	.15	96	11.8	3.89	123	–36.0	.016	3	.16	–42
8.0	.23	76	10.8	3.46	92	–34.3	.019	4	.10	–54
9.0	.32	63	9.5	2.98	63	–29.3	.034	12	.04	159
10.0	.43	52	8.6	2.68	38	–27.6	.041	–11	.09	116

35 Micro-X Package Dimensions



HEWLETT® PACKARD

0.1–6 GHz 3 V, 14 dBm Amplifier

Technical Data

MGA-81563

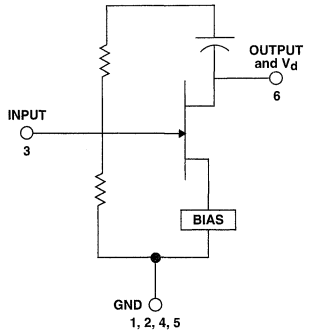
Features

- **+14.8 dBm P_{1dB} at 2.0 GHz**
  +17 dBm P_{sat} at 2.0 GHz
- **Single +3V Supply**
- **2.8 dB Noise Figure at 2.0 GHz**
- **12.4 dB Gain at 2.0 GHz**
- **Ultra-miniature Package**
- **Unconditionally Stable**

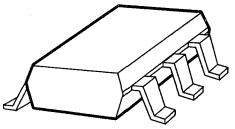
Applications

- **Buffer or Driver Amp for PCS, PHS, ISM, SATCOM and WLL Applications**
- **High Dynamic Range LNA**

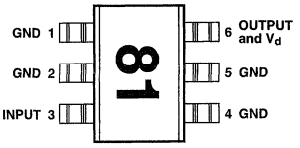
Simplified Schematic



Surface Mount Package SOT-363 (SC-70)



Pin Connections and Package Marking



Note: Package marking provides orientation and identification.

Description

Hewlett-Packard's MGA-81563 is an economical, easy-to-use GaAs MMIC amplifier that offers excellent power and low noise figure for applications from 0.1 to 6 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

The output of the amplifier is matched to 50 Ω (better than 2.1:1 VSWR) across the entire bandwidth. The input is partially matched to 50 Ω (better than 2.5:1 VSWR) below 4 GHz and fully matched to 50 Ω (better than 2:1 VSWR) above. A simple series inductor can be added to the input to improve the input match below 4 GHz. The amplifier allows a wide dynamic range by offering a 2.7 dB NF coupled with a +27 dBm Output IP_3.

The circuit uses state-of-the-art PHEMT technology with proven reliability. On-chip bias circuitry allows operation from a single +3 V power supply, while resistive feedback ensures stability (K>1) over all frequencies and temperatures.

MGA-81563 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Device Voltage, RF Output to Ground	V	6.0
V_{gd}	Device Voltage, Gate to Drain	V	-6.0
V_{in}	Range of RF Input Voltage to Ground	V	+0.5 to -1.0
P_{in}	CW RF Input Power	dBm	+13
T_{ch}	Channel Temperature	°C	165
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{ch-c} = 220°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board.)

MGA-81563 Electrical Specifications, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_d = 3$ V

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.	Std Dev[2]
G_{test}	Gain in test circuit[1]	f = 2.0 GHz		10.5	12.4		0.44
NF_{test}	Noise Figure in test circuit[1]	f = 2.0 GHz			2.8	3.8	0.21
NF_{50}	Noise Figure in 50 Ω system	f = 0.5 GHz f = 1.0 GHz f = 2.0 GHz f = 3.0 GHz f = 4.0 GHz f = 6.0 GHz	dB		3.1 3.0 2.7 2.7 2.8 3.5		0.21
$\|S_{21}\|^2$	Gain in 50 Ω system	f = 0.5 GHz f = 1.0 GHz f = 2.0 GHz f = 3.0 GHz f = 4.0 GHz f = 6.0 GHz	dB		12.5 12.5 12.3 11.8 11.4 10.2		0.44
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz f = 1.0 GHz f = 2.0 GHz f = 3.0 GHz f = 4.0 GHz f = 6.0 GHz	dBm		15.1 14.8 14.8 14.8 14.8 14.7		0.86
IP_3	Output Third Order Intercept Point	f = 2.0 GHz	dBm		+27		1.0
$VSWR_{in}$	Input VSWR	f = 2.0 GHz			2.7:1		
$VSWR_{out}$	Output VSWR	f = 2.0 GHz			2.0:1		
I_d	Device Current		mA	31	42	51	

Notes:
1. Guaranteed specifications are 100% tested in the circuit in Figure 10 in the Applications Information section.
2. Standard deviation number is based on measurement of at least 500 parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.

MGA-81563 Typical Performance, $T_C = 25°$ C, $V_d = 3$ V

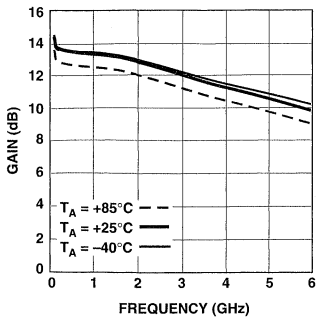


Figure 1. 50 Ω Power Gain vs. Frequency and Temperature.

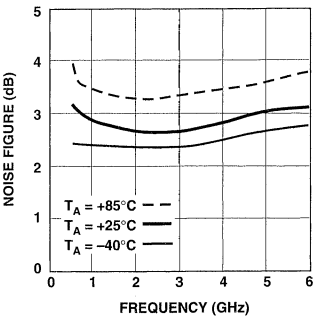


Figure 2. Noise Figure (into 50 Ω) vs. Frequency and Temperature.

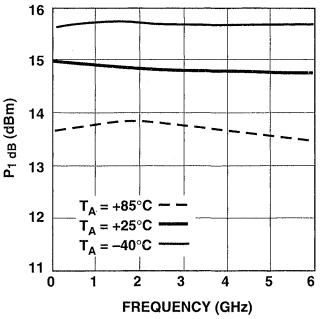


Figure 3. Output Power @ 1 dB Gain Compression vs. Frequency and Temperature.

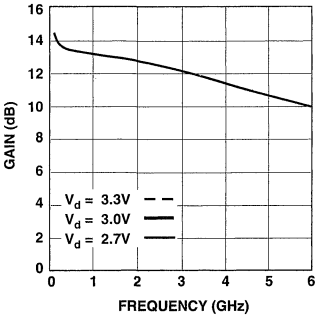


Figure 4. 50 Ω Power Gain vs. Frequency and Voltage.

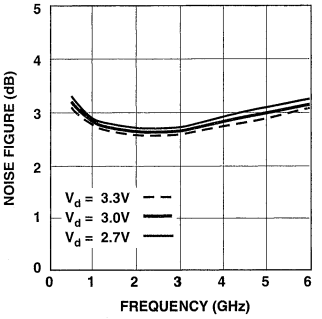


Figure 5. Noise Figure (into 50 Ω) vs. Frequency and Voltage.

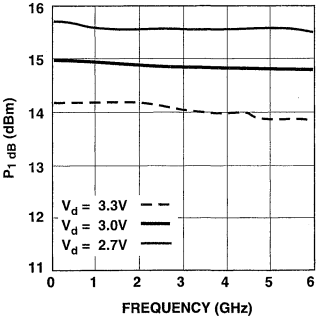


Figure 6. Output Power @ 1 dB Gain Compression) vs. Frequency and Voltage.

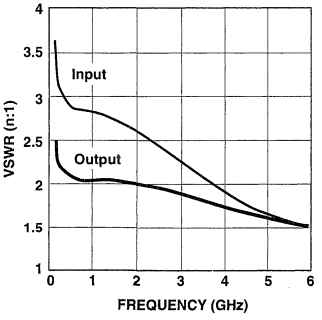


Figure 7. Input and Output VSWR into 50 Ω vs. Frequency.

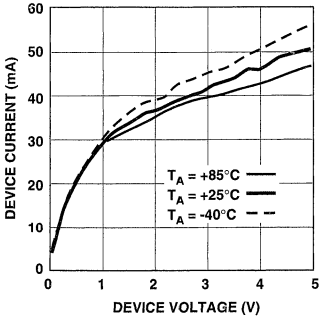


Figure 8. Device Current vs. Voltage and Temperature.

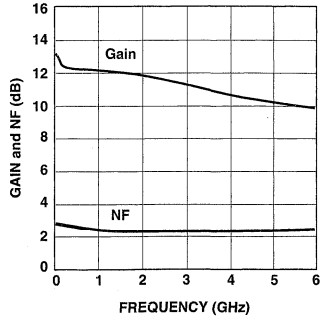


Figure 9. Minimum Noise Figure and Associated Gain vs. Frequency.

MGA-81563 Typical Scattering Parameters[1], T_C = 25°C, Z_O = 50 Ω, V_d = 3 V

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		K Factor
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.1	0.57	-16	13.02	4.48	172	-25	0.051	312	0.43	-14	1.47
0.2	0.52	-13	12.58	4.258	171	-25	0.057	17	0.38	-13	1.58
0.5	0.49	-16	12.35	4.15	164	-25	0.059	8	0.35	-9	1.64
1.0	0.48	-28	12.18	4.06	152	-25	0.061	5	0.35	-15	1.65
1.5	0.47	-40	12.00	3.98	140	-25	0.063	5	0.34	-22	1.65
2.0	0.45	-52	11.82	3.90	128	-24	0.067	4	0.34	-30	1.65
2.5	0.43	-63	11.63	3.81	116	-24	0.070	2	0.32	-39	1.66
3.0	0.39	-75	11.37	3.70	104	-24	0.074	-1	0.31	-46	1.69
3.5	0.35	-87	11.11	3.59	93	-22	0.077	-4	0.29	-53	1.73
4.0	0.32	-100	10.85	3.49	81	-22	0.081	-7	0.27	-60	1.77
4.5	0.28	-114	10.58	3.38	70	-22	0.083	-11	0.25	-67	1.82
5.0	0.25	-130	10.30	3.27	59	-21	0.087	-15	0.23	-74	1.85
5.5	0.22	-146	10.02	3.17	49	-21	0.09	-20	0.21	-81	1.91
6.0	0.20	-166	9.75	3.07	38	-21	0.091	-25	0.19	-90	1.93
6.5	0.18	174	9.46	2.97	27	-21	0.093	-30	0.17	-96	1.98
7.0	0.17	150	9.12	2.86	16	-21	0.094	-36	0.14	-100	2.05

MGA-81563 Typical Noise Parameters[1]

T_C = 25°C, Z_O = 50 Ω, V_d = 3 V

Frequency GHz	NF_O dB	Γ_{opt}		$R_n/50\ \Omega$ —
		Mag.	Ang.	
0.5	2.90	0.16	1	1.57
1.0	2.80	0.15	17	0.96
1.5	2.70	0.14	28	0.75
2.0	2.69	0.14	37	0.41
2.5	2.68	0.13	44	0.39
3.0	2.68	0.11	50	0.38
3.5	2.68	0.09	56	0.36
4.0	2.69	0.06	65	0.34
4.5	2.69	0.03	76	0.33
5.0	2.68	0.01	137	0.32
5.5	2.67	0.02	-135	0.32
6.0	2.67	0.05	-109	0.32
6.5	2.71	0.07	-95	0.33
7.0	2.77	0.09	-78	0.36

Note:

1. Reference plane per Figure 11 in Applications Information section.

MGA-81563 Applications Information

Introduction

This high performance GaAs MMIC amplifier was developed for commercial wireless applications from 100 MHz to 6 GHz.

The MGA-81563 runs on only 3 volts and typically requires only 42 mA to deliver 14.8 dBm of output power at 1 dB gain compression.

An innovative internal bias circuit regulates the device's internal current to enable the MGA-81563 to operate over a wide temperature range with a single, positive power supply of 3 volts. The MGA-81563 will operate with reduced performance with voltages as low as 1.5 volts.

The MGA-81563 uses resistive feedback to simultaneously achieve flat gain over a wide bandwidth and match the input and output impedances to 50 Ω. The MGA-81563 is unconditionally stable (K>1) over its entire frequency range, making it both very easy to use and yielding consistent performance in the manufacture of high volume wireless products.

With a combination of high linearity (+27 dBm output IP_3) and low noise figure (3 dB), the MGA-81563 offers outstanding performance for applications requiring a high dynamic range, such as receivers operating in dense signal environments. A wide dynamic range amplifier such as the MGA-81563 can often be used to relieve the requirements of bulky, lossy filters at a receiver's input.

The 14.8 dBm output power (P_{1dB}) also makes the MGA-81563 extremely useful for pre-driver, driver and buffer stages. For transmitter gain stage applications that require higher output power, the MGA-81563 can provide 50 mW (17 dBm) of saturated output power with a high power added efficiency of 45%.

Test Circuit

The circuit shown in Figure 10 is used for 100% RF testing of Noise Figure and Gain. The 3.9 nH inductor at the input fix-tunes the circuit to 2 GHz. The only purpose of the RFC at the output is to apply DC bias to the device under test. Tests in this circuit are used to guarantee the NF_{test} and G_{test} parameters shown in the table of Electrical Specifications.

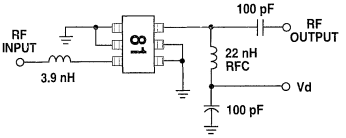


Figure 10. Test Circuit.

Phase Reference Planes

The positions of the reference planes used to specify the S-Parameters and Noise Parameters for this device are shown in Figure 11. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

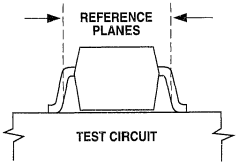


Figure 11. Phase Reference Planes.

Specifications and Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either "minimum or maximum," "typical," or "standard deviations."

The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on of a minimum of 500 parts taken from 3 non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard "bell curve."

Parameters considered to be the most important to system performance are bounded by *minimum* or *maximum* values. For the MGA-81563, these parameters are: Gain (G_{test}), Noise Figure (NF_{test}), and Device Current (I_d). Each of these guaranteed parameters is 100% tested.

Values for most of the parameters in the table of Electrical Specifications that are described by *typical* data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as the Noise and S-parameter tables or performance curves, the data represents a nominal part taken from the "center" of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate circuit using the MGA-81563, but to also optimize and evaluate trade-offs that affect a complete wireless system, the *standard deviation* (σ) is provided for many of the Electrical Specifications parameters (at 25°) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean. Referring to Figure 12 for example, the probability of a parameter being between $\pm 1\sigma$ is 68.3%; between $\pm 2\sigma$ is 95.4%; and between $\pm 3\sigma$ is 99.7%.

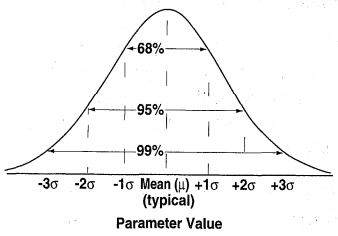


Figure 12. Normal Distribution.

RF Layout

The RF layout in Figure 13 is suggested as a starting point for microstripline designs using the MGA-81563 amplifier. Adequate grounding is needed to obtain optimum performance and to maintain stability. All of the ground pins of the MMIC should be connected to the RF groundplane on the backside of the PCB by means of plated through holes (vias) that are placed near the package terminals. As a minimum, one via should be located next to each ground pin to ensure good RF grounding. It is a good practice to use multiple vias to further minimize ground path inductance.

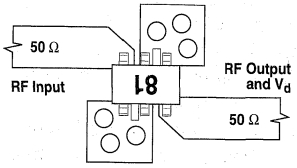


Figure 13. RF Layout.

It is recommended that the PCB pads for the ground pins *not* be connected together underneath the body of the package. PCB traces hidden under the package cannot be adequately inspected for SMT solder quality.

PCB Material

FR-4 or G-10 printed circuit board materials are a good choice for most low cost wireless applications. Typical board thickness is 0.020 to 0.031 inches. The width of the 50 Ω microstriplines on PC boards in this thickness range is also very convenient for mounting chip components such as the series inductor at the input or DC blocking and bypass capacitors.

For higher frequencies or for noise figure critical applications, the additional cost of PTFE/glass dielectric materials may be warranted to minimize transmission line loss at the amplifier's input. A 0.5 inch length of 50 Ω microstripline on FR-4, for example, has approximately 0.3 dB loss at 4 GHz. This loss will add directly to the noise figure of the MGA-81563.

Biasing

The MGA-81563 is a voltage-biased device and is designed to operate from a single, +3 volt power supply with a typical current drain of 42 mA. The internal current regulation circuit allows the amplifier to be operated with voltages as high +5 volts or as low as +1.5 volt. Refer to the section titled "Operation at Bias Voltages Other than 3 Volts" for information on performance and precautions when using other voltages.

Typical Application Example

The printed circuit layout in Figure 14 can serve as a design guide. This layout is a microstripline design (solid groundplane on the backside of the circuit board) with a 50 Ω input and output. The circuit is fabricated on 0.031-inch thick FR-4 dielectric material. Plated through holes (vias) are used to bring the ground to the top side of the circuit where needed. Multiple vias are used to reduce the inductance of the paths to ground.

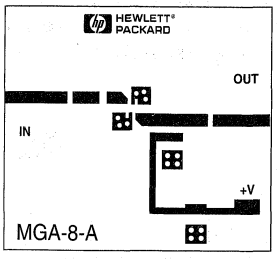


Figure 14. PCB Layout.

A schematic diagram of the application circuit is shown in Figure 15. DC blocking capacitors (C1 and C2) are used at the input and output of the MMIC to isolate the device from adjacent circuits.

Although the input terminal of the MGA-81563 is at ground potential, it is not a current sink. If the input is connected to a preceding stage that has a voltage present, the use of the DC blocking capacitor (C1) is required.

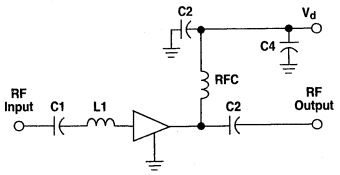


Figure 15. Schematic Diagram.

DC bias is applied to the MGA-81563 through the RF Output pin. An inductor (RFC), or length of high impedance transmission line (preferably $\lambda/4$ at the band center), is used to isolate the RF from the DC supply.

The power supply is bypassed to ground with capacitor C3 to keep RF off of the DC lines and to prevent gain dips or peaks in the response of the amplifier.

An additional bypass capacitor, C4, may be added to the bias line near the V_d connection to eliminate unwanted feedback through bias lines that could cause oscillation. C4 will not normally be needed unless several stages are cascaded using a common power supply.

When multiple bypass capacitors are used, consideration should be given to potential resonances. It is important to ensure that the capacitors when combined with additional parasitic L's and C's on the circuit board do not form resonant circuits. The addition of a small value resistor in the bias supply line between bypass capacitors will often "de-Q" the bias circuit and eliminate the effect of a resonance.

The value of the DC blocking and RF bypass capacitors (C1 – C3) should be chosen to provide a small reactance (typically < 5 ohms) at the lowest operating frequency. The reactance of the RF choke (RFC) should be high (e.g., several hundred ohms) at the lowest frequency of operation.

The MGA-81563's response at low frequencies is limited to approximately 100 MHz by the size of capacitors integrated on the MMIC chip.

The input of the MGA-81563 is partially matched internally to 50 Ω. Without external matching elements, the input VSWR of the MGA-81563 is 3.0:1 at 300 MIHz and decreases to 1.5:1 at 6 GHz. This will be adequate for many applications. If a better input VSWR is required, the use of a series inductor, L1 in the applications example, (or, alternatively a length of high impedance transmission line) is all that is needed to improve the match. The table in Figure 16 shows suggested values for L1 for various wireless frequency bands.

Frequency (GHz)	Inductor, L1 (nH)
0.9	10
1.5	6.8
1.9	3.9
2.4	2.7
4.0	0.5
5.8	0

Figure 16. Values for L1.

These values for L1 take into account the short length of 50 Ω transmission line between the inductor and the input pin of the device.

For applications requiring minimum noise figure (NF_o), some improvement over a 50 Ω match is possible by matching the signal input to the optimum noise match impedance, Γ_o, as specified in the "Typical Noise Parameters" table.

For most applications, as shown in the example circuit, the output of the MGA-81563 is already sufficiently well matched to 50 Ω and no additional matching is needed. The nominal device output VSWR is ≤ 2.2:1 from 300 MHz through 6 GHz.

The completed application amplifier with all components and SMA connectors is shown in Figure 17.

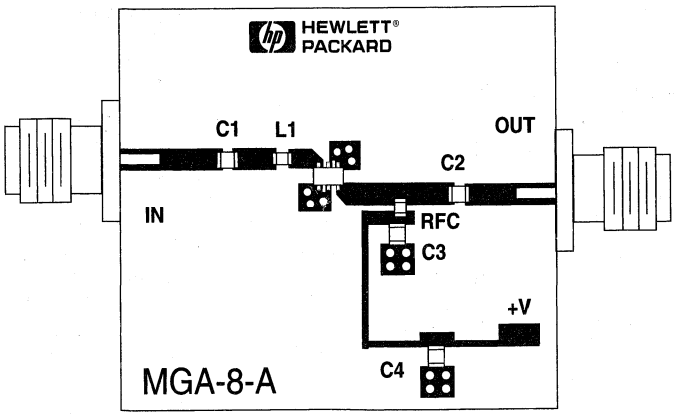


Figure 17. Complete Application Circuit.

Operation in Saturation for Higher Output Power

For applications such as predriver and driver stages in transmitters, the MGA-81563 can be operated in saturation to deliver up to 50 mW (17 dBm) of output power. The power added efficiency increases to 45% at these power levels.

There are several design considerations related to reliability and performance that should be taken into account when operating the amplifier in saturation.

First of all, it is important that the stage preceding the MGA-81563 not overdrive the device. Referring to the "Absolute Maximum Ratings" table, the maximum allowable input power is +13 dBm. This should be regarded as the input power level above which the device could be permanently damaged.

Driving the amplifier into saturation will also affect electrical performance. Figure 18 presents the Output Power, Third Order Intercept Point (Output IP_3), and Power Added Efficiency (PAE) as a function of Input Power. This data represents performance into a 50 Ω load. Since the output impedance of the device changes when driven into saturation, it is possible to obtain even more output power with a "power match." The optimum impedance match for maximum output power is dependent on frequency and actual output power level and can be arrived at empirically.

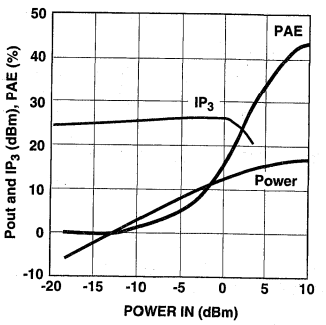


Figure 18. Output Power, IP_3, and Power-Added-Efficiency vs. Input Power. (V_d = 3.0 V)

As the input power is increased beyond the linear range of the amplifier, the gain becomes more compressed. Gain as a function of either input or output power may be derived from Figure 18. Gain compression renders the amplifier less sensitive to variations in the power level from the preceding stage. This can be a benefit in systems requiring fairly constant output power levels from the MGA-81563.

Increased efficiency (45% at full output power) is another benefit of saturated operation. At high output power levels, the bias supply current drops by about 15%. This is normal and is taken into account for the PAE data in Figure 18.

Noise figure and input impedance are also affected by saturated power operation. As a guideline, the input impedance is lowered, resulting in an improvement in input VSWR of approximately 20%.

Like other active devices, the intermodulation products of the MGA-81563 increase as the device is driven further into nonlinear operation. The 3rd, 5th, and 7th order intermodulation products of the MGA-81563 are shown in Figure 19 along with the fundamental response. This data was measured in the test circuit in Figure 10.

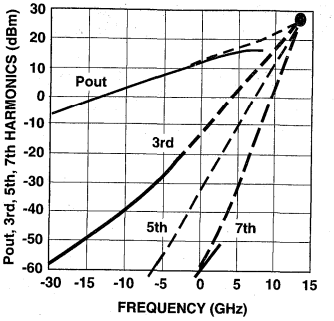


Figure 19. Intermodulation Products vs. Input Power. (V_d = 3.0 V)

Operation at Bias Voltages Other than 3 Volts

While the MGA-81563 is designed primarily for use in +3 volt applications, the internal bias regulation circuitry allows it to be operated with any power supply voltage from +1.5 to +5 volts. Performance of Gain, Noise Figure, and Output Power over a wide range of bias voltage is shown in Figure 20. As can be seen, the gain and NF are fairly flat, but an increase in output power is possible by using higher voltages. The use of +5 volts increases the P_{1dB} by 2 dBm.

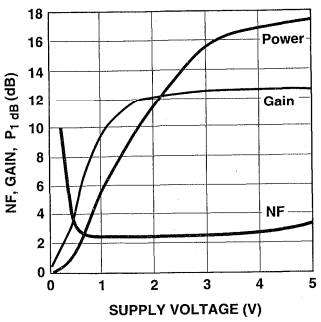


Figure 20. Gain, Noise Figure, and Output Power vs. Supply Voltage.

Some thermal precautions must be observed for operation at higher bias voltages. For reliable operation, the channel temperature should be kept within the 165° C indicated in the "Absolute Maximum Ratings" table. As a guideline, operating life tests have established a MTTF in excess of 10^6 hours for channel temperatures up to 150° C.

There are several means of biasing the MGA-81563 at 3 volts in systems that use higher power supply voltages. The simplest method, shown in Figure 21a, is to use a series resistor to drop the device voltage to 3 volts. For example, a 47 Ω resistor will drop a 5-volt supply to 3 volts at the nominal current of 42 mA. Some variation in performance could be expected for this method due to variations in current within the specified 31 to 51 mA min/max range.

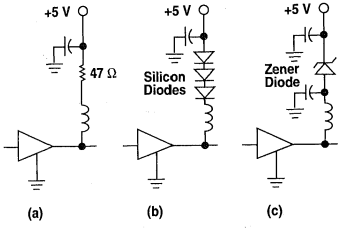


Figure 21. Biasing From Higher Supply Voltages.

A second method illustrated in Figure 21b, is to use forward-biased diodes in series with the power supply. For example, three silicon diodes connected in series will drop a 5-volt supply to approximately 3 volts.

The use of the series diode approach has the advantage of less dependency on current variation in the amplifiers since the forward voltage drop of a diode is somewhat current independent.

Reverse breakdown diodes (e.g., Zener diodes) could also be used as in Figure 21c. However, care should be taken to ensure that the noise generated by diodes in either Zener or reverse breakdown is adequately filtered (e.g., bypassed to ground) such that the diode's noise is not added to the amplifier's signal.

SOT-363 PCB Footprint

A recommended PCB pad layout for the miniature SOT-363 (SC-70) package used by the MGA-81563 is shown in Figure 22 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the MGA-81563. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads.

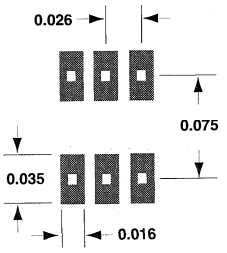


Figure 22. PCB Pad Layout (dimensions in inches).

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-363 package, will reach solder reflow temperatures faster than those with a greater mass.

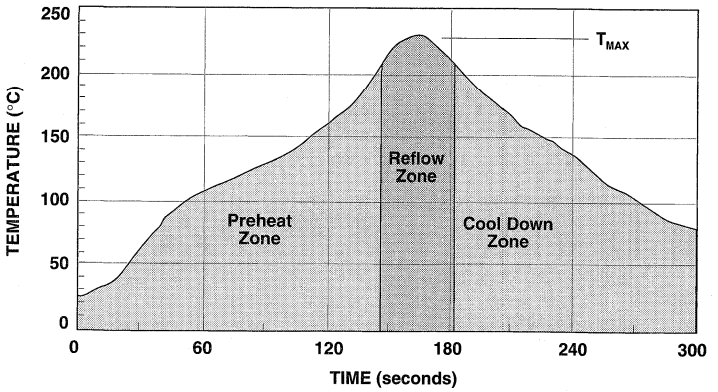


Figure 23. Surface Mount Assembly Profile.

The MGA-81563 is has been qualified to the time-temperature profile shown in Figure 23. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235 °C.

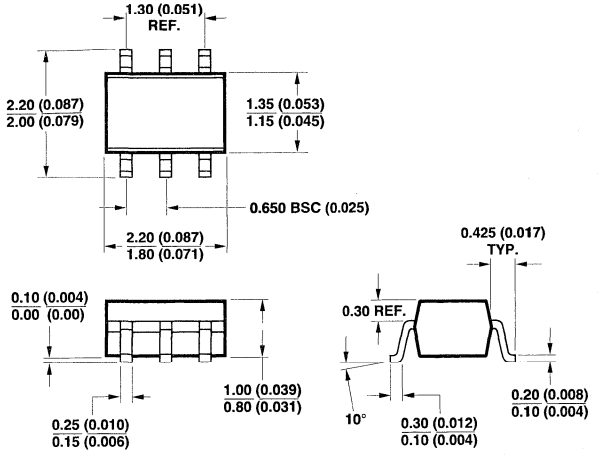
These parameters are typical for a surface mount assembly process for the MGA-81563. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

Electrostatic Sensitivity

GaAs MMICs are electrostatic discharge (ESD) sensitive devices. Although the MGA-81563 is robust in design, permanent damage may occur to these devices if they are subjected to high energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without detection and may result in degradation in performance or failure. The MGA-81563 is an ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, and assembling these devices to avoid damage.

Package Dimensions

Outline 63 (SOT-363/SC-70)

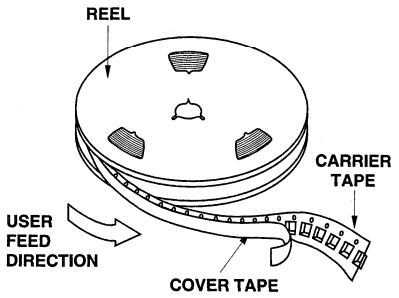


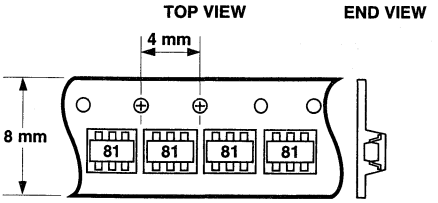
DIMENSIONS ARE IN MILLIMETERS (INCHES)

MGA-81563 Part Number Ordering Information

Part Number	No. of Devices	Container
MGA-81563-TR1	3000	7" Reel
MGA-81563-BLK	100	antistatic bag

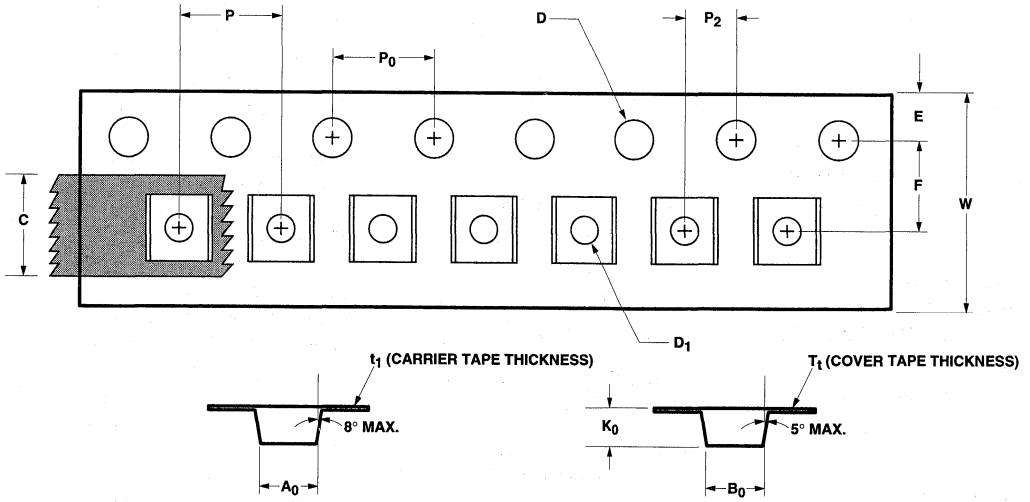
Device Orientation





Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

0.1–6 GHz 3V, 17 dBm Amplifier

Technical Data

MGA-82563

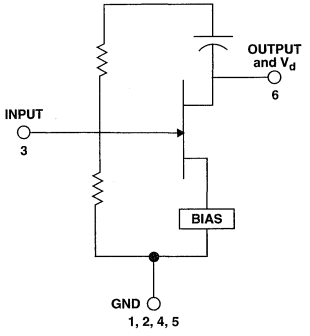
Features

- **+17.3 dBm $P_{1\,dB}$ at 2.0 GHz**
  +20 dBm P_{sat} at 2.0 GHz
- **Single +3V Supply**
- **2.2 dB Noise Figure at 2.0 GHz**
- **13.2 dB Gain at 2.0 GHz**
- **Ultra-miniature Package**
- **Unconditionally Stable**

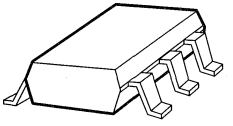
Applications

- **Buffer or Driver Amp for PCS, PHS, ISM, SATCOM and WLL Applications**
- **High Dynamic Range LNA**

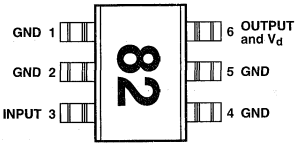
Simplified Schematic



Surface Mount Package SOT-363 (SC-70)



Pin Connections and Package Marking



Note: Package marking provides orientation and identification.

Description

Hewlett-Packard's MGA-82563 is an economical, easy-to-use GaAs MMIC amplifier that offers excellent power and low noise figure for applications from 0.1 to 6 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

The input and output of the amplifier are matched to 50 Ω (below 2:1 VSWR) across the entire bandwidth, eliminating the expense of external matching. The amplifier allows a wide dynamic range by offering a 2.2 dB NF coupled with a +31 dBm Output IP_3.

The circuit uses state-of-the-art PHEMT technology with proven reliability. On-chip bias circuitry allows operation from a single +3 V power supply, while resistive feedback ensures stability (K>1) over all frequencies and temperatures.

MGA-82563 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Device Voltage, RF Output to Ground	V	5.0
V_{gd}	Device Voltage, Gate to Drain	V	-6.0
V_{in}	Range of RF Input Voltage to Ground	V	+0.5 to -1.0
P_{in}	CW RF Input Power	dBm	+13
T_{ch}	Channel Temperature	°C	165
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{ch-c} = 180°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board.)

MGA-82563 Electrical Specifications, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_d = 3$ V

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.	Std Dev[2]
G_{test}	Gain in test circuit[1]	f = 2.0 GHz		12.0	13.2		0.35
NF_{test}	Noise Figure in test circuit[1]	f = 2.0 GHz			2.2	2.9	0.20
NF_{50}	Noise Figure in 50 Ω system	f = 0.5 GHz	dB		2.3		
		f = 1.0 GHz			2.2		
		f = 2.0 GHz			2.2		0.20
		f = 3.0 GHz			2.2		
		f = 4.0 GHz			2.4		
		f = 6.0 GHz			2.7		
$\|S_{21}\|^2$	Gain in 50 Ω system	f = 0.5 GHz	dB		14.7		
		f = 1.0 GHz			14.5		
		f = 2.0 GHz			13.5		0.35
		f = 3.0 GHz			12.1		
		f = 4.0 GHz			10.7		
		f = 6.0 GHz			8.8		
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		17.4		
		f = 1.0 GHz			17.5		
		f = 2.0 GHz			17.3		0.54
		f = 3.0 GHz			17.1		
		f = 4.0 GHz			17.0		
		f = 6.0 GHz			16.8		
IP_3	Output Third Order Intercept Point	f = 2.0 GHz	dBm		+31		1.0
$VSWR_{in}$	Input VSWR	f = 0.2–5.0 GHz			1.8:1		
$VSWR_{out}$	Output VSWR	f = 0.2–5.0 GHz			1.2:1		
I_d	Device Current		mA	63	84	101	

Notes:
1. Guaranteed specifications are 100% tested in the circuit in Figure 10 in the Applications Information section.
2. Standard deviation number is based on measurement of at least 500 parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.

MGA-82563 Typical Performance, $T_C = 25°$ C, $V_d = 3$ V

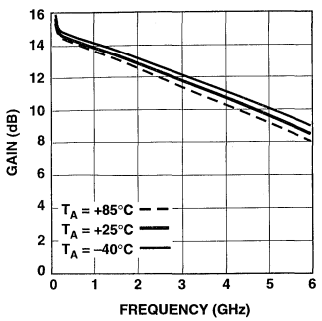


Figure 1. 50 Ω Power Gain vs. Frequency and Temperature.

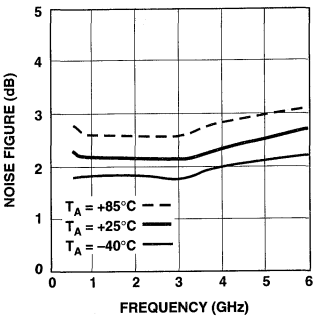


Figure 2. Noise Figure (into 50 Ω) vs. Frequency and Temperature.

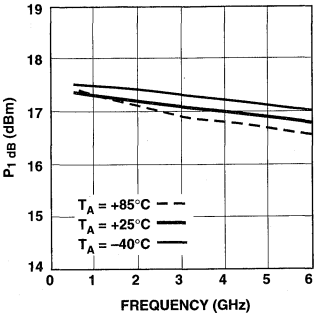


Figure 3. Output Power @ 1 dB Gain Compression vs. Frequency and Temperature.

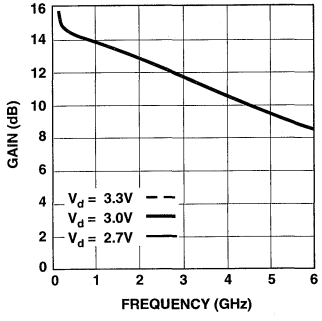


Figure 4. 50 Ω Power Gain vs. Frequency and Voltage.

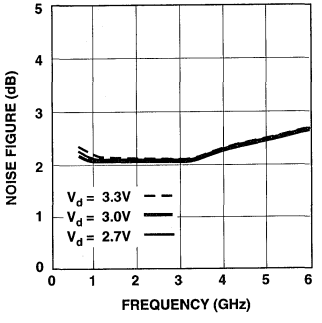


Figure 5. Noise Figure (into 50 Ω) vs. Frequency and Voltage.

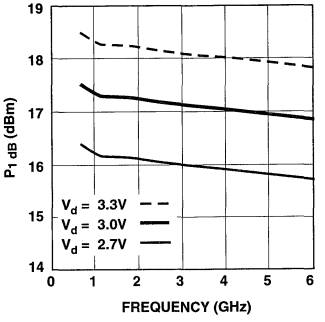


Figure 6. Output Power @ 1 dB Gain Compression vs. Frequency and Voltage.

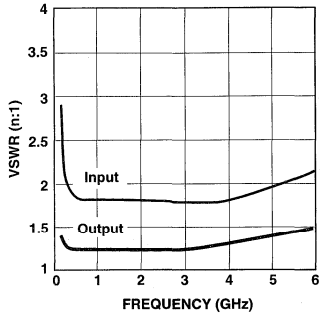


Figure 7. Input and Output VSWR into 50 Ω vs. Frequency.

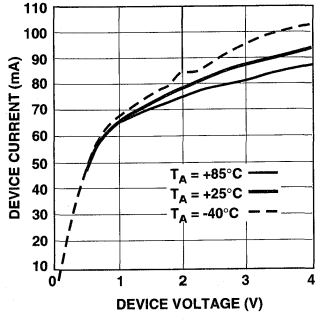


Figure 8. Device Current vs. Voltage and Temperature.

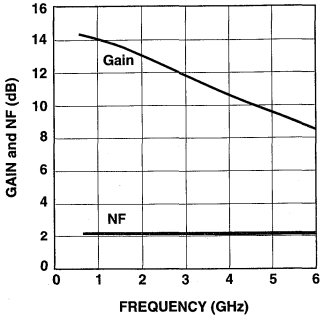


Figure 9. Minimum Noise Figure and Associated Gain vs. Frequency.

MGA-82563 Typical Scattering Parameters[1], T_C = 25°C, Z_O = 50 Ω, V_d = 3 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	Factor
0.1	0.48	-39	15.71	6.10	164	-23	0.070	27	0.16	-99	1.02
0.2	0.35	-35	14.81	5.50	165	-22	0.076	14	0.12	-134	1.20
0.5	0.29	-37	14.34	5.21	159	-22	0.079	6	0.11	177	1.29
1.0	0.29	-57	13.95	4.98	144	-22	0.080	3	0.11	156	1.33
1.5	0.29	-78	13.50	4.73	128	-22	0.082	2	0.10	142	1.37
2.0	0.29	-99	12.99	4.46	114	-22	0.085	1	0.10	131	1.41
2.5	0.29	-118	12.45	4.19	99	-21	0.089	-1	0.10	124	1.44
3.0	0.28	-138	11.84	3.91	86	-21	0.093	-3	0.11	118	1.48
3.5	0.28	-158	11.24	3.65	74	-21	0.098	-6	0.12	111	1.51
4.0	0.29	-177	10.67	3.42	61	-20	0.103	-9	0.13	106	1.52
4.5	0.30	166	10.11	3.20	50	-20	0.107	-13	0.15	100	1.53
5.0	0.32	151	9.58	3.01	38	-19	0.112	-18	0.16	94	1.54
5.5	0.34	136	9.07	2.84	27	-19	0.117	-23	0.18	87	1.55
6.0	0.36	123	8.57	2.68	16	-19	0.121	-29	0.19	82	1.54
6.5	0.38	110	8.06	2.53	5	-19	0.125	-35	0.22	74	1.55
7.0	0.40	97	7.51	2.37	-5	-18	0.126	-41	0.24	66	1.59

MGA-82563 Typical Noise Parameters[1]

T_C = 25°C, Z_O = 50 Ω, V_d = 3 V

Frequency	NF_O	Γ_{opt}		$R_n/50\ \Omega$
GHz	dB	Mag.	Ang.	—
0.5	2.10	0.15	25	1.20
1.0	2.10	0.15	45	0.60
1.5	2.10	0.14	65	0.29
2.0	2.12	0.15	75	0.27
2.5	2.12	0.15	94	0.25
3.0	2.15	0.144	113	0.23
3.5	2.16	0.14	134	0.21
4.0	2.16	0.15	155	0.19
4.5	2.19	0.17	177	0.18
5.0	2.18	0.20	-166	0.18
5.5	2.19	0.22	-152	0.18
6.0	2.23	0.25	-138	0.19
6.5	2.28	0.27	-125	0.23
7.0	2.39	0.29	-111	0.28

Note:

1. Reference plane per Figure 11 in Applications Information section.

MGA-82563 Applications Information

Introduction

This medium power GaAs MMIC amplifier was developed for commercial wireless applications from 100 MHz to 6 GHz. The MGA-82563 runs on only 3 volts and typically requires only 84 mA to deliver over 17 dBm of output power at 1 dB gain compression.

The 17.3 dBm output power ($P_{1\,dB}$) makes the MGA-82563 extremely useful for pre-driver and driver stages in transmit cascades or for final output stages in lower power systems. For transmitter gain stage applications that require even higher output power, the MGA-82563 can provide 100 mW (20 dBm) of saturated output power with a power added efficiency approaching 50%. The low cost of the MGA-82563 makes it feasible to power combine two (or more) devices for even higher output power amplifiers.

The MGA-82563 offers an excellent combination of high linearity (+31 dBm output IP_3) and very low noise figure (2.2 dB) for applications requiring a very high dynamic range.

The MGA-82563 uses resistive feedback to simultaneously achieve flat gain over a wide bandwidth and to match the input and output impedances to 50 Ω. The MGA-82563 is also unconditionally stable (K>1) over its entire frequency range, making it both very easy to use and yielding consistent performance in the manufacture of high volume wireless products.

An innovative internal bias circuit regulates the device's internal current to enable the MGA-82563 to operate over a wide temperature range with a single, positive power supply of 3 volts. The MGA-82563 will operate with reduced power and gain with a bias supply as low as 1.5 volts.

Test Circuit

The circuit shown in Figure 10 is used for 100% RF testing of Gain and Noise Figure. The test circuit is merely a 50 Ω input/output PC board with a RFC at the output to apply DC bias to the device under test. Tests in this circuit are used to guarantee the NF_{test} and G_{test} parameters shown in the table of Electrical Specifications.

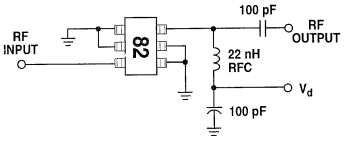


Figure 10. Test Circuit.

Phase Reference Planes

The positions of the reference planes used to specify the S-Parameters and Noise Parameters for this device are shown in Figure 11. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

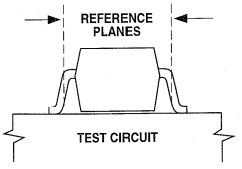


Figure 11. Phase Reference Planes.

Specifications and Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either "minimum or maximum," "typical," or "standard deviations."

The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on of a minimum of 500 parts taken from 3 non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard "bell curve."

Parameters considered to be the most important to system performance are bounded by *minimum* or *maximum* values. For the MGA-82563, these parameters are: Gain (G_{test}), Noise Figure (NF_{test}), and Device Current (I_d). Each of these guaranteed parameters is 100% tested.

Values for most of the parameters in the table of Electrical Specifications that are described by *typical* data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as the Noise and S-parameter tables or performance curves, the data represents a nominal part taken from the "center" of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate circuit using the MGA-82563, but to also optimize and evaluate trade-offs that affect a complete wireless system, the *standard deviation* (σ) is provided for many of the Electrical Specifications parameters (at 25°) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean. Referring to Figure 12 for example, the probability of a parameter being between $\pm 1\sigma$ is 68.3%; between $\pm 2\sigma$ is 95.4%; and between $\pm 3\sigma$ is 99.7%.

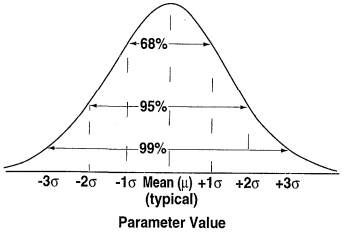


Figure 12. Normal Distribution.

RF Layout

The RF layout in Figure 13 is suggested as a starting point for microstripline designs using the MGA-82563 amplifier. Adequate grounding is needed to obtain optimum performance and to maintain stability. All of the ground pins of the MMIC should be connected to the RF groundplane on the backside of the PCB by means of plated through holes (vias) that are placed near the package terminals. As a minimum, one via should be located next to each ground pin to ensure good RF grounding. It is a good practice to use multiple vias to further minimize ground path inductance.

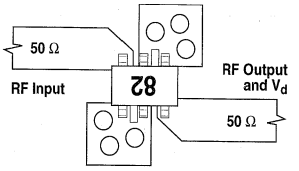


Figure 13. RF Layout.

In addition to the RF considerations, the use of multiple vias for grounding is important for the purpose of providing a lower resistance thermal path to the heatsink.

It is recommended that the PCB pads for the ground pins *not* be connected together underneath the body of the package. PCB traces hidden under the package cannot be adequately inspected for SMT solder quality.

PCB Material

FR-4 or G-10 printed circuit board materials are a good choice for most low cost wireless applications. Typical board thickness is 0.020 to 0.031 inches. The width of the 50 Ω microstriplines on PC boards in this thickness range is also very convenient for mounting chip components such as the series inductor at the input or DC blocking and bypass capacitors.

For higher frequencies or for noise figure critical applications, the additional cost of PTFE/glass dielectric materials may be warranted to minimize transmission line loss at the amplifier's input. A 0.5 inch length of 50 Ω microstripline on FR-4, for example, has approximately 0.3 dB loss at 4 GHz. This loss will add directly to the noise figure of the MGA-82563.

Biasing

The MGA-82563 is a voltage-biased device and is designed to operate from a single, +3 volt power supply with a typical current drain of 84 mA. The internal current regulation circuit allows the amplifier to be operated with voltages as low as +1.5 volts. Refer to the section titled "Operation at Bias Voltages Other than 3 Volts" for information on performance and precautions when using other voltages.

Typical Application Example

The printed circuit layout in Figure 14 can serve as a design guide. This layout is a microstripline design (solid groundplane on the backside of the circuit board) with a 50 Ω input and output. The circuit is fabricated on 0.031-inch thick FR-4 dielectric material. Plated through holes (vias) are used to bring the ground to the top side of the circuit where needed. Multiple vias are used to reduce the inductance of the paths to ground.

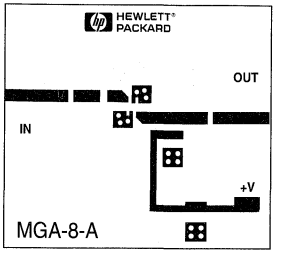


Figure 14. PCB Layout.

A schematic diagram of the application circuit is shown in Figure 15. DC blocking capacitors (C1 and C2) are used at the input and output of the MMIC to isolate the device from adjacent circuits. While the input terminal of the MGA-82563 is at ground potential, it is not a current sink. If the input is connected to a preceding stage that has a voltage present, the use of the DC blocking capacitor (C1) is required.

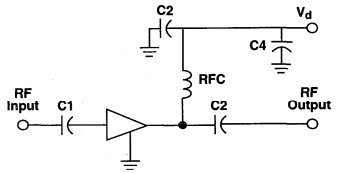


Figure 15. Schematic Diagram.

DC bias is applied to the MGA-82563 through the RF Output pin. An inductor (RFC), or length of high impedance transmission line (preferably $\lambda/4$ at the band center), is used to isolate the RF from the DC supply.

The power supply is bypassed to ground with capacitor C3 to keep RF off of the DC lines and to prevent gain dips or peaks in the response of the amplifier.

An additional bypass capacitor, C4, may be added to the bias line near the V_d connection to eliminate unwanted feedback through bias lines that could cause oscillation. C4 will not normally be needed unless several stages are cascaded using a common power supply.

When multiple bypass capacitors are used, consideration should be given to potential resonances. It is important to ensure that the capacitors when combined with additional parasitic L's and C's on the circuit board do not form resonant circuits. The addition of a small value resistor in the bias supply line between bypass capacitors will often "de-Q" the bias circuit and eliminate the effect of a resonance.

The value of the DC blocking and RF bypass capacitors (C1 - C3) should be chosen to provide a small reactance (typically <5 ohms) at the lowest operating frequency. The reactance of the RF choke (RFC) should be high (e.g., several hundred ohms) at the lowest frequency of operation.

The MGA-82563's response at low frequencies is limited to approximately 100 MHz by the size of capacitors integrated on the MMIC chip.

The input and output of the MGA-82563 are well matched to 50 Ω. Without external matching elements, the input VSWR of the MGA-82563 is ≤ 2.0:1 from 300 MHz to 6 GHz and the Output VSWR is ≤ 1.6:1 from 100 MHz through 6 GHz.

For applications requiring minimum noise figure (NF_o), some improvement over a 50 Ω match is possible by matching the signal input to the optimum noise match impedance, Γ_o, as specified in the "Typical Noise Parameters" table. The data in the table shows the noise match to be very close to 50 Ω.

The completed application amplifier with all components and SMA connectors is shown in Figure 16.

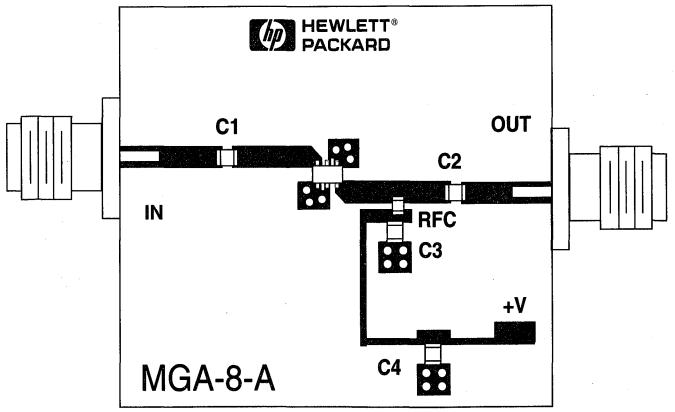


Figure 16. Complete Application Circuit.

Operation in Saturation for Higher Output Power

For applications such as pre-driver, driver, and output stages in transmitters, the MGA-82563 can be operated in saturation to deliver up to 100 mW (20 dBm) of output power. The power added efficiency approaches 50% at these power levels.

There are several design considerations related to reliability and performance that should be taken into account when operating the amplifier in saturation.

First of all, it is important that the stage preceding the MGA-82563 not overdrive the device. Referring to the "Absolute Maximum Ratings" table, the maximum allowable input power is +13 dBm. This should be regarded as the input power level above which the device could be permanently damaged.

Driving the amplifier into saturation will also affect electrical performance. Figure 17 presents the Output Power, Third Order Intercept Point (Output IP_3), and Power Added Efficiency (PAE) as a function of Input Power. This data represents performance into a 50 Ω load. Since the output impedance of the device changes when driven into saturation, it is possible to obtain even more output power with a "power match." The optimum impedance match for maximum output power is dependent on specific frequency and actual output power level and can be arrived at empirically.

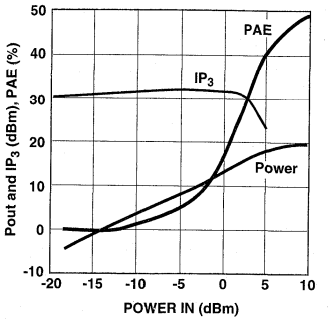


Figure 17. Output Power, IP_3, and Power-Added-Efficiency vs. Input Power. (V_d = 3.0 V)

As the input power is increased beyond the linear range of the amplifier, the gain becomes more compressed. Gain as a function of either input or output power may be derived from Figure 17. Gain compression renders the amplifier less sensitive to variations in the power level from the preceding stage. This can be a benefit in systems requiring fairly constant output power levels from the MGA-82563.

Increased efficiency (up to 45% at full output power) is another benefit of saturated operation. At high output power levels, the bias supply current drops by about 15%. This is normal and is taken into account for the PAE data in Figure 17.

Like other active devices, the intermodulation products of the MGA-82563 increase as the device is driven further into nonlinear operation. The 3rd, 5th, and 7th order intermodulation products of the MGA-82563 are shown in Figure 18 along with the fundamental response. This data was measured in the test circuit in Figure 10.

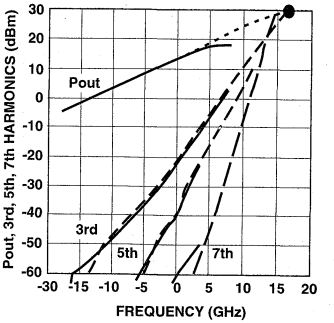


Figure 18. Intermodulation Products vs. Input Power. (V_d = 3.0 V)

Operation at Bias Voltages Other than 3 Volts

While the MGA-82563 is designed primarily for use in +3 volt applications, the internal bias regulation circuitry allows it to be operated with power supply voltages from +1.5 to +4 volts. Performance of Gain, Noise Figure, and Output Power over a wide range of bias voltage is shown in Figure 19. (This data was measured in the test circuit in Figure 10.) As can be seen, the gain and NF are fairly flat, but an increase in output power is possible by using higher voltages. The use of +4 volts increases the P_{1dB} by over 2 dBm.

If bias voltages greater than 3 volts are used, particular attention should be given to thermal management. Refer to the "Thermal Design Considerations" section for more details.

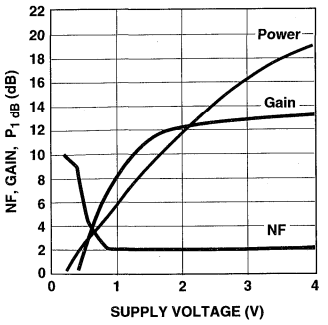


Figure 19. Gain, Noise Figure, and Output Power vs. Supply Voltage.

There are several means of biasing the MGA-82563 at 3 volts in systems that use higher power supply voltages. The simplest method, shown in Figure 20a, is to use a series resistor to drop the device voltage to 3 volts. For example, a 24 Ω resistor will drop a 5-volt supply to 3 volts at the nominal current of 84 mA. Some variation in performance could be expected for this method due to variations in current within the specified 63 to 101 mA min/max range.

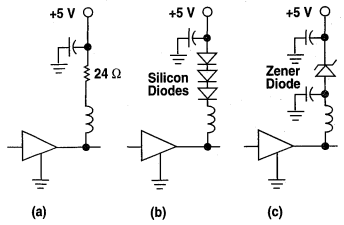


Figure 20. Biasing From Higher Supply Voltages.

A second method illustrated in Figure 20b, is to use forward-biased diodes in series with the power supply. For example, three silicon diodes connected in series will drop a 5-volt supply to approximately 3 volts.

The use of the series diode approach has the advantage of less dependency on current variation in the amplifiers since the forward voltage drop of a diode is somewhat current independent.

Reverse breakdown diodes (e.g., Zener diodes) could also be used as in Figure 20c. However, care should be taken to ensure that the noise generated by diodes in either Zener or reverse breakdown is adequately filtered (e.g., bypassed to ground) such that the diode's noise is not added to the amplificr's signal.

Note that the voltage-dropping component in each of these three methods must be able to safely dissipate up to 200 mW.

Thermal Design Considerations

Good thermal design is important in the application of medium power devices, especially when housed in miniature packages such as the SOT-363/SC-70.

As previously mentioned in the "RF Layout" section, the use of multiple vias near all of the ground pins provides an important part of the heatsinking function. For reliable operation, the channel temperature should be kept within the 165° C indicated in the "Absolute Maximum Ratings" table.

As an illustration of a thermal calculation, consider the example of a MGA-82563 biased at 3.0 volts for an application with a MTTF goal of 10^6 hours (114 years). Operating life tests have established a MTTF in excess of 10^6 hours (114 years) for a channel temperature of 150° C. The maximum device current specification is 101 mA at 3 volts. From Figure 8, it can be seen that the current will increase by approximately 9 mA to 110 mA at an elevated temperature. The device power dissipation is then:

$$P_d = 3.0 \text{ volts} * 110 \text{ mA},$$

which is equal to 330 mW. The channel-to-"case" thermal resistance (θ_{ch-c}) from the "Absolute Maximum Ratings" table is 180° C/watt. Note that "case" is defined as the interface between the SOT-363 package pins and the mounting surface (i.e., PCB).

The temperature rise from the mounting surface to the MMIC channel is:

$$\Delta T = 0.330 \text{ watt} * 180° \text{ C/watt},$$

or 59° C. To achieve the MTTF goal of 10^6 hours, the circuit to which the device is mounted should not exceed:

$$T_{case} = 150° - 59° \text{ C},$$

which is equal to 91° C.

For other MTTF goals and/or operating temperatures, Hewlett-Packard publishes reliability data sheets based on operating life tests to enable designers to arrive at a thermal design for their particular operating environment. For a reliability data sheet covering the MGA-82563, request Hewlett-Packard publication number 5964-4128E, titled "GaAs MMIC Amplifier Reliability Data." (This reliability data sheet covers the MGA-82563 as part of this family of GaAs MMICs.)

SOT-363 PCB Footprint

A recommended PCB pad layout for the miniature SOT-363 (SC-70) package used by the MGA-82563 is shown in Figure 21 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the MGA-82563. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads.

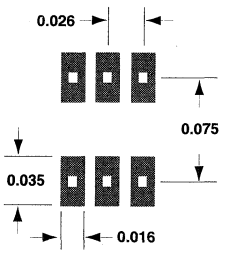


Figure 21. PCB Pad Layout (dimensions in inches).

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-363 package, will reach solder reflow temperatures faster than those with a greater mass.

The MGA-82563 is has been qualified to the time-temperature profile shown in Figure 22. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

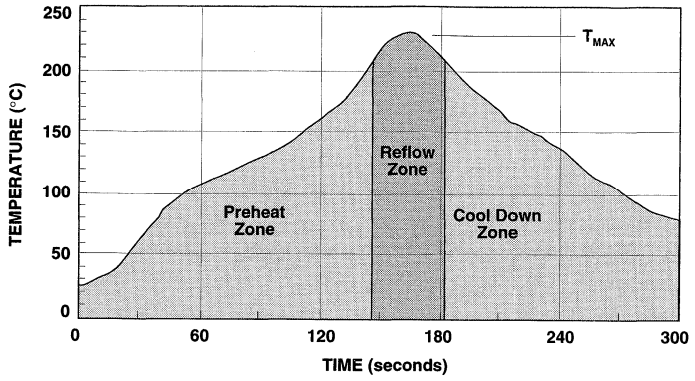


Figure 22. Surface Mount Assembly Profile.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235 °C.

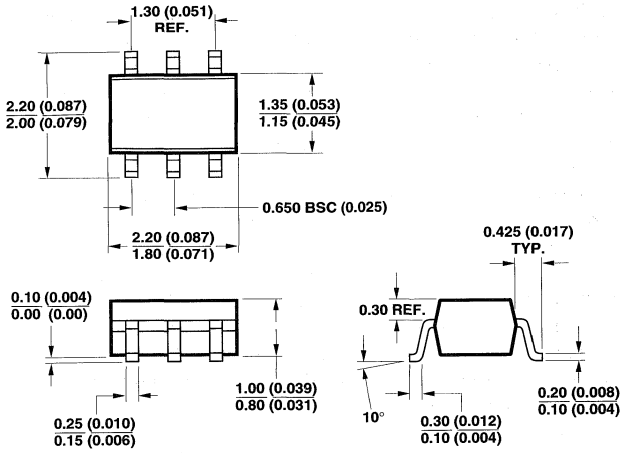
These parameters are typical for a surface mount assembly process for the MGA-82563. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

Electrostatic Sensitivity

GaAs MMICs are electrostatic discharge (ESD) sensitive devices. Although the MGA-82563 is robust in design, permanent damage may occur to these devices if they are subjected to high energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without detection and may result in degradation in performance or failure. The MGA-82563 is a ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, and assembling these devices to avoid damage.

Package Dimensions

Outline 63 (SOT-363/SC-70)

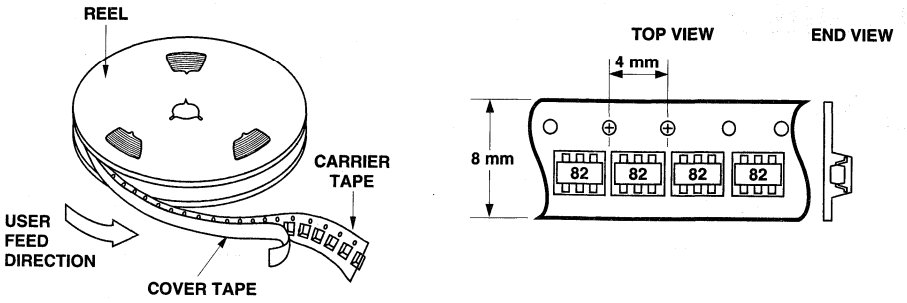


DIMENSIONS ARE IN MILLIMETERS (INCHES)

MGA-82563 Part Number Ordering Information

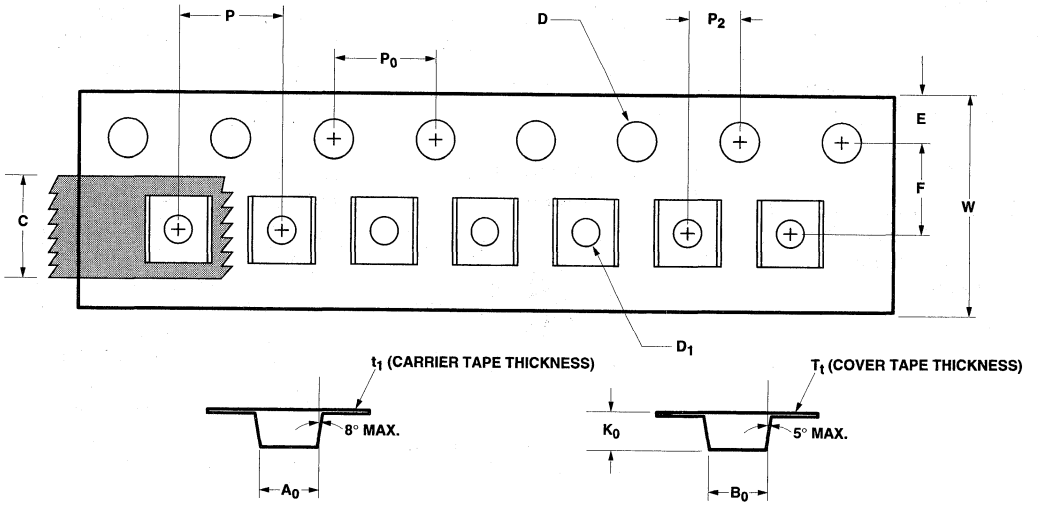
Part Number	No. of Devices	Container
MGA-82563-TR1	3000	7" Reel
MGA-82563-BLK	100	antistatic bag

Device Orientation



Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

0.5 – 6 GHz Low Noise GaAs MMIC Amplifier

Technical Data

MGA-86563

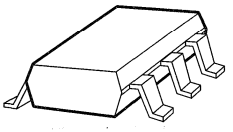
Features

- **Ultra-Miniature Package**
- **Internally Biased, Single +5 V Supply (14 mA)**
- **1.6 dB Noise Figure at 2.4 GHz**
- **21.8 dB Gain at 2.4 GHz**
- **+3.1 dBm P_{1dB} at 2.4 GHz**

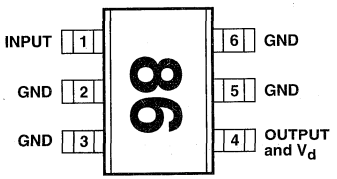
Applications

- **LNA or Gain Stage for ISM, PCS, MMDS, GPS, TVRO, and Other C band Applications**

Surface Mount Package SOT-363 (SC-70)

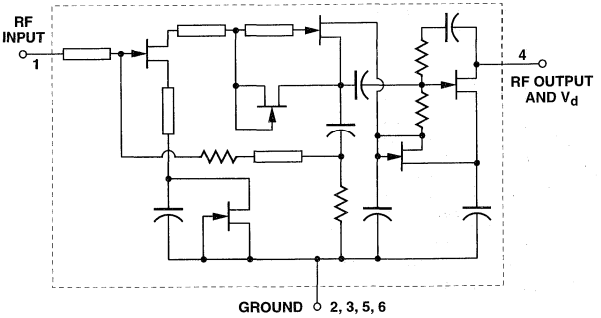


Pin Connections and Package Marking



Note:
Package marking provides orientation and identification.

Equivalent Circuit



Description

Hewlett-Packard's MGA-86563 is an economical, easy-to-use GaAs MMIC amplifier that offers low noise figure and excellent gain for applications from 0.5 to 6 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of the SOT-143.

The MGA-86563 may be used without impedance matching as a high performance 2 dB NF gain block. Alternatively, with the addition of a simple shunt-series inductor at the input, the device noise figure can be reduced to 1.6 dB at 2.4 GHz. For 1.5 GHz applications and above, the output is well matched to 50 Ω. Below 1.5 GHz, gain can be increased by using conjugate matching.

The circuit uses state-of-the-art PHEMT technology with self-biasing current sources, a source-follower interstage, resistive feedback, and on-chip impedance matching networks. A patented, on-chip active bias circuit allows operation from a single +5 V power supply. Current consumption is only 14 mA, making this part suitable for battery powered applications.

MGA-86563 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Device Voltage, RF Output to Ground	V	9
V_{in}	RF Input Voltage to Ground	V	+0.5 –1.0
P_{in}	CW RF Input Power	dBm	+13
T_{ch}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{ch-c} = 160°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

Electrical Specifications, $T_C = 25°C$, $Z_O = 50\ \Omega$ unless noted, $V_d = 5$ V

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G_{test}	Gain in Test Circuit[1]	f = 2.0 GHz		17	20	
NF_{test}	Noise Figure in Test Circuit[1]	f = 2.0 GHz			1.8	2.3
NF_O	Optimum Noise Figure	f = 0.9 GHz	dB		2.0	
	(Tuned for lowest noise figure)	f = 2.0 GHz			1.5	
		f = 2.4 GHz			1.6	
		f = 4.0 GHz			1.7	
		f = 6.0 GHz			2.0	
G_A	Associated Gain at NF_O	f = 0.9 GHz	dB		20.8	
	(Tuned for lowest noise figure)	f = 2.0 GHz			22.7	
		f = 2.4 GHz			22.5	
		f = 4.0 GHz			18.0	
		f = 6.0 GHz			13.7	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.9 GHz	dBm		3.6	
	(50 Ω Performance)	f = 2.0 GHz			4.1	
		f = 2.4 GHz			4.2	
		f = 4.0 GHz			4.3	
		f = 6.0 GHz			3.3	
IP_3	Third Order Intercept Point	f = 2.4 GHz	dBm		+15	
$VSWR_{in}$	Input VSWR	f = 2.4 GHz			2.3:1	
$VSWR_{out}$	Output VSWR	f = 2.4 GHz			1.7:1	
I_d	Device Current		mA		14	

Note:
1. Guaranteed specifications are 100% tested in the circuit in Figure 10 in the Applications Information section.

MGA-86563 Typical Performance, $T_C = 25°C$, $V_d = 5$ V

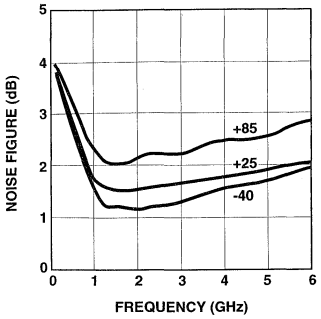


Figure 1. Minimum Noise Figure (Optimum Tuning) vs. Frequency and Temperature.

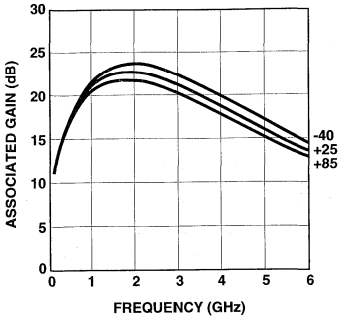


Figure 2. Associated Gain (Optimum Tuning) vs. Frequency and Temperature.

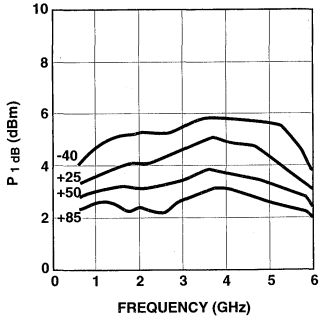


Figure 3. Output Power for 1 dB Gain Compression (into 50 Ω) vs. Frequency and Temperature.

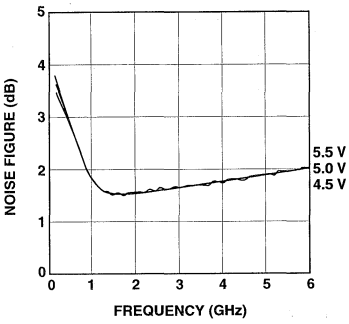


Figure 4. Minimum Noise Figure (Optimum Tuning) vs. Frequency and Voltage.

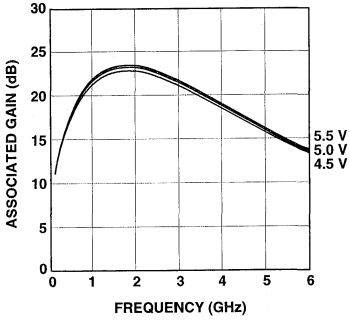


Figure 5. Associated Gain (Optimum Tuning) vs. Frequency and Voltage.

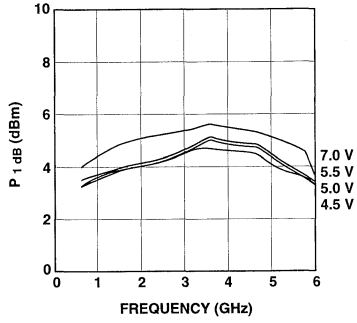


Figure 6. Output Power for 1 dB Gain Compression (into 50 Ω) vs. Frequency and Voltage.

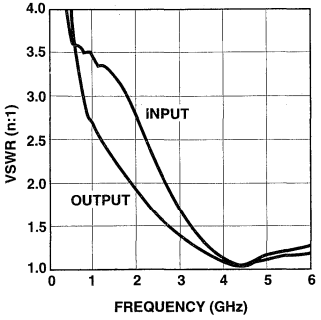


Figure 7. Input and Output VSWR (into 50 Ω) vs. Frequency.

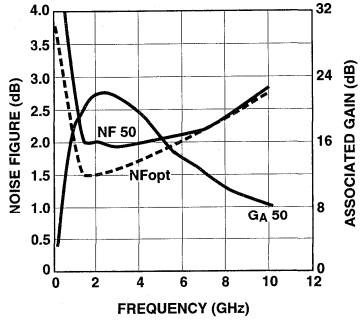


Figure 8. 50 Ω Noise Figure and Associated Gain vs. Frequency.

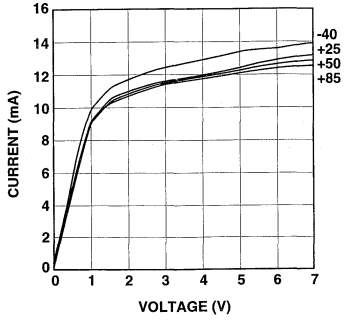


Figure 9. Device Current vs. Voltage.

MGA-86563 Typical Scattering Parameters[1], T_C = 25°C, Z_O = 50 Ω, V_d = 5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Factor
0.1	0.84	-17	3.1	1.42	76	-39.8	0.010	15	0.85	-15	3.27
0.5	0.57	-29	14.7	5.41	41	-44.3	0.006	-23	0.59	-39	6.77
1.0	0.55	-41	18.9	8.77	4	-51.2	0.003	-2	0.46	-53	10.49
1.5	0.53	-57	20.8	10.97	-29	-52.1	0.002	70	0.38	-66	14.23
2.0	0.47	-73	21.7	12.14	-62	-45.2	0.005	96	0.32	-78	5.94
2.5	0.38	-89	21.8	12.33	-94	-40.7	0.009	102	0.24	-89	3.78
3.0	0.26	-104	21.3	11.61	-125	-37.4	0.014	100	0.16	-99	2.92
3.5	0.14	-115	20.2	10.23	-152	-34.4	0.018	97	0.09	-102	2.75
4.0	0.04	-106	18.8	8.75	-177	-32.6	0.023	92	0.03	-82	2.58
4.5	0.04	-6	17.4	7.44	162	-30.9	0.027	88	0.03	1	2.58
5.0	0.07	2	16.1	6.41	143	-29.6	0.032	83	0.05	20	2.53
5.5	0.09	-4	14.9	5.57	126	-28.1	0.038	78	0.06	19	2.45
6.0	0.11	-17	13.9	4.93	110	-26.0	0.044	72	0.08	14	2.38
6.5	0.12	-28	12.9	4.40	94	-24.9	0.050	65	0.08	4	2.35
7.0	0.13	-36	12.0	3.96	79	-23.8	0.057	59	0.09	-3	2.29
7.5	0.15	-44	11.1	3.58	65	-22.6	0.065	53	0.11	-12	2.21
8.0	0.17	-53	10.4	3.30	51	-22.6	0.074	44	0.13	-21	2.10

MGA-86563 Typical Noise Parameters[1],

T_C = 25°C, Z_O = 50 Ω, V_d = 5 V

Frequency	NF_o	Γ_{opt}		
(GHz)	(dB)	Mag.	Ang.	$R_N/50\ \Omega$
5	2.8	0.61	4	1.16
1.0	1.8	0.56	24	0.47
1.5	1.5	0.50	33	0.34
2.0	1.5	0.45	40	0.38
2.5	1.6	0.41	50	0.33
3.0	1.6	0.38	57	0.30
4.0	1.7	0.32	73	0.28
5.0	1.9	0.24	98	0.27
6.0	2.1	0.15	131	0.24

Note:

1. Reference plane per Figure 11 in Applications Information section.

MGA-86563 Applications Information

Introduction

The MGA-86563 is a high gain, low noise RF amplifier for use in wireless RF applications within the 0.5 to 6 GHz frequency range. The MGA-86563 is a three-stage, GaAs Microwave Monolithic Integrated Circuit (MMIC) amplifier that uses internal feedback to provide wideband gain and impedance matching.

A patented, active bias circuit makes use of current sources to "re-use" the drain current in all three stages of gain, thus minimizing the required supply current and decreasing sensitivity to variations in power supply voltage.

Test Circuit

The circuit shown in Figure 10 is used for 100% RF testing of Noise Figure and Gain. The input of this circuit is fixed tuned for a conjugate power match (maximum power transfer, or, minimum Input VSWR) at 2 GHz. Tests in this circuit are used to guarantee the NF_{test} and G_{test} parameters shown in the Electrical Specifications Table.

The 3.3 nH inductor, L1 (Coilcraft, Cary, IL or equivalent) in series with the input of the amplifier matches the input to 50 Ω at 2 GHz.

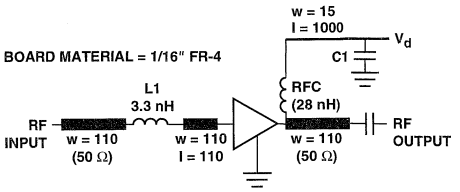


Figure 10. Test Circuit for 2 GHz.

The parameter test circuit uses a high impedance RF choke to apply V_d to the MMIC while isolating the power supply from the RF Output of the amplifier.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters and to specify Γ_{opt} for the Noise Parameters are shown in Figure 11. As seen in the illustration, the reference planes are located at the extremities of the package leads.

Biasing

The MGA-86563 is a voltage-biased device and operates from a single +5 volt power supply. With a typical current drain of only 14 mA, the MGA-86563 is suitable for use in battery powered applications. RF performance is very stable over a wide variation of power supply voltage.

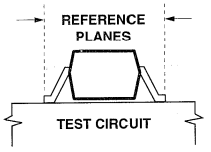


Figure 11. Reference Planes.

Since DC bias is applied to the MGA-86563 through the RF Output pin, some method of isolating the RF from the DC must be provided. An RF choke or length of high impedance transmission line is typically used for this purpose.

SOT-363 PCB Layout

A PCB pad layout for the miniature SOT-363 (SC-70) package used by the MGA-86563 is shown in Figure 12 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the MGA-86563. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads.

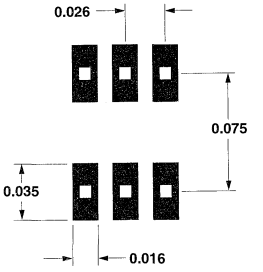


Figure 12. PCB Pad Layout (dimensions in inches).

RF Layout

The RF layout in Figure 13 is suggested as a starting point for amplifier designs using the MGA-86563 MMIC. Adequate grounding is needed to obtain maximum performance and to obviate potential instability. All four ground pins of the MMIC should be connected to RF ground by using plated through holes (vias) near the package terminals.

It is recommended that the PCB pads for the ground pins NOT be connected together underneath the body of the package. PCB traces hidden under the package cannot be adequately inspected for SMT solder quality.

PCB Material

FR-4 or G-10 printed circuit board material is a good choice for most low cost wireless applications. Typical board thickness is 0.020 or 0.031 inches. The width of 50 Ω microstriplines in PC boards of these thicknesses is also convenient for mounting chip components such as the series inductor that is used at the input for impedance matching or for DC blocking capacitors.

For applications requiring the lowest noise figures, the use of PTFE/glass dielectric materials may be warranted to minimize transmission line losses at the amplifier input. A 0.5 inch length of 50 Ω microstripline on FR-4 has approximately 0.3 dB loss at 4 GHz which will add directly to the noise figure of the MGA-86563.

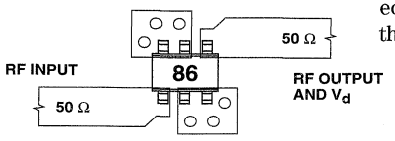


Figure 13. RF Layout.

Typical Application Circuit

A typical implementation of the MGA-86563 as a low noise amplifier is shown in Figure 14.

A 50 Ω microstripline with a series DC blocking capacitor, C1, is used to feed RF to the MMIC. The input of the MGA-86563 is already partially matched for noise figure and gain to 50 Ω. The use of a simple input matching circuit, such as a series inductor, will minimize amplifier noise figure. Since the impedance match for NF_O (minimum noise figure) is very close to a conjugate power match, a low noise figure can be realized simultaneously with a low input VSWR.

DC power is applied to the MMIC through the same pin that is shared with the RF output. A 50 Ω microstripline is used to connect the device to the following stage. A bias decoupling network is used to feed in V_d while simultaneously providing a DC block to the RF signal. The bias decoupling network shown in Figure 14, consisting of resistor R1, a short length of high impedance microstripline, and bypass capacitor C3, will provide excellent performance over a wide frequency range. Surface mount chip inductors could be used in place of the high impedance transmission line to act as an RF choke. Consideration should be given to potential resonances and signal radiation when using lumped inductors.

For operation at frequencies below approximately 2 GHz, the addition of a simple impedance matching circuit to the output will increase the gain and output power by 0.5 to 1.5 dB. The output matching circuit will not effect the noise figure.

A small value resistor placed in series with the V_{dd} line may be useful to "de-Q" the bias circuit. Typical values of R1 are in the 10 Ω to 100 Ω range. Depending on the value of resistance used, the supply voltage may have to be increased to compensate for voltage drop across R1. The power supply should be capacitively bypassed (C3) to ground to prevent undesirable gain variations and to eliminate unwanted feedback through the bias lines that could cause oscillation.

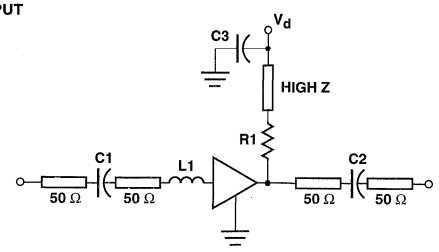


Figure 14. Typical Amplifier Circuit.

Higher Bias Voltages

While the MGA-86563 is designed primarily for use in +5 volt applications, the internal bias regulation circuitry allows it to be operated with any power supply voltage from +5 to +7 volts. The use of +7 volts increases the P_{1dB} by approximately 1 dBm. The effect on noise figure, gain, and VSWR with higher V_d is negligible.

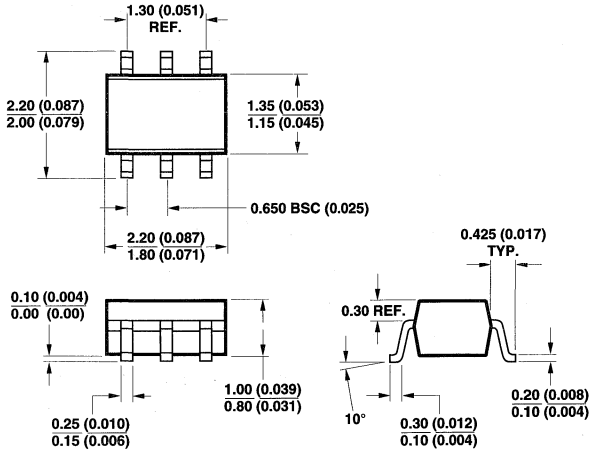
For more information call your nearest HP sales office.

MGA-86563 Part Number Ordering Information

Part Number	Devices per Container	Container
MGA-86563-TR1	3000	7" reel
MGA-86563-BLK	100	Antistatic bag

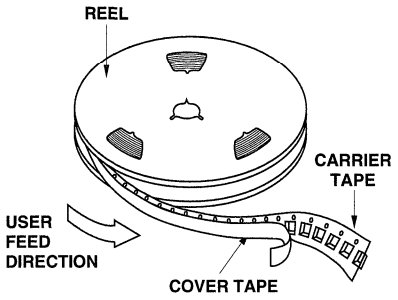
Package Dimensions

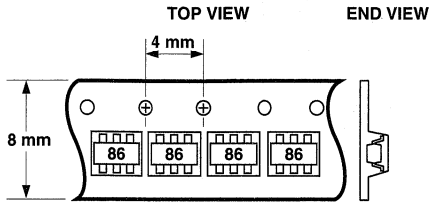
Outline 63 (SOT-363/SC-70)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

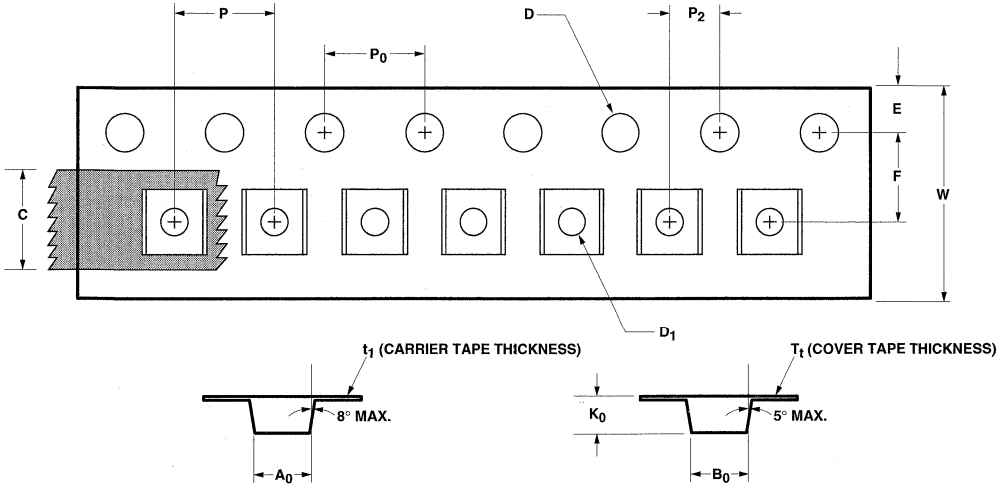
Device Orientation





Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

1.5 – 8 GHz Low Noise GaAs MMIC Amplifier

Technical Data

MGA-86576

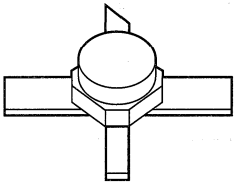
Features

- **1.6 dB Noise Figure at 4 GHz**
- **23 dB Gain at 4 GHz**
- **+6 dBm P_{1dB} at 4 GHz**
- **Single +5 V Bias Supply**

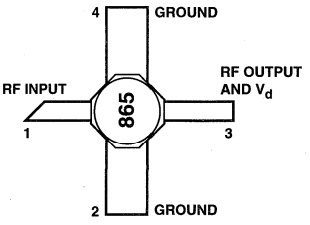
Applications

- **LNA or Gain Stage for 2.4 GHz and 5.7 GHz ISM Bands**
- **Front End Amplifier for GPS Receivers**
- **LNA or Gain Stage for PCN and MMDS Applications**
- **C-Band Satellite Receivers**
- **Broadband Amplifier for Instrumentation**

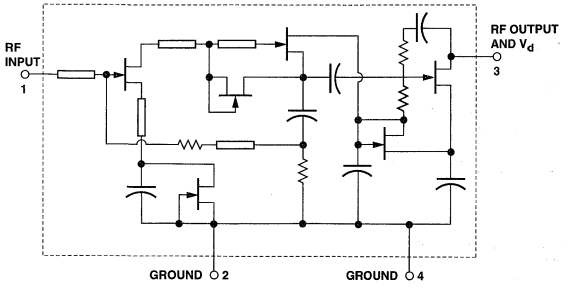
Surface Mount Ceramic Package



Pin Connections



Schematic Diagram



Description

Hewlett-Packard's MGA-86576 is an economical, easy-to-use GaAs MMIC amplifier that offers low noise and excellent gain for applications from 1.5 to 8 GHz.

The MGA-86576 may be used without impedance matching as a high performance 2 dB NF gain block. Alternatively, with the addition of a simple series inductor at the input, the device noise figure can be reduced to 1.6 dB at 4 GHz.

The circuit uses state-of-the-art PHEMT technology with self-biasing current sources, a source-follower interstage, resistive feedback, and on chip impedance matching networks.

A patented, on-chip active bias circuit allows operation from a single +5 V power supply. Current consumption is only 16 mA.

These devices are 100% RF tested to assure consistent performance.

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Device Voltage, RF output to ground	V	9
V_g	Device Voltage, RF input to ground	V	+0.5 -1.0
P_{in}	CW RF Input Power	dBm	+13
T_{ch}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{ch\text{-}c} = 110°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_c = 25°C$ (T_c is defined to be the temperature at the package pins where contact is made to the circuit board).

MGA-86576 Electrical Specifications, $T_C = 25°C$, $Z_o = 50\ \Omega$, $V_d = 5\ V$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
Gp	Power Gain ($\|S_{21}\|^2$)	f = 1.5 GHz	dB		21.2	
		f = 2.5 GHz			23.7	
		f = 4.0 GHz		20	23.1	
		f = 6.0 GHz			19.3	
		f = 8.0 GHz			15.4	
NF_{50}	50 Ω Noise Figure	f = 1.5 GHz	dB		2.2	
		f = 2.5 GHz			1.9	
		f = 4.0 GHz			2.0	2.3
		f = 6.0 GHz			2.3	
		f = 8.0 GHz			2.5	
NF_o	Optimum Noise Figure (Input tuned for lowest noise figure)	f = 1.5 GHz	dB		1.6	
		f = 2.5 GHz			1.5	
		f = 4.0 GHz			1.6	
		f = 6.0 GHz			1.8	
		f = 8.0 GHz			2.1	
P_{1dB}	Output Power at 1 dB Gain Compression	f = 1.5 GHz	dBm		6.4	
		f = 2.5 GHz			7.0	
		f = 4.0 GHz			6.3	
		f = 6.0 GHz			4.3	
		f = 8.0 GHz			3.8	
IP_3	Third Order Intercept Point	f = 4.0 GHz	dBm		16.0	
VSWR	Input VSWR	f = 1.5 GHz			3.6:1	
		f = 2.5 GHz			3.3:1	
		f = 4.0 GHz			2.2:1	3.6:1
		f = 6.0 GHz			1.4:1	
		f = 8.0 GHz			1.2:1	
	Output VSWR	f = 1.5 GHz			2.5:1	
		f = 2.5 GHz			2.1:1	
		f = 4.0 GHz			1.7:1	
		f = 6.0 GHz			1.4:1	
		f = 8.0 GHz			1.3:1	
I_d	Device Current		mA	9	16	22

MGA-86576 Typical Performance, T_C = 25°C, Z_o = 50 Ω, V_d = 5 V

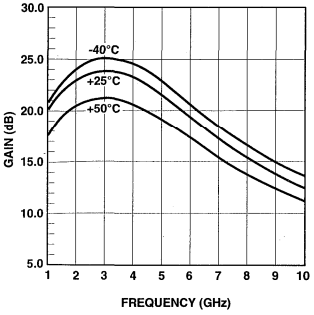


Figure 1. Power Gain vs. Frequency at Three Temperatures.

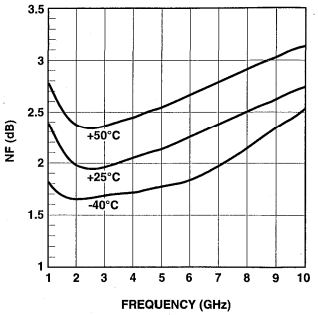


Figure 2. 50 Ω Noise Figure vs. Frequency at Three Temperatures.

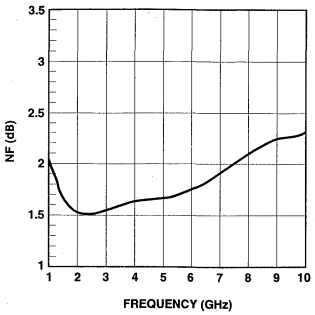


Figure 3. Matched Noise Figure vs. Frequency.

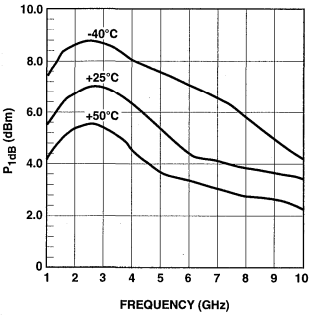


Figure 4. P_{1dB} vs. Frequency at Three Temperatures.

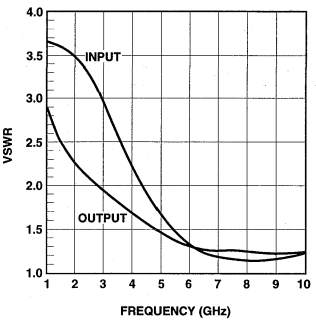


Figure 5. Input and Output VSWR vs. Frequency.

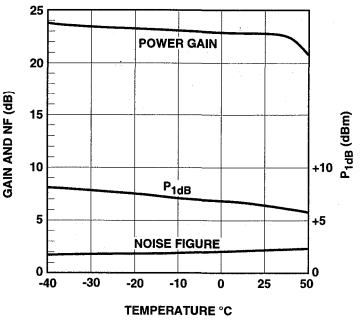


Figure 6. Gain, NF_{50}, and P_{1dB} vs. Temperature at 4 GHz.

MGA-86576 Typical Scattering Parameters [3], T_C = 25°C, Z_o = 50 Ω, V_d = 5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	0.57	-21	15.5	5.99	46	-46.5	0.005	-15	0.62	-35
1.0	0.55	-30	19.8	9.72	17	-51.3	0.003	11	0.49	-47
1.5	0.54	-44	21.7	12.15	-7	-51.2	0.003	58	0.43	-57
2.0	0.52	-59	22.8	13.84	-31	-47.0	0.004	85	0.39	-68
2.5	0.48	-77	23.5	14.98	-54	-43.0	0.007	96	0.36	-79
3.0	0.43	-96	23.8	15.56	-77	-39.7	0.010	100	0.33	-92
3.5	0.37	-116	23.7	15.28	-100	-37.0	0.014	99	0.29	-105
4.0	0.30	-137	23.2	14.49	-122	-35.0	0.018	95	0.25	-118
4.5	0.24	-159	22.4	13.18	-142	-33.2	0.022	92	0.21	-130
5.0	0.19	178	21.5	11.82	-160	-31.9	0.026	89	0.19	-139
5.5	0.14	151	20.5	10.54	-177	-30.6	0.030	85	0.14	-151
6.0	0.12	129	19.2	9.14	166	-29.6	0.033	81	0.17	-151
6.5	0.10	111	18.1	8.08	156	-28.7	0.037	82	0.14	-116
7.0	0.08	91	17.5	7.48	142	-27.4	0.042	76	0.08	-158
7.5	0.08	75	16.4	6.64	129	-26.6	0.047	72	0.11	-153
8.0	0.07	64	15.5	5.99	118	-25.8	0.051	69	0.09	-151
8.5	0.06	48	14.7	5.45	107	-25.0	0.056	65	0.09	-146
9.0	0.04	31	14.0	5.03	96	-24.2	0.062	62	0.09	-140
9.5	0.02	18	13.4	4.66	86	-23.4	0.068	58	0.11	-143
10.0	0.01	93	12.7	4.33	76	-22.6	0.074	53	0.11	-154

MGA-86576 Typical Noise Parameters[3],

$T_C = 25°C$, $Z_o = 50\ \Omega$, $V_d = 5\ V$

Frequency GHz	NF_o dB	Γopt		$R_N/50\ \Omega$
		Mag.	Ang.	
1.0	2.1	0.56	27	0.43
1.5	1.6	0.54	31	0.40
2.5	1.5	0.47	40	0.36
4.0	1.6	0.38	54	0.32
6.0	1.8	0.28	77	0.28
8.0	2.1	0.22	107	0.25

[3]Reference plane taken at point where leads meet body of package.

MGA-86576 Applications Information

Introduction

The MGA-86576 is a high gain, broad band, low noise amplifier. The use of plated through holes or an equivalent minimal inductance grounding technique placed precisely under each ground lead at the device is highly recommended. A minimum of two plated through holes under each ground lead is preferred with four being highly suggested. A long ground path to pins 2 and 4 will add additional inductance which can cause gain peaking in the 2 to 4 GHz frequency range. This can also be accompanied by a decrease in stability. A suggested layout is shown in Figure 7. The circuit is designed for use on 0.031 inch thick FR-4/G-10 epoxy glass dielectric material.

Printed circuit board thickness is also a major consideration. Thicker printed circuit boards dictate longer plated through holes which provide greater undesired inductance. The parasitic inductance associated with a pair of plated through holes passing through 0.031 inch thick printed circuit board is approximately 0.1 nH, while the inductance of a pair of plated through holes passing through 0.062 inch thick board is about 0.2 nH. Hewlett-Packard does not recommend using the MGA-86576 MMIC on boards thicker than 0.040 inch.

The effects of inductance associated with the board material are easily analyzed and very predictable. As a minimum, the circuit simulation should consist of the data sheet S-Parameters and an additional circuit file describing the plated through holes and any additional inductance associated with lead length between the device and the start of the plated through hole. To obtain a complete analysis of the entire amplifier circuit, the effects of the input and output microstriplines and bias decoupling circuits should be incorporated into the circuit file.

Device Connections V_d and RF Output (Pin 3)

RF and DC connections are shown in Figure 8. DC power is provided to the MMIC through the same pin used to obtain RF output. A 50 Ω microstripline is used to connect the device to the following stage or output connector. A bias decoupling network is used to feed in V_{dd}

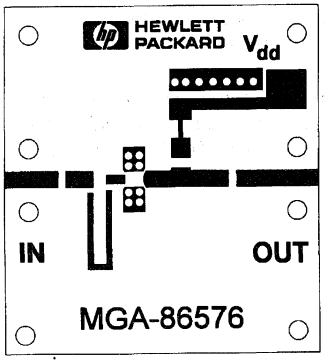


Figure 7. Layout for MGA-86576 Demonstration Amplifier. PCB dimensions are 1.18 inches wide by 1.30 inches high.

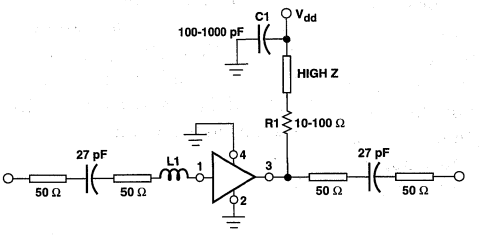


Figure 8. Demonstration Amplifier Schematic.

while simultaneously providing a DC block to the RF signal. The bias decoupling network shown in Figure 8, consisting of resistor R1, a short length of high impedance microstripline, and bypass capacitor C1, provides the best overall performance in the 2 to 8 GHz frequency range.

The use of lumped inductors is not desired since they tend to radiate and cause undesired feedback. Moving the bypass capacitor, C1, down the microstripline towards the V_{dd} terminal, as shown in Figure 9, will improve the gain below 2 GHz by trading off some high end gain. A minimum value of 10 Ω for R1 is

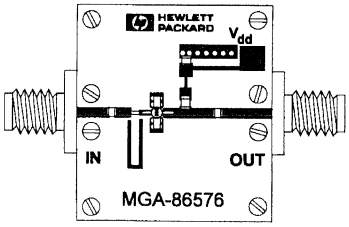


Figure 9. Complete MGA-86576 Demonstration Amplifier.

recommended to de-Q the bias decoupling network, although 100 Ω will provide the highest circuit gain over the entire 1.5 to 8 GHz frequency range. V_{dd} will have to be increased accordingly for higher values of R1. For operation in the 2 to 6 GHz frequency range, a 10 pF capacitor may be used for DC blocking on the output microstripline. A larger value such as 27 pF is more appropriate for operation at 1.5 GHz.

Ground (Pins 2 and 4)

Ground pins should attach directly to the backside ground plane by the shortest distance possible using the design hints suggested in the earlier section. Liberal use of plated through vias is recommended.

RF Input (Pin 1)

A 50 Ω microstripline can be used to feed RF to the device. A blocking capacitor in the 10 pF range will provide a suitable DC block in the 2 to 6 GHz frequency range. Although there is no voltage present at pin 1, it is highly suggested that a DC blocking capacitor be used to prevent accidental application of a voltage from a previous amplifier stage. With no further input matching, the MGA-86576 is capable of noise figures as low as 2 dB in the 2 to 6 GHz frequency range. Since Γ_o is not 50 Ω, it is possible to design and implement a very simple matching network in order to improve noise figure and input return loss over a narrow frequency range. The circuit board layout shown in Figure 7 provides an option for tuning for a low noise match anywhere in the 1.5 to 4 GHz frequency range. For optimum noise figure performance in the 4 GHz frequency range, L1 can be a 0.007 inch diameter wire 0.080 inches in length as shown in Figure 9. Alternatively, L1 can be replaced by a 0.020 inch wide microstripline whose length can be adjusted for minimum noise figure in the 1.5 to 4 GHz frequency range.

Table 1 provides the approximate inductor length for minimum noise figure at a given frequency for the circuit board shown in Figure 7.

Table 1. L1 Length vs. Frequency for Optimum Noise Figure.

Frequency GHz	Length Inches
1.5	0.70
1.8	0.60
2.1	0.50
2.4	0.40
2.5	0.30
3.0	0.20
3.7	0.10
4.0	0.05

7 Volt Bias for Operation at Higher Temperatures

The MGA-86576 was designed primarily for 5 volt operation over the -25 to +50°C temperature range. For applications requiring use to +85°C, a 7 volt bias supply is recommended to minimize changes in gain and noise figure at elevated temperature. Figure 10 shows typical gain, noise figure, and output power performance over temperature at 4 GHz with 7 volts applied. With a 7 volt bias supply, output power is increased approximately 1.5 dB. Other parameters are relatively unchanged from 5 volt data. S-parameter and noise parameter data for 7 volts are available upon request from Hewlett-Packard.

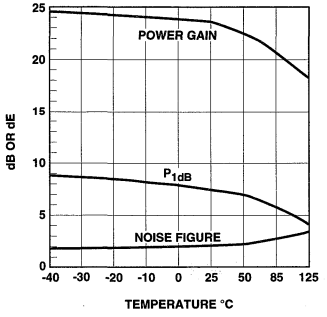


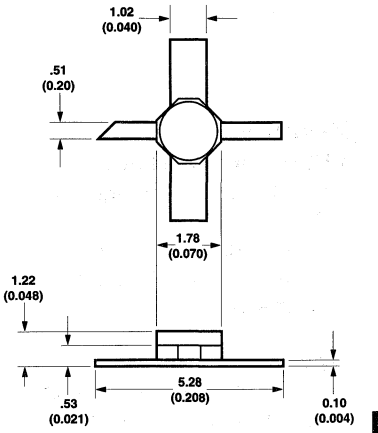
Figure 10. Gain, NF_{50}, and P_{1dB} vs. Temperature at 4 GHz with 7 Volt Bias Supply.

Printed Circuit Board Materials

Most commercial applications dictate the need to use inexpensive epoxy glass materials such as FR-4 or G-10. Unfortunately the losses of this type of material can become excessive above 2 GHz. As an example, a 0.5 inch long 50 Ω microstripline etched on FR-4 along with a blocking capacitor has a measured loss of 0.35 dB at 4 GHz. The 0.35 dB loss adds directly to the noise figure of the MGA-86576. The use of a low loss PTFE based dielectric material will preserve the inherent low noise of the MGA-86576.

Package Dimensions

76 Package



TYPICAL DIMENSIONS ARE IN MILLIMETERS (INCHES).

MGA-86576 Part Number Ordering Information

Part Number	No. of Devices	Container
MGA-86576-STR	10	Strip
MGA-86576-TR1	1000	7-inch Reel

For more information call your nearest HP sales office.

HEWLETT® PACKARD

0.5 – 4 GHz 3 V Low Current GaAs MMIC LNA

Technical Data

MGA-87563

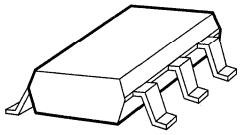
Features

- **Ultra-Miniature Package**
- **1.6 dB Min. Noise Figure at 2.4 GHz**
- **12.5 dB Gain at 2.4 GHz**
- **Single +3 V or 5 V Supply, 4.5 mA Current**

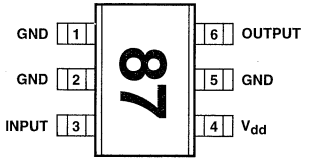
Applications

- **LNA or Gain Stage for PCS, ISM, Cellular, and GPS Applications**

Surface Mount SOT-363 (SC-70) Package

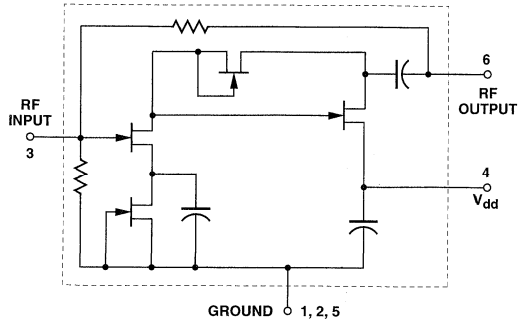


Pin Connections and Package Marking



Note:
Package marking provides orientation and identification.

Equivalent Circuit



Description

Hewlett-Packard's MGA-87563 is an economical, easy-to-use GaAs MMIC amplifier that offers low noise and excellent gain for applications from 0.5 to 4 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

With the addition of a simple shunt-series inductor at the input, the device is easily matched to achieve a noise of 1.6 dB at 2.4 GHz. For 2.4 GHz applications and above, the output is well matched to 50 Ohms. Below 2 GHz, gain can be increased by using conjugate matching.

The circuit uses state-of-the-art PHEMT technology with self-biasing current sources, a source-follower interstage, resistive feedback, and on-chip impedance matching networks. A patented, on-chip active bias circuit allows operation from a single +3 V or +5 V power supply. Current consumption is only 4.5 mA, making this part ideal for battery powered designs.

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{dd}	Device Voltage, RF Output to Ground	V	6
V_{in} V_{out}	RF input or RF Output Voltage to Ground	V	+0.5 −1.0
P_{in}	CW RF Input Power	dBm	+13
T_{ch}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{ch\text{-}c} = 160°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

MGA-87563 Electrical Specifications[3], $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{dd} = 3\ V$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G_{test}[3]		f = 2.0 GHz		11	14	
NF_{test}[3]		f = 2.0 GHz			1.8	2.3
NF_o	Optimum Noise Figure	f = 0.9 GHz	dB		1.9	
	(Tuned for lowest noise figure)	f = 1.5 GHz			1.6	
		f = 2.0 GHz			1.6	
		f = 2.4 GHz			1.6	
		f = 4.0 GHz			2.0	
G_a	Associated Gain at NF_O	f = 0.9 GHz	dB		14.6	
	(Tuned for lowest noise figure)	f = 1.5 GHz			14.5	
		f = 2.0 GHz			14.0	
		f = 2.4 GHz			12.5	
		f = 4.0 GHz			10.3	
P_{1dB}	Output Power at 1 dB Gain Compression	f = 0.9 GHz	dBm		-2.0	
		f = 1.5 GHz			-1.8	
		f = 2.0 GHz			-2.0	
		f = 2.4 GHz			-2.0	
		f = 4.0 GHz			-2.6	
IP_3	Third Order Intercept Point	f = 2.4 GHz	dBm		+8	
VSWR	Output VSWR	f = 2.4 GHz			1.8	
I_{dd}	Device Current		mA		4.5	

Note:
3. Guaranteed specifications are 100% tested in the circuit in Figure 10 in the Applications Information section.

MGA-87563 Typical Performance, $T_C = 25°C$, $V_{dd} = 3$ V

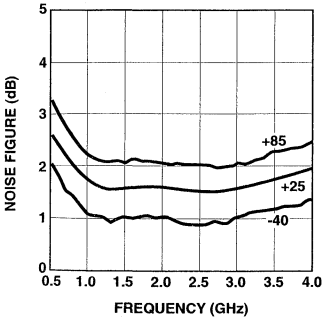


Figure 1. Minimum Noise Figure (Optimum Tuning) vs. Frequency and Temperature.

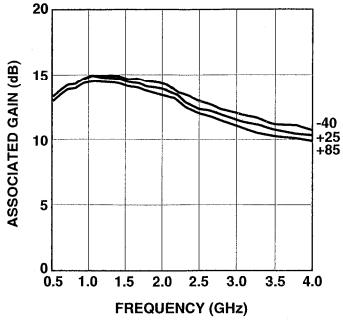


Figure 2. Associated Gain (Optimum Tuning) vs. Frequency and Temperature.

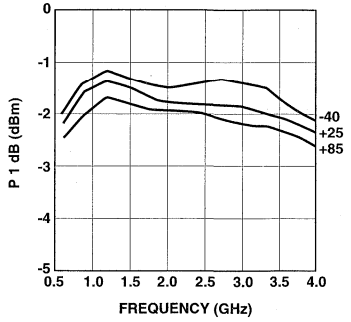


Figure 3. Output Power for 1 dB Gain Compression (into 50 Ω) vs. Frequency and Temperature.

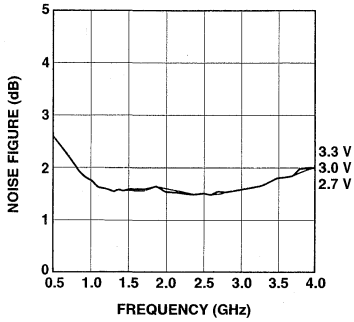


Figure 4. Minimum Noise Figure (Optimum Tuning) vs. Frequency and Voltage.

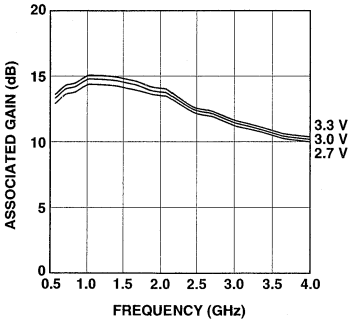


Figure 5. Associated Gain (Optimum Tuning) vs. Frequency and Voltage.

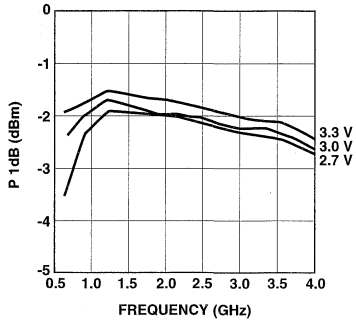


Figure 6. Output Power for 1 dB Gain Compression (into 50 Ω) vs. Frequency and Voltage.

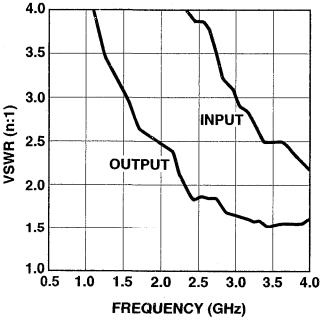


Figure 7. Input and Output VSWR (into 50 Ω) vs. Frequency.

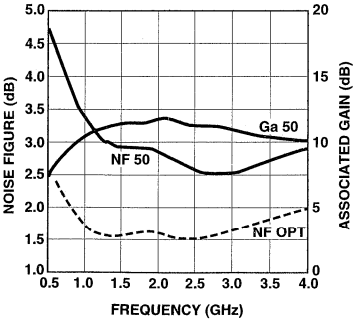


Figure 8. 50 Ω Noise Figure and Associated Gain vs. Frequency.

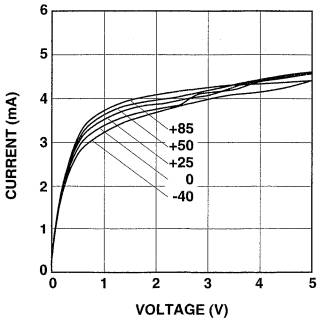


Figure 9. Device Current vs. Voltage.

MGA-87563 Typical Scattering Parameters[4], T_C = 25°C, Z_O = 50 Ω, V_{dd} = 3 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	Factor
0.1	0.92	-5	-5.6	0.53	-90	-22.7	0.073	-7	0.86	-11	0.41
0.2	0.91	-8	-0.7	0.92	-100	-22.7	0.073	-9	0.85	-18	0.29
0.5	0.88	-20	6.7	2.15	-131	-23.4	0.068	-18	0.78	-43	0.33
1.0	0.79	-35	10.1	3.22	-170	-25.2	0.055	-26	0.61	-75	0.72
1.5	0.73	-49	11.2	3.63	163	-26.2	0.049	-33	0.50	-100	1.02
2.0	0.67	-60	11.4	3.72	140	-26.6	0.047	-39	0.42	-122	1.32
2.5	0.59	-69	11.0	3.54	119	-29.1	0.035	-40	0.31	-141	2.38
3.0	0.50	-78	10.7	3.41	101	-32.5	0.024	-52	0.25	-167	4.29
3.5	0.43	-83	10.1	3.20	85	-35.1	0.018	-12	0.20	172	6.74
4.0	0.37	-96	10.0	3.16	71	-37.7	0.013	-10	0.24	143	9.83
4.5	0.31	-91	8.7	2.72	52	-26.1	0.050	20	0.11	123	3.33
5.0	0.30	-105	8.1	2.55	42	-25.9	0.050	-3	0.17	127	3.48

MGA-87563 Typical Noise Parameters[4], T_C = 25°C, Z_O = 50 Ω, V_{dd} = 3 V

Frequency	NF_o	Γ_{opt}		
(GHz)	(dB)	Mag.	Ang.	$R_N/50\ \Omega$
0.5	2.6	0.71	1	1.57
1.0	1.7	0.68	17	0.96
1.5	1.6	0.68	28	0.75
2.0	1.6	0.66	36	0.67
2.5	1.6	0.63	42	0.56
3.0	1.6	0.59	49	0.53
3.5	1.8	0.56	55	0.55
4.0	2.0	0.53	62	0.58

Notes:
4. Reference plane per Figure 11 in Applications Information section.

MGA-87563 Applications Information

Introduction

The MGA-87563 low noise RF amplifier is designed to simplify wireless RF applications in the 0.5 to 4 GHz frequency range. The MGA-87563 is a two-stage, GaAs Microwave Monolithic Integrated Circuit (MMIC) amplifier that uses feedback to provide wideband gain. The output is matched to 50 Ω and the input is partially matched for optimum noise figure.

A patented, active bias circuit makes use of current sources to "re-use" the drain current in both stages of gain, thus minimizing the required supply current and decreasing sensitivity to variations in power supply voltage.

Test Circuit

The circuit shown in Figure 10 is used for 100% RF testing of Noise Figure and Gain. The input of this circuit is fixed tuned for a conjugate power match (maximum power transfer, or, minimum Input VSWR) at 2 GHz. Tests in this circuit are used to guarantee the NF_{test} and G_{test} parameters shown in the Electrical Specifications table.

The 4.7 nH inductor, L1 (Coilcraft, Cary, IL part number series 1008CT-040) placed in series with the input of the amplifier is all that is necessary to match the input to 50 Ω at 2 GHz.

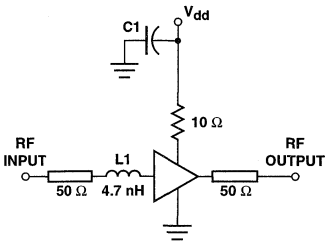


Figure 10. Test Circuit for 2 GHz.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters and to specify Γ_{opt} for the Noise Parameters are shown in Figure 11. As seen in the illustration, the reference planes are located at the extremities of the package leads.

Biasing

The MGA-87563 is a voltage-biased device and operates from a single +3 volt power supply. With a typical current drain of only 4.5 mA, the MGA-87563 is very well suited for use in battery powered applications. All bias regulation circuitry is integrated into the MMIC, eliminating the need for external DC components. RF performance is very consistent for 3-volt battery supplies that may range from 2.7 to 3.3 volts, depending on battery "freshness" or state of charge for rechargeable batteries. Operation up to +5 volts is discussed at the end of the Applications section.

The test circuit in Figure 10 illustrates a suitable method for bringing bias into the MGA-87563. The bias connection must be designed so that it adequately bypasses the V_{dd} terminal while not inadvertently creating any resonances at frequencies where the MGA-87563 has gain.

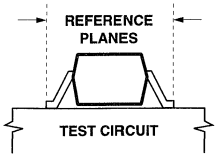


Figure 11. Reference Planes.

The 10 Ω resistor, R1, serves to "de-Q" any potential resonances in the bias line that could lead to low gain, unwanted gain variations or device instability. The power supply end of R1 is bypassed to ground with capacitor C1. The suggested value for C1 is 100 pF. Significantly higher values for C1 are not recommended. Many higher value chip capacitors (e.g., 1000 pF) are not of sufficiently high quality at these frequencies to function well as a RF bypass without adding harmful parasitics or self-resonances.

While the input and output terminals are internally resistively grounded, these pins should not be considered to be current sinks. Connection of the MGA-87563 amplifier to circuits that are at ground potential may be made without the additional cost and PCB space needed for DC blocking capacitors. If the amplifier is to be cascaded with active circuits having non-zero voltages present, the use of series blocking capacitors is recommended.

Input Matching

The input of the MGA-87563 is partially matched internally to 50 Ω. The use of a simple input conjugate matching circuit (such as shown in Figure 10 for 2 GHz), will lower the noise figure considerably. A significant advantage of the MGA-87563's design is that the impedance match for NF_o (minimum noise figure) is very close to a conjugate power match. This means that a very low noise figure can be realized simultaneously with a low input VSWR. The typical difference

between the noise figure obtainable with a conjugate power match at the input and NF_0 is only about 0.2 dB.

Output Matching

The output of the MGA-87563 is matched internally to 50 Ω above 1.8 GHz. The use of a conjugate matching circuit, such as a simple series inductor, can increase the gain considerably at lower frequencies. Matching the output will not affect the noise figure.

Stability

If the MGA-87563 is cascaded with highly reactive stages (such as filters) some precautions may be needed to ensure stability. The low frequency stability (under 1.5 GHz) of the MGA-87563 can be enhanced by adding a series R-L network in shunt with the output, as shown in Figure 12. The inductor can be either a chip component or a high impedance transmission line as shown in the figure. Component values are selected such that the output of the MGA-87563 will be resistively loaded at low frequencies while allowing high frequency signals to pass the stability load with minimal loss.

Typical values for the resistor are in the 25 to 50 Ω range. A suggested starting place for the inductor is a 0.35 to 0.40-inch long microstripline with a width of 0.020 inches, using 0.031-inch thick FR-4 (ε_r = 4.8) circuit board as the substrate.

For applications near 1.5 GHz, gain (and output power) may be traded off for increased stability.

Some precautions regarding the V_{dd} connection of the MGA-87563 are also recommended to ensure stability within the operating frequency range of the device. It is important that the connection to the power supply be properly bypassed to realize full amplifier performance. Refer to the Biasing section above for more information.

SOT-363 PCB Layout

A PCB pad layout for the miniature SOT-363 (SC-70) package is shown in Figure 13 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the MGA-87563. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads.

RF Layout

The RF layout in Figure 14 is suggested as a starting point for designs using the MGA-87563 amplifier. Adequate grounding is needed to obtain maximum performance and to obviate potential instability. All three ground pins of the MMIC should be connected to RF ground by using plated through holes (vias) near the package terminals.

It is recommended that the PCB traces for the ground pins NOT be connected together underneath the body of the package. PCB pads hidden under the package cannot be adequately inspected for SMT solder quality.

FR-4 or G-10 PCB material is a good choice for most low cost wireless applications. Typical board thickness is 0.025 or 0.031 inches. The width of 50 Ω microstriplines in these PCB thicknesses is also convenient for mounting chip components such as the series inductor at the input

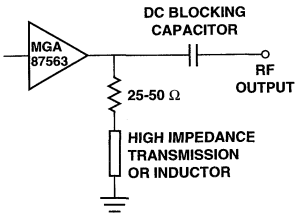


Figure 12. Output Circuitry for Low Frequency Stability.

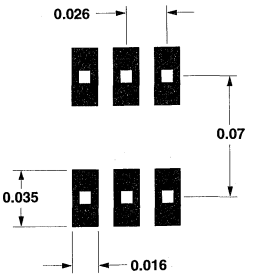


Figure 13. PCB Pad Layout (dimensions in inches).

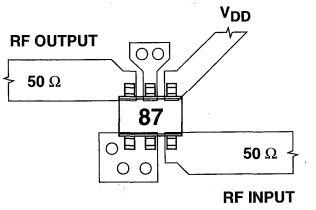


Figure 14. RF Layout.

for impedance matching or for DC blocking capacitors. For noise figure sensitive applications, the use of PTFE/glass dielectric materials may be warranted to minimize transmission line losses at the amplifier input.

Higher Bias Voltages

While the MGA-87563 is designed for use in +3 volt battery powered applications, the internal bias regulation circuitry allows it to be easily operated with any power supply voltage from +2.7 to 5 volts. Figure 15 shows an increase of approximately 1 dB in the associated gain with +5 volts applied. The P_{1dB} output power (Figure 17) is also higher by about 1 dBm. The effect of higher V_{dd} on noise figure is negligible as indicated in Figure 16.

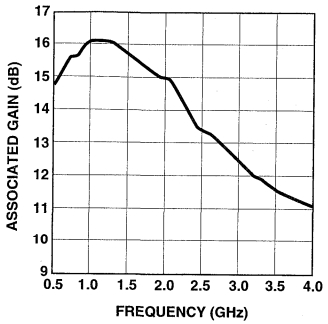


Figure 15. Associated Gain vs. Frequency at V_{dd} = 5 Volts.

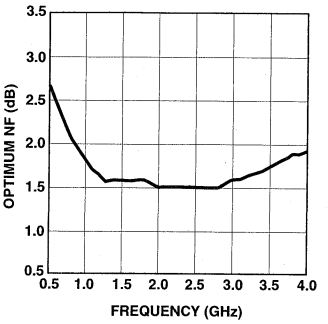


Figure 16. Optimum Noise Figure vs. Frequency at V_{dd} = 5 Volts.

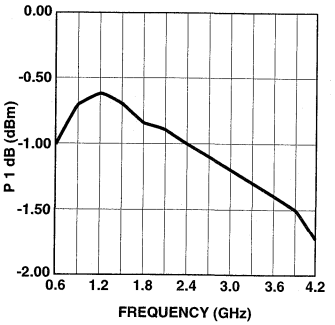


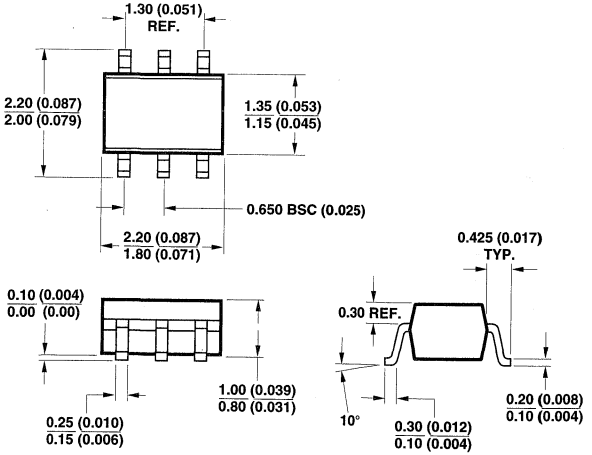
Figure 17. Output Power at 1 dB Gain Compression vs. Frequency at V_{dd} = 5 Volts.

MGA-87563 Part Number Ordering Information

Part Number	Devices per Container	Container
MGA-87563-TR1	3,000	7" reel
MGA-87563-BLK	100	Antistatic bag

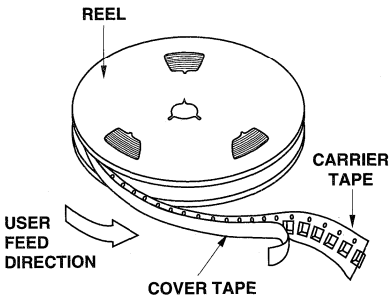
Package Dimensions

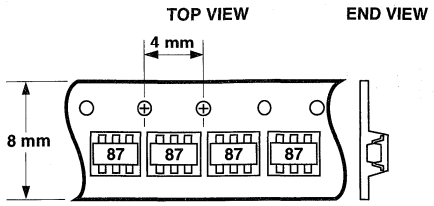
Outline 63 (SOT-363/SC-70)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

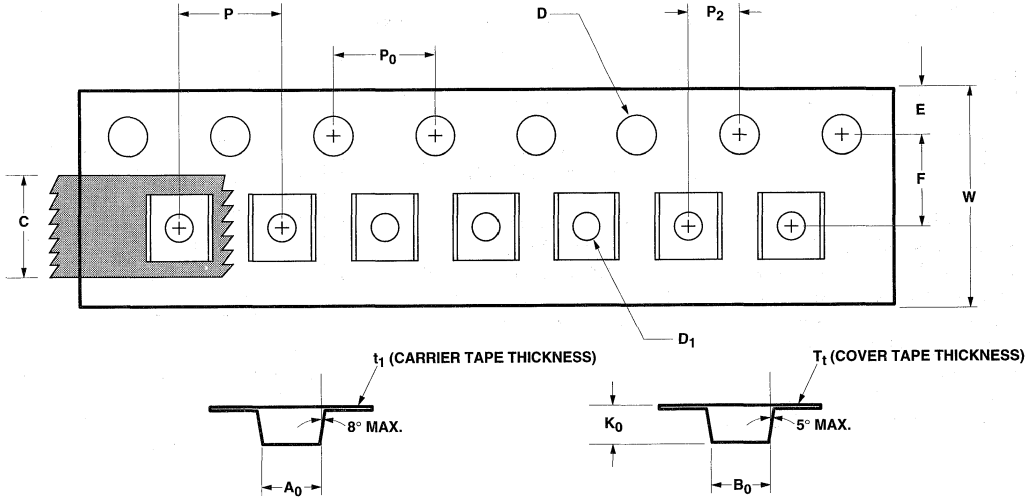
Device Orientation





Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0100

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 1.3 GHz
- **High Gain:** 18.5 dB Typical at 0.5 GHz
- **Unconditionally Stable (k>1)**

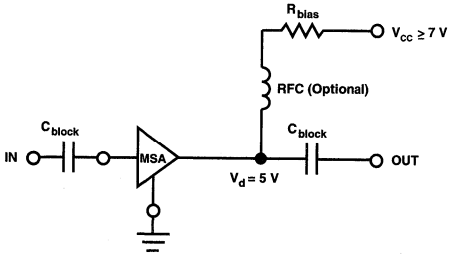
Description

The MSA-0100 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

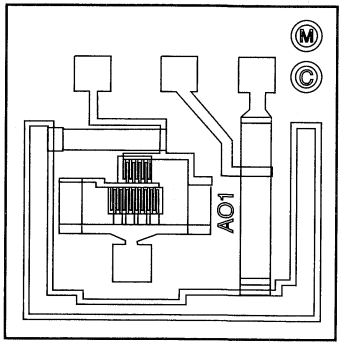
The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1] See APPLICATIONS section, "Chip Use".

Typical Biasing Configuration



Chip Outline[1]



Note:

1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

MSA-0100 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+20 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 45°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 22.2 mW/°C for T_{MS} > 191°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		19.0	
ΔG_P	Gain Flatness	f = 0.1 to 0.7 GHz	dB		±0.6	
$f_{3\ dB}$	3 dB Bandwidth		GHz		1.3	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec		150	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Notes:
1. The recommended operating current range for this device is 13 to 25 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0100-GP4	100

MSA-0100 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 17 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.08	171	19.0	8.91	174	-22.7	.073	2	.10	-11
0.2	.07	161	18.9	8.82	169	-22.5	.075	6	.11	-24
0.3	.07	152	18.8	8.72	163	-22.3	.077	9	.10	-35
0.4	.06	143	18.6	8.56	156	-22.4	.076	12	.11	-44
0.5	.06	133	18.5	8.37	151	-22.1	.079	14	.11	-53
0.6	.05	115	18.2	8.15	146	-21.9	.080	19	.12	-60
0.8	.04	84	17.7	7.68	136	-21.3	.086	22	.12	-75
1.0	.04	3	17.1	7.17	126	-20.3	.096	26	.12	-88
1.5	.08	-39	15.5	5.95	106	-19.3	.109	32	.10	-107
2.0	.12	-76	13.7	4.86	90	-17.9	.127	32	.08	-128
2.5	.15	-102	12.2	4.09	82	-16.9	.142	36	.06	-130
3.0	.19	-122	10.8	3.47	71	-16.4	.151	36	.06	-125
3.5	.25	-137	9.4	2.96	60	-15.6	.165	34	.07	-107
4.0	.27	-147	8.2	2.56	51	-15.2	.173	32	.10	-86
4.5	.28	-157	7.0	2.24	42	-14.8	.182	29	.13	-80
5.0	.28	-171	6.0	2.00	35	-14.4	.190	28	.16	-77

Note:

1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

MSA-0100 Typical Performance, T_A = 25°C

(unless otherwise noted)

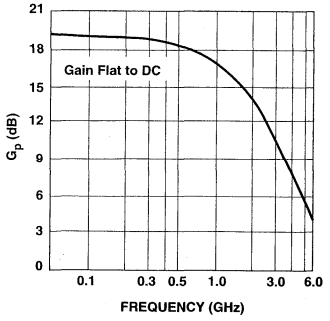


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 17 mA.

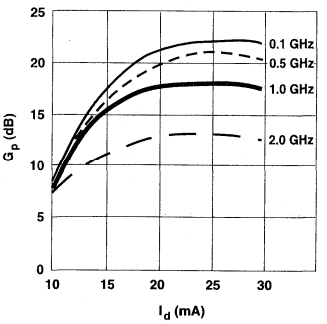


Figure 2. Power Gain vs. Current.

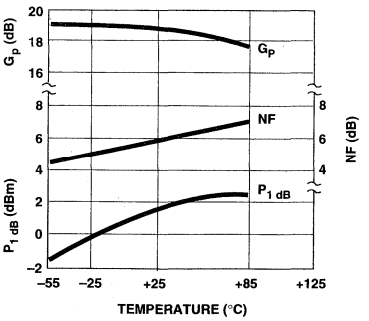


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 0.5 GHz, I_d = 17 mA.

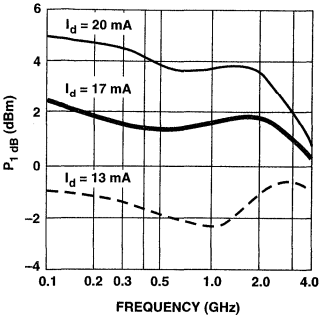


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

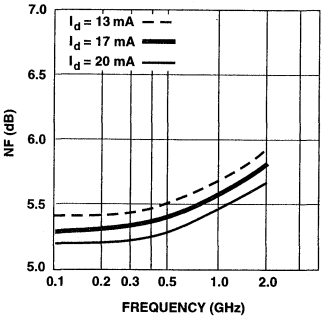
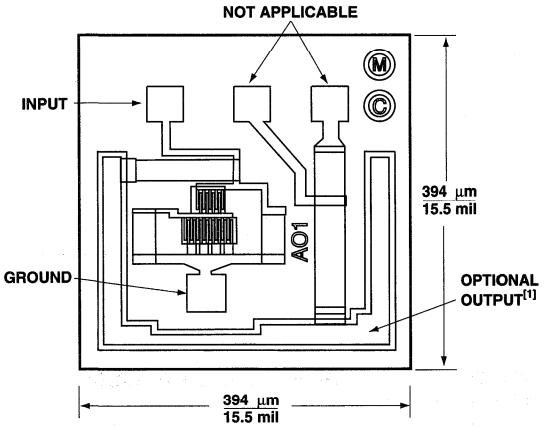


Figure 5. Noise Figure vs. Frequency.

MSA-0100 Chip Dimensions



Chip thickness is 114 µm/4.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side.
Note 1: Output contact is made by die attaching the backside of the die.

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0104

Features

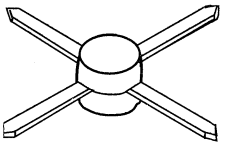
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 0.8 GHz
- **High Gain:** 17.0 dB Typical at 0.5 GHz
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

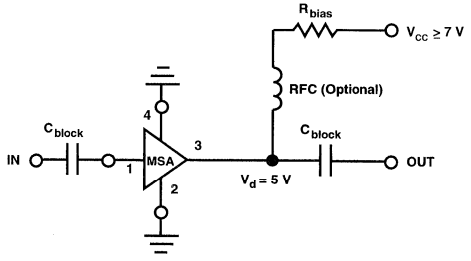
The MSA-0104 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and wide bandwidth IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package



Typical Biasing Configuration



MSA-0104 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 100°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 10 mW/°C for T_C > 130°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

MSA-0104 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz	dB	17.0	18.5 17.0	
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±1.0	
$f_{3\,dB}$	3 dB Bandwidth		GHz		0.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.4:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec		180	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Notes:
1. The recommended operating current range for this device is 13 to 25 mA. Typical performance as a function of current is on the following page.

MSA-0104 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 17 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.06	141	18.4	8.31	170	–22.3	.077	5	.07	–9
0.2	.08	112	18.1	8.07	160	–22.3	.077	9	.07	–15
0.3	.10	94	17.8	7.75	151	–22.0	.079	15	.07	–22
0.4	.12	77	17.4	7.38	142	–21.6	.083	16	.07	–32
0.5	.13	70	16.9	7.01	134	–21.0	.089	19	.07	–37
0.6	.14	56	16.4	6.60	127	–20.7	.092	21	.08	–44
0.8	.16	41	15.4	5.87	114	–19.5	.106	27	.08	–53
1.0	.17	28	14.3	5.21	102	–18.9	.114	29	.08	–61
1.5	.17	5	12.1	4.02	78	–16.6	.148	30	.08	–73
2.0	.13	–12	10.2	3.25	59	–14.9	.179	25	.07	–90
2.5	.08	–20	8.9	2.77	46	–13.6	.209	25	.05	–112
3.0	.02	–37	7.7	2.42	31	–12.7	.232	18	.05	–134
3.5	.05	128	6.7	2.15	15	–11.9	.253	10	.06	–160
4.0	.12	113	5.7	1.92	–1	–11.3	.272	2	.06	–175
4.5	.19	97	4.8	1.73	–15	–10.8	.289	–7	.07	173
5.0	.27	80	3.9	1.56	–30	–10.6	.294	–15	.07	150

A model for this device is available in the DEVICE MODELS section.

MSA-0104 Typical Performance, T_A = 25°C

(unless otherwise noted)

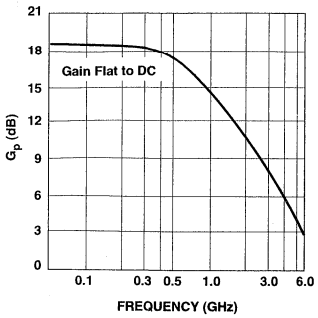


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 17 mA.

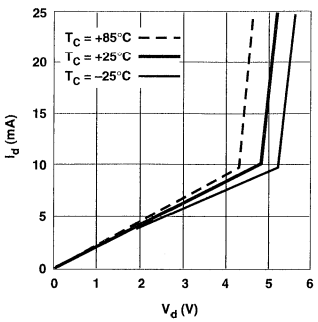


Figure 2. Device Current vs. Voltage.

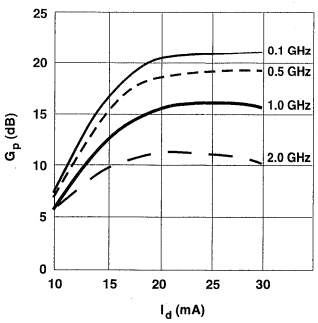


Figure 3. Power Gain vs. Current.

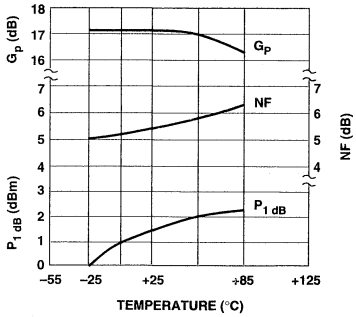


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 17 mA.

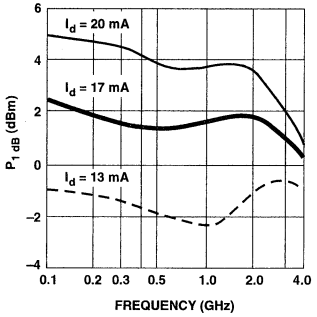


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

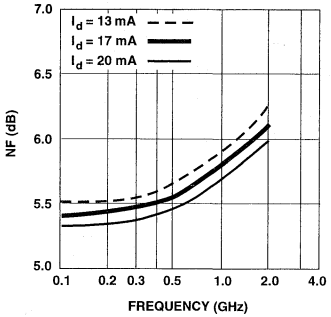
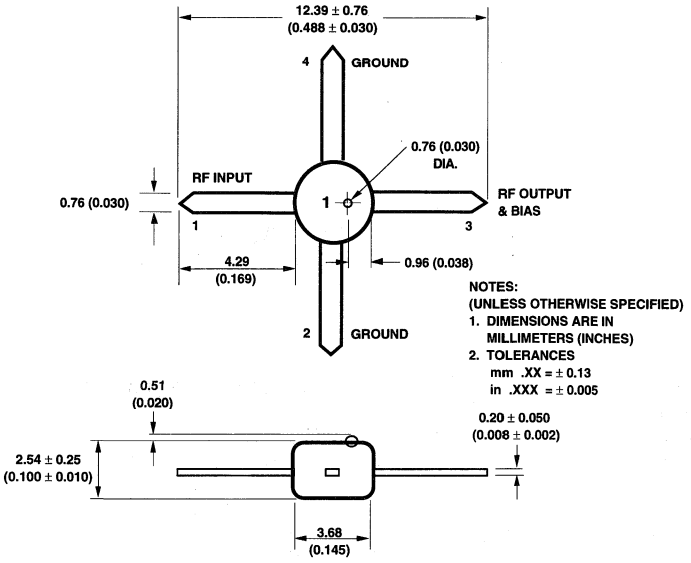


Figure 6. Noise Figure vs. Frequency.

04A Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES).

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifiers

Technical Data

MSA-0135, -0136

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 1.2 GHz
- **High Gain:** 18.5 dB Typical at 0.5 GHz
- **Unconditionally Stable (k>1)**
- **Cost Effective Ceramic Microstrip Package**

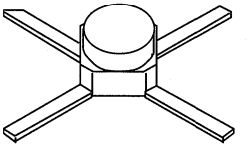
Description

The MSA-0135 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Available in cut lead version (package 36) as MSA-0136.

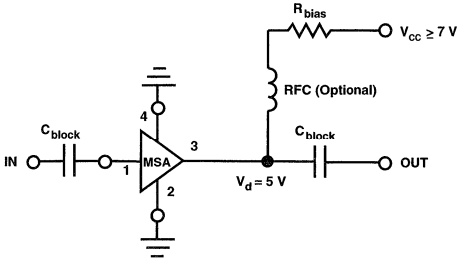
35 micro-X Package[1]



Note:

1. Short leaded 36 package available upon request.

Typical Biasing Configuration



MSA-0135, -0136 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,5]:
θ_{jc} = 150°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.7 mW/°C for T_C > 170°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

MSA-0135, -0136 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	18.0	19.0	
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.2	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec		160	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Notes:
1. The recommended operating current range for this device is 13 to 25 mA. Typical performance as a function of current is on the following page.

MSA-0135, -0136 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 17 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.08	158	19.1	9.01	172	–23.0	.071	3	.07	–2
0.2	.08	134	18.9	8.84	165	–22.4	.076	6	.07	–10
0.3	.08	116	18.7	8.65	157	–22.5	.075	12	.07	–10
0.4	.08	97	18.5	8.40	150	–22.2	.078	13	.07	–15
0.5	.09	83	18.2	8.13	143	–21.7	.082	16	.07	–17
0.6	.09	68	17.9	7.84	136	–21.6	.083	17	.07	–21
0.8	.11	47	17.2	7.25	125	–20.7	.092	22	.07	–30
1.0	.11	27	16.5	6.64	113	–19.9	.101	23	.07	–34
1.5	.11	–18	14.6	5.37	90	–18.3	.122	27	.06	–34
2.0	.09	–62	12.8	4.38	70	–16.8	.144	24	.05	–39
2.5	.08	–114	11.3	3.67	58	–16.1	.157	24	.03	–61
3.0	.12	–158	10.0	3.15	43	–15.0	.177	20	.03	–67
3.5	.18	178	8.7	2.72	28	–14.5	.189	14	.05	–88
4.0	.21	163	7.5	2.37	15	–14.0	.200	9	.10	–92
4.5	.23	145	6.4	2.10	2	–13.4	.213	4	.14	–99
5.0	.27	125	5.5	1.88	–10	–13.2	.220	–2	.15	–102

A model for this device is available in the DEVICE MODELS section.

MSA-0135, -0136 Typical Performance, T_A = 25°C

(unless otherwise noted)

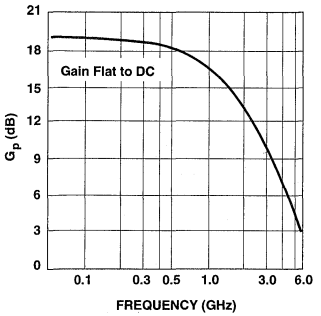


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 17 mA.

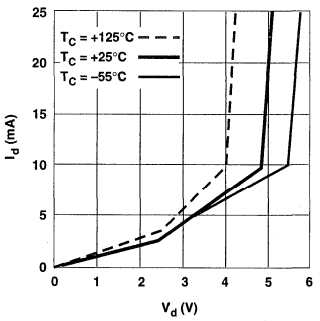


Figure 2. Device Current vs. Voltage.

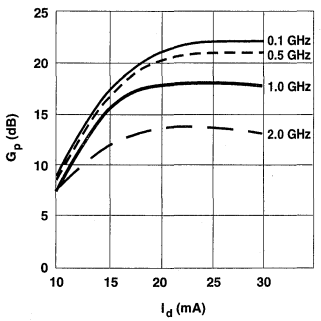


Figure 3. Power Gain vs. Current.

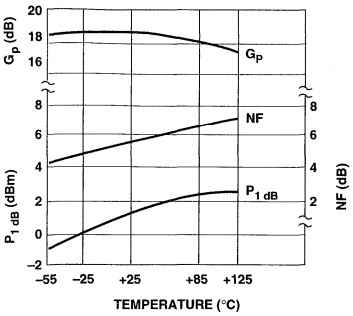


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 17 mA.

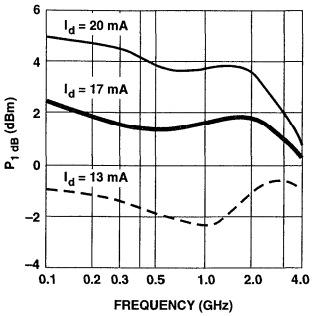


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

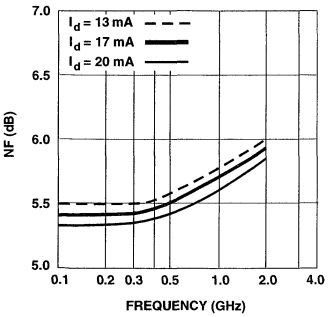
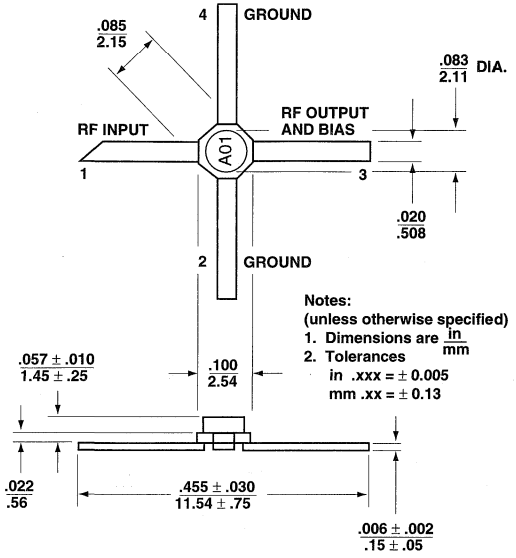


Figure 6. Noise Figure vs. Frequency.

35 micro-X Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0170

Features

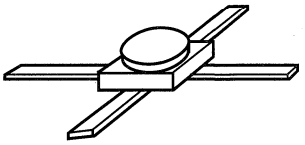
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 1.3 GHz
- **High Gain:** 18.5 dB Typical at 0.5 GHz
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-ceramic Microstrip Package**

Description

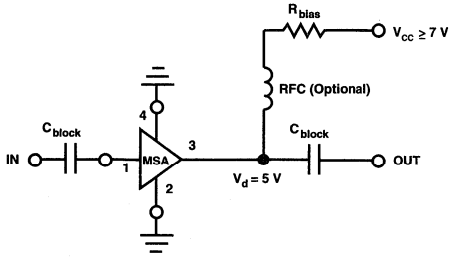
The MSA-0170 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic high reliability package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package



Typical Biasing Configuration



MSA-0170 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 125°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 8 mW/°C for T_C > 175°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

MSA-0170 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	18.0	19.0	
ΔG_P	Gain Flatness	f = 0.1 to 0.7 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.3	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec		150	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Note:
1. The recommended operating current range for this device is 13 to 25 mA. Typical performance as a function of current is on the following page.

MSA-0170 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 17 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.08	171	19.0	8.88	173	–22.7	.073	2	.10	–13
0.2	.07	161	18.9	8.77	167	–22.5	.075	6	.11	–27
0.3	.07	152	18.7	8.64	160	–22.3	.077	8	.10	–39
0.4	.06	143	18.5	8.45	153	–22.4	.076	11	.11	–49
0.5	.05	133	18.3	8.23	147	–22.0	.079	13	.11	–59
0.6	.04	115	18.0	7.98	141	–21.8	.081	17	.12	–67
0.8	.03	79	17.5	7.46	130	–21.2	.087	20	.12	–83
1.0	.04	–14	16.8	6.90	119	–20.2	.098	23	.12	–96
1.5	.08	–52	15.0	5.64	96	–19.0	.112	26	.10	–116
2.0	.12	–87	13.2	4.58	78	–17.7	.131	24	.08	–134
2.5	.15	–112	11.7	3.85	67	–16.7	.147	25	.07	–135
3.0	.19	–132	10.3	3.27	54	–16.1	.156	22	.07	–129
3.5	.24	–148	8.9	2.80	41	–15.4	.170	18	.09	–117
4.0	.26	–159	7.7	2.43	29	–15.0	.177	13	.13	–106
4.5	.27	–170	6.6	2.14	18	–14.7	.184	8	.17	–105
5.0	.27	175	5.7	1.92	8	–14.3	.192	5	.20	–106

A model for this device is available in the DEVICE MODELS section.

MSA-0170 Typical Performance, T_A = 25°C

(unless otherwise noted)

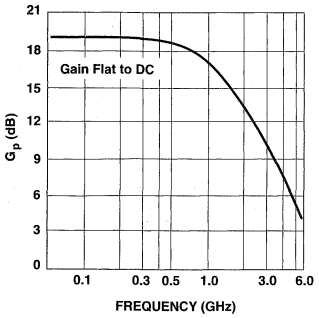


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 17 mA.

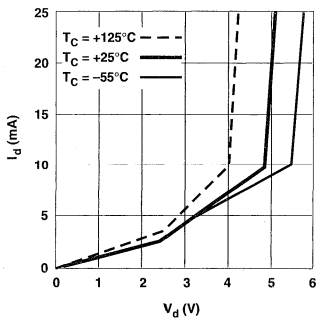


Figure 2. Device Current vs. Voltage.

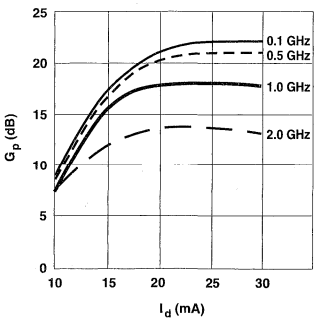


Figure 3. Power Gain vs. Current.

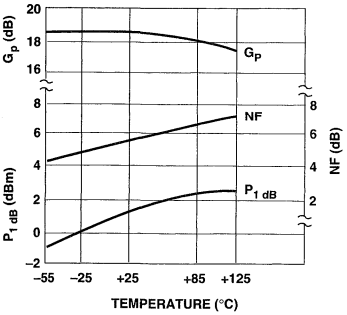


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 17 mA.

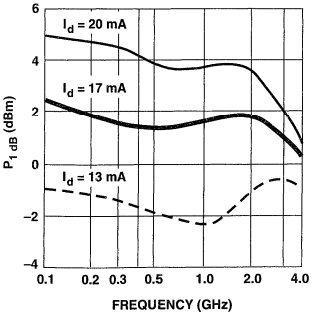


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

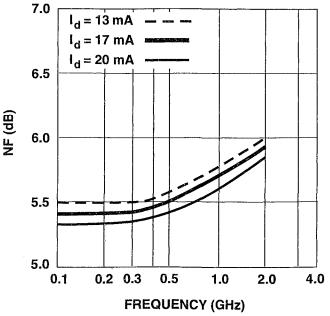
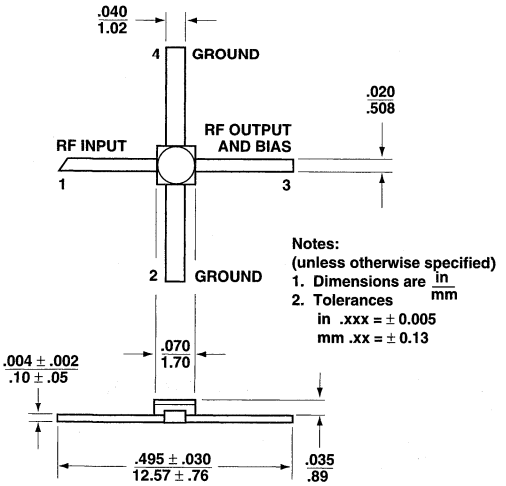


Figure 6. Noise Figure vs. Frequency.

70 mil Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0185

Features

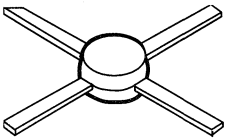
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 1.0 GHz
- **High Gain:** 17.5 dB Typical at 0.5 GHz
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

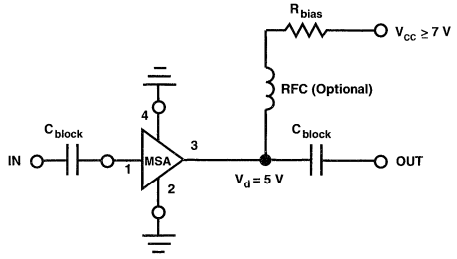
The MSA-0185 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package



Typical Biasing Configuration



MSA-0185 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 105°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 9.5 mW/°C for T_C > 129°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

MSA-0185 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz	dB	 16.0	18.5 17.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±0.6	
$f_{3\ dB}$	3 dB Bandwidth		GHz		1.0	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec		150	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Note:
1. The recommended operating current range for this device is 13 to 25 mA. Typical performance as a function of current is on the following page.

MSA-0185 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 17 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.06	166	18.4	8.36	172	–22.6	.074	3	.07	–17
0.2	.06	149	18.3	8.20	165	–22.0	.079	8	.07	–28
0.3	.06	133	18.1	8.01	158	–22.2	.078	11	.08	–43
0.4	.06	120	17.8	7.78	151	–21.9	.080	14	.09	–56
0.5	.06	105	17.5	7.53	144	–21.4	.085	18	.09	–68
0.6	.06	94	17.2	7.23	138	–21.4	.085	19	.09	–75
0.8	.07	72	16.5	6.66	127	–20.7	.092	24	.10	–89
1.0	.07	49	15.7	6.09	116	–19.7	.104	27	.10	–100
1.5	.07	12	13.8	4.89	94	–18.0	.126	32	.11	–120
2.0	.04	–13	12.0	3.98	76	–16.2	.154	31	.11	–134
2.5	.03	–84	10.6	3.38	65	–15.1	.175	33	.11	–138
3.0	.07	–159	9.2	2.88	52	–14.2	.194	29	.09	–146
3.5	.12	–174	8.0	2.50	38	–13.3	.216	24	.08	–135
4.0	.16	170	6.8	2.19	26	–12.8	.229	19	.08	–120
4.5	.21	150	5.7	1.93	14	–12.3	.242	13	.08	–107
5.0	.25	126	4.7	1.72	3	–12.2	.245	–6	.07	–110

A model for this device is available in the DEVICE MODELS section.

MSA-0185 Typical Performance, T_A = 25°C

(unless otherwise noted)

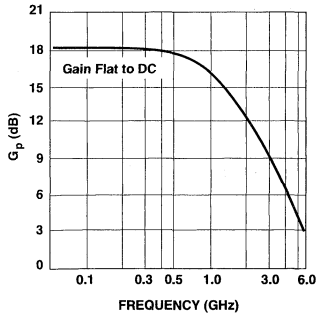


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 17 mA.

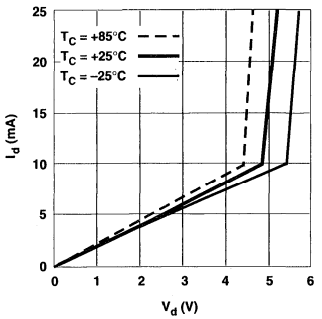


Figure 2. Device Current vs. Voltage.

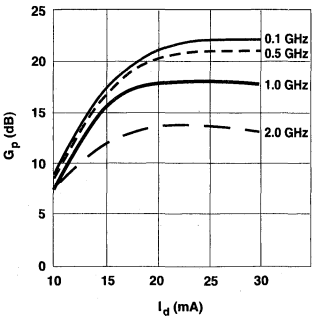


Figure 3. Power Gain vs. Current.

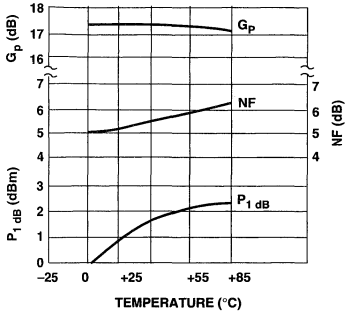


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 17 mA.

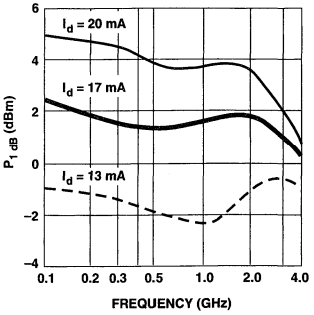


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

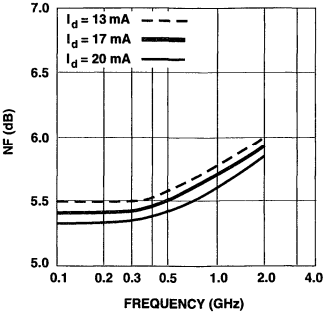
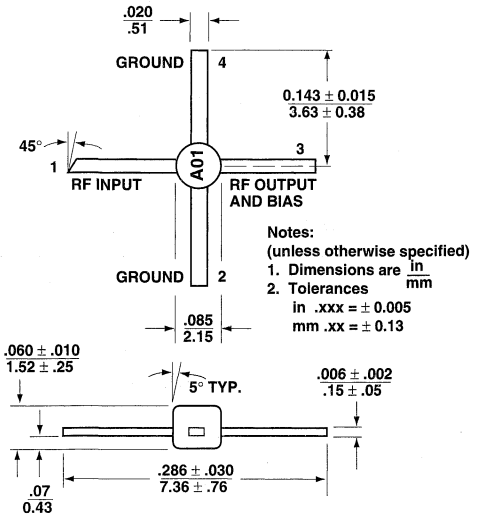


Figure 6. Noise Figure vs. Frequency.

85 Plastic Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0186

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 0.9 GHz
- **High Gain:** 17.5 dB Typical at 0.5 GHz
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

Note:

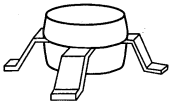
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices".

Description

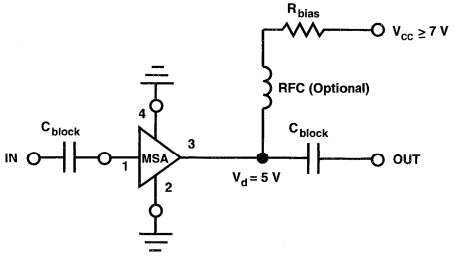
The MSA-0186 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

86 Plastic Package



Typical Biasing Configuration



MSA-0186 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 115°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 8.7 mW/°C for T_C > 127°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz	dB	 15.5	18.5 17.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		0.9	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.2:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec		200	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Note:
1. The recommended operating current range for this device is 13 to 25 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0186-BLK	100	Antistatic Bag
MSA-0186-TR1	1000	7" Reel

For more information refer to PACKAGING section, "Tape and Reel Packaging for Semiconductor Devices."

MSA-0186 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 17 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.05	148	18.5	8.39	171	–23.0	.071	4	.08	–7
0.2	.06	124	18.3	8.22	162	–22.8	.073	9	.08	–14
0.3	.07	103	18.1	8.03	154	–22.6	.074	13	.07	–24
0.4	.08	89	17.7	7.67	146	–22.2	.078	14	.07	–31
0.5	.08	76	17.4	7.42	139	–21.9	.081	17	.06	–39
0.6	.09	66	17.0	7.06	131	–21.4	.085	21	.06	–47
0.8	.10	50	16.2	6.47	119	–20.5	.094	25	.07	–67
1.0	.10	35	15.3	5.83	107	–19.6	.105	29	.07	–89
1.5	.07	12	13.2	4.57	83	–17.7	.131	30	.08	–165
2.0	.02	–12	11.3	3.67	64	–16.1	.157	27	.08	156
2.5	.06	165	9.8	3.09	50	–14.8	.182	24	.08	134
3.0	.14	150	8.3	2.60	34	–13.9	.202	19	.09	124
3.5	.23	137	7.0	2.24	20	–13.4	.213	12	.09	117
4.0	.31	125	5.7	1.93	6	–13.0	.223	5	.09	114
5.0	.45	105	3.3	1.46	–17	–12.7	.231	–5	.09	132

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

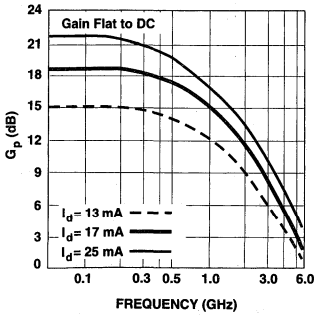


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 17 mA.

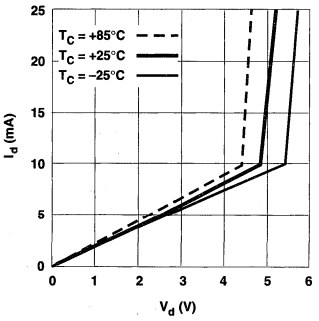


Figure 2. Device Current vs. Voltage.

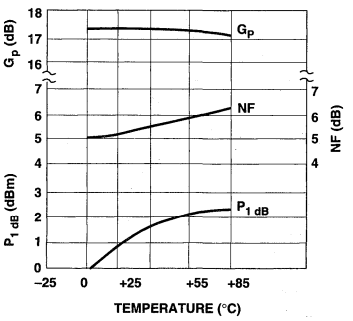


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 17 mA.

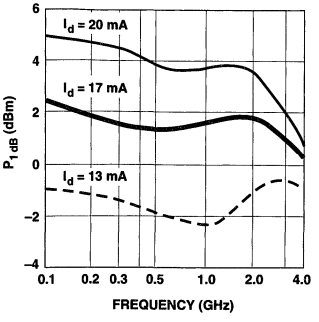


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

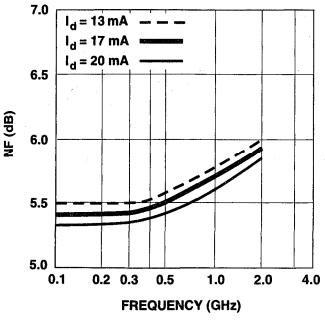
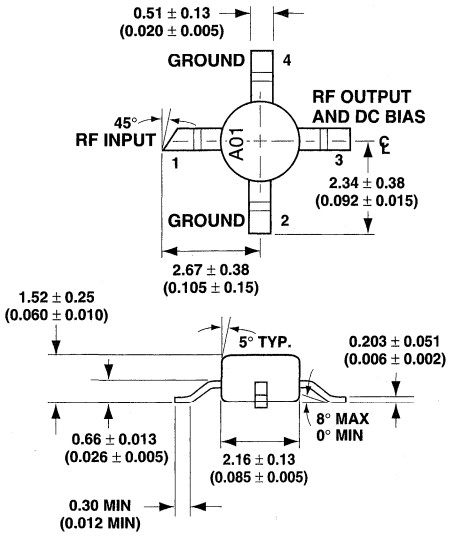


Figure 5. Noise Figure vs. Frequency.

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0200

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.8 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**

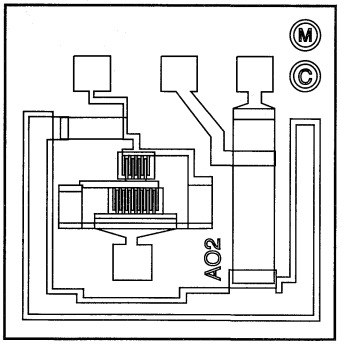
Description

The MSA-0200 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1] See APPLICATIONS section, "Chip Use".

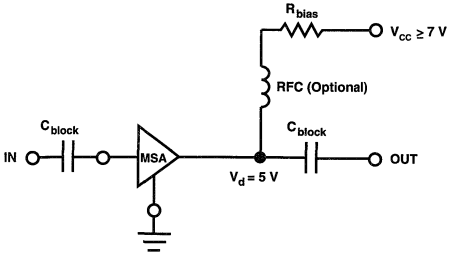
Chip Outline[1]



Note:

1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 35°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 28.6 mW/°C for T_{MS} > 189°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

MSA-0200 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.8 GHz	dB		±0.6	
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.4:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 18 to 40 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0200-GP4	100

MSA-0200 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 25 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.11	179	12.6	4.27	177	–18.4	.120	1	.11	–7
0.2	.11	174	12.6	4.26	172	–18.6	.117	4	.11	–12
0.4	.10	170	12.5	4.24	165	–18.4	.120	5	.12	–25
0.6	.09	166	12.5	4.22	158	–18.2	.123	7	.13	–38
0.8	.08	162	12.4	4.17	152	–18.2	.123	10	.13	–47
1.0	.06	161	12.3	4.13	144	–18.0	.126	13	.14	–55
1.5	.02	–170	12.0	3.99	126	–17.3	.137	17	.15	–72
2.0	.05	–105	11.5	3.74	109	–16.4	.152	20	.15	–89
2.5	.10	–103	10.8	3.46	97	–15.8	.163	25	.13	–91
3.0	.17	–124	9.8	3.10	83	–15.3	.172	26	.11	–100
3.5	.22	–137	8.7	2.71	68	–14.7	.184	22	.13	–94
4.0	.26	–144	7.4	2.35	55	–14.3	.192	22	.16	–85
5.0	.29	–165	5.1	1.80	35	–13.8	.203	17	.22	–76
6.0	.33	–162	3.3	1.46	20	–13.5	.211	14	.23	–82

Note:

1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

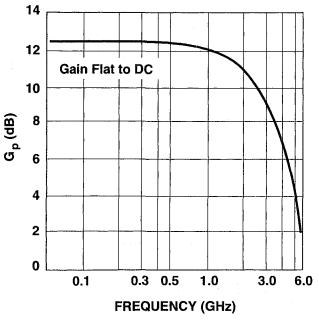


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 25 mA.

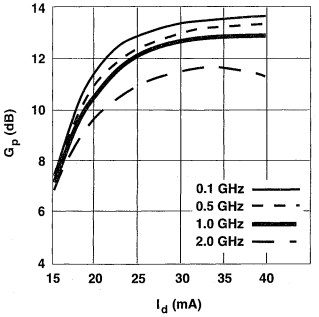


Figure 2. Power Gain vs. Current.

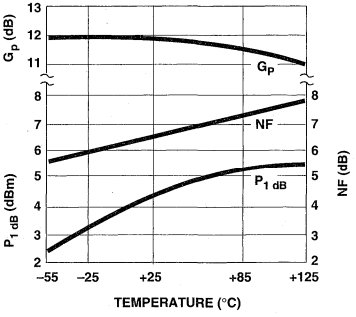


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 1.0 GHz, I_d = 25 mA.

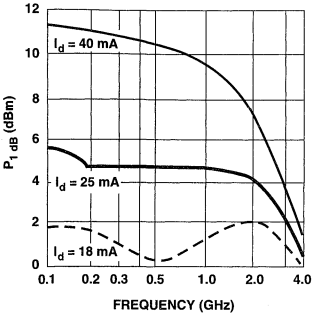


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

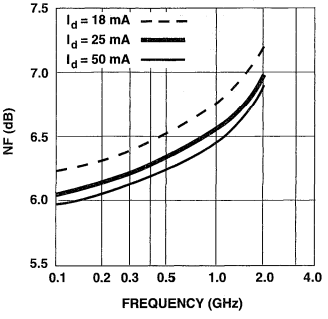
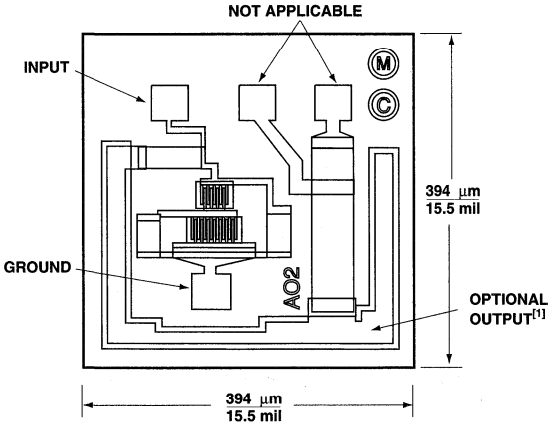


Figure 5. Noise Figure vs. Frequency.

MSA-0200 Chip Dimensions



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils. Chip thickness is 114 µm/4.5 mil. Bond pads are 41 µm/1.6 mil typical on each side.
Note 1: Output contact is made by die attaching the backside of the die.

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0204

Features

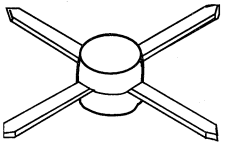
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 1.8 GHz
- **11.0 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

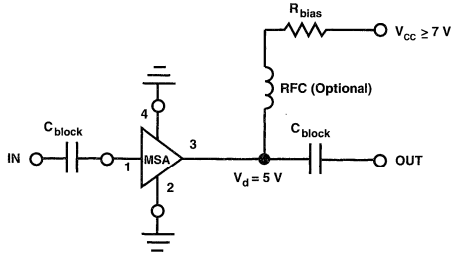
The MSA-0204 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package



Typical Biasing Configuration



MSA-0204 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 90°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 11.1 mW/°C for T_C > 121°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz f = 1.0 GHz	dB	 10.0	12.5 12.0 11.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.4 GHz	dB		±1.0	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec		150	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 18 to 40 mA. Typical performance as a function of current is on the following page.

MSA-0204 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 25 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.12	170	12.5	4.20	174	–18.5	.119	2	.12	–7
0.2	.12	160	12.4	4.16	168	–18.5	.119	4	.12	–14
0.4	.11	140	12.2	4.05	156	–18.1	.124	6	.12	–29
0.6	.11	121	11.9	3.93	144	–17.9	.127	8	.12	–42
0.8	.10	104	11.6	3.78	134	–17.6	.132	12	.12	–52
1.0	.10	84	11.2	3.62	123	–17.0	.142	14	.13	–61
1.5	.09	42	10.2	3.22	99	–16.1	.157	16	.12	–79
2.0	.07	16	9.1	2.86	77	–14.8	.181	15	.11	–96
2.5	.05	17	8.2	2.57	63	–13.9	.202	16	.09	–115
3.0	.02	96	7.3	2.32	46	–13.2	.220	13	.08	–141
3.5	.08	112	6.5	2.12	29	–12.4	.239	7	.09	–167
4.0	.14	100	5.7	1.93	12	–11.8	.258	0	.11	171
5.0	.35	72	4.0	1.58	–22	–11.2	.276	–15	.17	120
6.0	.59	51	1.6	1.20	–54	–11.3	.272	–33	.32	80

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

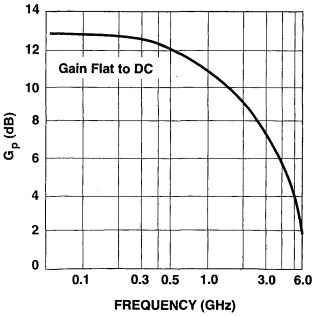


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 25 mA.

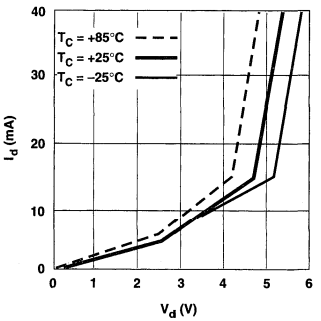


Figure 2. Device Current vs. Voltage.

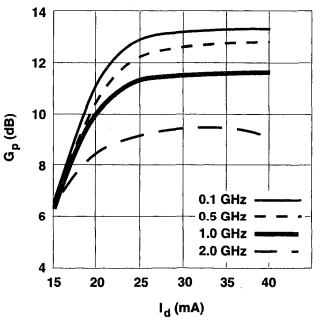


Figure 3. Power Gain vs. Current.

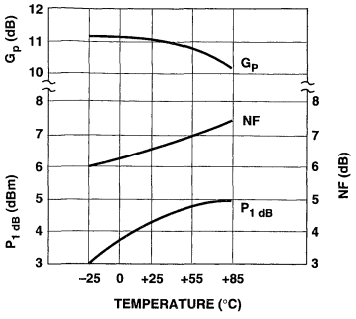


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 25 mA.

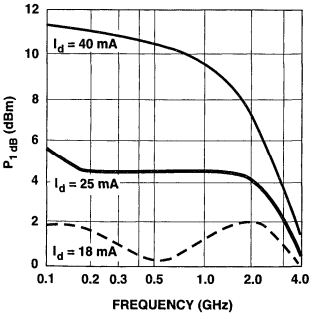


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

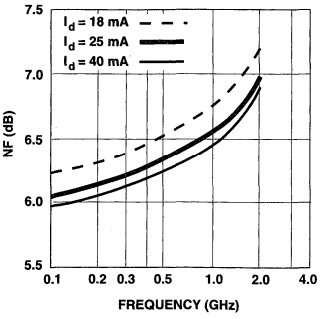
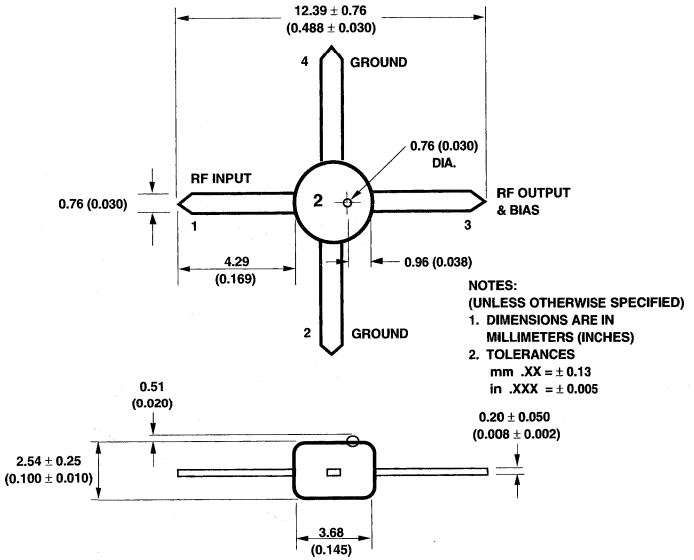


Figure 6. Noise Figure vs. Frequency.

04A Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES).

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifiers

Technical Data

MSA-0235, -0236

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.7 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Cost Effective Ceramic Microstrip Package**

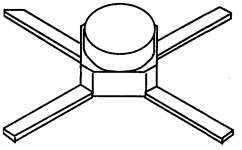
Description

The MSA-0235 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Available in cut lead version (package 36) as MSA-0236.

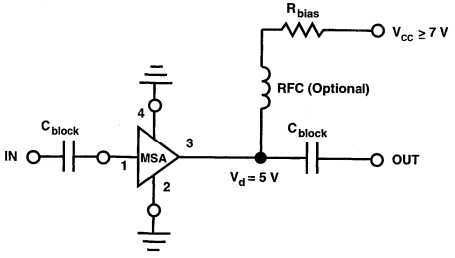
35 micro-X Package[1]



Note:

1. Short leaded 36 package available upon request.

Typical Biasing Configuration



MSA-0235, -0236 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65 to 200°C

Thermal Resistance[2,5]:
θ_{jc} = 145°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.9 mW/°C for T_C > 153°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.7	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.2:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 18 to 40 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0235	10	Strip
MSA-0236-BLK	100	Antistatic Bag
MSA-0236-TR1	1000	7" Reel

For more information refer to PACKAGING section, "Tape and Reel Packaging for Semiconductor Devices."

MSA-0235, -0236 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 25 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.08	170	12.6	4.25	176	-18.6	.118	2	.16	-6
0.2	.08	163	12.5	4.23	171	-18.5	.119	2	.15	-10
0.4	.08	147	12.5	4.19	161	-18.4	.120	4	.15	-21
0.6	.08	130	12.4	4.14	152	-18.3	.121	4	.15	-30
0.8	.07	112	12.2	4.09	143	-18.1	.125	7	.15	-39
1.0	.07	91	12.1	4.02	134	-18.0	.126	10	.15	-46
1.5	.06	47	11.6	3.80	112	-17.3	.137	11	.13	-66
2.0	.03	-1	11.0	3.53	91	-16.3	.153	10	.11	-89
2.5	.03	-115	10.2	3.24	75	-15.4	.169	12	.09	-111
3.0	.09	-157	9.3	2.92	57	-15.1	.176	8	.08	-127
3.5	.16	-175	8.3	2.60	39	-14.4	.190	3	.09	-129
4.0	.20	173	7.2	2.29	23	-14.1	.198	-2	.11	-118
5.0	.27	136	5.2	1.81	-6	-13.5	.211	-11	.15	-117
6.0	.41	94	3.2	1.44	-33	-13.5	.212	-24	.11	-148

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

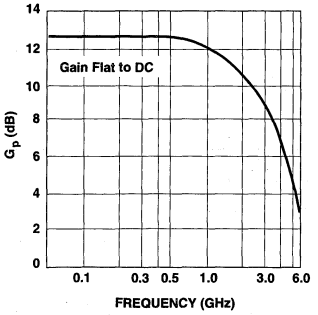


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 25 mA.

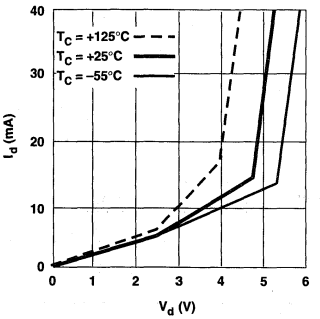


Figure 2. Device Current vs. Voltage.

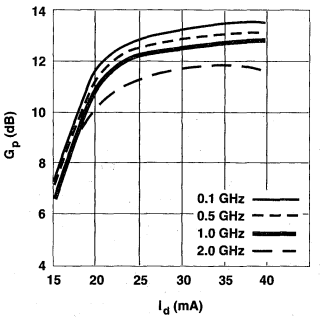


Figure 3. Power Gain vs. Current.

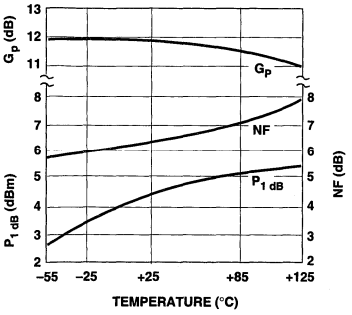


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 1.0 GHz, I_d = 25 mA.

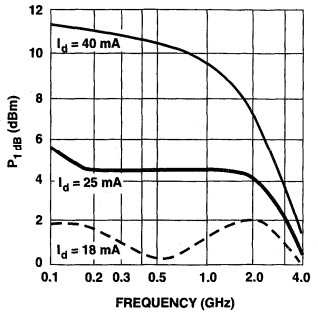


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

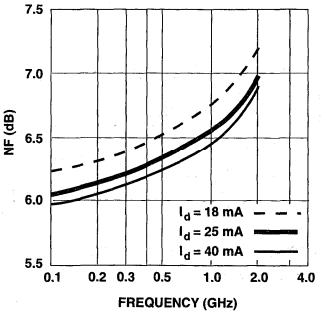
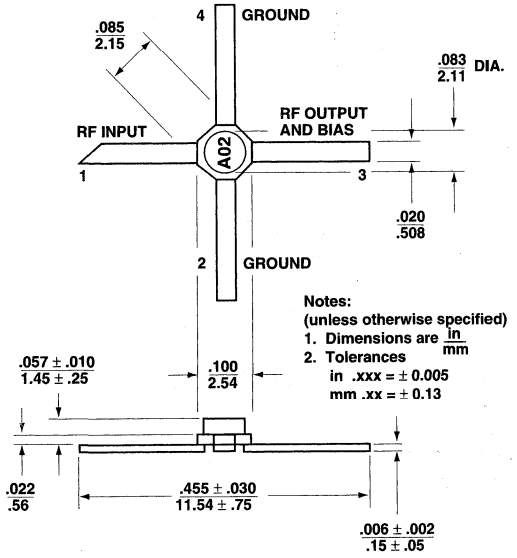


Figure 6. Noise Figure vs. Frequency.

35 micro-X Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0270

Features

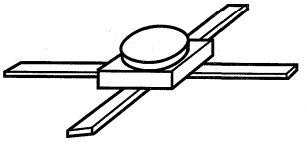
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.8 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-ceramic Microstrip Package**

Description

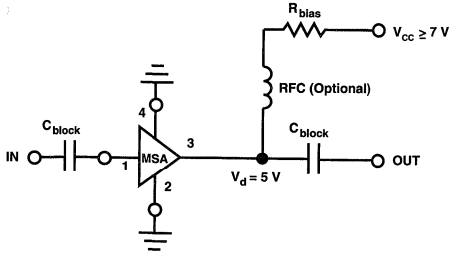
The MSA-0270 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package



Typical Biasing Configuration



MSA-0270 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 120°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 8.3 mW/°C for T_C > 161°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.8 GHz	dB		±0.6	±1.0
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.4:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 18 to 40 mA. Typical performance as a function of current is on the following page.

MSA-0270 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 25 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.11	179	12.6	4.26	176	–18.4	.120	1	.12	–8
0.2	.11	174	12.6	4.24	171	–18.6	.117	3	.12	–15
0.4	.10	169	12.5	4.21	162	–18.4	.120	4	.13	–30
0.6	.09	165	12.4	4.17	154	–18.2	.123	5	.14	–44
0.8	.08	161	12.3	4.11	146	–18.2	.123	7	.14	–55
1.0	.06	161	12.2	4.05	137	–18.0	.126	9	.15	–64
1.5	.02	–150	11.7	3.85	116	–17.2	.138	11	.16	–84
2.0	.06	–110	11.1	3.57	96	–16.3	.153	11	.16	–102
2.5	.11	–112	10.3	3.27	82	–15.7	.165	14	.14	–106
3.0	.17	–134	9.3	2.92	65	–15.2	.174	12	.13	–114
3.5	.22	–147	8.2	2.56	48	–14.7	.185	6	.15	–111
4.0	.26	156	7.0	2.23	33	–14.3	.192	3	.19	–107
5.0	.28	179	4.7	1.72	8	–14.0	.199	–6	.27	–107
6.0	.30	143	3.0	1.41	–13	–13.8	.204	–14	.29	–119

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

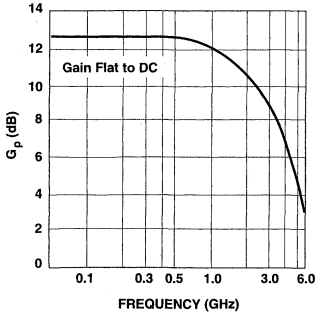


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 25 mA.

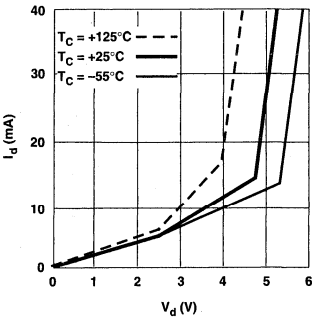


Figure 2. Device Current vs. Voltage.

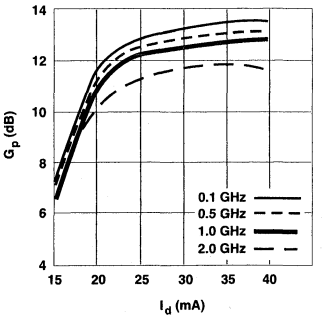


Figure 3. Power Gain vs. Current.

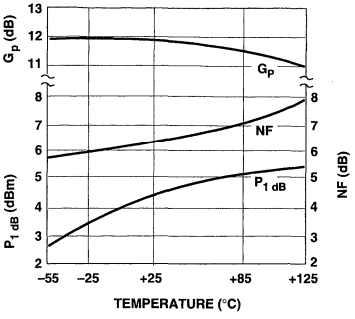


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 1.0 GHz, I_d = 25 mA.

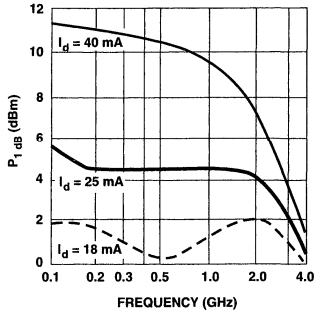


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

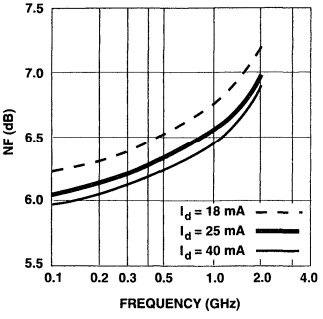
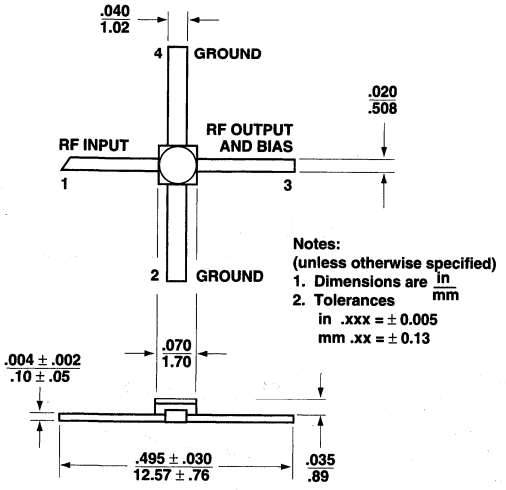


Figure 6. Noise Figure vs. Frequency.

70 mil Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0285

Features

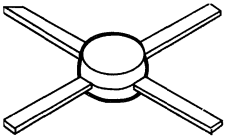
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.6 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

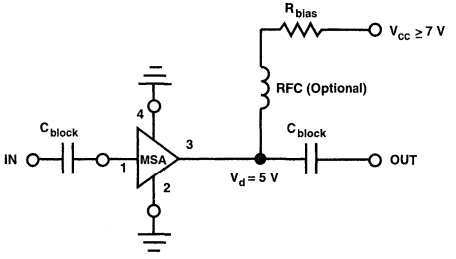
The MSA-0285 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package



Typical Biasing Configuration



MSA-0285 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 95°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 10.5 mW/°C for T_C > 119°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.0	12.5 12.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.6	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 18 to 40 mA. Typical performance as a function of current is on the following page.

MSA-0285 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 25 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.10	174	12.6	4.25	175	-18.6	.118	2	.14	-7
0.2	.10	168	12.5	4.22	171	-18.5	.119	3	.13	-12
0.4	.10	157	12.4	4.17	161	-18.3	.122	6	.14	-26
0.6	.09	143	12.3	4.10	153	-18.3	.121	7	.14	-38
0.8	.08	132	12.1	4.03	144	-18.0	.126	11	.14	-48
1.0	.08	122	11.9	3.95	135	-17.5	.133	12	.14	-60
1.5	.04	95	11.4	3.70	115	-17.0	.142	16	.13	-85
2.0	.02	117	10.6	3.40	95	-16.0	.158	17	.12	-110
2.5	.05	-173	9.9	3.11	82	-15.0	.177	20	.12	-128
3.0	.12	-175	8.9	2.78	65	-14.7	.185	19	.11	-148
3.5	.16	179	7.9	2.49	49	-14.0	.199	14	.10	-145
4.0	.21	169	6.9	2.22	35	-13.7	.207	11	.10	-134
5.0	.28	139	5.0	1.77	9	-13.0	.224	4	.12	-118
6.0	.41	100	3.0	1.42	-16	-12.9	.226	-5	.09	-154

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

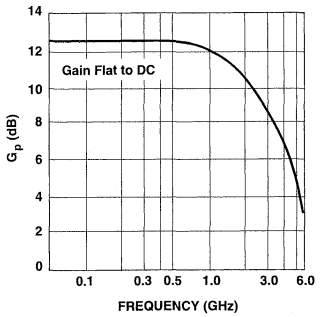


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 25 mA.

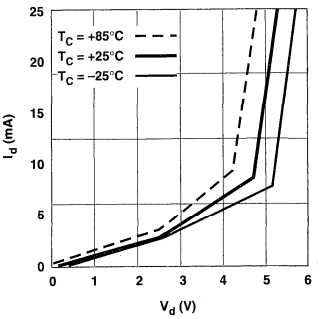


Figure 2. Device Current vs. Voltage.

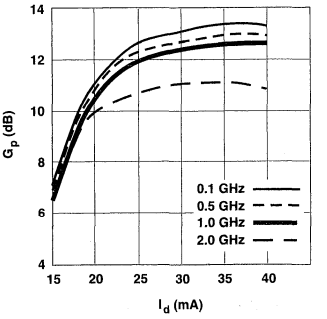


Figure 3. Power Gain vs. Current.

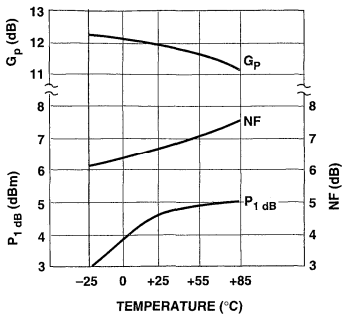


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 25 mA.

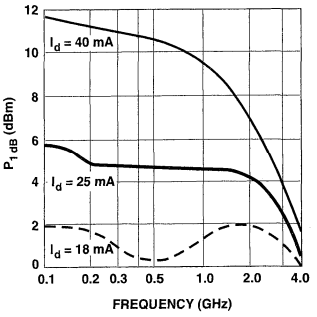


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

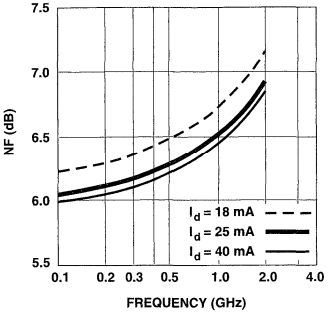
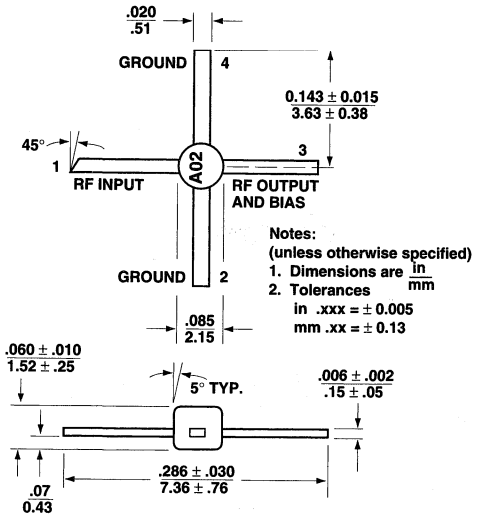


Figure 6. Noise Figure vs. Frequency.

85 Plastic Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0286

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.5 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

Note:

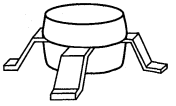
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Description

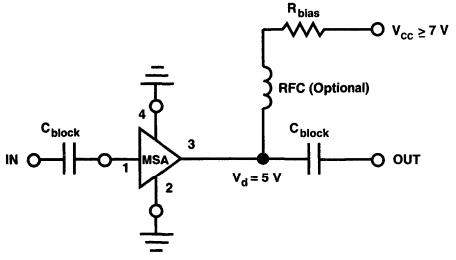
The MSA-0286 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

86 Plastic Package



Typical Biasing Configuration



MSA-0286 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 105°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 9.5 mW/°C for T_C > 116°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.0	12.5 12.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec		140	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 18 to 40 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0286-TR1	1000	7" Reel
MSA-0286-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0286 Typical Scattering Parameters (Z_0 = 50 Ω, T_A = 25°C, I_d = 25 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.10	171	12.5	4.22	175	–18.5	.119	1	.16	–5
0.2	.10	161	12.5	4.20	170	–18.3	.121	3	.16	–11
0.4	.10	144	12.4	4.16	159	–18.2	.122	6	.15	–24
0.6	.09	129	12.2	4.09	149	–18.0	.126	6	.15	–36
0.8	.08	119	12.1	4.01	139	–18.0	.127	9	.14	–48
1.0	.08	108	11.9	3.91	129	–17.4	.135	8	.14	–62
1.5	.06	111	11.3	3.67	106	–16.5	.149	12	.11	–99
2.0	.08	141	10.5	3.35	84	–15.7	.164	11	.11	–141
2.5	.14	150	9.6	3.01	67	–14.8	.182	9	.12	–176
3.0	.21	142	8.6	2.68	48	–14.3	.194	5	.13	155
3.5	.29	132	7.5	2.37	30	–14.0	.200	1	.14	140
4.0	.36	121	6.4	2.09	15	–13.5	.211	–3	.16	134
5.0	.50	101	4.1	1.61	–12	–13.3	.216	–12	.20	132

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

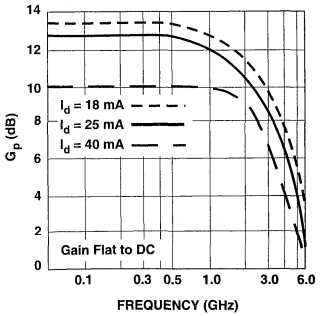


Figure 1. Typical Power Gain vs. Frequency.

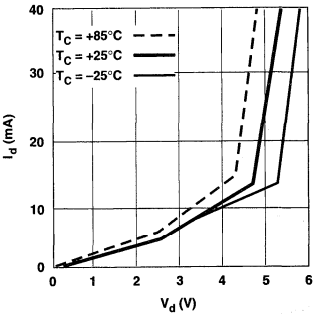


Figure 2. Device Current vs. Voltage.

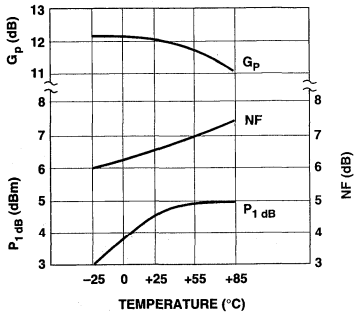


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 25 mA.

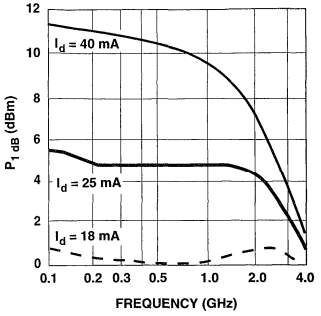


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

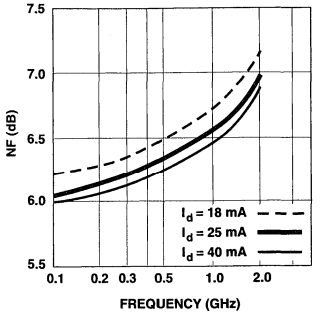
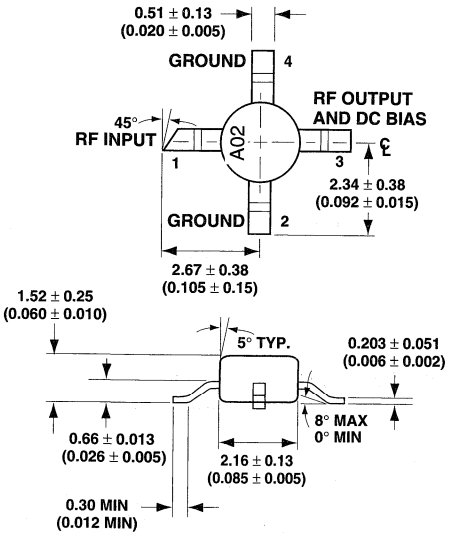


Figure 5. Noise Figure vs. Frequency.

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0300

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.8 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **10.0 dBm Typical $P_{1\,dB}$ at 1.0 GHz**

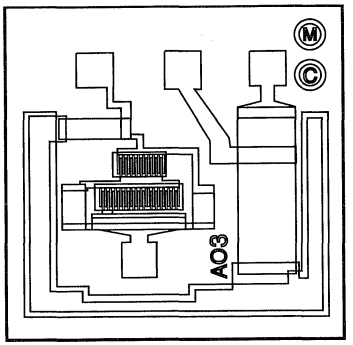
Description

The MSA-0300 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1] See APPLICATIONS section, "Chip Use".

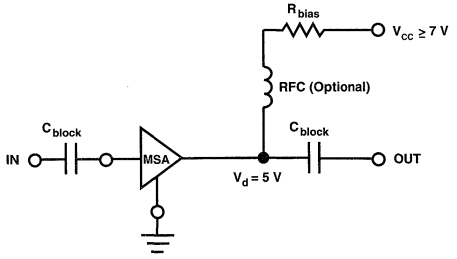
Chip Outline[1]



Note:

1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



MSA-0300 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	425 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 45°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 22.2 mW/°C for T_C > 181°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.8 GHz	dB		±0.6	
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.8:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.8:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 20 to 50 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0300-GP4	100

MSA-0300 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.1	.13	–179	12.6	4.28	177	–18.6	.118	2	.09	–13	1.21
0.2	.13	–179	12.6	4.27	172	–18.3	.121	3	.10	–27	1.19
0.4	.12	–179	12.5	4.24	165	–18.3	.121	5	.12	–48	1.19
0.6	.11	–177	12.5	4.22	158	–18.2	.123	8	.14	–65	1.18
0.8	.11	–172	12.4	4.19	152	–17.8	.129	11	.17	–76	1.15
1.0	.10	–166	12.4	4.15	144	–17.7	.130	1	.20	–85	1.14
1.5	.11	–145	12.0	4.00	126	–17.1	.139	1	.24	–104	1.09
2.0	.16	–140	11.5	3.76	109	–16.2	.154	2	.27	–122	1.03
2.5	.23	–141	10.8	3.47	97	–15.6	.166	2	.28	–133	0.99
3.0	.29	–149	9.8	3.10	82	–15.2	.173	24	.28	–145	0.99
3.5	.35	–157	8.7	2.72	67	–14.5	.188	21	.27	–148	0.97
4.0	.38	–164	7.6	2.40	55	–14.3	.193	22	.25	–146	1.00
5.0	.41	179	5.5	1.88	35	–13.7	.206	17	.21	–134	1.14
6.0	.43	153	3.6	1.51	18	–13.3	.217	14	.21	–137	1.27

Note:

1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

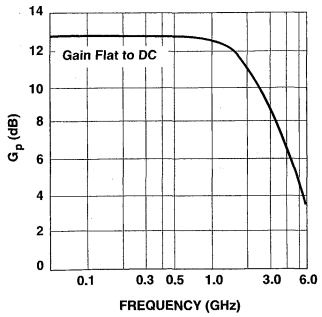


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 35 mA.

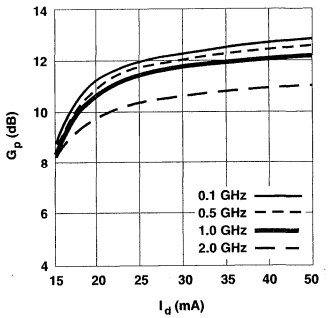


Figure 2. Power Gain vs. Current.

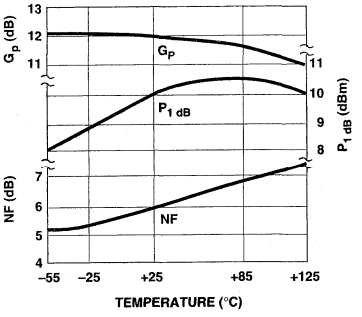


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 1.0 GHz, I_d = 35 mA.

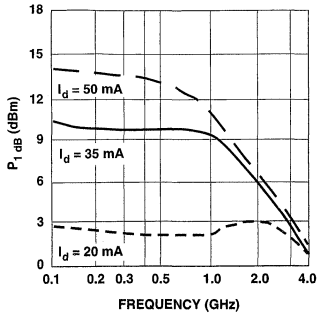


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

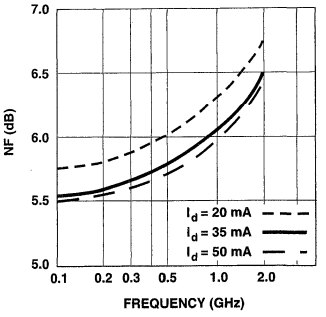
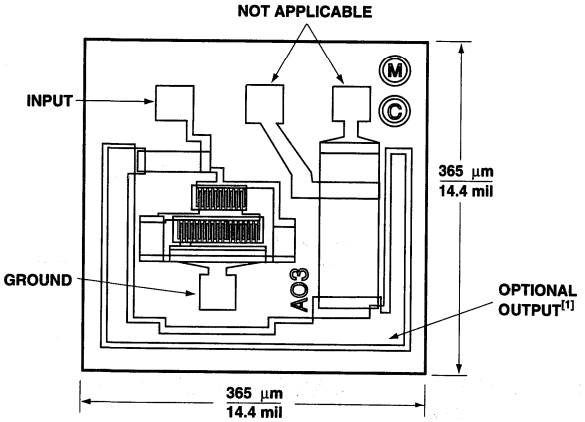


Figure 5. Noise Figure vs. Frequency.

MSA-0300 Chip Dimensions



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils. Chip thickness is 5.5 ± 0.5 mils. Bond Pads are 41 µm/1.6 mil typical on each side.
Note 1: Output contact is made by die attaching the backside of the die.

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0304

Features

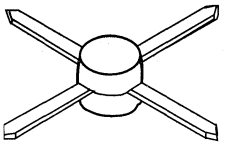
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 1.6 GHz
- **11.0 dB Typical Gain at 1.0 GHz**
- **10.0 dBm Typical $P_{1\,dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

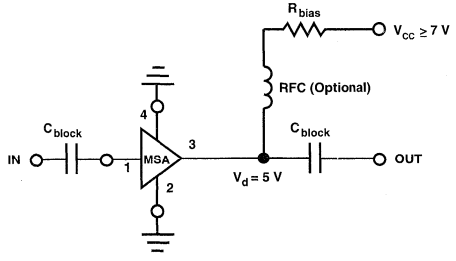
The MSA-0304 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package



Typical Biasing Configuration



MSA-0304 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	70 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
$\theta_{jc} = 100°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 10 mW/°C for $T_C > 110°C$.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], $T_A = 25°C$

Symbol	Parameters and Test Conditions: $I_d = 35$ mA, $Z_O = 50\ \Omega$		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz f = 1.0 GHz	dB	 10.0	12.5 12.0 11.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.3 GHz	dB		±1.0	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.6	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.6:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec		150	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 20 to 50 mA. Typical performance as a function of current is on the following page.

MSA-0304 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.10	173	12.5	4.24	173	-18.5	.120	3	.12	-13
0.2	.10	162	12.5	4.21	167	-18.2	.123	4	.12	-24
0.4	.09	142	12.2	4.08	153	-18.0	.125	7	.13	-46
0.6	.08	127	11.9	3.93	141	-17.8	.128	10	.15	-64
0.8	.07	110	11.5	3.76	130	-17.3	.136	14	.16	-78
1.0	.06	92	11.1	3.58	118	-16.8	.144	16	.17	-91
1.5	.03	58	10.0	3.15	93	-15.5	.169	19	.19	-117
2.0	.03	175	8.8	2.76	71	-14.1	.197	18	.20	-139
2.5	.05	163	7.8	2.46	55	-13.2	.218	18	.21	-158
3.0	.12	148	6.8	2.20	38	-12.2	.246	15	.22	-174
3.5	.19	129	5.9	1.98	20	-11.2	.275	7	.24	171
4.0	.26	110	5.0	1.77	3	-10.6	.296	1	.26	158
5.0	.44	77	3.0	1.41	-28	-9.9	.319	-15	.29	128
6.0	.63	52	0.4	1.05	-56	-10.2	.310	-31	.37	94

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

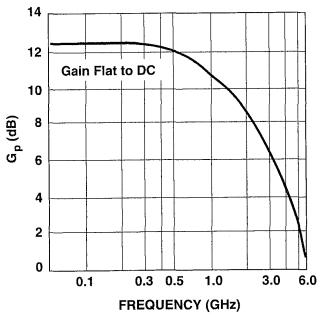


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 35 mA.

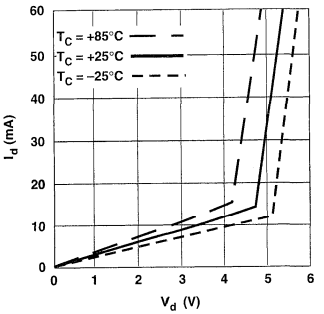


Figure 2. Device Current vs. Voltage.

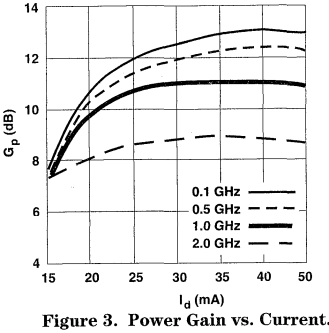


Figure 3. Power Gain vs. Current.

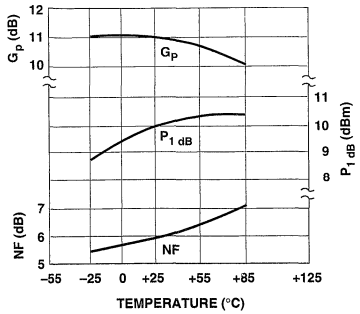


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 35 mA.

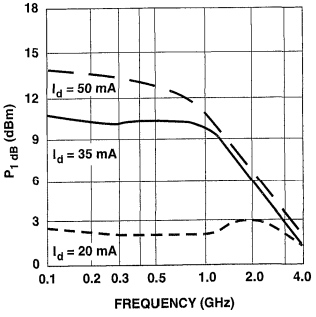


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

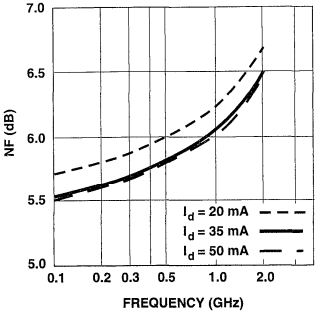
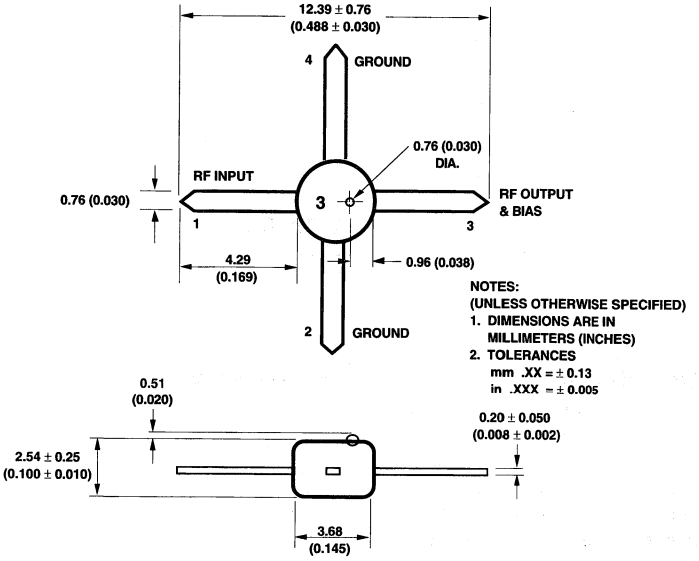


Figure 6. Noise Figure vs. Frequency.

04A Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES).

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0311

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.3 GHz
- **11.0 dB Typical Gain at 1.0 GHz**
- **9.0 dBm Typical $P_{1\ dB}$ at --1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

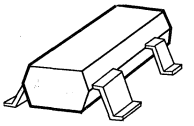
Note:
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices".

Description

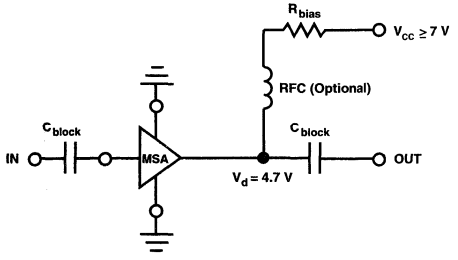
The MSA-0311 is a low cost silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in the surface mount plastic SOT-143 package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

SOT-143 Package



Typical Biasing Configuration



MSA-0311 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	240 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 500°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 2.0 mW/°C for T_C > 30°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 9.0	11.5 11.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.3	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.7:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		9.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		22.0	
t_D	Group Delay	f = 1.0 GHz	psec		140	
V_d	Device Voltage	T_C = 25°C	V	3.8	4.7	5.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 20 to 40 mA. Typical gain performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0311-TR1	3000	7" Reel
MSA-0311-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0311 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.06	25	11.7	3.84	175	–17.9	.127	2	.24	–7
0.2	.07	31	11.7	3.83	170	–17.9	.128	3	.23	–13
0.4	.07	38	11.6	3.78	159	–17.8	.129	6	.24	–28
0.6	.07	30	11.4	3.72	149	–17.6	.132	18	.24	–40
0.8	.08	21	11.2	3.65	140	–17.3	.136	11	.24	–53
1.0	.08	10	11.0	3.56	130	–17.0	.141	13	.24	–65
1.5	.09	–32	10.4	3.31	106	–15.9	.160	17	.24	–91
2.0	.09	–105	9.5	2.99	84	–14.9	.179	16	.23	–115
2.5	.13	–151	8.5	2.66	70	–14.1	.197	19	.23	–133
3.0	.19	–176	7.4	2.35	51	–13.5	.212	15	.22	–145
3.5	.24	166	6.2	2.04	35	–13.0	.224	11	.23	–151
4.0	.27	152	5.1	1.80	20	–12.7	.232	6	.24	–151
5.0	.36	114	2.9	1.39	–6	–12.1	.250	–1	.25	–152
6.0	.50	88	0.8	1.10	–28	–11.8	.258	–8	.25	–166

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

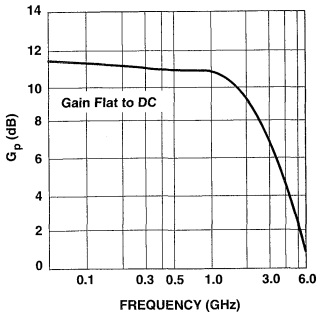


Figure 1. Typical Power Gain vs. Frequency, I_d = 35 mA.

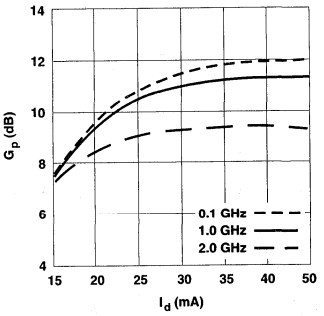


Figure 2. Power Gain vs. Current.

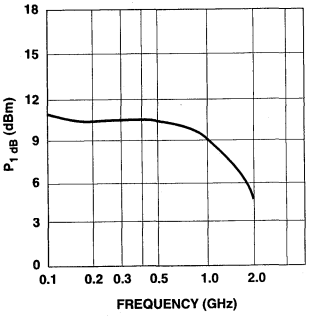


Figure 3. Output Power at 1 dB Gain Compression vs. Frequency, I_d = 35 mA.

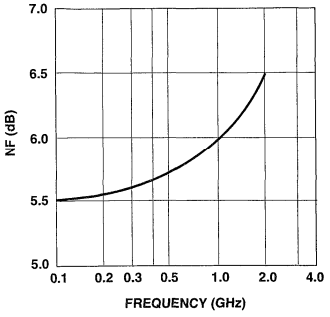
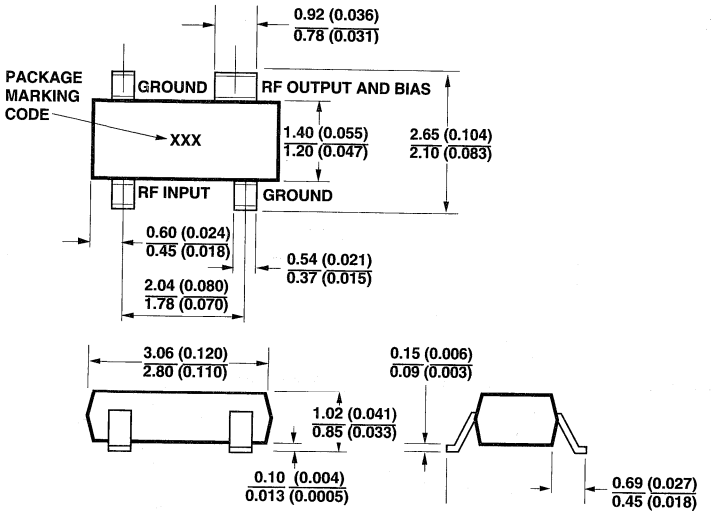


Figure 4. Noise Figure vs. Frequency, I_d = 35 mA.

SOT-143 Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Package marking code is "A03"

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifiers

Technical Data

MSA-0335, -0336

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.7 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **10.0 dBm Typical P_{1dB} at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Cost Effective Ceramic Microstrip Package**

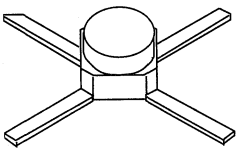
Description

The MSA-0335 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

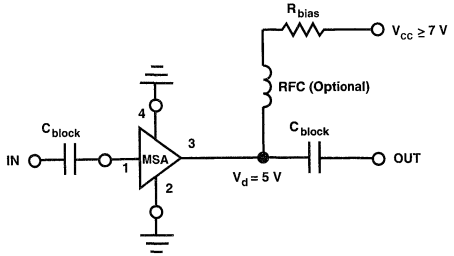
Available in cut lead version (package 36) as MSA-0336.

35 micro-X Package[1]



Note:
1. Short leaded 36 package available upon request.

Typical Biasing Configuration



MSA-0335, -0336 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	425 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65 to 200°C

Thermal Resistance[2,5]:
θ_{jc} = 150°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.7 mW/°C for T_C > 136°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.7	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.6:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.7:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		10.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		6.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 20 to 50 mA. Typical performance as a function of current is on the following page.

MSA-0335, -0336 Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0335	10	Strip
MSA-0336-BLK	100	Antistatic Bag
MSA-0336-TR1	1000	7" Reel

For more information, see "Tape and Reel Packaging for Semiconductor Devices."

MSA-0335, -0336 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.05	177	12.6	4.25	175	–18.6	.118	1	.17	–8
0.2	.05	170	12.5	4.24	170	–18.3	.121	2	.17	–17
0.4	.04	161	12.5	4.20	160	–18.3	.122	3	.17	–33
0.6	.04	156	12.4	4.15	151	–18.3	.121	5	.18	–47
0.8	.03	149	12.2	4.09	142	–17.9	.128	8	.19	–61
1.0	.02	154	12.1	4.02	132	–17.6	.131	9	.20	–73
1.5	.03	–104	11.6	3.79	109	–16.8	.145	13	.20	–102
2.0	.08	–136	10.9	3.49	87	–15.7	.164	11	.21	–133
2.5	.14	–157	10.0	3.16	71	–14.9	.180	13	.23	–155
3.0	.21	–176	9.0	2.81	53	–14.6	.187	8	.24	–173
3.5	.27	170	7.9	2.49	36	–13.9	.202	4	.25	178
4.0	.31	157	6.9	2.20	20	–13.6	.209	–1	.24	177
5.0	.37	125	4.9	1.76	–10	–12.9	.226	–12	.20	165
6.0	.51	87	2.8	1.38	–38	–12.8	.230	–25	.22	130

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

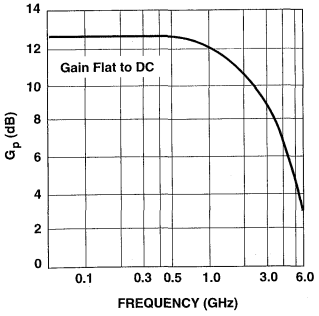


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 35 mA.

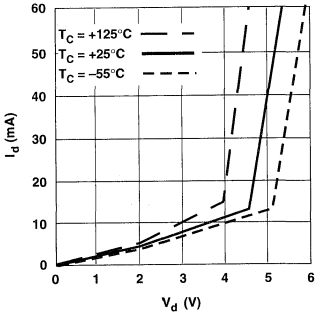


Figure 2. Device Current vs. Voltage.

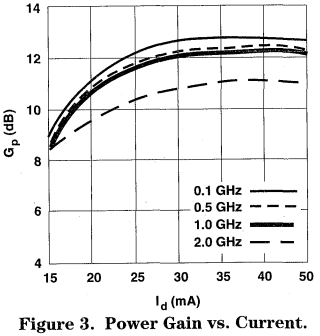


Figure 3. Power Gain vs. Current.

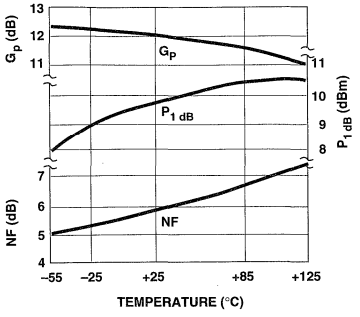


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 1.0 GHz, I_d = 35 mA.

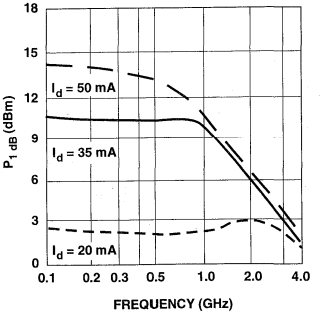


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

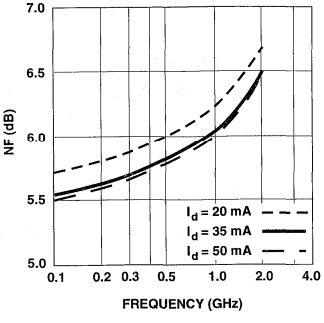
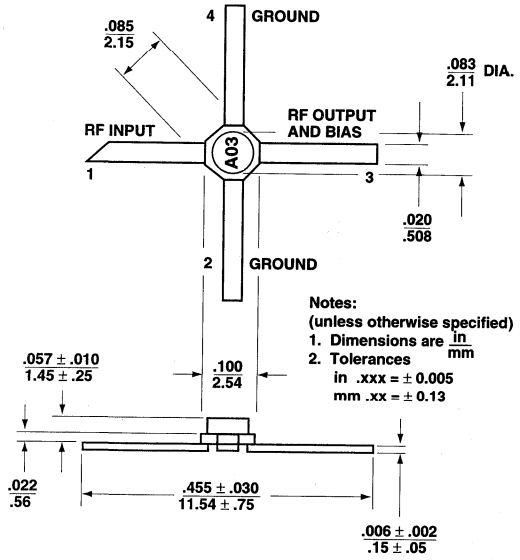


Figure 6. Noise Figure vs. Frequency.

35 micro-X Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifiers

Technical Data

MSA-0370

Features

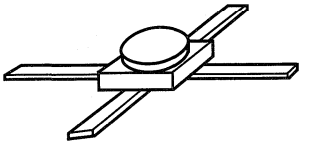
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.8 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **10.0 dBm Typical P_{1dB} at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-ceramic Microstrip Package**

Description

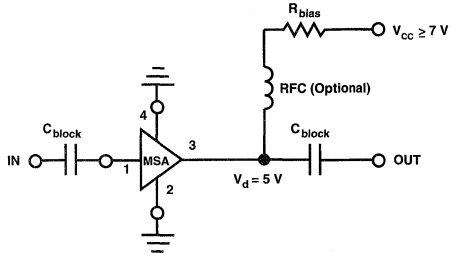
The MSA-0370 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package



Typical Biasing Configuration



MSA-0370 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	425 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 125°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 8 mW/°C for T_C > 147°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.8 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.8:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.8:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 20 to 50 mA. Typical performance as a function of current is on the following page.

MSA-0370 Typical Scattering Parameters (Z_0 = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.13	–179	12.6	4.27	176	–18.6	.118	2	.09	–14
0.2	.13	–180	12.6	4.25	171	–18.3	.121	2	.10	–29
0.4	.12	–180	12.5	4.21	162	–18.4	.121	4	.12	–52
0.6	.11	–178	12.4	4.17	154	–18.2	.123	6	.14	–70
0.8	.11	–174	12.3	4.11	146	–17.8	.129	8	.17	–82
1.0	.10	–168	12.2	4.06	137	–17.7	.130	8	.20	–92
1.5	.11	–149	11.7	3.85	116	–17.1	.140	11	.24	–114
2.0	.16	–147	11.1	3.57	96	–16.2	.155	11	.27	–134
2.5	.22	–151	10.3	3.27	82	–15.6	.167	14	.27	–146
3.0	.28	–160	9.3	2.91	65	–15.2	.174	11	.27	–159
3.5	.33	–169	8.2	2.58	48	–14.5	.188	7	.26	–163
4.0	.36	–177	7.1	2.27	34	–14.3	.192	3	.25	–162
5.0	.38	163	5.1	1.81	9	–13.8	.203	–5	.23	–153
6.0	.39	132	3.4	1.48	–14	–13.5	.213	–13	.24	–160

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

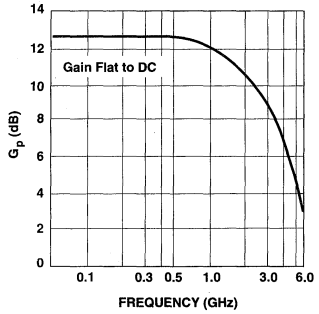


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 35 mA.

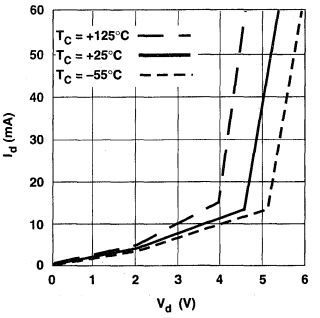


Figure 2. Device Current vs. Voltage.

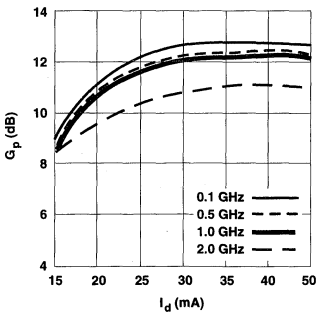


Figure 3. Power Gain vs. Current.

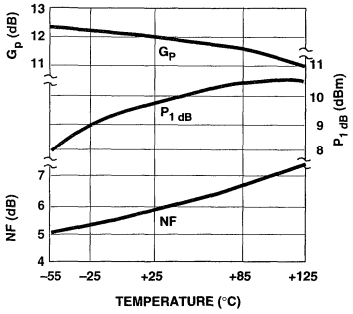


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 1.0 GHz, I_d = 35 mA.

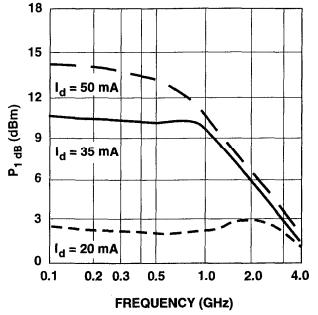


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

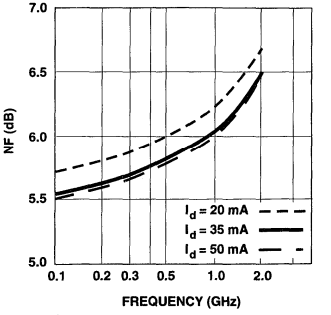
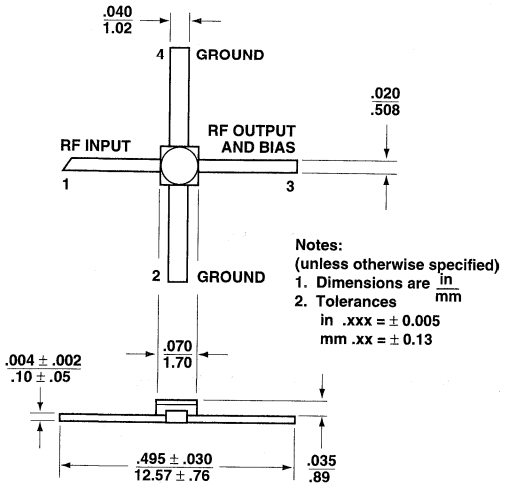


Figure 6. Noise Figure vs. Frequency.

70 mil Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0385

Features

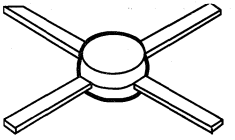
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.5 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **10.0 dBm Typical $P_{1\,dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

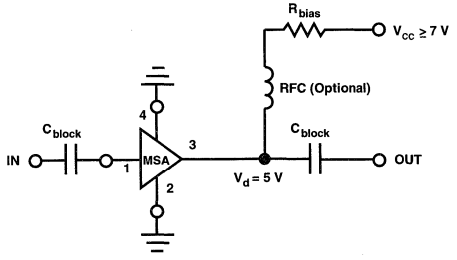
The MSA-0385 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package



Typical Biasing Configuration



MSA-0385 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	70 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 105°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 9.5 mW/°C for T_C > 108°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.0	12.5 12.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.7:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 20 to 50 mA. Typical performance as a function of current is on the following page.

MSA-0385 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.09	178	12.6	4.26	175	–18.1	.124	2	.13	–10
0.2	.09	171	12.5	4.24	170	–18.4	.120	3	.13	–20
0.4	.08	166	12.4	4.17	161	–18.4	.121	6	.14	–41
0.6	.07	160	12.3	4.10	151	–18.0	.126	8	.15	–57
0.8	.07	155	12.1	4.01	142	–17.9	.127	12	.16	–71
1.0	.06	152	11.9	3.92	133	–17.6	.132	12	.18	–84
1.5	.05	–169	11.2	3.63	112	–16.5	.149	18	.21	–112
2.0	.08	–174	10.4	3.29	92	–15.6	.167	19	.23	–136
2.5	.12	–173	9.5	2.98	79	–14.6	.186	22	.25	–150
3.0	.20	178	8.4	2.64	63	–14.1	.198	20	.26	–166
3.5	.25	170	7.5	2.36	47	–13.5	.211	17	.25	–174
4.0	.28	160	6.5	2.12	33	–13.0	.207	13	.24	–180
5.0	.42	134	4.7	1.71	7	–12.2	.224	4	.20	168
6.0	.50	99	2.7	1.37	–18	–12.0	.252	–7	.23	133

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

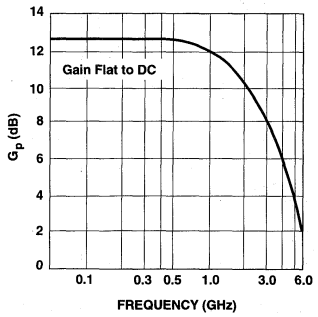


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 35 mA.

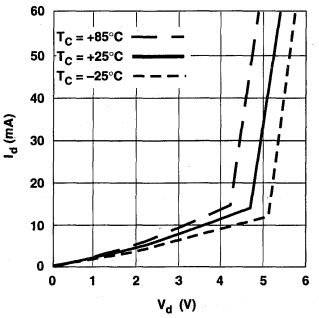


Figure 2. Device Current vs. Voltage.

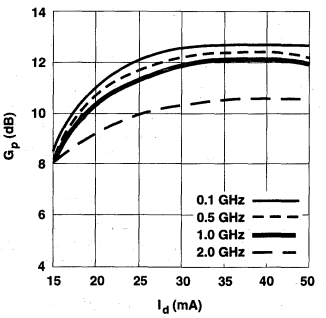


Figure 3. Power Gain vs. Current.

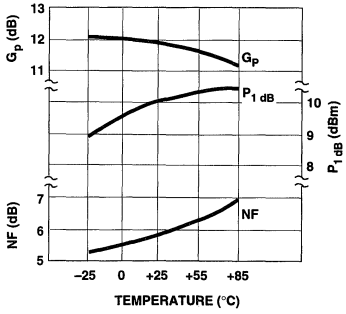


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 35 mA.

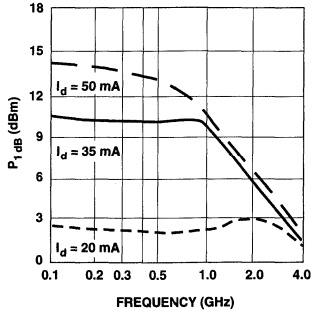


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

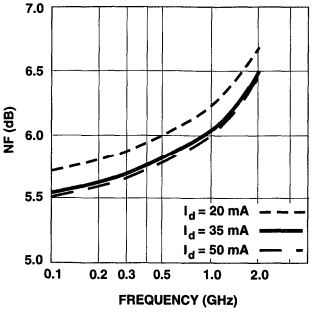
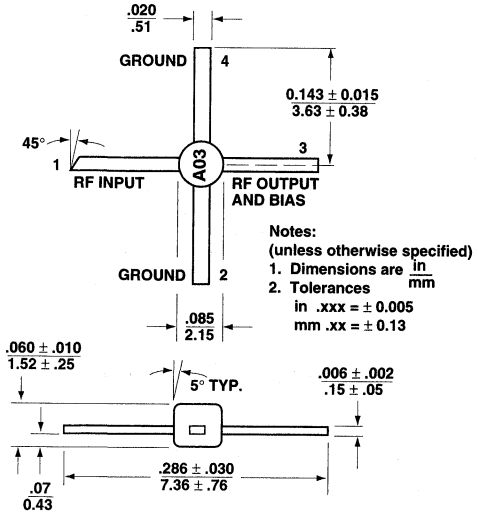


Figure 6. Noise Figure vs. Frequency.

85 Plastic Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0386

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.4 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **10.0 dBm Typical $P_{1\ dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Note:

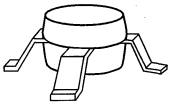
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Description

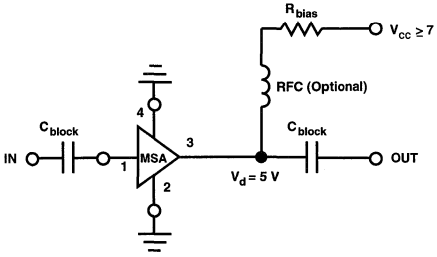
The MSA-0386 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

86 Plastic Package



Typical Biasing Configuration



MSA-0386 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	70 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 115°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 9.5 mW/°C for T_C > 116°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.0	12.5 12.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.4	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.7:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec		140	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 20 to 40 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0386-TR1	1000	7" Reel
MSA-0386-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0386 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.11	174	12.5	4.22	175	–18.3	.122	1	.13	–11
0.2	.11	169	12.5	4.20	170	–18.2	.124	2	.13	–20
0.4	.11	159	12.4	4.16	159	–18.1	.124	5	.14	–41
0.6	.10	149	12.2	4.09	149	–17.9	.128	8	.15	–60
0.8	.10	142	12.1	4.00	139	–17.6	.131	9	.16	–78
1.0	.09	137	11.9	3.93	129	–17.4	.136	11	.18	–93
1.5	.09	139	11.2	3.61	106	–16.6	.149	14	.20	–129
2.0	.12	149	10.3	3.28	83	–15.3	.171	13	.23	–157
2.5	.18	150	9.4	2.95	66	–14.4	.190	12	.26	–176
3.0	.25	142	8.3	2.60	48	–13.7	.207	9	.29	167
3.5	.32	133	7.2	2.29	31	–13.2	.219	3	.30	152
4.0	.40	124	6.0	2.01	15	–13.0	.224	–1	.31	142
5.0	.53	106	3.7	1.53	–13	–12.8	.228	–11	.32	128

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

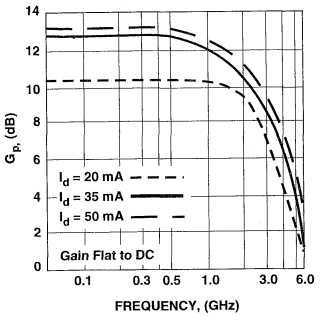


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C.

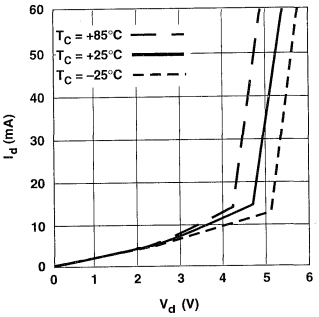


Figure 2. Device Current vs. Voltage.

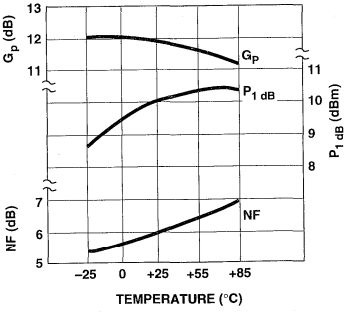


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 35 mA.

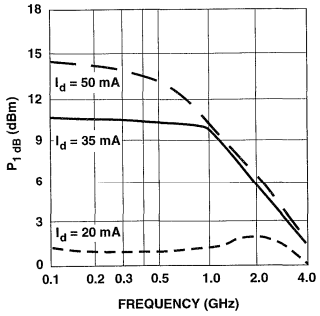


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

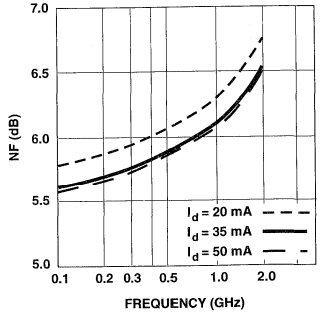
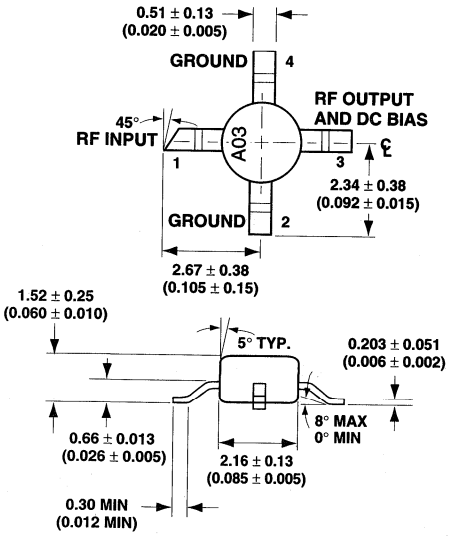


Figure 5. Noise Figure vs. Frequency.

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0400

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 4.0 GHz
- **8.5 dB Typical Gain at 1.0 GHz**
- **16.0 dBm Typical $P_{1\,dB}$ at 1.0 GHz**

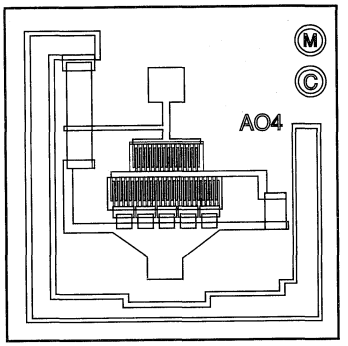
Description

The MSA-0400 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See APPLICATIONS section, "Chip Use".

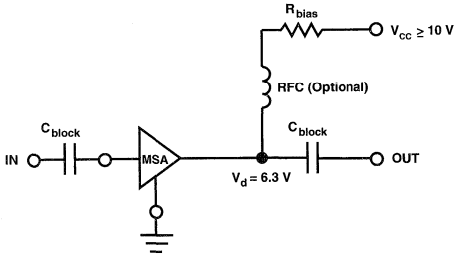
Chip Outline[1]



Note:

1. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



MSA-0400 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	120 mA
Power Dissipation[2,3]	850 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 35°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 28.6 mW/°C for T_{MS} > 170°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0400-GP4	100

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 90 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		8.5	
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.6	
$f_{3\ dB}$	3 dB Bandwidth		GHz		4.3	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.8:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz, I_d = 50 mA	dBm		12.5	
	Output Power at 1 dB Gain Compression	f = 1.0 GHz, I_d = 90 mA	dBm		16.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		30.0	
t_D	Group Delay	f = 1.0 GHz	psec		140	
V_d	Device Voltage		V	5.7	6.3	6.9
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 40 to 110 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 50 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.18	179	8.6	2.68	177	–16.4	.151	1	.10	–13	1.37
0.5	.18	–179	8.6	2.68	163	–16.3	.153	7	.16	–54	1.34
1.0	.16	–171	8.5	2.65	145	–15.8	.161	10	.22	–83	1.28
1.5	.16	–161	8.4	2.63	127	–15.4	.169	16	.29	–101	1.19
2.0	.21	–156	8.2	2.56	109	–14.6	.187	18	.33	–119	1.07
2.5	.27	–152	7.8	2.45	98	–13.8	.205	24	.37	–128	0.98
3.0	.33	–159	7.0	2.23	82	–13.4	.213	24	.42	–140	0.91
4.0	.42	–171	5.2	1.81	54	–12.5	.237	21	.42	–151	0.86
5.0	.45	172	3.4	1.49	3	–11.7	.259	17	.38	–153	0.94

Note:
1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

MSA-0400 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 90 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.25	179	8.7	2.73	177	-16.4	.152	2	.03	-36	1.33
0.5	.24	173	8.8	2.76	164	-16.3	.153	5	.10	-83	1.31
1.0	.22	166	8.8	2.74	148	-15.9	.160	10	.19	-91	1.26
1.5	.16	164	8.8	2.74	132	-15.3	.172	16	.27	-94	1.18
2.0	.13	173	8.7	2.73	116	-14.5	.189	22	.32	-98	1.10
2.5	.12	-162	8.3	2.60	106	-13.9	.203	31	.36	-95	1.04
3.0	.14	-147	8.0	2.50	90	-13.1	.222	33	.40	-95	0.97
4.0	.17	-154	6.7	2.17	64	-10.9	.286	36	.43	-93	0.87
5.0	.20	146	5.2	1.83	41	-9.2	.346	36	.40	-94	0.89

Note:

1. S-parameters are de-embedded from 200 mil BeO package measured data using the package model found in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

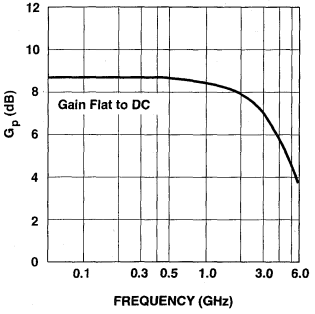


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 90 mA.

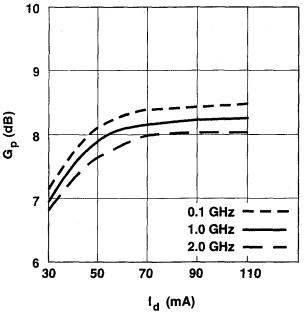


Figure 2. Power Gain vs. Current.

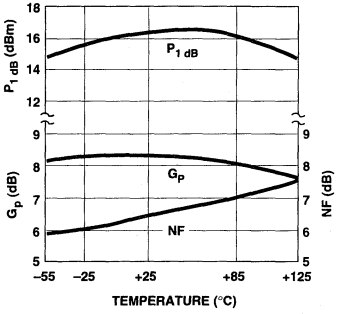


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 1.0 GHz, I_d = 90 mA.

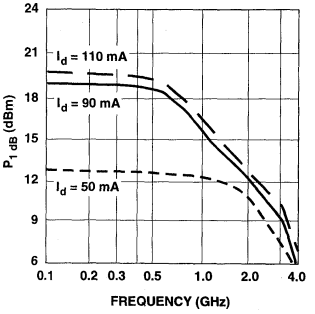


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

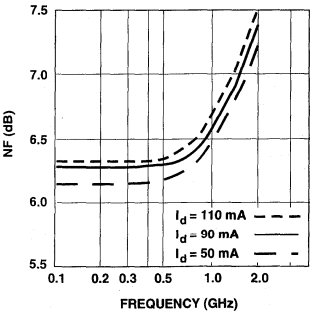
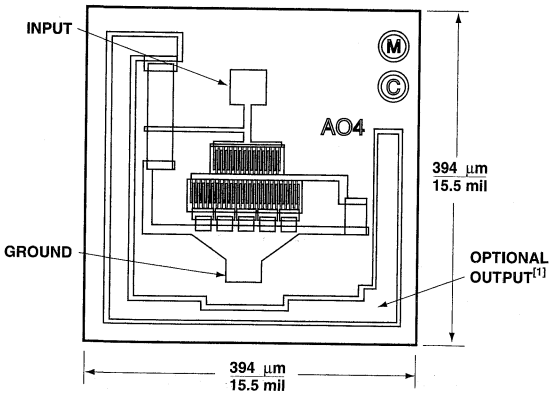


Figure 5. Noise Figure vs. Frequency.

MSA-0400 Chip Dimensions



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils. Chip thickness is 114 µm/4.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side.
Note 1: Output contact is made by die attaching the backside of the die.

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0404

Features

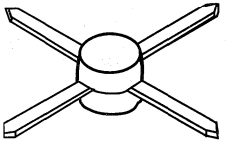
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 2.5 GHz
- **7.5 dB Typical Gain at 1.0 GHz**
- **11.5 dBm Typical $P_{1\ dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

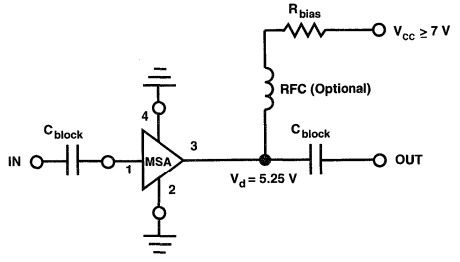
The MSA-0404 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package



Typical Biasing Configuration



MSA-0404 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	85 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 85°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 10 mW/°C for T_C > 108°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 50 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz f = 1.0 GHz	dB	7.0	8.3 8.0 7.5	
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±1.0	
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.4:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.8:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		7.0	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		11.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		24.5	
t_D	Group Delay	f = 1.0 GHz	psec		150	
V_d	Device Voltage		V	4.75	5.25	5.75
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 30 to 70 mA. Typical performance as a function of current is on the following page.

MSA-0404 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 50 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.16	175	8.3	2.59	174	–16.2	.156	0	.13	–13
0.2	.16	170	8.2	2.58	168	–16.2	.155	2	.13	–25
0.4	.15	161	8.1	2.54	156	–16.0	.158	4	.14	–47
0.6	.14	152	8.0	2.51	145	–16.0	.158	6	.16	–64
0.8	.12	145	7.8	2.46	133	–15.8	.163	8	.19	–79
1.0	.11	141	7.7	2.41	122	–15.4	.169	9	.21	–91
1.5	.07	141	7.2	2.29	96	–14.6	.186	13	.24	–118
2.0	.09	161	6.6	2.14	71	–13.3	.215	12	.26	–140
2.5	.14	159	5.9	1.98	53	–12.4	.240	13	.28	–157
3.0	.22	148	5.1	1.80	33	–11.7	.260	7	.29	–176
3.5	.30	128	4.3	1.64	13	–10.9	.286	0	.32	167
4.0	.38	109	3.2	1.45	–6	–10.4	.301	–7	.33	153
5.0	.47	91	2.1	1.27	–23	–10.2	.310	–15	.35	137
6.0	.55	75	1.0	1.09	–39	–10.1	.312	–24	.37	120

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

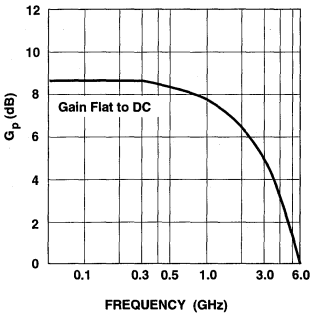


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 50 mA.

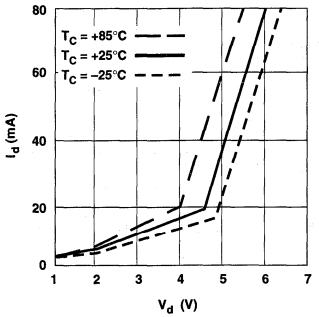


Figure 2. Device Current vs. Voltage.

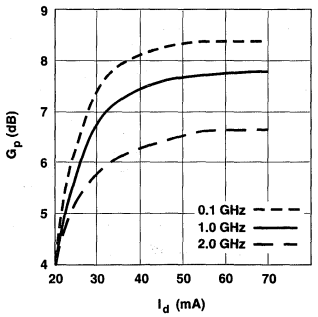


Figure 3. Power Gain vs. Current.

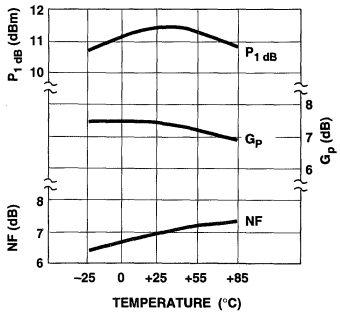


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 50 mA.

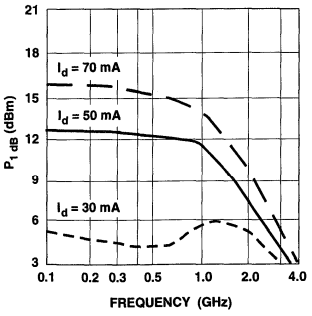


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

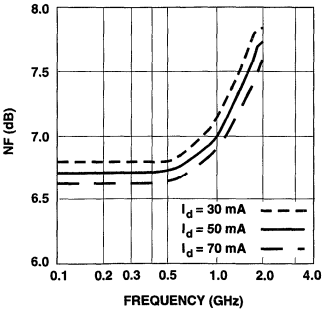
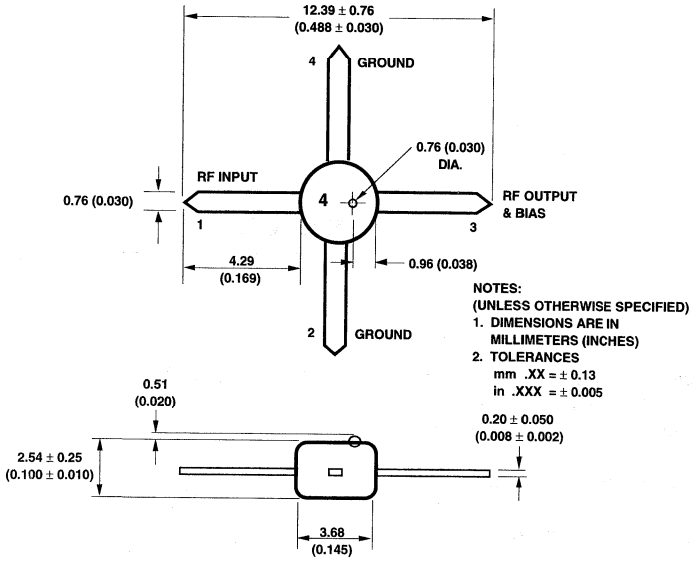


Figure 6. Noise Figure vs. Frequency.

04A Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES).

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0420

Features

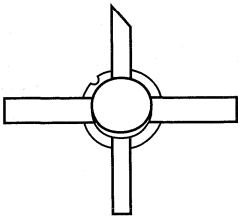
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 4.0 GHz
- **8.5 dB Typical Gain at 1.0 GHz**
- **16.0 dBm Typical $P_{1\ dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Metal/Beryllia Microstrip Package**

Description

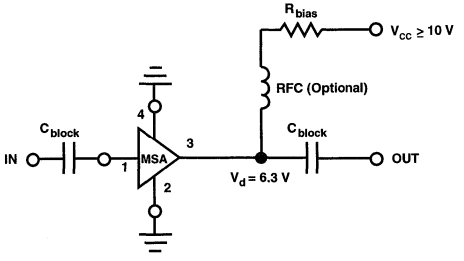
The MSA-0420 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

200 mil BeO Package



Typical Biasing Configuration



MSA-0420 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	120 mA
Power Dissipation[2,3]	850 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 40°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 25 mW/°C for T_C > 166°C.
4. The small spot size of this technique results in a higher, though more accurate determination of q_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 90 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	7.5	8.5	9.5
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.6	±1.0
$f_{3\ dB}$	3 dB Bandwidth		GHz		4.3	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.8:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm	14.0	16.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		30.0	
t_D	Group Delay	f = 1.0 GHz	psec		140	
V_d	Device Voltage		V	5.7	6.3	6.9
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 40 to 110 mA. Typical performance as a function of current is on the following page.

MSA-0420 Typical Scattering Parameters (Z_0 = 50 Ω, T_A = 25°C, I_d = 90 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.25	177	8.6	2.70	175	–16.4	.151	1	.03	–30
0.2	.25	173	8.6	2.69	170	–16.5	.150	1	.04	–59
0.4	.24	167	8.6	2.69	159	–16.5	.150	–1	.07	–79
0.6	.22	160	8.5	2.67	149	–16.4	.152	–2	.10	–92
0.8	.21	154	8.5	2.66	139	–16.3	.154	–2	.13	–99
1.0	.20	148	8.3	2.60	129	–16.1	.156	–3	.16	–109
1.5	.14	136	8.1	2.54	104	–15.6	.166	–4	.22	–124
2.0	.10	136	7.9	2.48	80	–14.8	.181	–6	.25	–139
2.5	.08	161	7.4	2.34	62	–14.3	.193	–5	.28	–147
3.0	.10	178	7.0	2.24	39	–13.7	.206	–11	.31	–157
3.5	.13	176	6.6	2.13	18	–12.6	.233	–18	.34	–167
4.0	.14	163	5.9	1.97	–3	–11.9	.253	–25	.36	–176
4.5	.14	133	5.3	1.83	–23	–11.3	.273	–33	.37	174
5.0	.16	91	4.5	1.69	–343	–10.5	.299	–43	.37	162

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

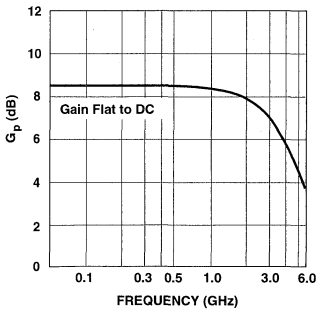


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 90 mA.

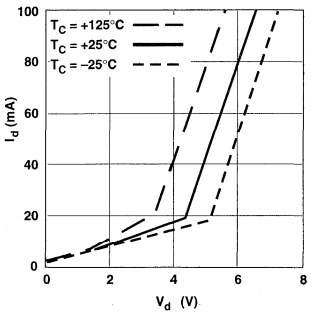


Figure 2. Device Current vs. Voltage.

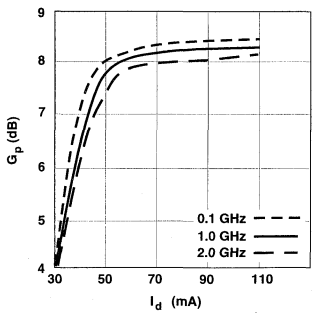


Figure 3. Power Gain vs. Current.

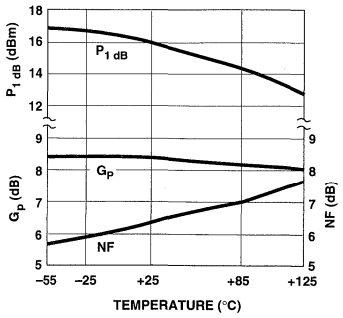


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 90 mA.

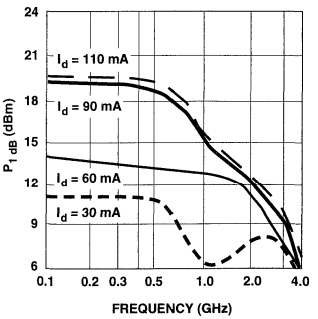


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

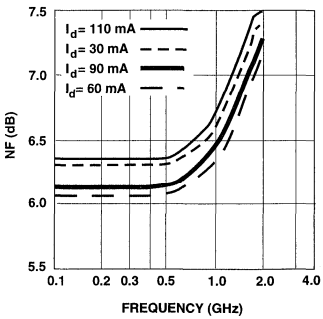
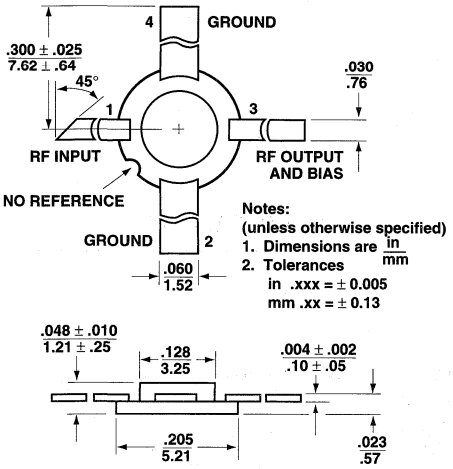


Figure 6. Noise Figure vs. Frequency.

200 mil BeO Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifiers

Technical Data

MSA-0435, -0436

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 3.8 GHz
- **12.5 dBm Typical $P_{1\ dB}$ at 1.0 GHz**
- **8.5 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Cost Effective Ceramic Microstrip Package**

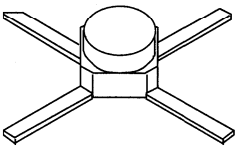
Description

The MSA-0435 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Available in cut lead version (package 36) as MSA-0436.

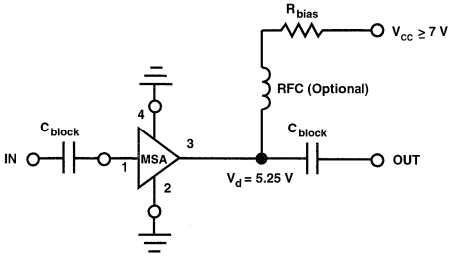
35 micro-X Package[1]



Note:

1. Short leaded 36 package available upon request.

Typical Biasing Configuration



MSA-0435, -0436 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	100 mA
Power Dissipation[2,3]	650 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65 to 200°C

Thermal Resistance[2,5]:
θ_{jc} = 140°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.1 mW/°C for T_C > 109°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of q_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 50 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	7.5	8.5	9.5
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		3.8	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.4:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.9:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		25.5	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.75	5.25	5.75
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 30 to 70 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0435	10	Strip
MSA-0436-BLK	100	Antistatic Bag
MSA-0436-TR1	1000	7" Reel

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0435, -0436 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 50 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.08	175	8.5	2.67	175	–16.4	.151	1	.20	–10
0.2	.08	172	8.5	2.68	170	–16.3	.153	2	.20	–16
0.4	.07	171	8.5	2.67	161	–16.4	.151	3	.20	–33
0.6	.07	166	8.5	2.66	151	–16.2	.155	6	.21	–45
0.8	.05	169	8.4	2.64	142	–16.1	.156	8	.22	–57
1.0	.05	175	8.3	2.61	136	–16.0	.159	10	.24	–68
1.5	.04	–142	8.1	2.55	109	–15.0	.178	13	.26	–96
2.0	.09	–145	7.8	2.46	87	–14.2	.196	15	.28	–123
2.5	.14	–154	7.3	2.33	71	–13.1	.221	18	.31	–140
3.0	.22	–175	6.6	2.14	50	–12.5	.238	14	.33	–160
3.5	.28	170	5.8	1.94	32	–11.7	.260	9	.35	–173
4.0	.34	156	4.8	1.74	15	–11.3	.271	4	.34	–179
4.5	.37	140	3.9	1.57	–1	–10.7	.291	–2	.33	–171
5.0	.42	120	3.0	1.41	–16	–10.4	.302	–8	.32	–160

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

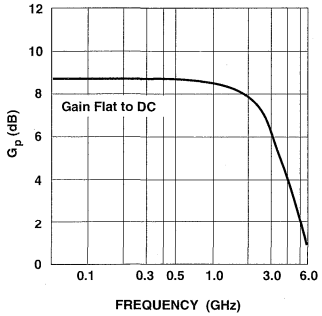


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 50 mA.

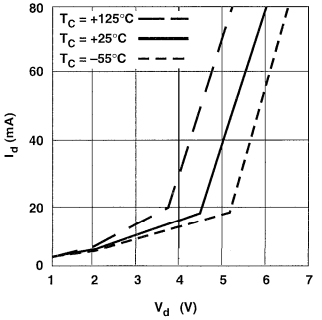


Figure 2. Device Current vs. Voltage.

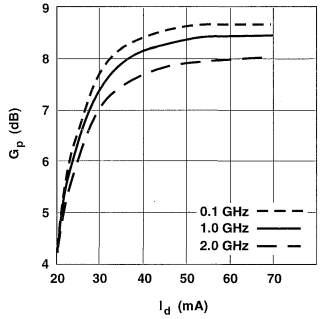


Figure 3. Power Gain vs. Current.

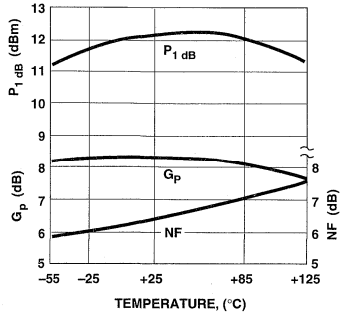


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 50 mA.

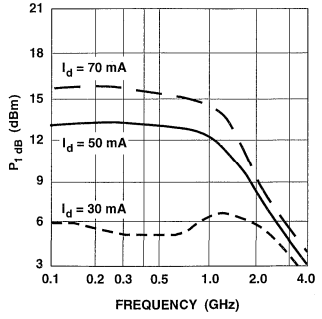


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

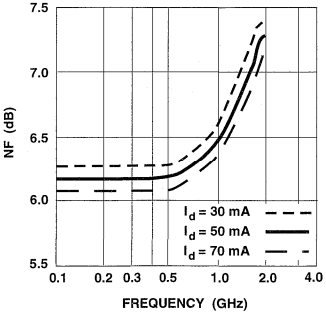
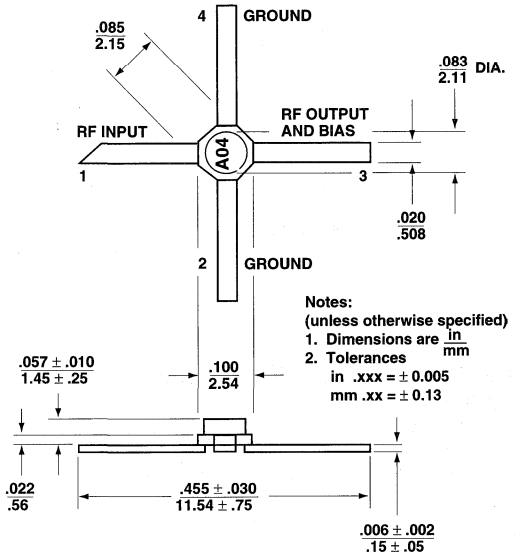


Figure 6. Noise Figure vs. Frequency.

35 micro-X Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0470

Features

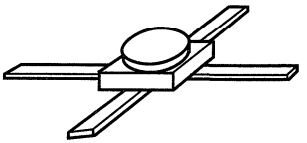
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 4.0 GHz
- **12.5 dBm Typical $P_{1\ dB}$ at 1.0 GHz**
- **8.5 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-ceramic Microstrip Package**

Description

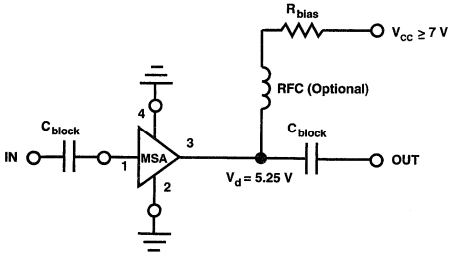
The MSA-0470 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package



Typical Biasing Configuration



MSA-0470 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	100 mA
Power Dissipation[2,3]	650 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 115°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 8.7 mW/°C for T_C > 125°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 50 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	7.5	8.5	9.5
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.6	±1.0
$f_{3\ dB}$	3 dB Bandwidth		GHz		4.0	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 2.5 GHz			2.0:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		25.5	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.75	5.25	5.75
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 30 to 70 mA. Typical performance as a function of current is on the following page.

MSA-0470 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 50 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.18	179	8.5	2.67	176	–16.4	.151	1	.10	–14
0.2	.18	179	8.5	2.67	172	–16.4	.151	2	.10	–30
0.4	.18	179	8.5	2.67	163	–16.4	.152	3	.13	–50
0.6	.17	–179	8.5	2.65	155	–16.2	.155	5	.16	–67
0.8	.16	–176	8.4	2.64	147	–16.1	.158	8	.19	–79
1.0	.16	–174	8.3	2.61	138	–15.9	.161	6	.22	–90
1.5	.16	–166	8.2	2.56	117	–15.5	.169	9	.29	–111
2.0	.21	–163	7.8	2.46	97	–14.6	.186	9	.33	–131
2.5	.26	–162	7.3	2.33	83	–13.8	.204	12	.36	–142
3.0	.32	–170	6.5	2.12	65	–13.5	.212	10	.40	–156
3.5	.37	–177	5.7	1.93	38	–13.2	.220	7	.40	–164
4.0	.40	175	4.7	1.73	33	–12.6	.234	3	.40	–170
4.5	.41	166	3.9	1.57	20	–12.4	.239	–1	.39	–173
5.0	.42	155	3.1	1.44	7	–11.9	.255	–6	.37	–176

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

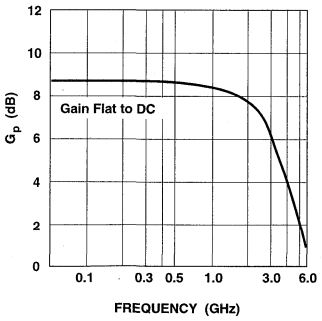


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 50 mA.

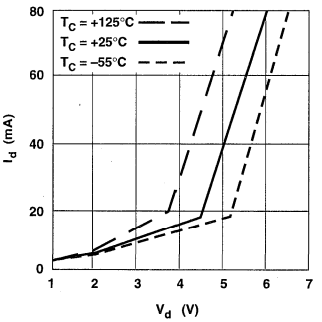


Figure 2. Device Current vs. Voltage.

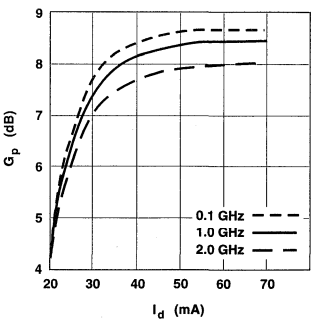


Figure 3. Power Gain vs. Current.

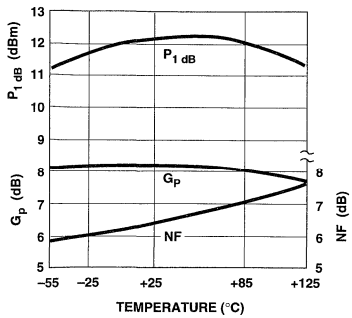


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 50 mA.

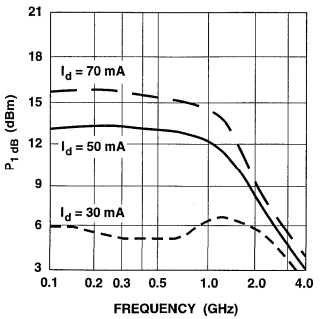


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

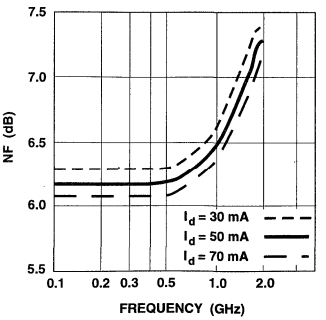
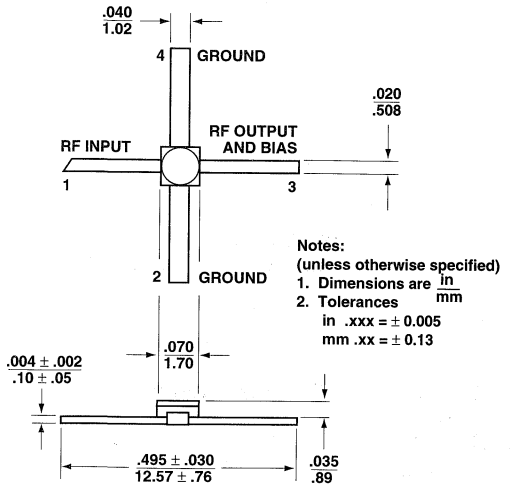


Figure 6. Noise Figure vs. Frequency.

70 mil Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0485

Features

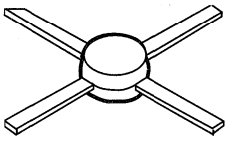
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 3.6 GHz
- **8.0 dB Typical Gain at 1.0 GHz**
- **12.5 dBm Typical $P_{1\,dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

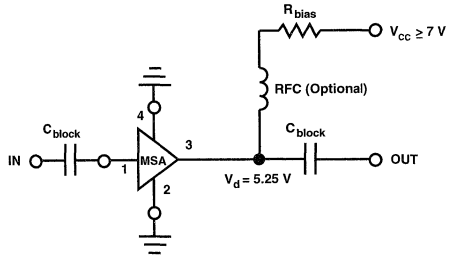
The MSA-0485 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package



Typical Biasing Configuration



MSA-0485 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	85 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 90°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 11.1 mW/°C for T_C > 105°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 50 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 7.0	8.3 8.0	
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.7	
$f_{3\ dB}$	3 dB Bandwidth		GHz		3.6	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.6:1	
	Output VSWR	f = 0.1 to 2.5 GHz			2.0:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		7.0	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		25.5	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	4.2	5.25	6.3
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 30 to 70 mA. Typical performance as a function of current is on the following page.

MSA-0485 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 50 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.21	177	8.4	2.63	175	–16.1	.156	2	.08	–16
0.2	.20	176	8.3	2.60	171	–16.2	.155	2	.08	–30
0.4	.20	172	8.2	2.57	163	–16.1	.156	3	.10	–54
0.6	.19	171	8.1	2.55	155	–16.2	.155	5	.13	–71
0.8	.19	168	8.1	2.54	146	–16.0	.158	6	.16	–83
1.0	.18	166	8.0	2.52	138	–15.7	.164	9	.18	–93
1.5	.16	167	7.8	2.46	117	–15.3	.171	11	.25	–116
2.0	.18	168	7.4	2.34	97	–14.6	.187	12	.29	–136
2.5	.21	173	6.9	2.21	83	–13.8	.204	16	.34	–150
3.0	.27	169	6.3	2.07	65	–13.4	.213	13	.38	–161
3.5	.33	161	5.7	1.92	48	–12.6	.234	9	.39	–172
4.0	.38	154	4.8	1.74	33	–12.3	.242	6	.37	–179
4.5	.42	145	4.1	1.59	18	–12.1	.249	3	.36	–174
5.0	.44	131	3.3	1.46	4	–11.7	.259	–3	.34	–165

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

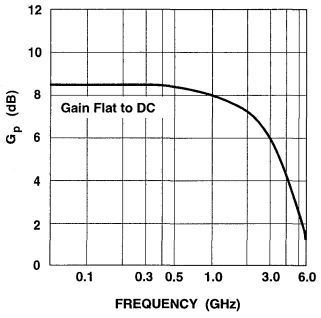


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 50 mA.

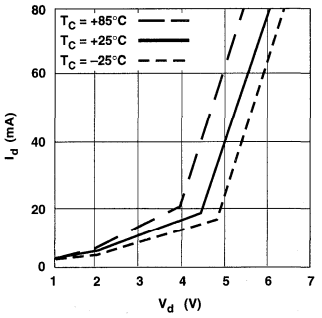


Figure 2. Device Current vs. Voltage.

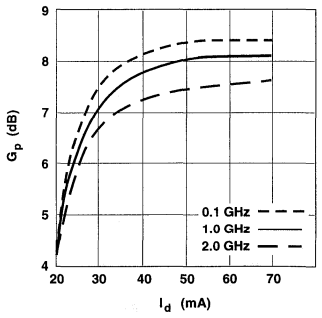


Figure 3. Power Gain vs. Current.

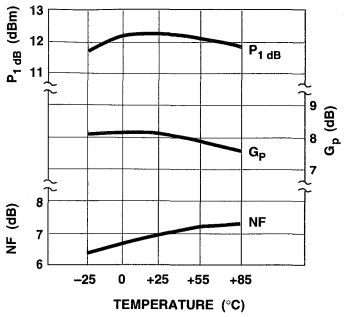


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 50 mA.

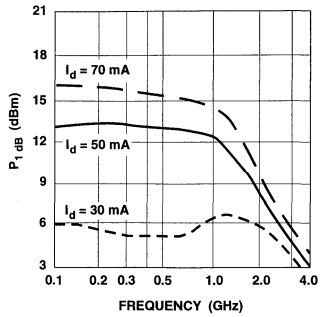


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

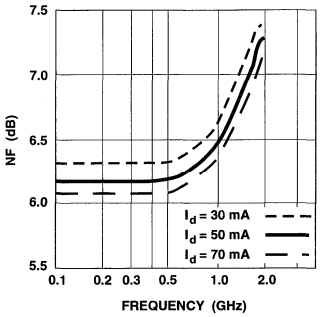
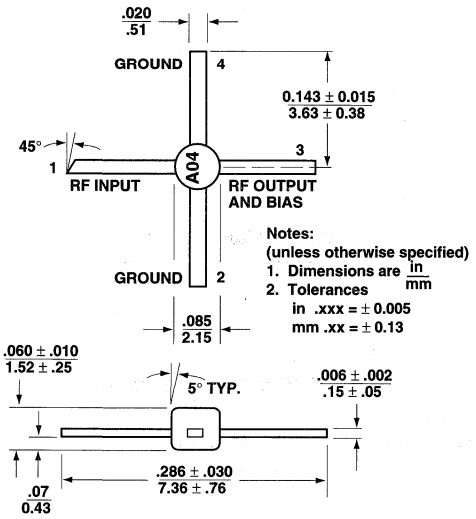


Figure 6. Noise Figure vs. Frequency.

85 Plastic Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0486

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 3.2 GHz
- **8 dB Typical Gain at 1.0 GHz**
- **12.5 dBm Typical $P_{1\ dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

Note:

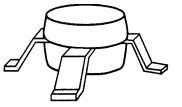
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Description

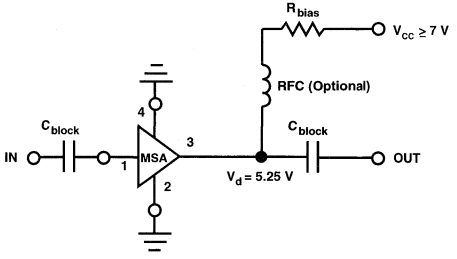
The MSA-0486 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

86 Plastic Package



Typical Biasing Configuration



MSA-0486 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	85 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 100°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 10 mW/°C for T_C > 100°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 50 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 7.0	8.3 8.0	
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		3.2	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.9:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		7.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		25.5	
t_D	Group Delay	f = 1.0 GHz	psec		140	
V_d	Device Voltage		V	4.2	5.25	6.3
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 30 to 70 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0486-TR1	1000	7" Reel
MSA-0486-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0486 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 50 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.14	178	8.4	2.62	175	–16.2	.154	1	.16	–10
0.2	.14	175	8.3	2.61	170	–16.3	.153	2	.16	–20
0.4	.14	171	8.2	2.57	161	–16.3	.154	3	.17	–39
0.6	.13	168	8.1	2.54	151	–16.0	.158	4	.18	–57
0.8	.13	166	8.0	2.52	141	–15.9	.161	5	.20	–74
1.0	.13	165	7.9	2.48	131	–15.7	.165	6	.21	–88
1.5	.15	168	7.7	2.42	108	–14.8	.182	8	.27	–121
2.0	.21	168	7.3	2.32	84	–14.0	.199	7	.32	–149
2.5	.29	165	6.8	2.18	65	–13.1	.222	4	.38	–168
3.0	.37	153	5.9	1.97	43	–12.7	.231	–1	.40	173
3.5	.44	142	4.8	1.74	24	–12.5	.238	–5	.41	157
4.0	.50	130	3.6	1.52	7	–12.5	.238	–10	.41	145
5.0	.61	109	1.3	1.16	–21	–12.7	.231	–17	.43	132

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

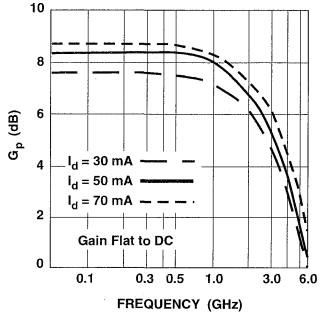


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C.

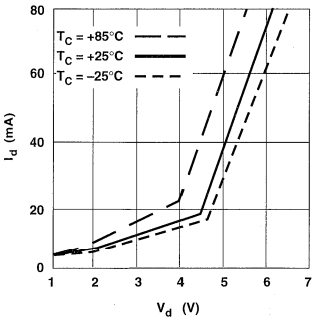


Figure 2. Device Current vs. Voltage.

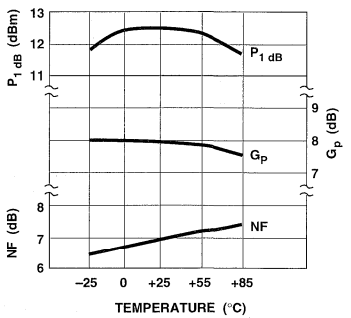


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 50 mA.

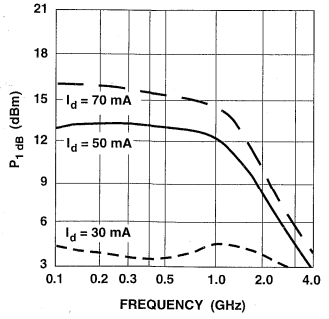


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

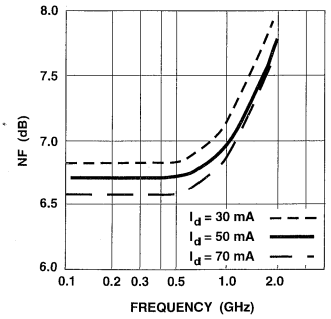
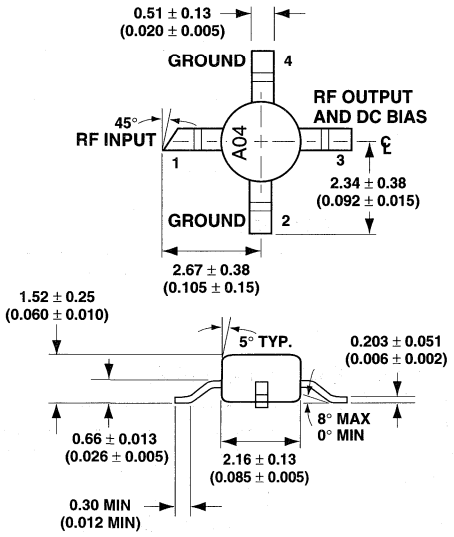


Figure 5. Noise Figure vs. Frequency.

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0500

Features

- **Cascadable 50 Ω Gain Block**
- **High Output Power:** +23 dBm Typical $P_{1\,dB}$ at 1.0 GHz
- **Low Distortion:** 33 dBm Typical IP_3 at 1.0 GHz
- **8.5 dB Typical Gain at 1.0 GHz**

Description

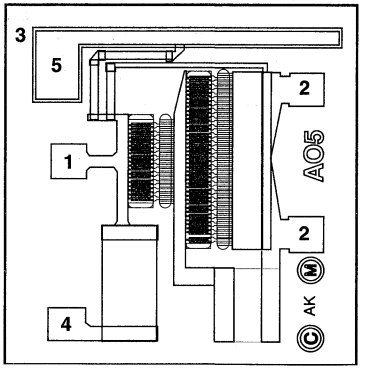
The MSA-0500 is a high performance, medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

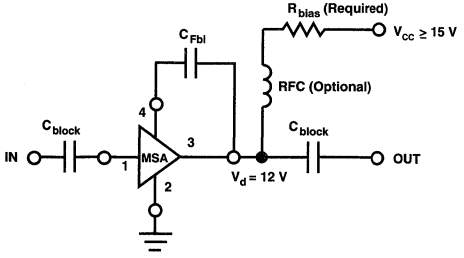
The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.

This chip is intended to be used with an external blocking capacitor completing the shunt feedback path (closed loop). Data sheet characterization is given for a 45 pF capacitor. Low frequency performance can be extended by using a larger valued capacitor.[1]

Chip Outline[1]



Typical Biasing Configuration



Note:

1. See Application Note, AN-S009: "Silicon MMIC Chip Use" for additional information.

MSA-0500 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	225 mA
Power Dissipation[2,3]	3.0 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
$\theta_{jc} = 20°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 50 mW/°C for T_{MS} > 140°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods.

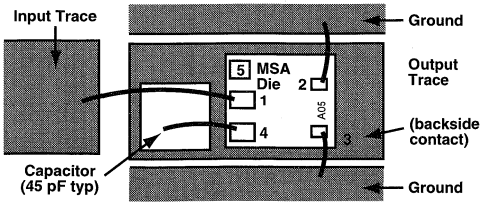
Electrical Specifications[1], T_A = 25°C

Unless otherwise noted, performance is for a MSA-0500 used with an external 45 pF capacitor. See bonding diagram.

Symbol	Parameters and Test Conditions[2]: I_d = 165 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		23.0	
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		9.0	
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.75	
$f_{3\,dB}$	3 dB Bandwidth[3]		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.0 GHz			2.5:1	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		33.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	10.5	12.0	13.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16.0	

Notes:
1. The recommended operating current range for this device is 80 to 200 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.
3. Referenced from 0.1 GHz gain (G_p).

Bonding Diagram



Numbers refer to pin contacts listed on the Chip Outline.

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0500-GP4	100

MSA-0500 Typical Scattering Parameters[1,2] (T_A = 25°C, I_d = 165 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.001	.68	–8	15.6	6.05	176	–26.2	.149	25	.79	–7	0.92
0.005	.57	–38	14.6	5.37	186	–19.3	.108	38	.67	–35	0.56
0.010	.43	–65	12.8	4.38	158	–15.7	.165	30	.50	–61	0.64
0.050	.16	–111	9.8	3.08	164	–14.2	.194	10	.19	–101	1.06
0.100	.12	–134	9.3	2.90	169	–14.0	.200	4	.13	–117	1.11
0.200	.12	–141	9.1	2.86	168	–13.9	.202	4	.12	–125	1.13
0.400	.13	–133	9.1	2.84	162	–13.8	.204	4	.17	–116	1.10
0.600	.16	–124	9.1	2.84	155	–13.7	.207	4	.22	–109	1.05
0.800	.21	–118	9.0	2.83	148	–13.6	.210	5	.28	–108	0.99
1.00	.25	–115	9.0	2.83	139	–13.4	.213	6	.34	–106	0.91
1.50	.36	–113	8.8	2.75	118	–12.7	.232	9	.44	–107	0.72
2.00	.45	–120	8.2	2.58	96	–11.6	.262	12	.66	–111	0.39
2.50	.51	–125	7.3	2.32	83	–11.0	.281	17	.58	–109	0.43
3.00	.52	–134	6.0	2.00	66	–10.5	.297	18	.58	–109	.46
3.50	.51	–144	4.8	1.75	52	–9.6	.329	20	.58	–106	0.49
4.00	.46	–157	3.7	1.53	39	–9.2	.347	21	.54	–104	0.60

Notes:

1. S-parameters are de-embedded from 200 mil BeO package measured data using the package model found in the DEVICE MODELS section.
2. S-parameter data assumes an external 45 pF capacitor. Low frequency performance can be extended using a larger valued capacitor.

Typical Performance, T_A = 25°C

(unless otherwise noted)

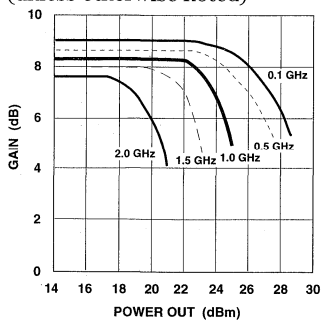


Figure 1. Typical Gain vs. Power Out, T_A = 25°C, I_d = 165 mA.

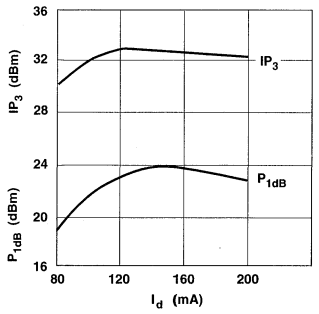


Figure 2. Output Power @ 1 dB Gain Compression, Third Order Intercept Point, f = 1.0 GHz.

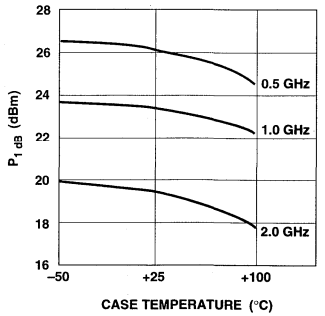


Figure 3. Output Power @ 1 dB Gain Compression vs. Temperature, I_d = 165 mA.

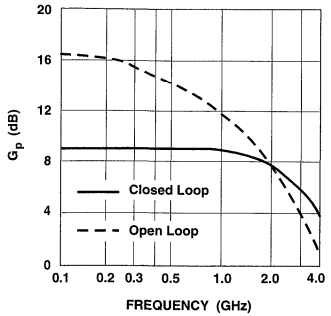
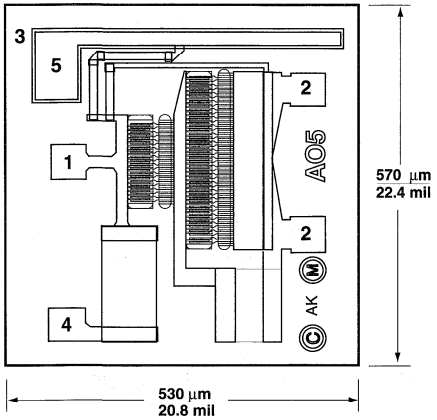


Figure 4. Gain vs. Frequency.

MSA-0500 Chip Dimensions[1]



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils. Chip thickness is 114 µm/4.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side. Note 1: Output contact is made by die attaching the backside of the die.

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0504

Features

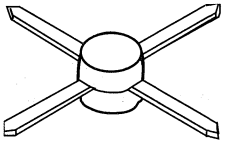
- **Cascadable 50 Ω Gain Block**
- **High Output Power:** 18.0 dBm Typical $P_{1\,dB}$ at 1.0 GHz
- **Low Distortion:** 29.0 dBm Typical IP_3 at 1.0 GHz
- **7.0 dB Typical Gain at 1.0 GHz**
- **Low Cost Plastic Package**

Description

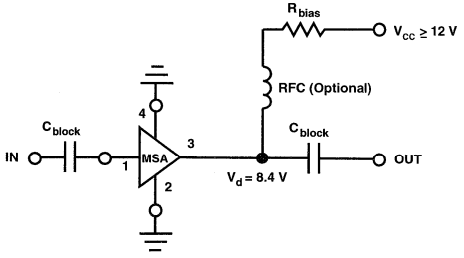
The MSA-0504 is a high performance medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package



Typical Biasing Configuration



MSA-0504 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	135 mA
Power Dissipation[2,3]	1.5 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 75°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 13.3 mW/°C for T_C > 88°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 80 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz f = 1.0 GHz	dBm dBm	 16.0	19.0 18.0	
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz f = 1.0 GHz	dB	 6.0	7.5 7.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.5 GHz	dB		±0.75	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.3	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.6:1	
	Output VSWR	f = 0.1 to 1.5 GHz			2.0:1	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		29.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
t_D	Group Delay	f = 1.0 GHz	psec		180	
V_d	Device Voltage		V	6.7	8.4	10.1
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16.0	

Notes:
1. The recommended operating current range for this device is 60 to 100 mA. Typical performance as a function of current is on the following page.
2. Referenced from 0.1 GHz Gain (G_P).

MSA-0504 Typical Scattering Parameters (T_A = 25°C, I_d = 80 mA)

Freq. MHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
5	.54	–43	14.7	5.43	160	–18.4	.120	37	.63	–39	0.60
25	.24	–112	9.3	2.92	155	–13.8	.204	12	.24	–101	0.99
50	.18	–142	8.1	2.54	161	–13.7	.206	3	.16	–125	1.17
100	.14	–156	7.8	2.45	166	–13.7	.207	3	.13	–137	1.18
200	.14	–168	7.6	2.40	163	–13.7	.206	1	.13	–146	1.20
400	.14	–174	7.5	2.37	150	–13.7	.206	1	.16	–143	1.19
600	.14	–175	7.4	2.34	137	–13.6	.208	–1	.20	–144	1.18
800	.15	–174	7.2	2.29	124	–13.5	.211	–1	.25	–148	1.15
1000	.17	–174	7.0	2.24	111	–13.6	.209	–3	.29	–154	1.14
1500	.23	–179	6.4	2.09	80	–13.3	.216	–4	.37	–168	1.06
2000	.33	171	5.5	1.88	51	–12.8	.230	–10	.48	178	0.91
2500	.42	156	4.3	1.64	27	–13.0	.224	–12	.51	165	0.90
3000	.49	146	3.2	1.44	6	–12.8	.230	–11	.55	157	0.92

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

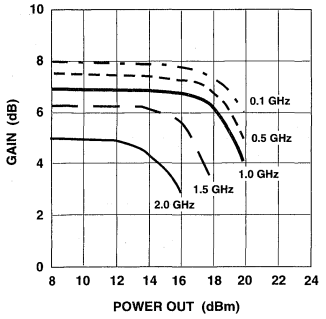


Figure 1. Typical Gain vs. Power Out, T_A = 25°C, I_d = 80 mA.

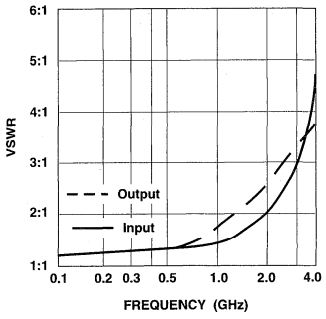


Figure 2. VSWR vs. Frequency, I_d = 80 mA.

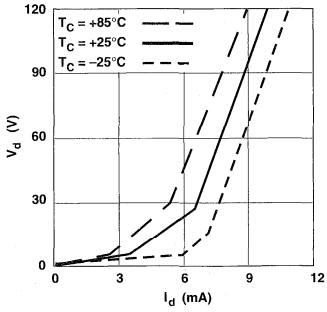


Figure 3. Device Current vs. Voltage.

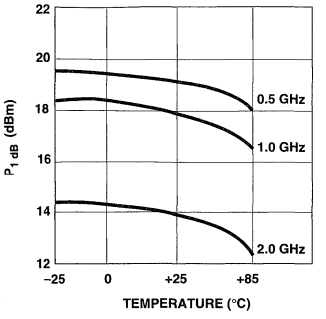


Figure 4. Output Power at 1 dB Gain Compression, vs. Case Temperature, I_d = 80 mA.

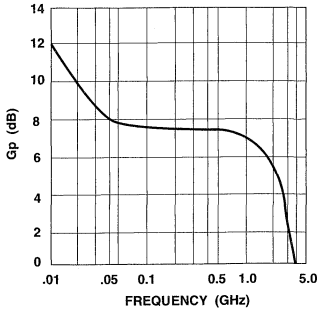


Figure 5. Gain vs. Frequency, I_d = 80 to 100 mA.

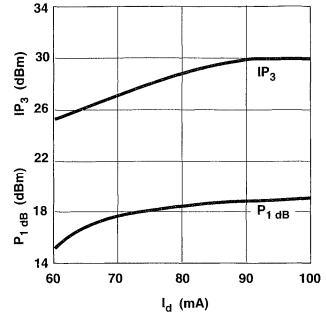
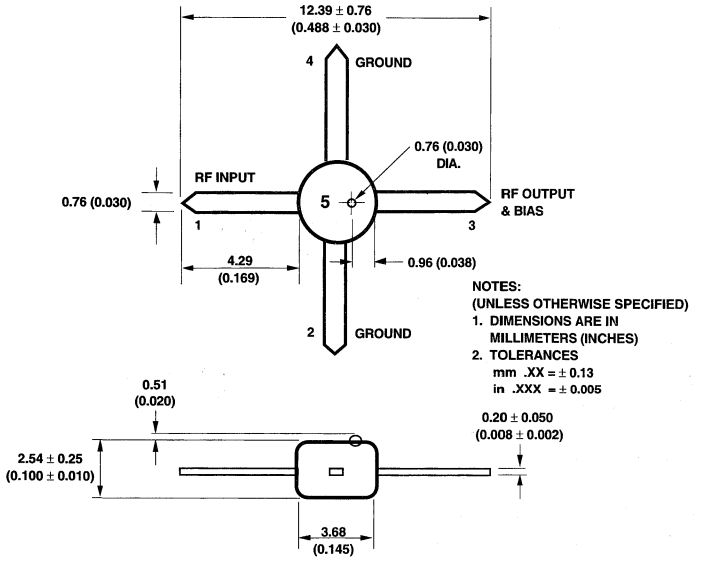


Figure 6. Output Power at 1 dB Gain Compression, Third Order Intercept vs. Current, f = 1.0 GHz.

04A Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES).

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0505

Features

- **Cascadable 50 Ω Gain Block**
- **High Output Power:** 18.0 dBm Typical $P_{1\,dB}$ at 1.0 GHz
- **Low Distortion:** 29.0 dBm Typical IP_3 at 1.0 GHz
- **7.0 dB Typical Gain at 1.0 GHz**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

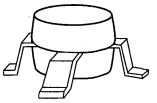
Note:
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."

Description

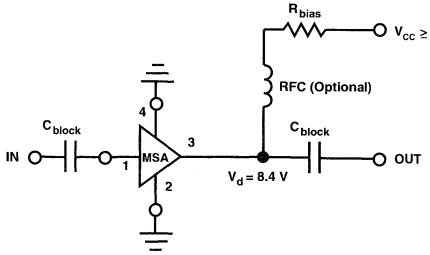
The MSA-0505 is a high performance medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

05 Plastic Package



Typical Biasing Configuration



MSA-0505 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	135 mA
Power Dissipation[2,3]	1.5 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
$\theta_{jc} = 85°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 11.8 mW/°C for $T_C > 73°C$.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], $T_A = 25°C$

Symbol	Parameters and Test Conditions: $I_d = 80$ mA, $Z_O = 50\ \Omega$		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz f = 1.0 GHz	dBm dBm	 16.0	19.0 18.0	
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz f = 1.0 GHz	dB	 6.0	7.5 7.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.5 GHz	dB		±0.75	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.3	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.6:1	
	Output VSWR	f = 0.1 to 1.5 GHz			2.0:1	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		29.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
t_D	Group Delay	f = 1.0 GHz	psec		190	
V_d	Device Voltage		V	6.7	8.4	10.1
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16.0	

Notes:
1. The recommended operating current range for this device is 60 to 100 mA. Typical performance as a function of current is on the following page.
2. Referenced from 0.1 GHz Gain (G_P).

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0505-TR1	500	7" Reel
MSA-0505-STR	10	Strip

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0505 Typical Scattering Parameters (T_A = 25°C, I_d = 80 mA)

Freq. MHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
5	.56	–39	14.9	5.56	161	–18.5	.120	39	.65	–36	0.60
25	.24	–103	9.7	3.05	156	–13.9	.202	12	.25	–90	0.97
50	.15	–130	8.2	2.57	163	–13.7	.207	7	.15	–116	1.15
100	.13	–155	7.8	2.45	165	–13.7	.207	3	.11	–132	1.21
200	.12	–170	7.7	3.43	161	–13.5	.211	1	.11	–145	1.21
400	.12	178	7.5	2.37	148	–13.6	.209	–1	.14	–146	1.23
600	.13	172	7.4	2.34	134	–13.6	.209	–2	.17	–151	1.23
800	.13	168	7.2	2.29	119	–13.6	.209	–3	.21	–157	1.23
1000	.14	166	7.0	2.24	105	–13.4	.213	–4	.25	–164	1.21
1500	.21	159	6.4	2.09	72	–13.3	.217	–6	.34	176	1.16
2000	.30	148	5.2	1.82	42	–13.1	.222	–9	.42	159	1.12
2500	.40	136	4.1	1.60	17	–12.9	.227	–11	.48	146	1.05
3000	.52	121	2.7	1.36	–7	–12.6	.234	–16	.55	133	0.92

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

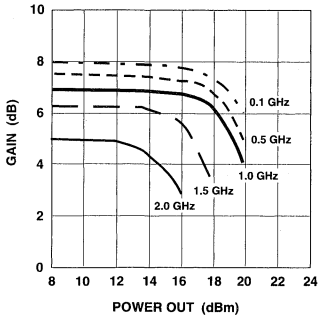


Figure 1. Typical Gain vs. Power Out, T_A = 25°C, I_d = 80 mA.

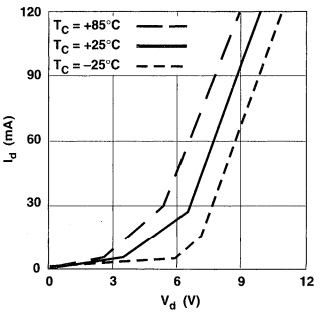


Figure 2. Device Current vs. Voltage.

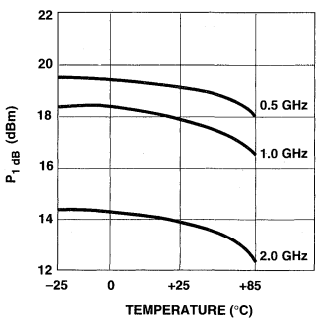


Figure 3. Output Power at 1 dB Gain Compression, vs. Case Temperature, I_d = 80 mA.

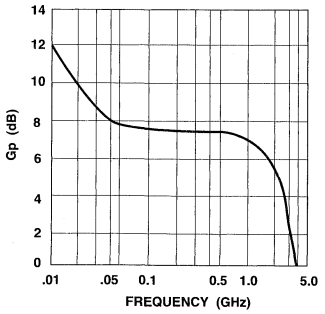


Figure 4. Gain vs. Frequency, I_d = 80 to 100 mA.

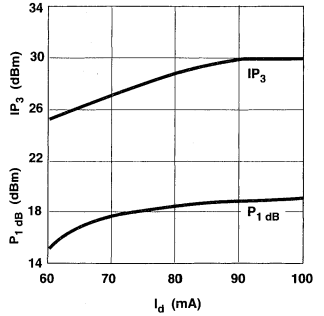
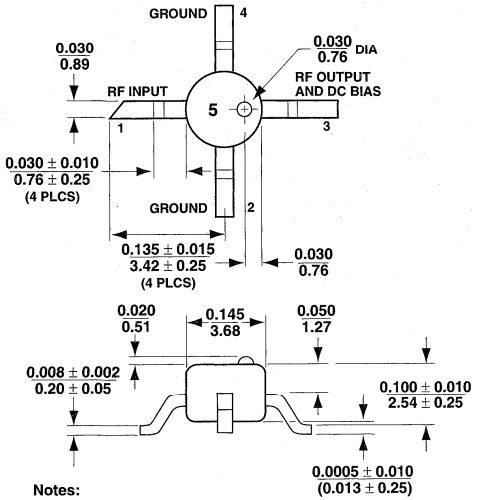


Figure 5. Output Power at 1 dB Gain Compression, Third Order Intercept vs. Case Temperature, f = 1.0 GHz.

05 Plastic Package Dimensions



Notes:
(unless otherwise specified)
1. Dimensions are $\frac{\text{in}}{\text{mm}}$
2. Tolerances
   in .xxx = ± 0.005
   mm .xx = ± 0.13

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0520

Features

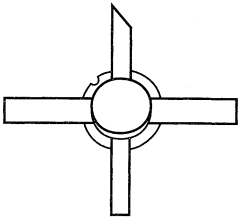
- **Cascadable 50 Ω Gain Block**
- **High Output Power:** +23 dBm Typical $P_{1\,dB}$ at 1.0 GHz
- **Low Distortion:** 33 dBm Typical IP_3 at 1.0 GHz
- **8.5 dB Typical Gain at 1.0 GHz**
- **Hermetic Metal/Beryllia Microstrip Package**

Description

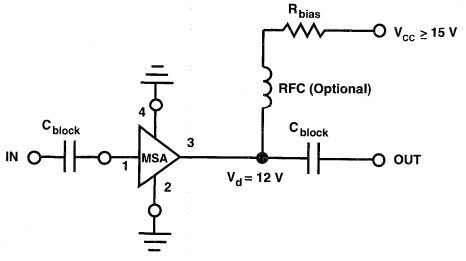
The MSA-0520 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, BeO disk package for good thermal characteristics. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

200 mil BeO Package



Typical Biasing Configuration



MSA-0520 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	225 mA
Power Dissipation[2,3]	3.0 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 25°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 40 mW/°C for T_C > 125°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 165 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm	21.0	23.0	
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	7.5	8.5	9.5
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.75	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.0 GHz			2.5:1	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		33.0	
$NF_{50\,\Omega}$	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
t_D	Group Delay	f = 1.0 GHz	psec		170	
V_d	Device Voltage		V	10.5	12.0	13.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16.0	

Notes:
1. The recommended operating current range for this device is 80 to 200 mA. Typical performance as a function of current is on the following page.
2. Referenced from 0.1 GHz Gain (G_P).

MSA-0520 Typical Scattering Parameters (T_A = 25°C, I_d = 165 mA)

Freq. MHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
5	.57	–38	14.4	5.25	165	–19.4	.107	38	.67	–35	0.57
25	.25	–90	10.7	3.42	160	–14.9	.180	17	.29	–81	0.93
50	.15	–111	9.5	2.97	163	–14.4	.190	9	.18	–97	1.10
100	.11	–138	8.9	2.80	166	–14.2	.195	3	.11	–113	1.16
200	.10	–152	8.8	2.75	163	–14.1	.197	1	.10	–125	1.17
400	.10	–152	8.7	2.72	152	–14.1	.198	–2	.14	–123	1.16
600	.11	–147	8.6	2.70	140	–14.0	.199	–4	.18	–123	1.14
800	.13	–142	8.5	2.67	128	–14.1	.199	–6	.22	–127	1.12
1000	.15	–140	8.4	2.64	115	–14.1	.198	–8	.27	–131	1.09
1500	.22	–142	8.0	2.52	85	–13.7	.206	–12	.34	–143	0.98
2000	.30	–156	7.4	2.36	55	–13.3	.216	–16	.43	–158	0.85
2500	.37	–170	6.7	2.16	33	–12.9	.227	–18	.48	–166	0.75
3000	.41	170	5.6	1.91	8	–12.7	.232	–23	.51	–177	0.70
3500	.45	149	4.5	1.68	–16	–12.1	.249	–31	.55	173	0.63
4000	.46	124	3.3	1.45	–40	–11.7	.259	–39	.56	162	0.66

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

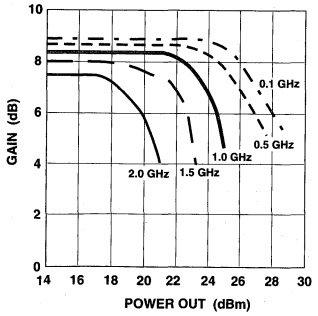


Figure 1. Typical Gain vs. Power Out, T_A = 25°C, I_d = 165 mA.

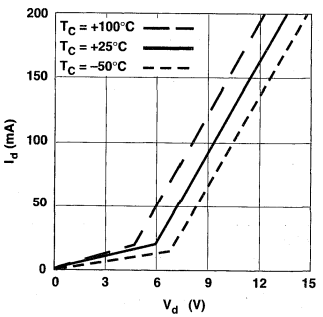


Figure 2. Device Current vs. Voltage.

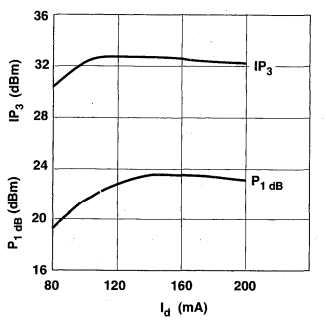


Figure 3. Output Power at 1 dB Gain Compression, Third Order Intercept vs. Current, f = 1.0 GHz.

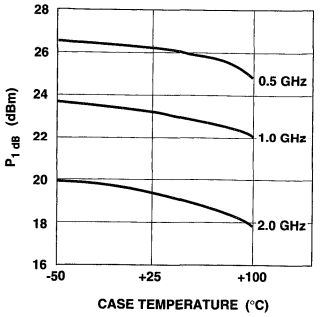


Figure 4. Output Power @ 1 dB Gain Compression vs. Temperature, I_d = 165 mA.

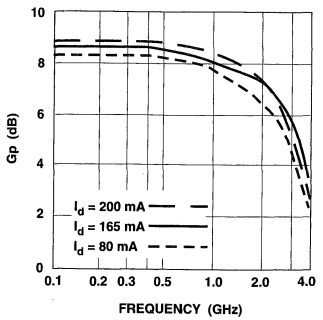


Figure 5. Gain vs. Frequency.

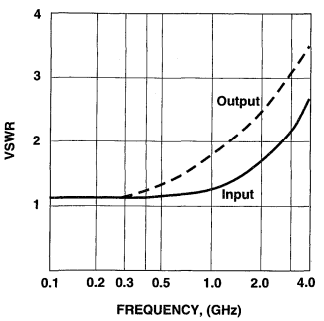
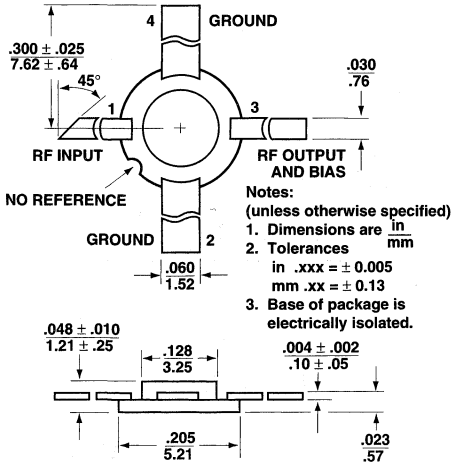


Figure 6. VSWR vs. Frequency, I_d = 165 mA.

200 mil BeO Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0600

Features

- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (3.5 V typical V_d)**
- **3 dB Bandwidth:** DC to 1.0 GHz
- **High Gain:** 19.5 dB Typical at 0.5 GHz
- **Low Noise Figure:** 2.8 dB Typical at 0.5 GHz

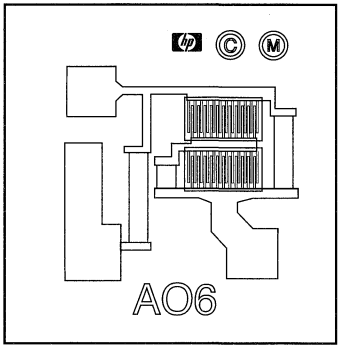
Description

The MSA-0600 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1] See APPLICATIONS section, "Chip Use".

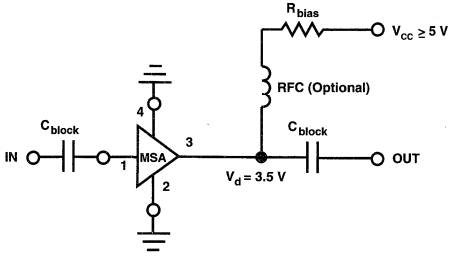
Chip Outline[1]



Note:

1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



MSA-0600 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 50°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 20 mW/°C for $T_{Mounting\ Surface}$ > 190°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		20.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±0.7	
$f_{3\ dB}$	3 dB Bandwidth		GHz		1.0	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.9:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.8:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.8	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.5	
t_D	Group Delay	f = 0.5 GHz	psec		200	
V_d	Device Voltage		V	3.1	3.5	3.9
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 12 to 30 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0600-GP4	100

MSA-0600 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 16 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.05	–148	20.6	10.66	173	–23.3	.068	4	.05	–67	1.05
0.2	.07	–134	20.4	10.48	166	–23.1	.070	8	.09	–91	1.04
0.3	.09	–125	20.2	10.28	159	–22.6	.074	13	.13	–102	1.01
0.4	.11	–121	20.0	10.01	151	–22.4	.076	15	.16	–110	1.00
0.5	.13	–120	19.7	9.71	145	–22.1	.078	17	.20	–117	0.98
0.6	.15	–119	19.4	9.34	140	–21.8	.081	20	.22	–124	0.97
0.8	.19	–121	18.7	8.60	123	–20.7	.092	25	.25	–136	0.93
1.0	.25	–123	17.9	7.82	117	–19.8	.102	26	.28	–148	0.90
1.5	.32	–134	15.7	6.10	96	–18.3	.122	29	.29	–168	0.89
2.0	.40	–149	13.5	4.73	79	–17.4	.136	27	.26	175	0.91
2.5	.45	–157	11.6	3.79	70	–16.9	.142	30	.23	169	0.97
3.0	.49	–171	9.9	3.12	61	–16.6	.148	28	.19	168	1.03
3.5	.51	–174	8.3	2.60	51	–16.4	.152	25	.16	173	1.10
4.0	.51	179	6.9	2.21	43	–16.3	.153	26	.12	–170	1.22
4.5	.51	170	5.7	1.93	37	–16.0	.159	24	.10	–149	1.31
5.0	.51	162	4.7	1.71	29	–15.9	.161	24	.11	–126	1.41

Note:

1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

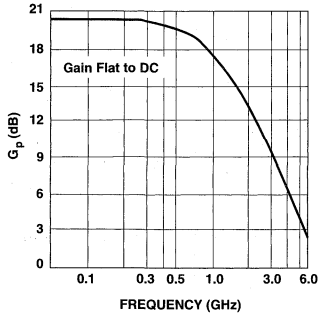


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 16 mA.

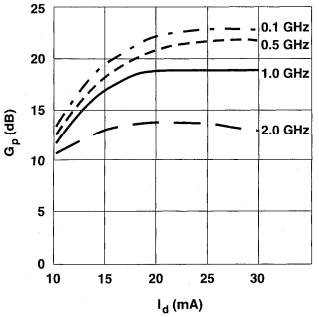


Figure 2. Power Gain vs. Current.

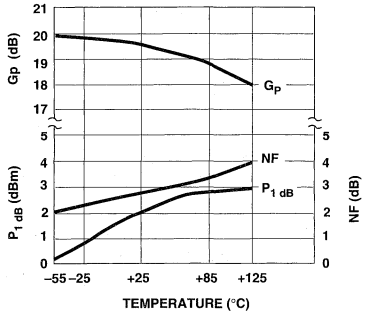


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 0.5 GHz, I_d = 16 mA.

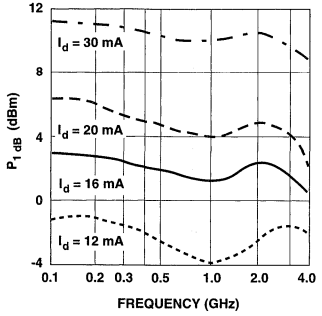


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

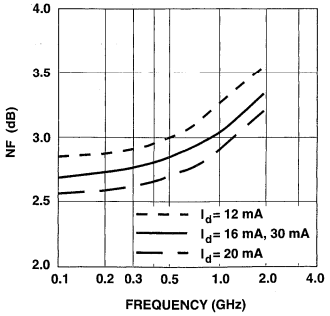
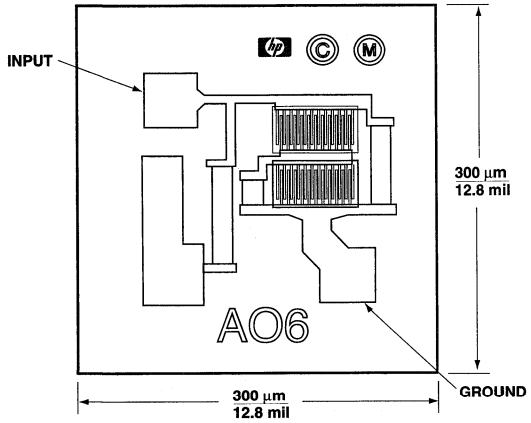


Figure 5. Noise Figure vs. Frequency.

MSA-0600 Chip Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0611

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 0.7 GHz
- **High Gain:** 18.0 dB Typical at 0.5 GHz
- **Low Noise Figure:** 3.0 dB Typical at 0.5 GHz
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

Note:

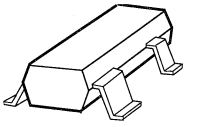
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices".

Description

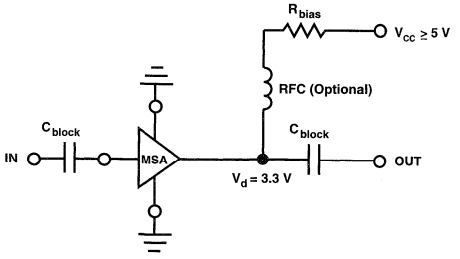
The MSA-0611 is a low cost silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in the surface mount plastic SOT-143 package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

SOT-143 Package



Typical Biasing Configuration



MSA-0611 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	125 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 505°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 2.0 mW/°C for T_C > 87°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz	dB	 16.0	19.5 18.0	
ΔG_P	Gain Flatness	f = 0.1 to 0.5 GHz	dB		±0.8	
$f_{3\,dB}$	3 dB Bandwidth		GHz		0.7	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.6:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec		225	
V_d	Device Voltage	T_C = 25°C	V	2.6	3.3	4.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 12 to 20 mA. Typical gain performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0611-TR1	3000	7" Reel
MSA-0611-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0611 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 16 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.04	–176	19.6	9.53	170	–23.0	.071	6	.04	–57	1.07
0.2	.03	–163	19.3	9.25	160	–22.7	.073	10	.07	–82	1.07
0.3	.03	–149	18.9	8.79	150	–22.8	.072	14	.09	–97	1.10
0.4	.04	–132	18.5	8.38	141	–21.9	.080	17	.11	–111	1.07
0.5	.05	–127	18.0	7.96	133	–21.6	.083	21	.13	–122	1.07
0.6	.07	–123	17.3	7.33	125	–21.2	.087	23	.15	–131	1.07
0.8	.10	–129	16.2	6.46	111	–19.7	.103	25	.17	–147	1.04
1.0	.13	–139	15.0	5.64	98	–19.0	.112	28	.18	–160	1.06
1.5	.22	–164	12.5	4.22	73	–17.1	.139	25	.19	175	1.07
2.0	.31	171	10.1	3.20	53	–16.1	.157	21	.19	160	1.13
2.5	.39	158	8.1	2.55	42	–15.4	.169	22	.20	153	1.19
3.0	.45	144	6.3	2.07	28	–15.0	.178	18	.19	150	1.26
3.5	.50	132	4.7	1.72	16	–14.6	.185	15	.16	152	1.33
4.0	.52	121	3.4	1.48	4	–14.1	.197	11	.14	166	1.37

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

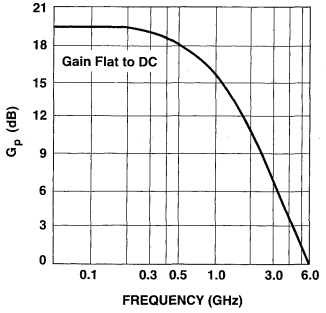


Figure 1. Power Gain vs. Frequency, T_A = 25°C, I_d = 16 mA.

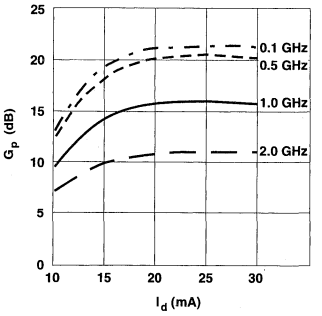


Figure 2. Power Gain vs. Current.

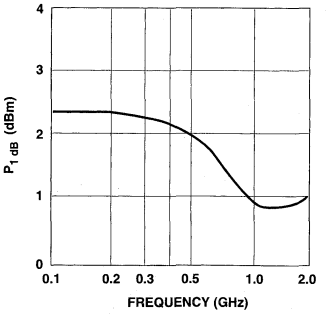


Figure 3. Output Power @ 1 dB Gain Compression vs. Frequency, I_d = 16 mA.

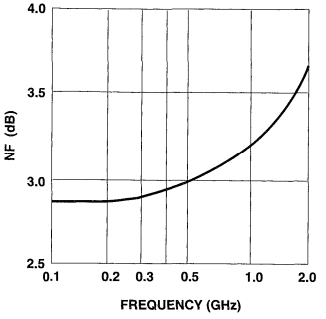
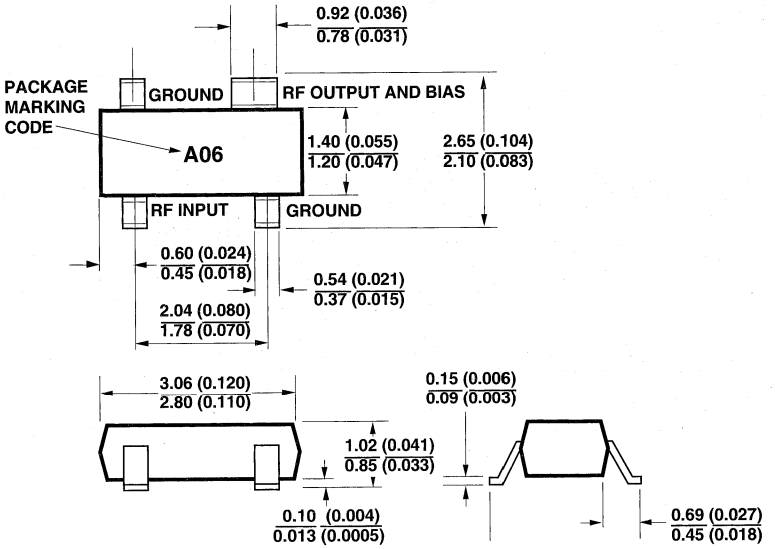


Figure 4. Noise Figure vs. Frequency, I_d = 16 mA.

SOT-143 Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifiers

Technical Data

MSA-0635, -0636

Features

- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage:** 3.5 V Typical V_d
- **3 dB Bandwidth:** DC to 0.9 GHz
- **High Gain:** 19.0 dB Typical at 0.5 GHz
- **Low Noise Figure:** 2.8 dB Typical at 0.5 GHz
- **Cost Effective Ceramic Microstrip Package**

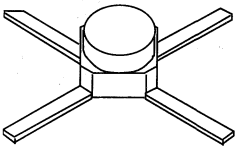
Description

The MSA-0635 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Available in cut lead version (package 36) as MSA-0636.

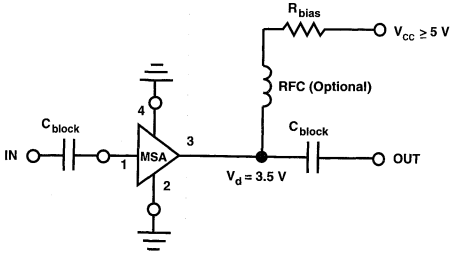
35 micro-X Package[1]



Note:

1. Short leaded 36 package available upon request.

Typical Biasing Configuration



MSA-0635, -0636 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65 to 200°C

Thermal Resistance[2,5]:
θ_{jc} = 155°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.5 mW/°C for T_C > 169°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	19.0	20.5	22.0
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.7	±1.0
$f_{3\ dB}$	3 dB Bandwidth		GHz		0.9	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.4:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.3:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.8	4.0
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.5	
t_D	Group Delay	f = 0.5 GHz	psec		200	
V_d	Device Voltage		V	3.1	3.5	3.9
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 12 to 30 mA. Typical performance as a function of current is on the following page.

MSA-0635, -0636 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 16 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.03	–178	20.5	10.59	171	–23.4	.068	5	.04	–44	1.05
0.2	.02	–177	20.3	10.31	161	–22.9	.071	8	.05	–68	1.04
0.3	.02	–164	20.0	9.96	152	–22.4	.076	14	.06	–87	1.04
0.4	.02	–116	19.6	9.55	144	–22.0	.079	19	.07	–104	1.03
0.5	.02	–100	19.2	9.08	136	–21.8	.081	21	.09	–114	1.04
0.6	.04	–89	18.7	8.59	128	–21.3	.086	24	.09	–123	1.04
0.8	.07	–96	17.7	7.66	115	–20.2	.098	29	.10	–140	1.03
1.0	.10	–108	16.6	6.79	103	–19.4	.107	31	.11	–156	1.02
1.5	.17	–134	14.2	5.13	79	–17.2	.138	30	.12	172	1.03
2.0	.24	–160	12.1	4.01	60	–15.8	.163	26	.12	148	1.04
2.5	.31	–178	10.3	3.26	48	–15.1	.175	27	.12	140	1.08
3.0	.37	166	8.7	2.72	34	–14.4	.190	24	.11	135	1.10
3.5	.42	151	7.4	2.33	21	–13.9	.203	19	.10	144	1.11
4.0	.46	139	6.2	2.04	9	–13.3	.216	16	.08	167	1.11
4.5	.48	126	5.1	1.81	–3	–12.8	.229	12	.08	–173	1.11
5.0	.52	110	4.2	1.62	–15	–12.2	.245	8	.09	–173	1.09

Note:
1. A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

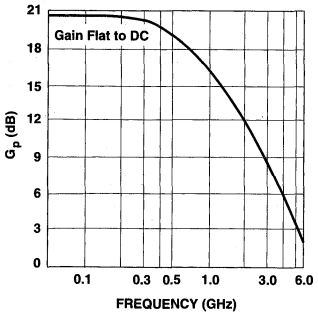


Figure 1. Typical Power Gain vs. Frequency, I_d = 16 mA.

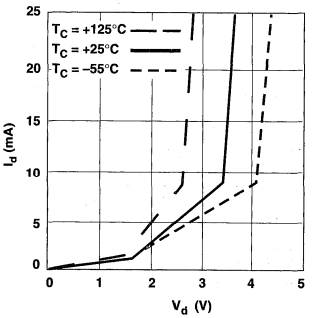


Figure 2. Device Current vs. Voltage.

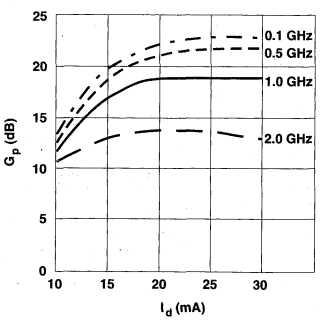


Figure 3. Power Gain vs. Current.

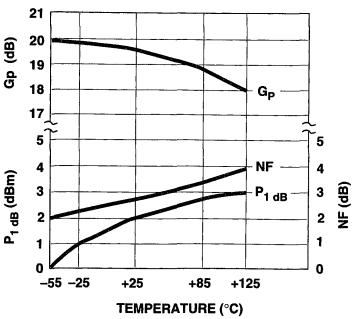


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 16 mA.

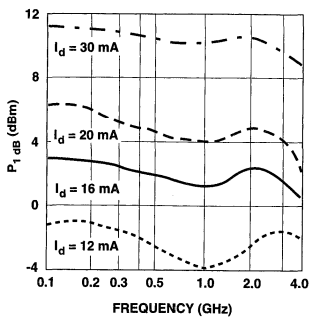


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

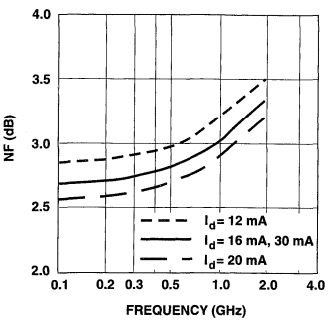
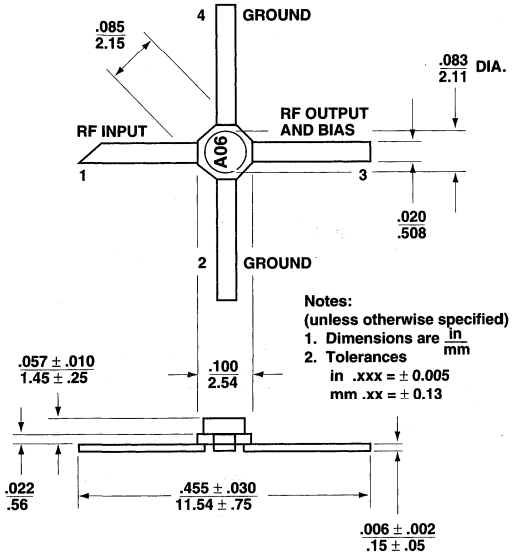


Figure 6. Noise Figure vs. Frequency.

35 micro-X Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0670

Features

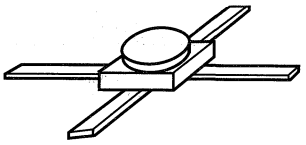
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage:** 3.5 V Typical V_d
- **3 dB Bandwidth:** DC to 1.0 GHz
- **High Gain:** 19.5 dB Typical at 0.5 GHz
- **Low Noise Figure:** 2.8 dB Typical at 0.5 GHz
- **Hermetic Gold-ceramic Microstrip Package**

Description

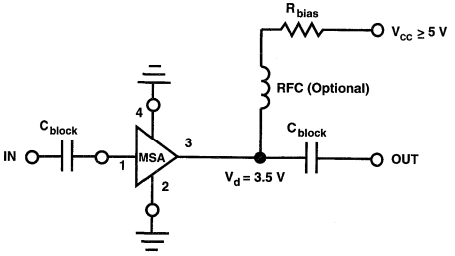
The MSA-0670 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package



Typical Biasing Configuration



MSA-0670 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 130°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.7 mW/°C for T_C > 174°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	19.0	20.5	22.0
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±0.7	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.0	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.9:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.8:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.8	4.0
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.5	
t_D	Group Delay	f = 0.5 GHz	psec		200	
V_d	Device Voltage		V	3.1	3.5	3.9
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 12 to 30 mA. Typical performance as a function of current is on the following page.

MSA-0670 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 16 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.05	–147	20.5	10.62	172	–23.3	.068	4	.05	–69	1.05
0.2	.07	–134	20.4	10.41	164	–23.0	.070	8	.09	–92	1.04
0.3	.09	–126	20.1	10.16	156	–22.6	.074	12	.13	–104	1.02
0.4	.11	–123	19.9	9.85	148	–22.4	.076	14	.16	–113	1.00
0.5	.13	–123	19.6	9.50	141	–22.0	.079	26	.20	–121	0.99
0.6	.15	–123	19.2	9.09	135	–21.3	.082	18	.22	–128	0.97
0.8	.19	–126	17.4	8.28	122	–20.7	.093	22	.25	–141	0.94
1.0	.24	–129	16.5	7.46	110	–19.8	.103	22	.27	–154	0.92
1.5	.31	–141	15.2	5.76	87	–18.2	.124	23	.27	–176	0.91
2.0	.38	–157	13.0	4.47	68	–17.2	.138	19	.24	166	0.94
2.5	.42	–167	11.1	3.59	57	–16.7	.146	20	.21	158	1.01
3.0	.46	178	9.5	2.97	45	–16.4	.152	16	.17	156	1.07
3.5	.48	173	7.9	2.49	33	–16.2	.155	11	.14	163	1.15
4.0	.48	164	6.6	2.13	22	–16.1	.156	9	.11	–175	1.27
4.5	.48	155	5.5	1.87	13	–15.9	.161	5	.11	–154	1.35
5.0	.48	143	4.5	1.67	3	–15.8	.163	3	.14	–141	1.46

Note:
1. A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C
(unless otherwise noted)

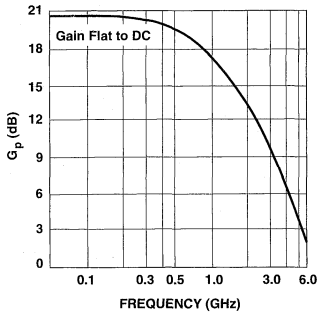


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 16 mA.

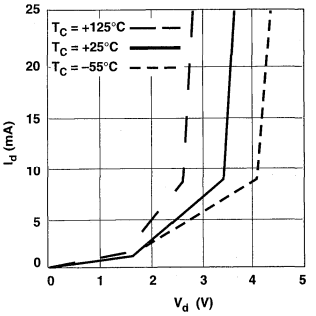


Figure 2. Device Current vs. Voltage.

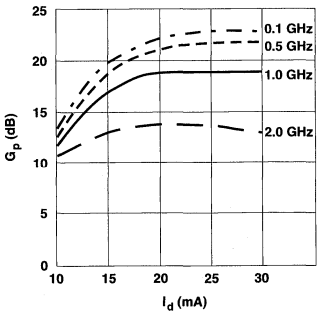


Figure 3. Power Gain vs. Current.

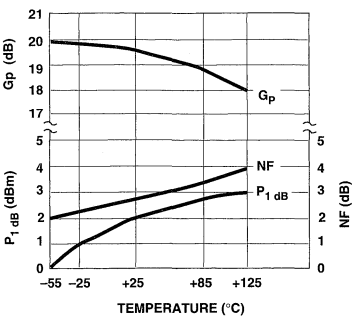


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 16 mA.

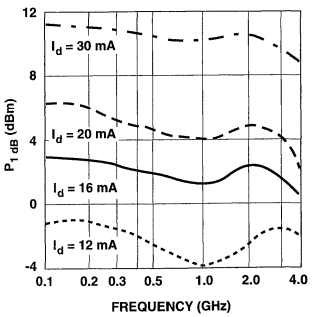


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

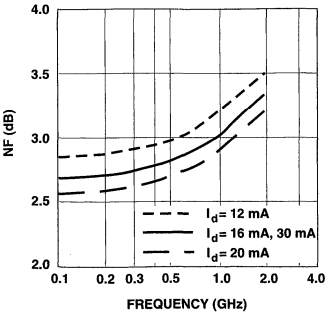
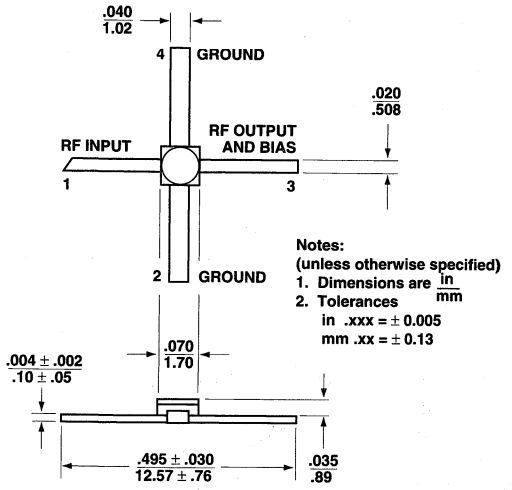


Figure 6. Noise Figure vs. Frequency.

70 mil Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0685

Features

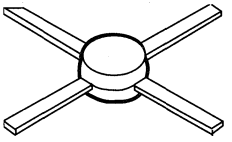
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage:** 3.5 V Typical V_d
- **3 dB Bandwidth:** DC to 0.8 GHz
- **High Gain:** 18.5 dB Typical at 0.5 GHz
- **Low Noise Figure:** 3.0 dB Typical at 0.5 GHz
- **Low Cost Plastic Package**

Description

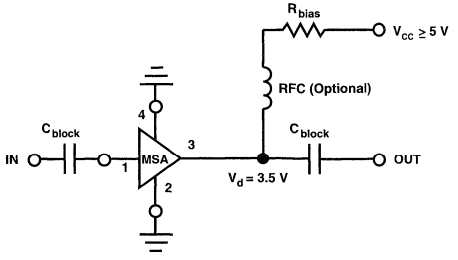
The MSA-0685 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package



Typical Biasing Configuration



MSA-0685 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 110°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 9.1 mW/°C for T_C > 128°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		20.0	
		f = 0.5 GHz		17.0	18.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.5 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		0.8	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.5:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.4:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.5	
t_D	Group Delay	f = 0.5 GHz	psec		200	
V_d	Device Voltage		V	2.8	3.5	4.2
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note:
1. The recommended operating current range for this device is 12 to 25 mA. Typical performance as a function of current is on the following page.

MSA-0685 Typical Scattering Parameters (Z = 50 Ω, T_A = 25°C, I_d = 16 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.1	.04	171	20.1	10.09	171	-22.5	.075	5	.04	-30	1.04
0.2	.02	-180	29.8	9.75	161	-22.4	.076	10	.05	-56	1.04
0.3	.02	-143	19.4	9.38	153	-22.2	.077	15	.07	-76	1.05
0.4	.03	-113	19.1	8.99	145	-21.8	.081	17	.08	-91	1.04
0.5	.05	-105	18.7	8.57	138	-21.3	.086	21	.10	-104	1.04
0.6	.07	-101	18.2	8.14	131	-20.7	.092	25	.11	-116	1.03
0.8	.10	-111	17.3	7.32	119	-19.7	.103	28	.13	-134	1.01
1.0	.13	-118	16.4	6.57	107	-18.8	.115	28	.14	-150	0.99
1.5	.21	-140	14.1	5.06	84	-17.1	.140	28	.15	180	1.00
2.0	.29	-163	12.0	3.98	65	-15.8	.163	26	.16	157	1.02
2.5	.34	-176	10.3	3.26	55	-15.2	.174	28	.16	150	1.06
3.0	.41	169	8.7	2.71	42	-14.8	.181	25	.15	143	1.10
3.5	.46	157	7.2	2.31	30	-14.2	.194	22	.13	144	1.11
4.0	.49	146	6.1	2.01	18	-13.8	.203	20	.10	156	1.13
4.5	.52	135	5.0	1.77	7	-13.4	.215	17	.09	173	1.14
5.0	.54	123	4.1	1.60	-3	-12.9	.226	15	.09	-178	1.14

Note:
1. A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

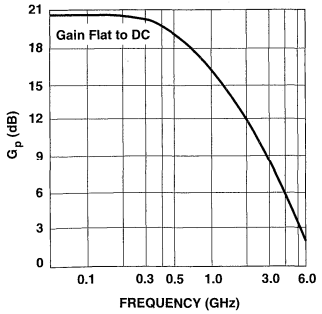


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C, I_d = 16 mA.

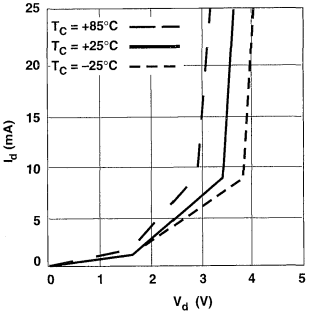


Figure 2. Device Current vs. Voltage.

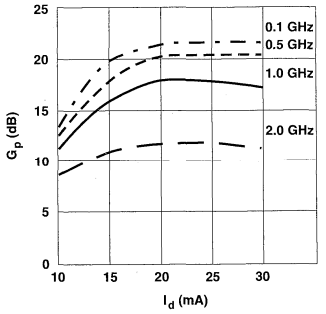


Figure 3. Power Gain vs. Current.

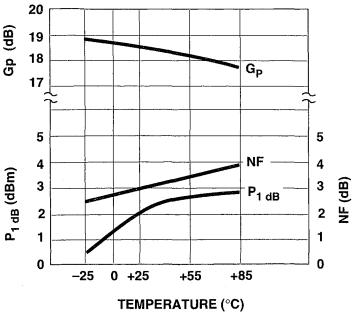


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 16 mA.

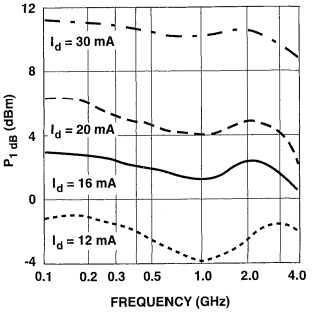


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

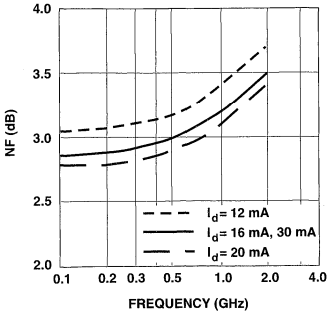
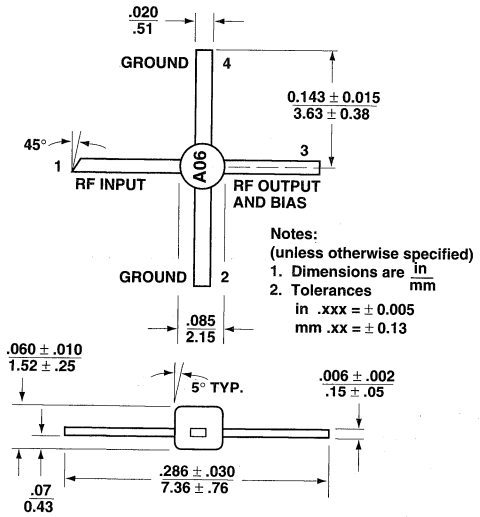


Figure 6. Noise Figure vs. Frequency.

85 Plastic Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0686

Features

- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage:** 3.5 V Typical V_d
- **3 dB Bandwidth:** DC to 0.8 GHz
- **High Gain:** 18.5 dB Typical at 0.5 GHz
- **Low Noise Figure:** 3.0 dB Typical at 0.5 GHz
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Available**[1]

Note:

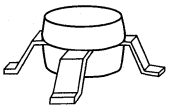
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Description

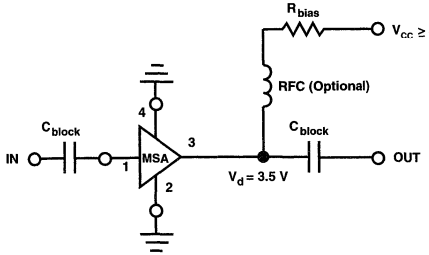
The MSA-0686 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

86 Plastic Package



Typical Biasing Configuration



MSA-0686 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 120°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 8.3 mW/°C for T_C > 126°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		20.0	
		f = 0.5 GHz		16.5	18.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.5 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		0.8	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.7:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.5	
t_D	Group Delay	f = 0.5 GHz	psec		225	
V_d	Device Voltage		V	2.8	3.5	4.2
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 12 to 20 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0686-TR1	1000	7" Reel
MSA-0686-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0686 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 16 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.1	.06	–175	20.1	10.08	170	–23.3	.069	4	.04	–84	1.05
0.2	.06	–169	19.8	9.77	161	–23.2	.069	8	.07	–103	1.05
0.3	.07	–164	19.4	9.35	152	–22.5	.075	13	.10	–113	1.03
0.4	.08	–158	19.1	8.98	144	–22.2	.078	16	.13	–123	1.02
0.5	.08	–154	18.7	8.58	135	–21.6	.083	18	.15	–131	1.01
0.6	.09	–152	18.0	7.94	128	–21.1	.088	21	.18	–140	1.01
0.8	.12	–152	17.2	7.25	114	–20.3	.097	25	.21	–155	1.00
1.0	.15	–154	16.3	6.51	102	–19.5	.106	25	.24	–168	0.99
1.5	.25	–171	14.0	5.01	76	–17.6	.133	22	.27	165	0.99
2.0	.34	171	11.9	3.94	56	–16.1	.157	19	.27	147	1.01
2.5	.43	155	9.8	3.09	42	–15.9	.161	16	.27	134	1.06
3.0	.49	140	8.0	2.51	28	–15.3	.171	11	.26	124	1.10
3.5	.56	128	6.4	2.09	15	–15.1	.175	6	.25	118	1.13
4.0	.61	118	5.0	1.78	3	–14.9	.180	3	.24	115	1.15
5.0	.70	99	2.4	1.32	–18	–14.7	.185	–2	.24	118	1.16

Note:
1. A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C
(unless otherwise noted)

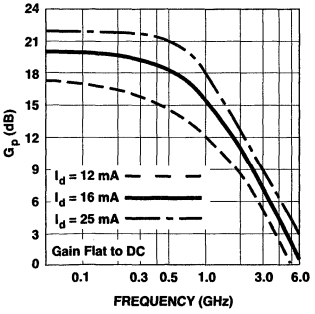


Figure 1. Typical Power Gain vs. Frequency, T_A = 25°C.

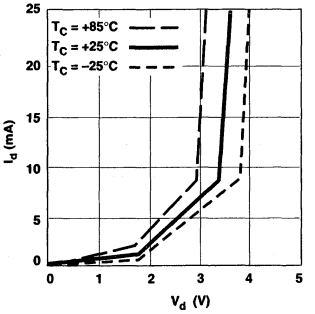


Figure 2. Device Current vs. Voltage.

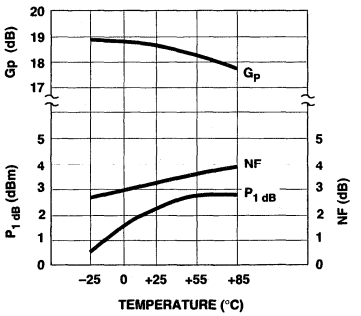


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 16 mA.

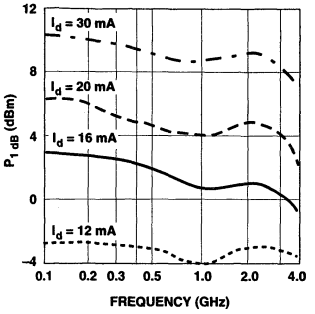


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

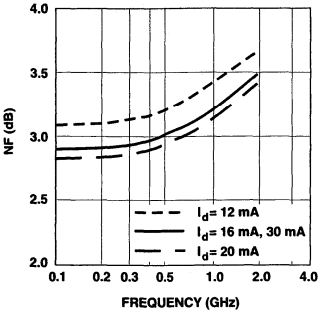
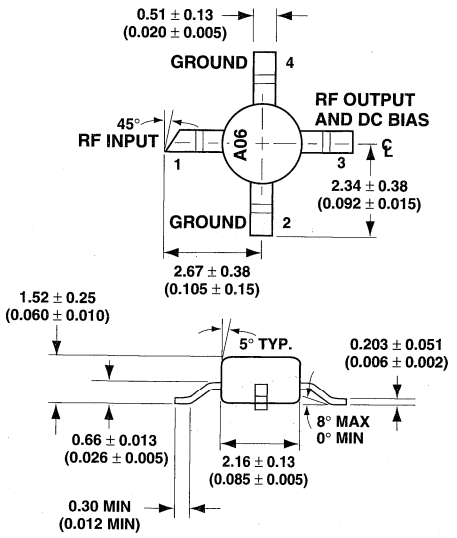


Figure 5. Noise Figure vs. Frequency.

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifiers

Technical Data

MSA-0700

Features

- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage:** 4.0 V Typical V_d
- **3 dB Bandwidth:** DC to 2.5 GHz
- **13.0 dB Typical Gain at 1.0 GHz**

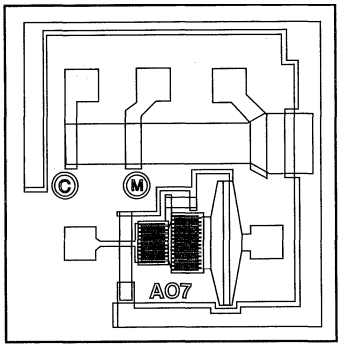
Description

The MSA-0700 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1] See APPLICATIONS section, "Chip Use".

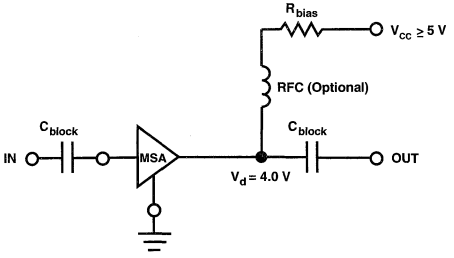
Chip Outline[1]



Note:

1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



MSA-0700 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	275 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
$\theta_{jc} = 50°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface} = 25°C$.
3. Derate at 20 mW/°C for $T_{Mounting\ Surface} > 186°C$.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], $T_A = 25°C$

Symbol	Parameters and Test Conditions[2]: $I_d = 22$ mA, $Z_O = 50\ \Omega$		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		13.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.5 GHz	dB		±0.6	
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.6:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		4.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		5.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		19.0	
t_D	Group Delay	f = 1.0 GHz	psec		130	
V_d	Device Voltage		V	3.6	4.0	4.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–7.0	

Notes:
1. The recommended operating current range for this device is 15 to 40 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0700-GP4	up to 100

MSA-0700 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 22 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.04	–5	13.5	4.75	176	–18.6	.118	2	.20	–9	1.14
0.2	.05	–8	13.5	4.74	172	–18.4	.120	3	.19	–16	1.14
0.4	.06	–19	13.5	4.74	163	–18.3	.121	7	.20	–30	1.13
0.6	.08	–32	13.5	4.71	156	–18.1	.124	9	.21	–44	1.12
0.8	.10	–41	13.4	4.67	147	–17.5	.133	12	.23	–69	1.07
1.0	.12	–50	13.2	4.59	138	–17.6	.133	13	.23	–68	1.07
1.5	.20	–73	12.7	4.30	117	–16.6	.147	17	.23	–91	1.01
2.0	.31	–98	12.1	4.05	97	–15.8	.163	17	.22	–105	0.94
2.5	.38	–112	11.0	3.55	85	–15.3	.171	18	.18	–103	0.93
3.0	.43	–128	9.6	3.01	69	–15.3	.171	17	.19	–96	0.97
3.5	.48	–141	8.2	2.57	56	–15.3	.172	17	.21	–87	1.01
4.0	.48	–153	6.8	2.20	45	–15.2	.174	14	.26	–83	1.07
5.0	.49	–179	4.6	1.70	26	–15.2	.174	12	.31	–86	1.22
6.0	.54	154	2.5	1.34	9	–15.6	.166	13	.33	–98	1.38

Note:
1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

Typical Performance, T_A = 25°C
(unless otherwise noted)

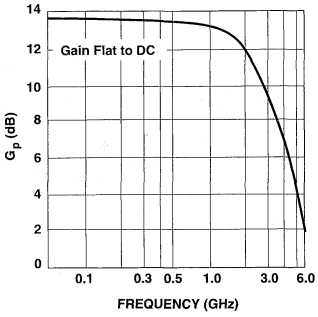


Figure 1. Typical Power Gain vs. Frequency, I_d = 22 mA.

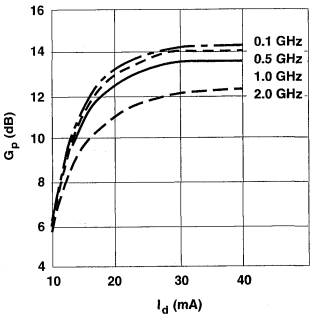


Figure 2. Power Gain vs. Current.

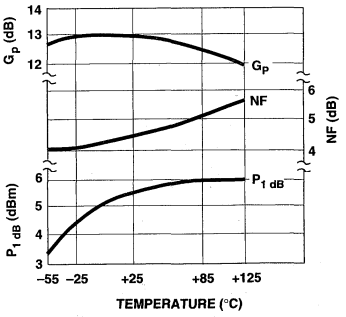


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 1.0 GHz, I_d = 22 mA.

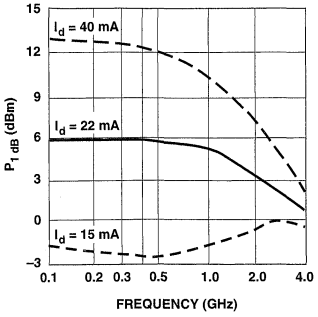


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

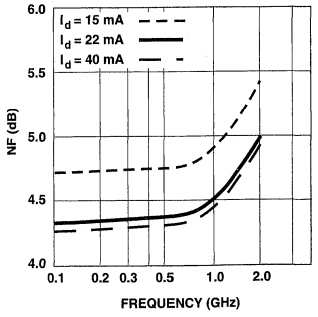
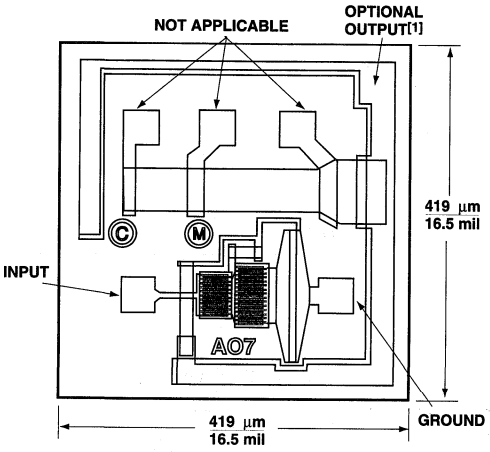


Figure 5. Noise Figure vs. Frequency.

MSA-0700 Chip Dimensions



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils. Chip thickness is 114 µm/4.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side. Note 1: Output contact is made by die attaching the backside of the die.

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0711

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:** DC to 1.9 GHz
- **12.0 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

Note:

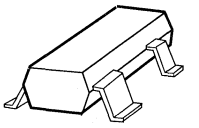
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Description

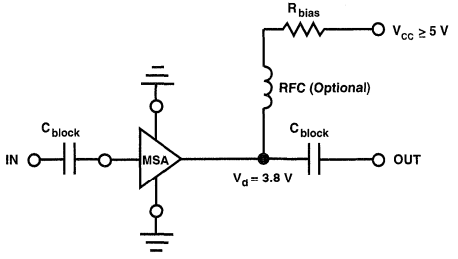
The MSA-0711 is a low cost silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in the surface mount plastic SOT-143 package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

SOT-143 Package



Typical Biasing Configuration



MSA-0711 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	175 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 505°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 2.0 mW/°C for T_C > 62°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.0	13.0 12.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.3 GHz	dB		±0.8	
$f_{3\,dB}$	3 dB Bandwidth		GHz		3.2	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 2.0 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		5.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		5.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		18.0	
t_D	Group Delay	f = 1.0 GHz	psec		145	
V_d	Device Voltage	T_C = 25°C	V	3.0	3.8	4.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–7.0	

Note:
1. The recommended operating current range for this device is 15 to 30 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0711-TR1	3000	7" Reel
MSA-0711-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0711 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 22 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.03	1	13.0	4.47	174	–18.6	.118	1	.19	–8
0.2	.04	1	12.9	4.42	168	–18.5	.119	2	.19	–18
0.4	.04	–4	12.8	4.38	157	–18.4	.120	4	.19	–36
0.6	.05	–19	12.6	4.28	146	–18.1	.125	9	.19	–52
0.8	.07	–32	12.3	4.14	135	–17.7	.130	10	.20	–68
1.0	.08	–44	12.0	3.99	123	–17.4	.135	12	.19	–82
1.5	.13	–88	10.9	3.52	98	–16.1	.157	13	.19	–113
2.0	.18	–130	9.8	3.08	75	–15.2	.173	8	.18	–138
2.5	.25	–155	8.6	2.68	61	–14.7	.184	9	.18	–151
3.0	.32	–178	7.2	2.30	42	–14.7	.185	5	.17	–158
3.5	.38	165	5.8	1.96	26	–14.8	.181	3	.17	–150
4.0	.42	152	4.5	1.68	12	–14.7	.184	1	.20	–142

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

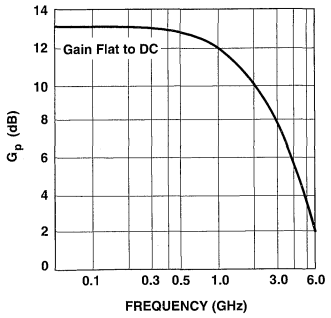


Figure 1. Power Gain vs. Frequency, I_d = 22 mA.

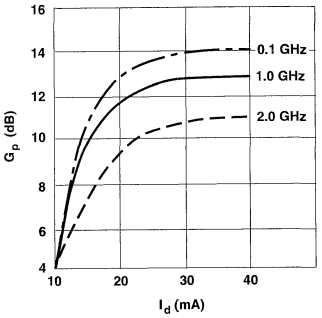


Figure 2. Power Gain vs. Current.

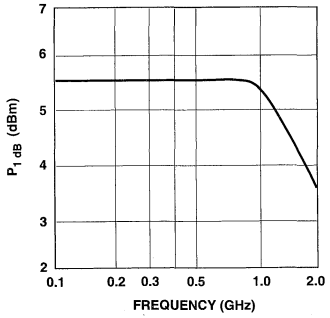


Figure 3. Output Power at 1 dB Gain Compression vs. Frequency, I_d = 22 mA.

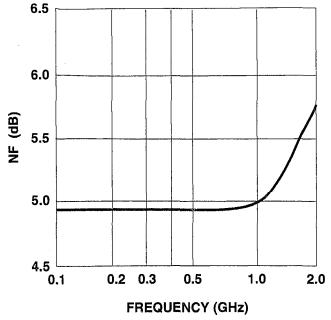
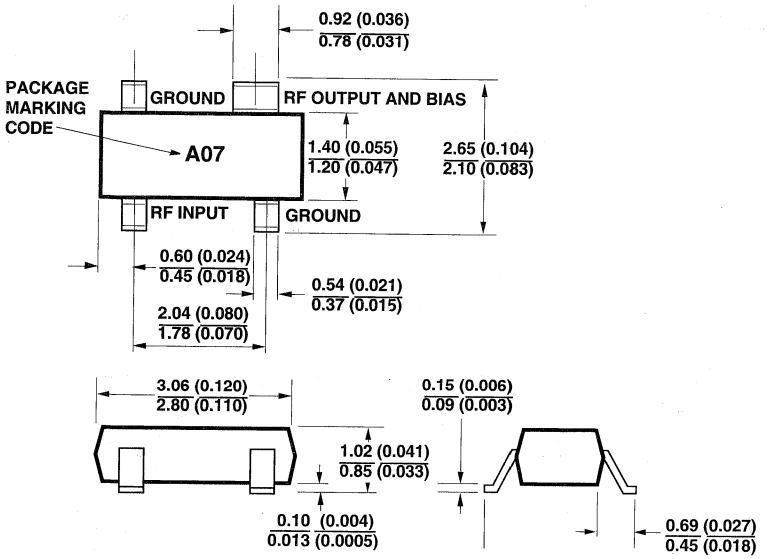


Figure 4. Noise Figure vs. Frequency, I_d = 22 mA.

SOT-143 Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifiers

Technical Data

MSA-0735, -0736

Features

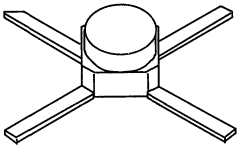
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage:** 4.0 V Typical V_d
- **3 dB Bandwidth:** DC to 2.4 GHz
- **13.0 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Cost Effective Ceramic Microstrip Package**

Description

The MSA-0735 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

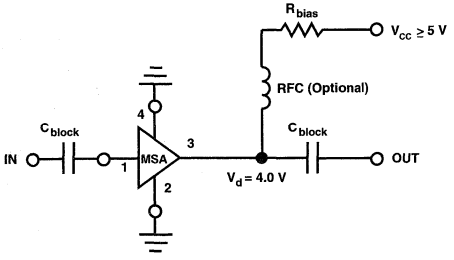
35 micro-X Package[1]



Note:

1. Short leaded 36 package available upon request.

Typical Biasing Configuration



MSA-0735, -0736 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	275 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,5]:
θ_{jc} = 155°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.5 mW/°C for T_C > 157°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. Ths small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	12.5	13.5	14.5
ΔG_P	Gain Flatness	f = 0.1 to 1.3 GHz	dB		±0.6	±1.0
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.4	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.8:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		4.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		5.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		19.0	
t_D	Group Delay	f = 1.0 GHz	psec		140	
V_d	Device Voltage		V	3.6	4.0	4.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–7.0	

Note:
1. The recommended operating current range for this device is 15 to 40 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0735	10	Strip
MSA-0736-BLK	100	Antistatic Bag
MSA-0736-TR1	1000	7" Reel

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0735, -0736 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 22 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.13	–3	13.5	4.71	175	–19.0	.112	2	.29	–7
0.2	.13	–6	13.4	4.69	170	–18.5	.119	3	.29	–12
0.4	.14	–13	13.4	4.68	160	–18.6	.118	6	.29	–24
0.6	.16	–20	13.3	4.64	150	–18.4	.120	7	.28	–35
0.8	.19	–29	13.2	4.60	140	–18.1	.125	8	.28	–47
1.0	.21	–40	12.9	4.42	129	–17.6	.131	10	.27	–58
1.5	.27	–71	12.2	4.07	104	–16.5	.149	10	.24	–83
2.0	.32	–107	11.5	3.74	79	–15.6	.165	7	.19	–103
2.5	.37	–134	10.3	3.26	62	–15.3	.173	5	.15	–113
3.0	.43	–160	8.8	2.76	44	–15.4	.171	0	.14	–120
3.5	.47	–179	7.5	2.37	27	–15.3	.173	–4	.16	–120
4.0	.49	167	6.2	2.05	12	–15.2	.168	–6	.21	–121
5.0	.51	134	4.0	1.59	–15	–15.2	.173	–11	.28	–135
6.0	.60	96	2.1	1.27	–42	–14.6	.185	–16	.29	–167

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

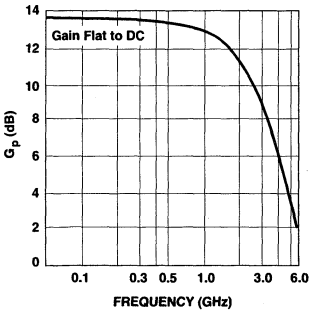


Figure 1. Typical Power Gain vs. Frequency, I_d = 22 mA.

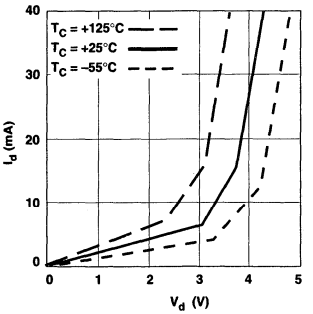


Figure 2. Device Current vs. Voltage.

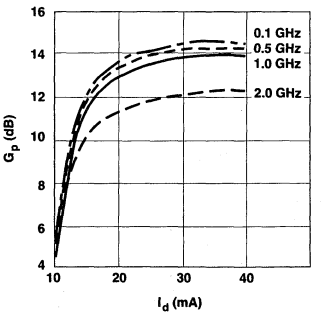


Figure 3. Power Gain vs. Current.

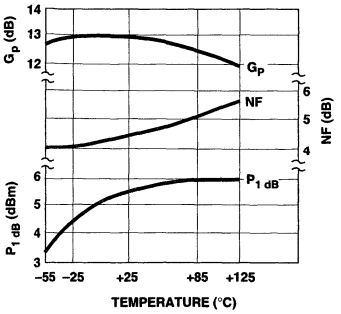


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 22 mA.

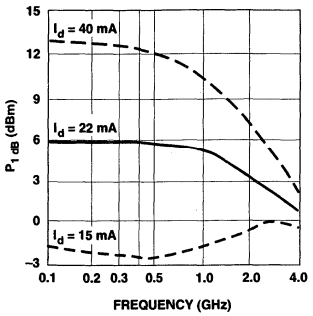


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

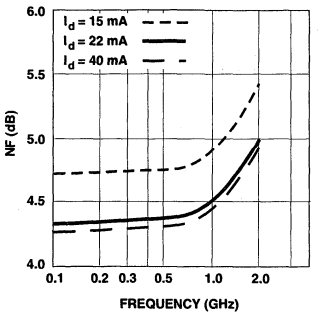
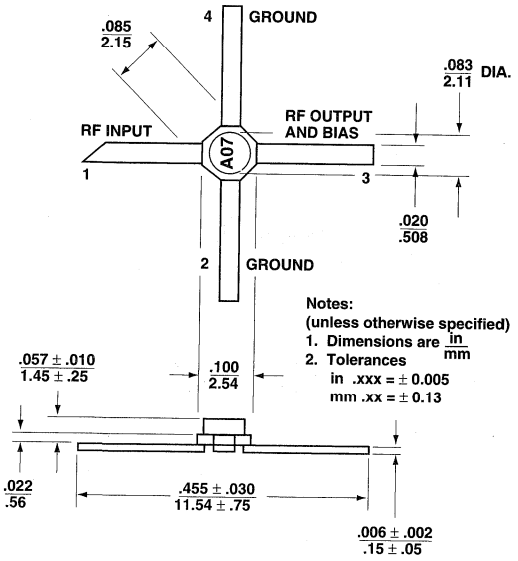


Figure 6. Noise Figure vs. Frequency.

35 micro-X Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0770

Features

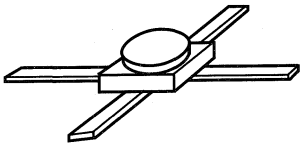
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage:** 4.0 V Typical V_d
- **3 dB Bandwidth:** DC to 2.5 GHz
- **13.0 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic, Gold-ceramic Microstrip Package**

Description

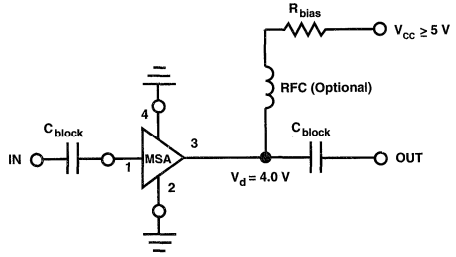
The MSA-0770 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package



Typical Biasing Configuration



MSA-0770 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	275 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 130°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.7 mW/°C for T_C > 164°C.
4. Ths small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	12.5	13.5	14.5
ΔG_P	Gain Flatness	f = 0.1 to 1.5 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.6:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		4.5	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		5.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		19.0	
t_D	Group Delay	f = 1.0 GHz	psec		130	
V_d	Device Voltage		V	3.6	4.0	4.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–7.0	

Note:
1. The recommended operating current range for this device is 15 to 40 mA. Typical performance as a function of current is on the following page.

MSA-0770 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 22 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.04	–7	13.5	4.74	175	–18.6	.118	2	.20	–10
0.2	.05	–11	13.5	4.72	170	–18.4	.120	2	.19	–18
0.4	.06	–24	13.4	4.70	160	–18.4	.121	6	.20	–34
0.6	.08	–38	13.4	4.65	151	–18.1	.124	7	.21	–50
0.8	.10	–48	13.2	4.58	141	–17.8	.133	9	.23	–76
1.0	.12	–58	13.0	4.47	131	–17.5	.133	9	.23	–76
1.5	.20	–82	12.3	4.12	107	–16.6	.148	10	.23	–101
2.0	.30	–107	11.6	3.82	85	–15.7	.163	8	.22	–116
2.5	.37	–123	10.4	3.33	70	–15.3	.171	7	.19	–116
3.0	.42	–140	9.0	2.83	52	–15.4	.170	3	.20	–111
3.5	.46	–154	7.7	2.42	37	–15.4	.170	1	.23	–107
4.0	.47	–167	6.4	2.08	23	–15.5	.169	–4	.29	–107
5.0	.47	163	4.2	1.63	–1	–15.5	.167	–9	.35	–116
6.0	.51	131	2.3	1.30	–23	–15.9	.160	–11	.38	–133

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

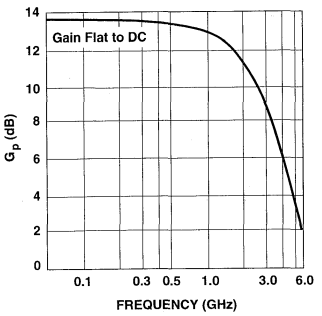


Figure 1. Typical Power Gain vs. Frequency, I_d = 22 mA.

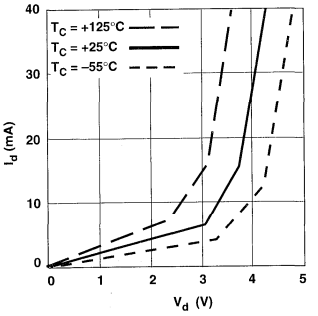


Figure 2. Device Current vs. Voltage.

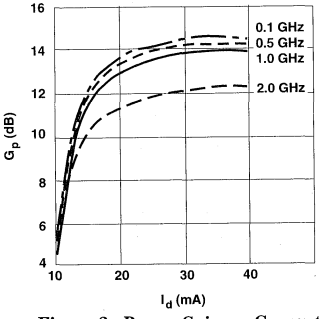


Figure 3. Power Gain vs. Current.

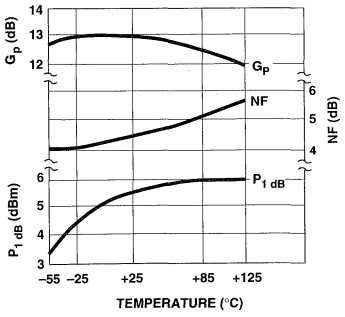


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 22 mA.

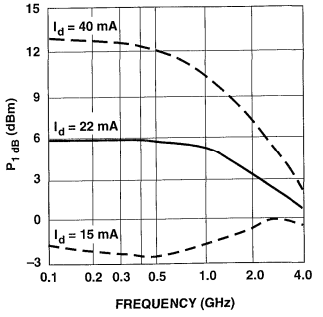


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

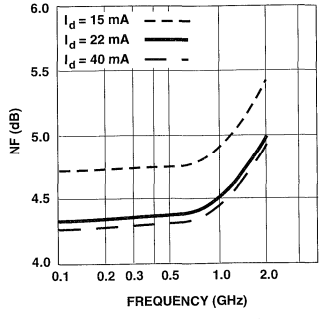
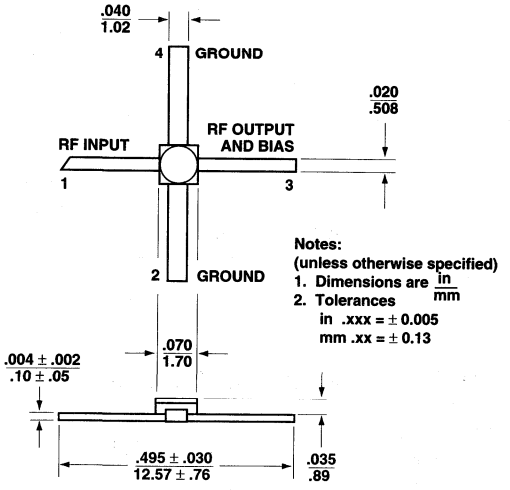


Figure 6. Noise Figure vs. Frequency.

70 mil Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0785

Features

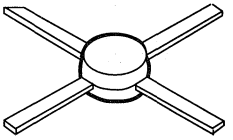
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage:** 4.0 V Typical V_d
- **3 dB Bandwidth:** DC to 2.0 GHz
- **12.5 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

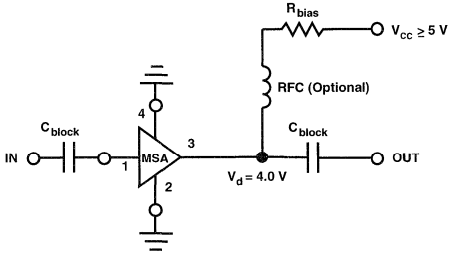
The MSA-0785 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package



Typical Biasing Configuration



MSA-0785 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	275 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 110°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 9.1 mW/°C for T_C > 120°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.5	13.5 12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.3 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.0	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.4:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		5.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		5.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		19.0	
t_D	Group Delay	f = 1.0 GHz	psec		140	
V_d	Device Voltage		V	3.2	4.0	4.8
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–7.0	

Note:
1. The recommended operating current range for this device is 15 to 40 mA. Typical performance as a function of current is on the following page.

MSA-0785 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 22 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.05	166	13.5	4.73	174	–18.4	.120	1	.14	–11
0.2	.05	151	13.4	4.70	169	–18.3	.122	3	.14	–21
0.4	.04	115	13.3	4.63	158	–18.3	.121	6	.14	–40
0.6	.04	65	13.1	4.53	148	–18.0	.125	7	.16	–58
0.8	.05	26	12.9	4.41	138	–17.8	.139	9	.17	–71
1.0	.06	–5	12.6	4.25	127	–17.6	.132	10	.18	–84
1.5	.08	–51	11.6	3.82	104	–16.5	.149	12	.18	–109
2.0	.11	–99	10.5	3.33	82	–15.9	.161	11	.17	–126
2.5	.14	–127	9.3	2.91	68	–15.2	.174	13	.16	–134
3.0	.20	–154	7.9	2.48	52	–14.8	.183	7	.16	–139
3.5	.25	–173	6.7	2.16	37	–14.7	.184	5	.16	–132
4.0	.29	171	5.5	1.88	23	–14.8	.182	1	.18	–130
5.0	.35	139	3.5	1.50	–1	–14.3	.193	–6	.21	–133
6.0	.46	100	1.7	1.22	–26	–14.5	.189	–14	.20	–169

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

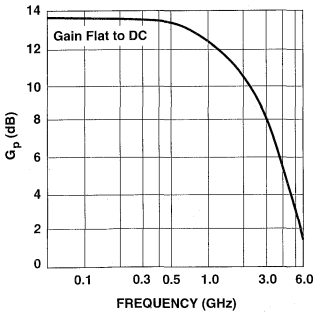


Figure 1. Typical Power Gain vs. Frequency, I_d = 22 mA.

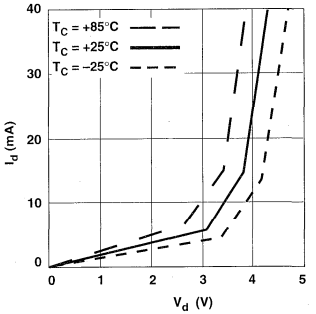


Figure 2. Device Current vs. Voltage.

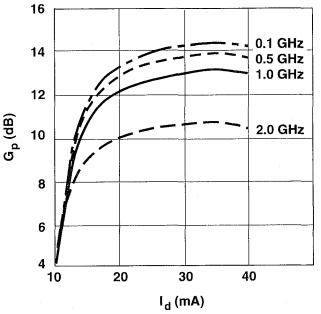


Figure 3. Power Gain vs. Current.

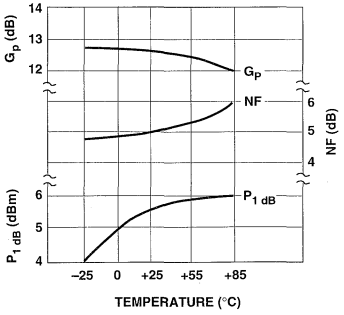


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 22 mA.

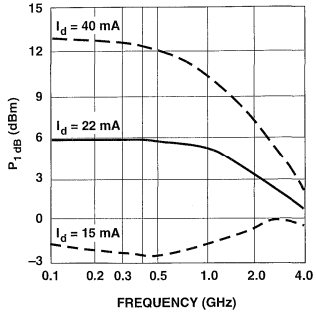


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

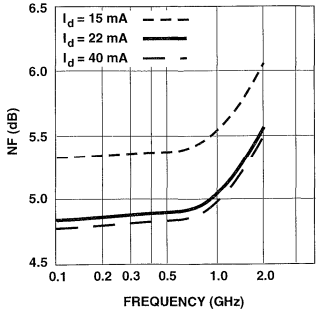
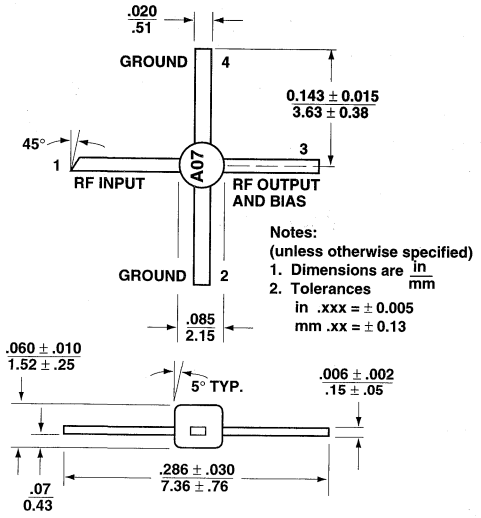


Figure 6. Noise Figure vs. Frequency.

85 Plastic Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0786

Features

- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage:** 4.0 V Typical V_d
- **3 dB Bandwidth:** DC to 2.0 GHz
- **12.5 dB Typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Note:

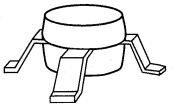
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."

Description

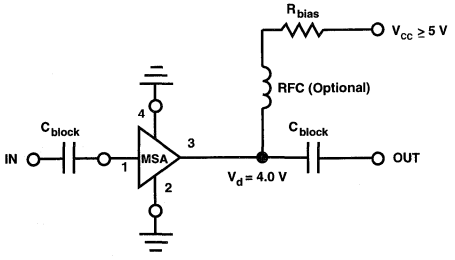
The MSA-0786 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block. Applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

86 Plastic Package



Typical Biasing Configuration



MSA-0786 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	275 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 120°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 8.3 mW/°C for T_C > 117°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		13.5	
		f = 1.0 GHz		10.5	12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.3 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.0	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.7:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		5.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		2.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		19.0	
t_D	Group Delay	f = 1.0 GHz	psec		150	
V_d	Device Voltage		V	3.2	4.0	4.8
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–7.0	

Note:
1. The recommended operating current range for this device is 15 to 40 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0786-TR1	1000	7" Reel
MSA-0786-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0786 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 22 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.05	175	13.5	4.74	174	-18.7	.116	1	.14	-12
0.2	.05	174	13.4	4.71	169	-18.7	.117	3	.14	-22
0.4	.04	167	13.3	4.64	158	-18.4	.120	4	.15	-44
0.6	.04	175	13.1	4.52	148	-18.3	.122	7	.16	-65
0.8	.05	-156	12.9	4.39	138	-18.0	.126	8	.17	-84
1.0	.06	-134	12.6	4.25	127	-17.5	.134	10	.18	-102
1.5	.08	-142	11.6	3.79	103	-16.6	.148	9	.21	-139
2.0	.15	-159	10.5	3.34	80	-15.7	.164	7	.23	-164
2.5	.25	-176	9.2	2.89	63	-15.1	.176	5	.24	174
3.0	.33	166	7.8	2.45	44	-14.7	.185	1	.24	159
3.5	.41	150	6.5	2.11	27	-14.9	.179	-5	.24	149
4.0	.49	137	5.2	1.82	12	-15.1	.177	-9	.23	145
5.0	.60	116	3.0	1.41	-14	-15.4	.169	-14	.26	145

Note:
1. A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

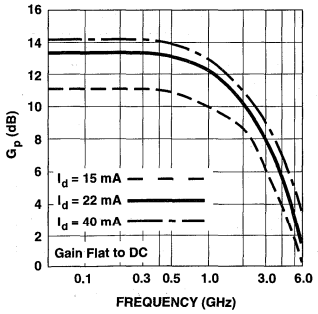


Figure 1. Typical Power Gain vs. Frequency.

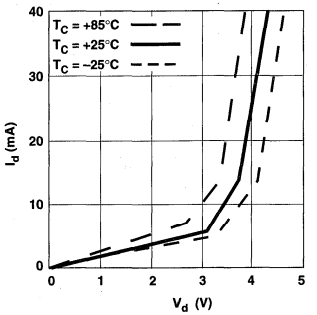


Figure 2. Device Current vs. Voltage.

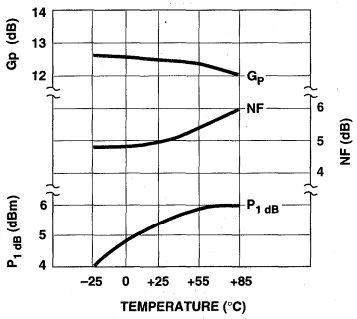


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 22 mA.

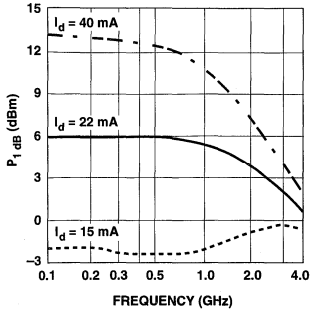


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

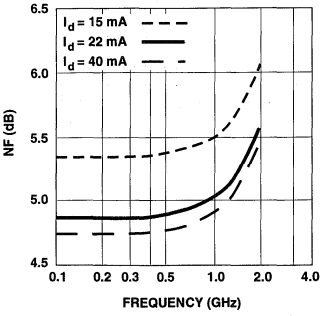
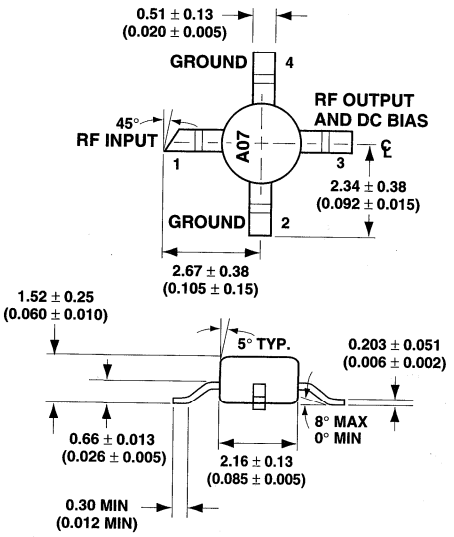


Figure 5. Noise Figure vs. Frequency.

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0800

Features

- **Usable Gain to 6.0 GHz**
- **High Gain:**
  32.5 dB Typical at 0.1 GHz
  23.5 dB Typical at 1.0 GHz
- **Low Noise Figure:**
  3.0 dB Typical at 1.0 GHz

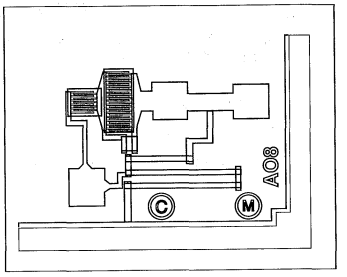
Description

The MSA-0800 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for use as a general purpose 50 Ω gain block above 0.5 GHz and can be used as a high gain transistor below this frequency. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

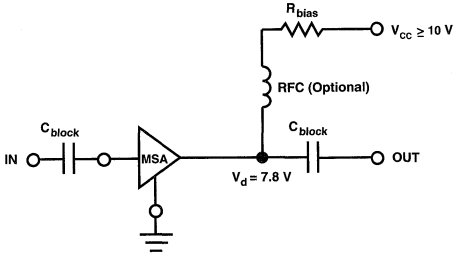
The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1] See APPLICATIONS section, "Chip Use".

Chip Outline[1]



Note:
1. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



MSA-0800 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	200°C

Thermal Resistance[2,4]:
θ_{jc} = 70°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 14.3 mW/°C for $T_{Mounting\ Surface}$ > 148°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASURE-

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 36 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz f = 4.0 GHz	dB		32.5 23.5 11.0	
VSWR	Input VSWR	f = 1.0 to 3.0 GHz			2.0:1	
	Output VSWR	f = 1.0 to 3.0 GHz			1.9:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.0	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		27.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	7.0	7.8	8.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–17.0	

Notes:
1. The recommended operating current range for this device is 20 to 40 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0800-GP4	100

MSA-0800 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 36 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.1	.65	–17	32.6	42.50	163	–36.9	.014	39	.64	–20	0.80
0.2	.61	–31	31.7	38.59	148	–34.1	.020	47	.59	–39	0.68
0.4	.50	–54	29.6	30.22	126	–31.0	.028	52	.49	–68	0.63
0.6	.43	–70	27.5	23.64	113	–28.5	.038	52	.40	–90	0.69
0.8	.38	–81	25.6	19.05	103	–26.7	.046	53	.35	–106	0.75
1.0	.34	–95	24.2	16.27	93	–25.4	.054	55	.30	–120	0.80
1.5	.31	–110	20.9	11.12	78	–23.6	.066	53	.23	–142	0.88
2.0	.32	–124	18.3	8.22	66	–22.6	.075	53	.17	–158	0.98
2.5	.33	–129	16.3	6.52	61	–20.7	.092	57	.13	–162	1.00
3.0	.34	–138	14.4	5.24	54	–20.3	.097	54	.07	–165	1.11
3.5	.36	–146	12.8	4.36	45	–19.0	.112	50	.07	–140	1.11
4.0	.36	–155	11.3	3.68	37	–18.3	.122	49	.10	–96	1.16
5.0	.35	177	8.7	2.73	23	–17.2	.138	43	.15	–75	1.28
6.0	.43	150	6.3	2.07	10	–16.6	.148	35	.15	–81	1.40

Note:

1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

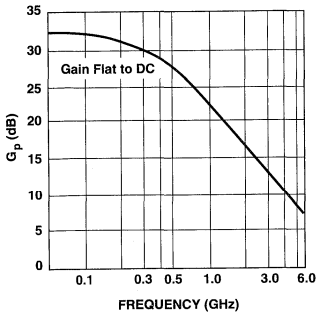


Figure 1. Typical Power Gain vs. Frequency, I_d = 36 mA.

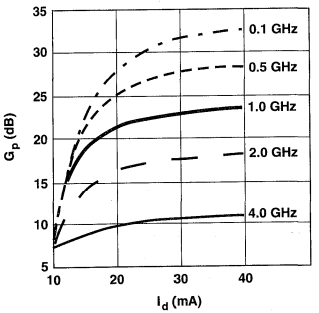


Figure 2. Power Gain vs. Current.

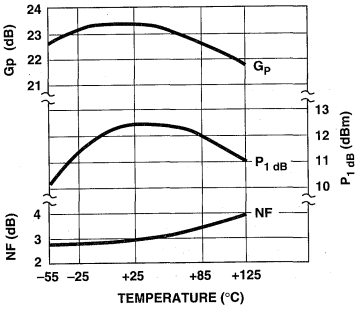


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, f = 1.0 GHz, I_d = 36 mA.

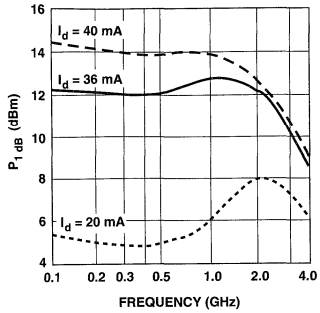


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

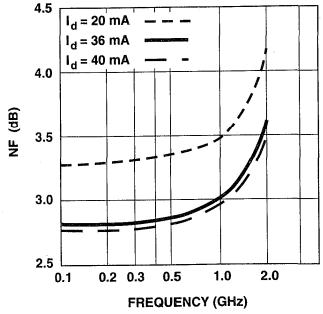
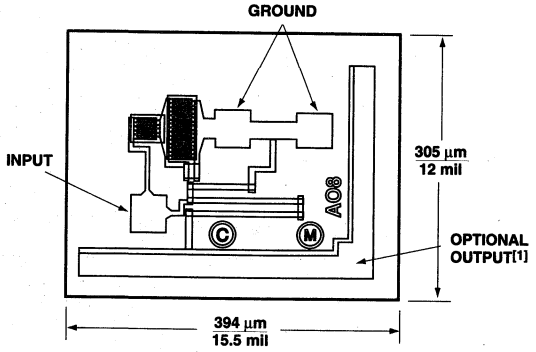


Figure 5. Noise Figure vs. Frequency.

MSA-0800 Chip Dimensions



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils. Chip thickness is 114 µm/4.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side.
Note 1: Output contact is made by die attaching the backside of the die.

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifiers

Technical Data

MSA-0835, -0836

Features

- **Usable Gain to 6.0 GHz**
- **High Gain:**
  32.5 dB Typical at 0.1 GHz
  23.0 dB Typical at 1.0 GHz
- **Low Noise Figure:**
  3.0 dB Typical at 1.0 GHz
- **Cost Effective Ceramic Microstrip Package**

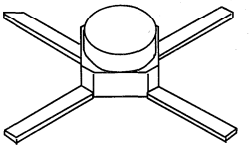
Description

The MSA-0835 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MMIC is designed for use as a general purpose 50 Ω gain block above 0.5 GHz and can be used as a high gain transistor below this frequency. Typical applications include narrow and moderate band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Available in cut lead version (package 36) as MSA-0836.

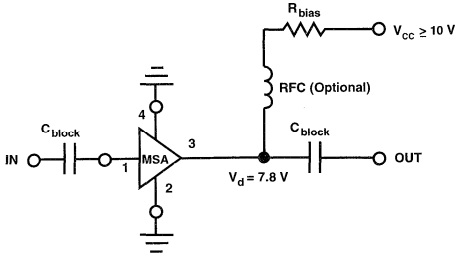
35 micro-X Package[1]



Note:

1. Short leaded 36 package available upon request.

Typical Biasing Configuration



MSA-0835, -0836 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65°C to 200°C

Thermal Resistance[2,5]:
θ_{jc} = 175°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 5.7 mW/°C for T_C > 69°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 36 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		32.5	
		f = 1.0 GHz		22.0	23.0	25.0
		f = 4.0 GHz			10.5	
VSWR	Input VSWR	f = 1.0 to 3.0 GHz			2.0:1	
	Output VSWR	f = 1.0 to 3.0 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		27.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	7.0	7.8	8.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–17.0	

Note:
1. The recommended operating current range for this device is 20 to 40 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0835	10	Strip
MSA-0836-BLK	100	Antistatic Bag
MSA-0836-TR1	1000	7" Reel

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0835, -0836 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 36 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.1	.63	–17	32.5	42.02	161	–37.7	.013	55	.63	–19	0.72
0.2	.58	–33	31.5	37.52	145	–33.7	.021	47	.56	–37	0.73
0.4	.49	–56	29.1	28.50	119	–29.7	.033	54	.42	–66	0.72
0.6	.40	–70	26.7	21.54	103	–27.9	.040	55	.32	–84	0.78
0.8	.35	–80	24.6	17.01	92	–26.0	.050	53	.24	–98	0.85
1.0	.33	–89	22.9	13.98	82	–24.9	.057	52	.18	–107	0.89
1.5	.30	–111	19.5	9.45	64	–22.1	.079	51	.09	–126	0.95
2.0	.30	–133	16.9	7.03	48	–20.2	.098	44	.07	–141	0.99
2.5	.32	–150	14.9	5.53	39	–19.2	.110	42	.06	–166	1.04
3.0	.34	–170	13.2	4.56	26	–18.3	.122	36	.06	–106	1.06
3.5	.38	175	11.7	3.86	14	–17.5	.133	32	.08	–100	1.08
4.0	.39	162	10.5	3.33	2	–16.7	.146	27	.12	–101	1.08
5.0	.41	132	7.9	2.47	–21	–15.6	.165	19	.21	–113	1.10
6.0	.52	95	5.8	1.94	–45	–14.6	.187	7	.20	–149	1.05

Note:
1. A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C
(unless otherwise noted)

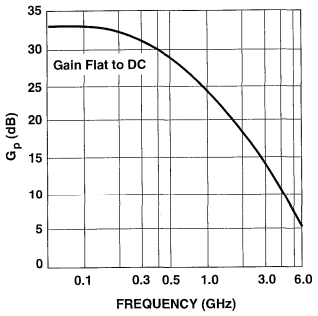


Figure 1. Typical Power Gain vs. Frequency, I_d = 36 mA.

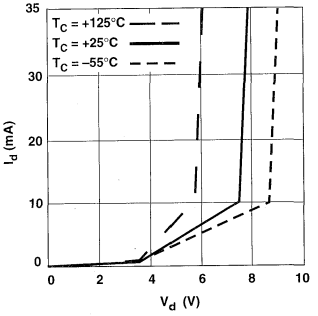


Figure 2. Device Current vs. Voltage.

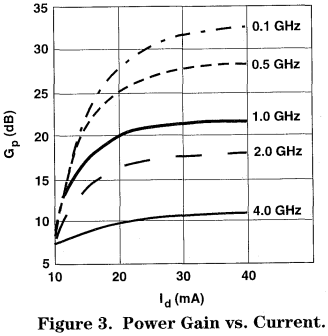


Figure 3. Power Gain vs. Current.

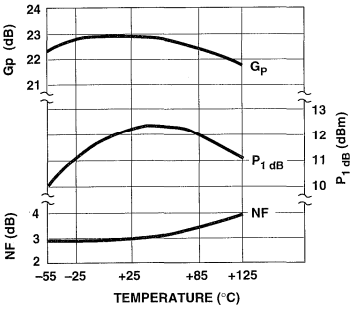


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 36 mA.

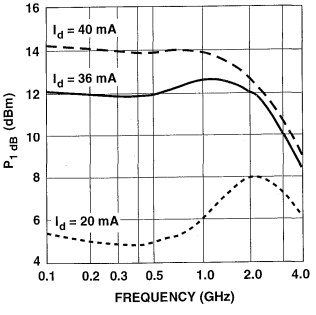


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

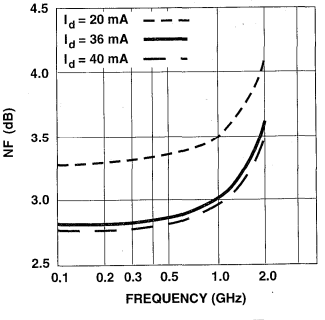
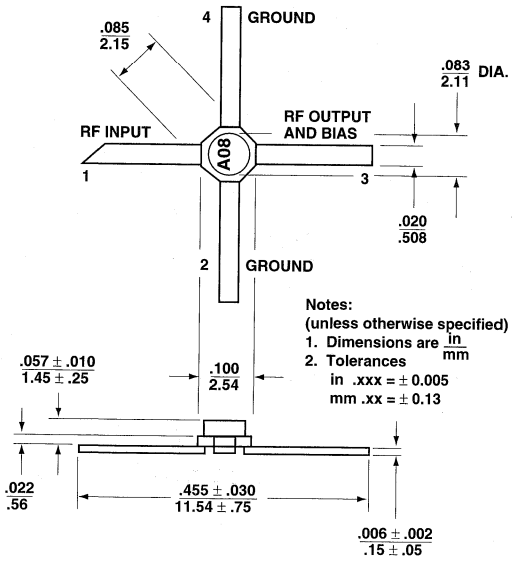


Figure 6. Noise Figure vs. Frequency.

35 micro-X Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0870

Features

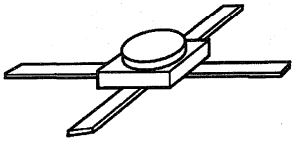
- **Usable Gain to 6.0 GHz**
- **High Gain:**
  32.5 dB Typical at 0.1 GHz
  23.5 dB Typical at 1.0 GHz
- **Low Noise Figure:**
  3.0 dB Typical at 1.0 GHz
- **Hermetic Gold-ceramic Microstrip Package**

Description

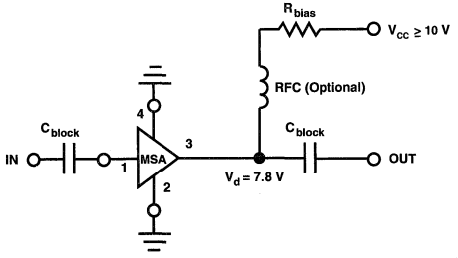
The MSA-0870 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MMIC is designed for use as a general purpose 50 Ω gain block above 0.5 GHz and can be used as a high gain transistor below this frequency. Typical applications include narrow and moderate band IF and RF amplifiers in industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package



Typical Biasing Configuration



MSA-0870 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 150°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.7 mW/°C for T_C > 88°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 36 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		32.5	
		f = 1.0 GHz		22.0	23.5	25.0
		f = 4.0 GHz			11.0	12.0
VSWR	Input VSWR	f = 1.0 to 3.0 GHz			2.0:1	
	Output VSWR	f = 1.0 to 3.0 GHz			1.9:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		27.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	7.0	7.8	8.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–17.0	

Note:
1. The recommended operating current range for this device is 20 to 40 mA. Typical performance as a function of current is on the following page.

MSA-0870 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 36 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.1	.65	–19	32.5	42.04	161	–36.3	.015	40	.64	–22	0.78
0.2	.60	–35	31.5	37.54	145	–33.7	.021	47	.58	–43	0.66
0.4	.48	–60	29.1	28.49	122	–30.5	.030	51	.47	–74	0.64
0.6	.40	–76	26.8	21.90	108	–28.0	.040	50	.38	–97	0.72
0.8	.35	–88	24.9	17.48	97	–26.2	.049	50	.33	–113	0.78
1.0	.32	–102	23.4	14.85	87	–24.9	.057	51	.28	–128	0.83
1.5	.29	–118	20.1	10.14	70	–23.0	.071	47	.22	–151	0.91
2.0	.30	–133	17.6	7.55	56	–21.9	.081	45	.16	–167	0.98
2.5	.31	–139	15.6	6.01	49	–20.0	.100	46	.12	–172	1.02
3.0	.32	–149	13.8	4.87	39	–19.5	.106	41	.07	–170	1.11
3.5	.34	–159	12.2	4.09	28	–18.4	.121	35	.07	–143	1.12
4.0	.34	–168	10.8	3.48	17	–17.7	.131	31	.12	–112	1.16
5.0	.33	161	8.4	2.63	–3	–16.6	.147	21	.19	–103	1.26
6.0	.39	128	6.2	2.04	–22	–16.2	.155	10	.21	–115	1.36

Note:
1. A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C
(unless otherwise noted)

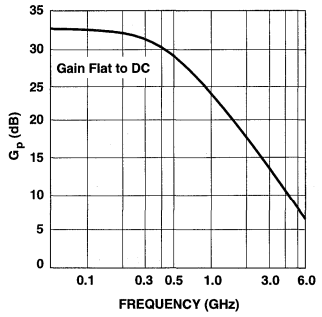


Figure 1. Typical Power Gain vs. Frequency, I_d = 36 mA.

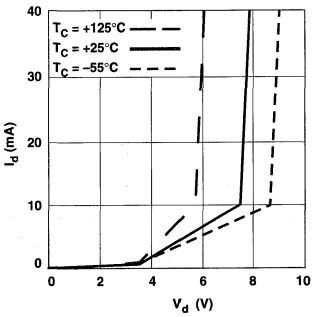


Figure 2. Device Current vs. Voltage.

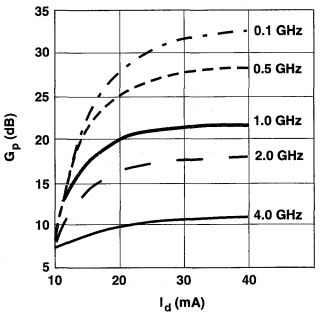


Figure 3. Power Gain vs. Current.

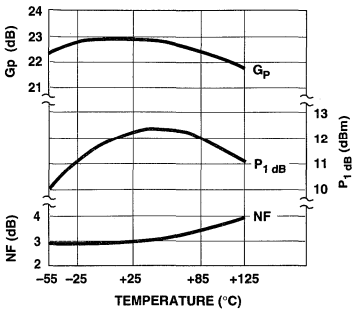


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 36 mA.

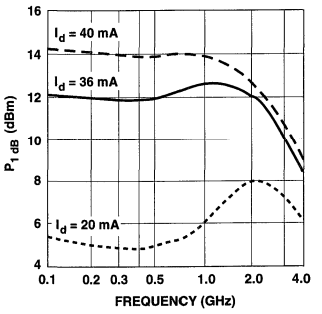


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

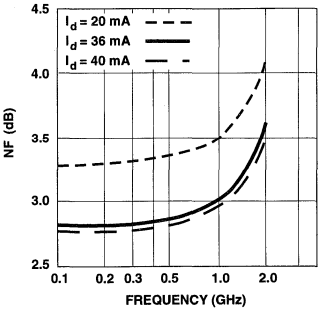
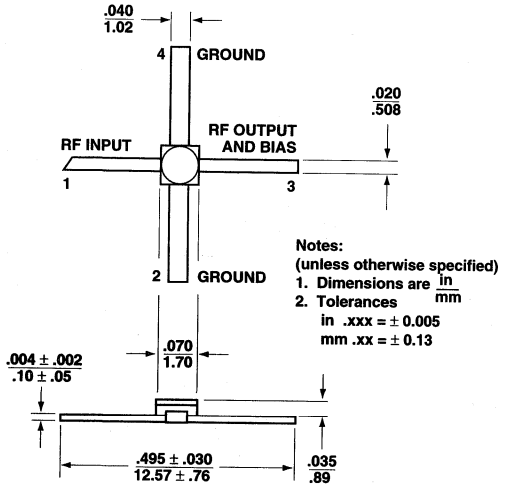


Figure 6. Noise Figure vs. Frequency.

70 mil Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0885

Features

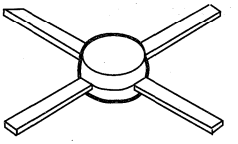
- **Usable Gain to 6.0 GHz**
- **High Gain:**
  32.5 dB Typical at 0.1 GHz
  22.5 dB Typical at 1.0 GHz
- **Low Noise Figure:**
  3.3 dB Typical at 1.0 GHz
- **Low Cost Plastic Package**

Description

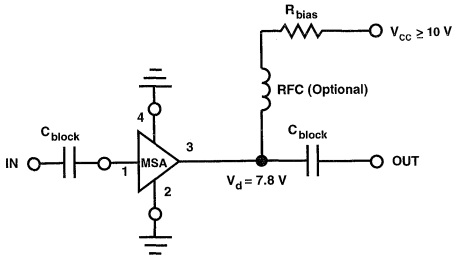
The MSA-0885 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block above 0.5 GHz and can be used as a high gain transistor below this frequency. Typical applications include narrow and moderate band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package



Typical Biasing Configuration



MSA-0885 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	65 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 130°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.7 mW/°C for T_C > 85°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 36 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 21.0	32.5 22.5	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.9:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.6:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.3	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		27.0	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	6.2	7.8	9.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–17.0	

Note:
1. The recommended operating current range for this device is 20 to 40 mA. Typical performance as a function of current is on the following page.

MSA-0885 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 36 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.64	–21	32.5	42.29	160	–36.5	.015	40	.61	–24	0.78
0.2	.58	–39	31.3	36.89	144	–32.8	.023	50	.54	–45	0.67
0.4	.44	–65	28.7	27.20	120	–29.4	.034	54	.42	–77	0.69
0.6	.36	–82	26.3	20.57	106	–27.2	.044	53	.33	–98	0.77
0.8	.31	–95	24.3	16.31	96	–25.2	.055	53	.28	–115	0.83
1.0	.27	–105	22.5	13.36	87	–24.2	.061	51	.25	–129	0.87
1.5	.24	–125	19.3	9.24	71	–21.4	.085	50	.18	–153	0.96
2.0	.26	–147	16.7	6.82	56	–19.7	.103	47	.15	–173	0.98
2.5	.29	–159	14.9	5.57	48	–18.4	.120	44	.12	180	1.00
3.0	.34	–175	13.1	4.51	37	–17.7	.130	42	.09	165	1.03
3.5	.38	172	11.6	3.80	25	–16.9	.144	37	.06	172	1.04
4.0	.42	161	10.1	3.21	14	–16.3	.153	33	.04	–139	1.06
5.0	.48	135	7.7	2.43	–7	–15.6	.167	24	.09	–90	1.09
6.0	.60	102	5.5	1.88	–29	–14.9	.179	17	.08	–140	1.06

Note:
1. A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C
(unless otherwise noted)

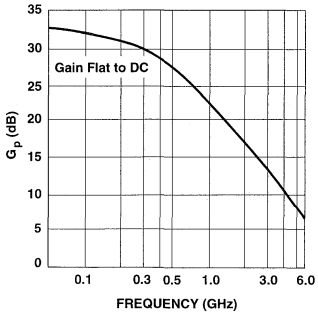


Figure 1. Typical Power Gain vs. Frequency, I_d = 36 mA.

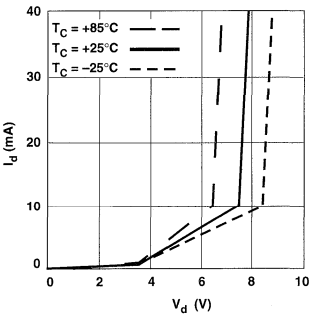


Figure 2. Device Current vs. Voltage.

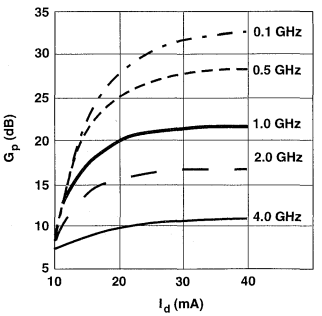


Figure 3. Power Gain vs. Current.

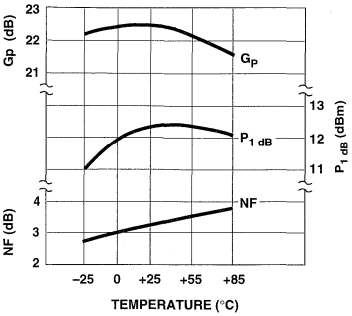


Figure 4. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 36 mA.

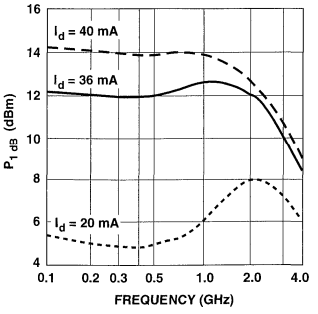


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

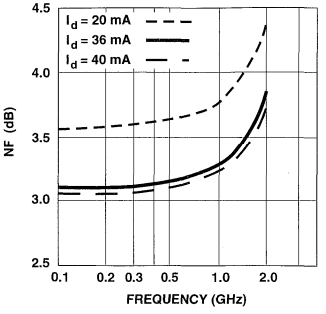
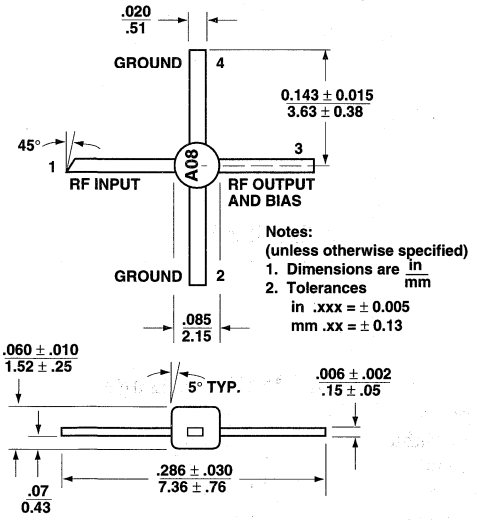


Figure 6. Noise Figure vs. Frequency.

85 Plastic Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0886

Features

- **Usable Gain to 5.5 GHz**
- **High Gain:**
  32.5 dB Typical at 0.1 GHz
  22.5 dB Typical at 1.0 GHz
- **Low Noise Figure:**
  3.3 dB Typical at 1.0 GHz
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

Note:

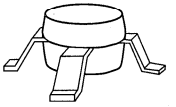
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."

Description

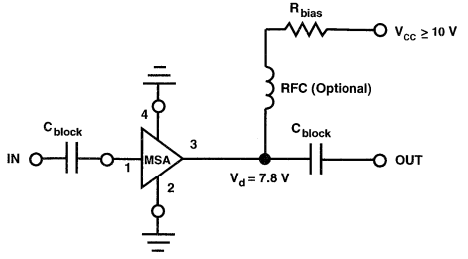
The MSA-0886 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MMIC is designed for use as a general purpose 50 Ω gain block above 0.5 GHz and can be used as a high gain transistor below this frequency. Typical applications include narrow and moderate band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

86 Plastic Package



Typical Biasing Configuration



MSA-0886 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	65 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 140°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.1 mW/°C for T_C > 80°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 36 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 20.5	32.5 22.5	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			2.1:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.9:1	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.3	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		27.0	
t_D	Group Delay	f = 1.0 GHz	psec		140	
V_d	Device Voltage		V	6.2	7.8	9.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–17.0	

Note:
1. The recommended operating current range for this device is 20 to 40 mA. Typical performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0886-TR1	1000	7" Reel
MSA-0886-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0886 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, I_d = 36 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.63	–22	32.5	42.12	160	–36.7	.015	54	.62	–24	0.68
0.2	.56	–41	31.3	36.68	143	–33.9	.020	50	.55	–46	0.64
0.4	.43	–69	28.6	26.94	119	–29.1	.035	52	.43	–79	0.69
0.6	.35	–88	26.4	20.89	104	–27.0	.045	49	.34	–103	0.77
0.8	.30	–104	24.2	16.21	93	–25.3	.054	50	.29	–124	0.83
1.0	.27	–116	22.4	13.20	83	–24.2	.062	49	.26	–139	0.87
1.5	.27	–144	19.2	9.15	65	–21.6	.083	46	.23	–172	0.93
2.0	.31	–166	16.7	6.84	49	–19.5	.105	41	.22	163	0.96
2.5	.35	178	14.8	5.50	38	–17.9	.128	36	.21	149	0.96
3.0	.40	162	12.9	4.41	25	–17.4	.135	30	.20	132	1.01
3.5	.45	149	11.4	3.72	13	–16.8	.145	25	.19	124	1.02
4.0	.51	137	9.9	3.14	1	–16.1	.157	19	.18	121	1.01
5.0	.61	116	7.3	2.31	–22	–15.7	.164	10	.17	130	1.00
6.0	.68	100	4.6	1.69	–42	–15.2	.173	4	.23	143	0.95

Note:

1. A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

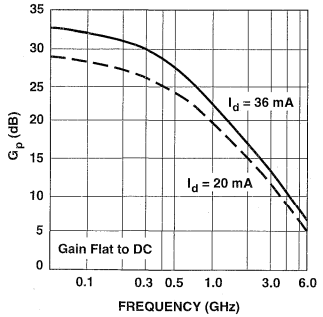


Figure 1. Typical Power Gain vs. Frequency, I_d = 36 mA.

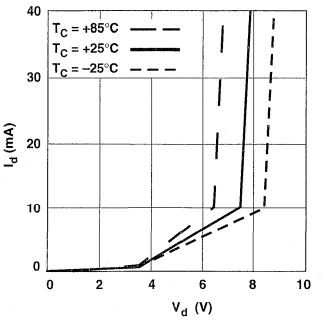


Figure 2. Device Current vs. Voltage.

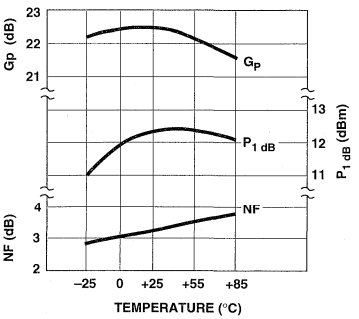


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 36 mA.

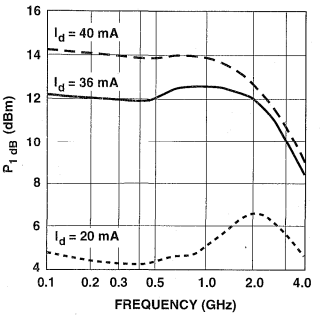


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

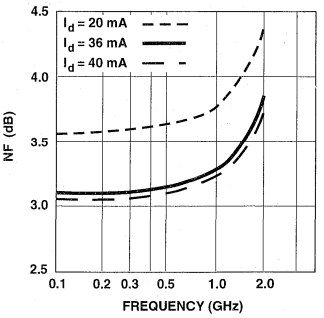
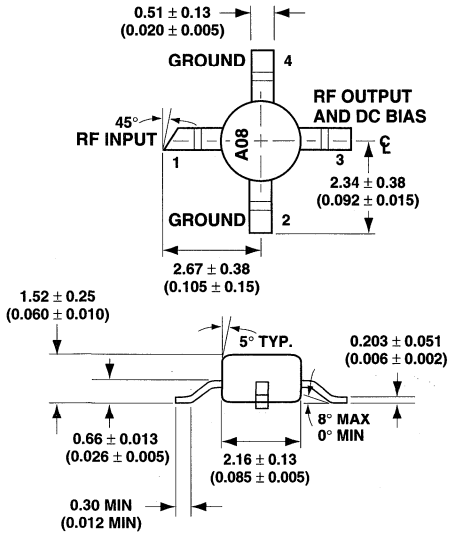


Figure 5. Noise Figure vs. Frequency.

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0900

Features

- **Broadband, Minimum Ripple Cascadable 50 Ω Gain Block**
- **8.0 ± 0.2 dB Typical Gain Flatness from 0.1 to 4.0 GHz**
- **3 dB Bandwidth:** 0.1 to 6.0 GHz
- **Low VSWR:** ≤1.5:1 from 0.1 to 4.0 GHz
- **11.5 dBm Typical P_{1dB} at 1.0 GHz**

Description

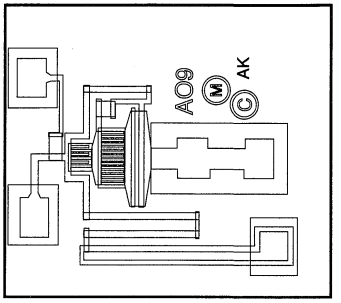
The MSA-0900 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for very wide bandwidth industrial and military applications that require flat gain and low VSWR.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.

This chip is intended to be used with an external blocking capacitor completing the shunt feedback path (closed loop). Data sheet characterization is given for a 45 pF capacitor. Low frequency performance can be extended by using a larger valued capacitor.[1]

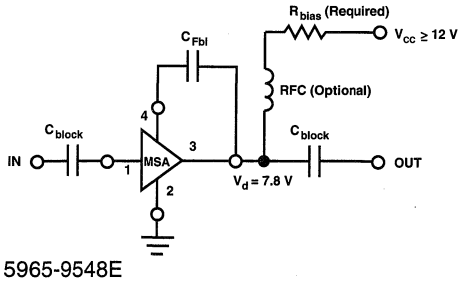
Chip Outline[1]



Note:

1. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



MSA-0900 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 70°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 14 mW/°C for $T_{Mounting\ Surface}$ > 148°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		8.0	
ΔG_P	Gain Flatness[3]	f = 0.1 to 4.0 GHz	dB		±0.2	
$f_{3\ dB}$	3 dB Bandwidth[3,4]		GHz		6.0	
VSWR	Input VSWR	f = 1.0 to 4.0 GHz			1.4:1	
	Output VSWR	f = 1.0 to 4.0 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 1.0 GHz f = 4.0 GHz	dB		6.0 6.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz f = 4.0 GHz	dBm		11.5 6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec		60	
V_d	Device Voltage		V	7.0	7.8	8.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16.0	

Notes:
1. The recommended operating current range for this device is 25 to 45 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
3. The value is the expected achievable performance for the MSA-0900 used with an external 45 pF capacitor mounted in a 100 mil stripline package.
4. Referenced from 0.1 GHz gain (G_P).

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0900-GP4	100

MSA-0900 Typical Scattering Parameters[1,2] (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.02	.32	–107	10.8	3.48	151	–13.9	.203	17	.32	–106	0.83
0.05	.22	–143	8.6	2.70	164	–13.6	.209	6	.22	–142	1.09
0.1	.11	–144	8.2	2.57	171	–13.3	.215	3	.11	–142	1.16
0.2	.10	–160	8.1	2.54	172	–13.5	.211	1	.10	–158	1.19
0.4	.10	–171	8.1	2.54	175	–13.4	.215	2	.10	–166	1.18
0.6	.09	–170	8.1	2.55	166	–13.3	.216	1	.10	–166	1.18
0.8	.08	–171	8.2	2.57	162	–13.3	.216	1	.11	–166	1.17
1.0	.08	–170	8.3	2.59	158	–13.1	.220	1	.11	–167	1.15
1.5	.07	–166	8.6	2.68	147	–13.1	.221	1	.14	–172	1.12
2.0	.07	–138	8.9	2.80	136	–12.6	.234	1	.15	–172	1.07
2.5	.08	–131	9.3	2.92	126	–12.6	.236	1	.18	179	1.04
3.0	.12	–119	9.6	3.01	112	–12.0	.250	1	.21	171	0.99
3.5	.17	–125	9.6	3.02	95	–11.8	.256	–1	.22	157	0.97
4.0	.22	–132	9.1	2.86	78	–11.5	.265	–3	.19	144	0.96
4.5	.27	–140	8.4	2.64	63	–11.5	.265	–5	.16	138	0.97
5.0	.32	–149	7.5	2.36	50	–11.4	.268	–6	.12	138	1.00
5.5	.34	–154	6.4	2.09	38	–11.3	.272	–6	.10	162	1.02
6.0	.36	–158	5.3	1.84	29	–11.3	.272	–6	.10	–166	1.07
6.5	.38	–158	4.2	1.62	22	–11.4	.271	–6	.16	–151	1.12
7.0	.39	–157	3.2	1.45	15	–11.5	.267	–6	.23	–147	1.17

Notes:

1. S-parameters are de-embedded from 100 mil BeO package measured data using the package model found in the DEVICE MODELS section.
2. S-parameter data assumes an external 45 pF capacitor. Low fequency performance can be extended using a larger valued capacitor.

Typical Performance, T_A = 25°C

(unless otherwise noted)

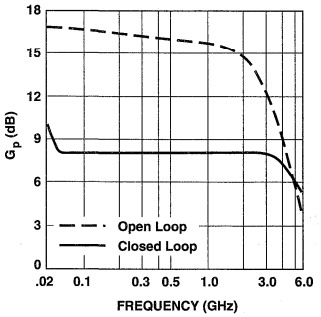


Figure 1. Typical Power Gain vs. Frequency, I_d = 35 mA.

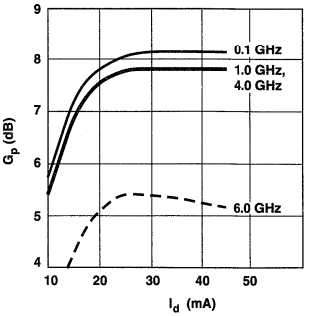


Figure 2. Power Gain vs. Current.

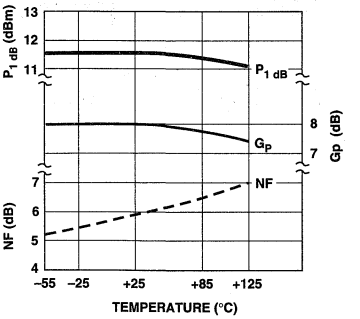


Figure 3. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 35 mA.

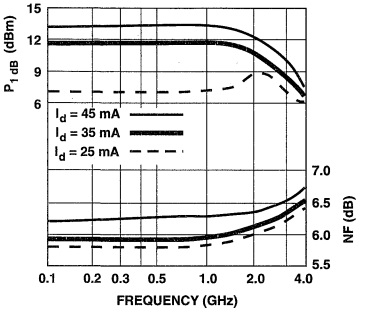
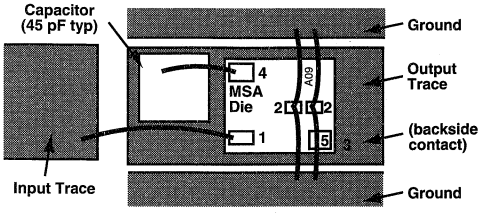


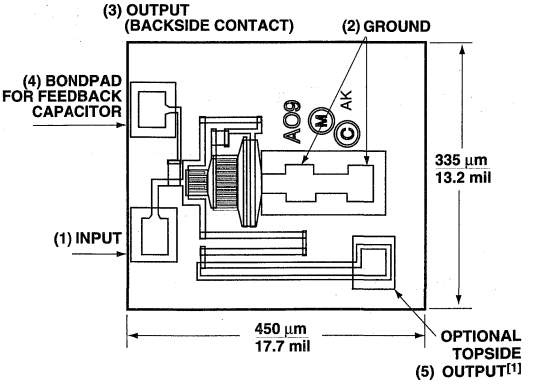
Figure 4. Output Power at 1 dB Gain Compression and Noise Figure vs. Frequency.

MSA-0900 Bonding Diagram



Numbers refer to pin contacts listed on the Chip Outline.

MSA-0900 Chip Dimensions



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils. Chip thickness is 114 µm/4.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side. Note 1: Output contact is made by die attaching the backside of the die.

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0910

Features

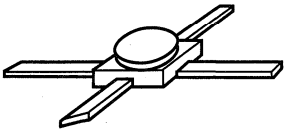
- **Broadband, Minimum Ripple Cascadable 50 Ω Gain Block**
- **8.0 ± 0.2 dB Typical Gain Flatness from 0.1 to 4.0 GHz**
- **3 dB Bandwidth:** 0.1 to 6.0 GHz
- **Low VSWR:** ≤1.5:1 from 0.1 to 4.0 GHz
- **11.5 dBm Typical P_{1dB} at 1.0 GHz**
- **Hermetic Gold-ceramic Microstrip Package**

Description

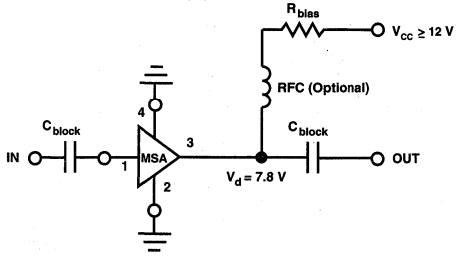
The MSA-0910 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MMIC is designed for very wide bandwidth industrial and military applications that require flat gain and low VSWR.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

100 mil Package



Typical Biasing Configuration



MSA-0910 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 145°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.9 mW/°C for T_C > 91°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	7.0	8.0	9.0
ΔG_P	Gain Flatness	f = 0.1 to 4.0 GHz	dB		±0.2	±0.5
$f_{3\ dB}$	3 dB Bandwidth[2]		GHz		6.0	
VSWR	Input VSWR	f = 1.0 to 4.0 GHz			1.3:1	
	Output VSWR	f = 1.0 to 4.0 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 1.0 GHz f = 4.0 GHz	dB		6.0 6.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz f = 4.0 GHz	dBm		11.5 6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec		100	
V_d	Device Voltage		V	7.0	7.8	8.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16.0	

Notes:
1. The recommended operating current range for this device is 25 to 45 mA. Typical performance as a function of current is on the following page.
2. Referenced from 0.1 GHz gain (G_P).

MSA-0910 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.02	.31	–108	10.6	3.38	150	–13.8	.202	16	.31	–107	0.85
0.05	.18	–114	8.8	2.75	160	–13.5	.212	8	.20	–117	1.06
0.1	.12	–141	8.1	2.53	166	–13.4	.214	3	.14	–139	1.16
0.2	.10	–166	7.9	2.47	167	–13.4	.215	1	.13	–157	1.19
0.4	.10	170	7.8	2.46	163	–13.3	.215	–1	.12	–165	1.20
0.6	.10	156	7.8	2.45	157	–13.3	.216	–3	.13	–167	1.20
0.8	.10	145	7.8	2.46	151	–13.3	.216	–4	.13	–168	1.19
1.0	.10	133	7.8	2.46	144	–13.3	.217	–6	.14	–169	1.19
1.5	.10	111	7.9	2.49	127	–13.2	.220	–10	.16	–173	1.17
2.0	.09	88	8.0	2.51	110	–13.0	.224	–13	.18	177	1.15
2.5	.07	89	8.2	2.58	96	–12.8	.230	–16	.21	167	1.11
3.0	.04	90	8.2	2.58	78	–12.8	.230	–21	.20	151	1.11
3.5	.06	145	8.2	2.57	59	–12.7	.233	–27	.19	137	1.11
4.0	.12	152	8.0	2.50	40	–12.7	.230	–33	.16	125	1.12
4.5	.19	142	7.5	2.38	22	–13.0	.223	–40	.13	116	1.16
5.0	.26	131	6.9	2.21	4	–13.5	.211	–47	.09	118	1.22
5.5	.32	120	6.2	2.04	–12	–14.1	.198	–52	.07	160	1.28
6.0	.38	109	5.3	1.84	–27	–14.8	.181	–56	.13	–173	1.38
6.5	.43	99	4.4	1.65	–42	–15.6	.167	–59	.21	–172	1.46

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

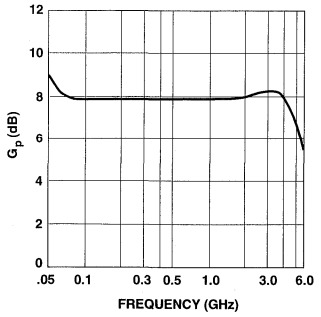


Figure 1. Typical Power Gain vs. Frequency, I_d = 35 mA.

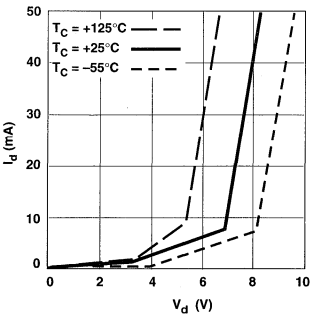


Figure 2. Device Current vs. Voltage.

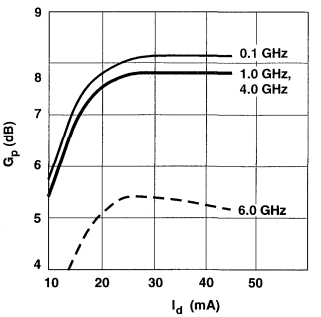


Figure 3. Power Gain vs. Current.

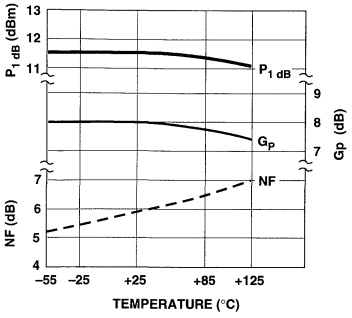


Figure 4. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 35 mA.

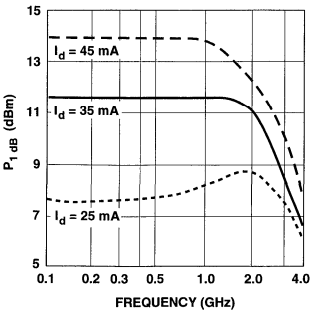


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

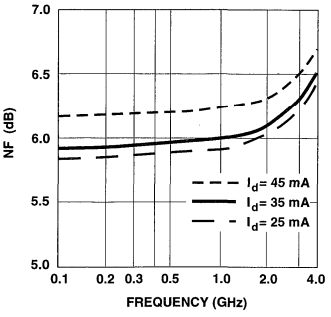
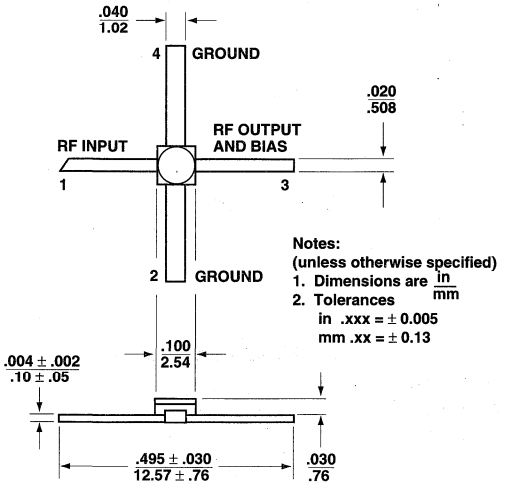


Figure 6. Noise Figure vs. Frequency.

100 mil Package Dimensions

Outline 10A



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0986

Features

- **Broadband, Minimum Ripple Cascadable 50 Ω Gain Block**
- **7.2 ± 0.5 dB Typical Gain Flatness from 0.1 to 3.0 GHz**
- **3 dB Bandwidth:** 0.1 to 5.5 GHz
- **10.5 dBm Typical P_{1dB} at 2.0 GHz**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Note:

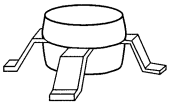
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."

Description

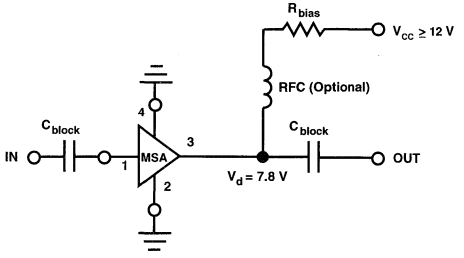
The MSA-0986 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MMIC is designed for very wide bandwidth industrial and commercial applications that require flat gain and low VSWR.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

86 Plastic Package



Typical Biasing Configuration



MSA-0986 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	65 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to +150°C

Thermal Resistance[2,4]:
θ_{jc} = 140°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.1 mW/°C for T_C > 80°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 2.0 GHz	dB	6.0	7.2	
ΔG_P	Gain Flatness	f = 0.1 to 3.0 GHz	dB		±0.5	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		5.5	
VSWR	Input VSWR	f = 1.0 to 3.0 GHz			1.6:1	
	Output VSWR	f = 1.0 to 3.0 GHz			1.8:1	
NF	50 Ω Noise Figure	f = 2.0 GHz	dB		6.2	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 2.0 GHz	dBm		10.5	
IP_3	Third Order Intercept Point	f = 2.0 GHz	dBm		23.0	
t_D	Group Delay	f = 2.0 GHz	psec		95	
V_d	Device Voltage		V	6.2	7.8	9.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16.0	

Notes:
1. The recommended operating current range for this device is 25 to 45 mA. Typical performance as a function of current is on the following page.
2. Referenced from 0.1 GHz gain (G_P).

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-0986-TR1	1000	7" Reel
MSA-0986-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-0986 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.02	.36	–105	11.4	3.72	145	–14.1	.198	18	.38	–102	0.73
0.05	.24	–145	8.5	2.65	156	–13.7	.205	5	.25	–143	1.08
0.1	.22	–164	7.7	2.43	166	–13.5	.211	4	.22	–158	1.17
0.2	.21	–179	7.5	2.37	167	–13.5	.212	1	.22	–172	1.20
0.4	.21	165	7.4	2.34	162	–13.4	.214	–1	.22	179	1.20
0.6	.22	155	7.4	2.33	156	–13.5	.212	–2	.22	175	1.21
0.8	.22	145	7.3	2.33	149	–13.4	.213	–2	.23	171	1.21
1.0	.23	136	7.3	2.32	142	–13.4	.214	–4	.24	167	1.20
1.5	.24	118	7.2	2.30	125	–13.3	.217	–6	.26	157	1.19
2.0	.25	106	7.2	2.28	109	–13.0	.224	–10	.28	148	1.16
2.5	.26	100	7.2	2.29	94	–13.0	.224	–12	.33	139	1.15
3.0	.26	94	7.1	2.26	77	–13.0	.224	–15	.34	128	1.15
3.5	.26	95	7.0	2.23	60	–12.8	.229	–21	.36	116	1.14
4.0	.28	96	6.7	2.17	43	–13.1	.221	–25	.35	104	1.18
4.5	.31	100	6.5	2.10	26	–13.6	.210	–31	.32	94	1.23
5.0	.37	101	6.0	2.00	9	–14.2	.196	–35	.26	86	1.30
5.5	.44	97	5.4	1.86	–7	–14.9	.181	–38	.19	88	1.38
6.0	.51	94	4.6	1.69	–22	–15.8	.162	–37	.14	107	1.47

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

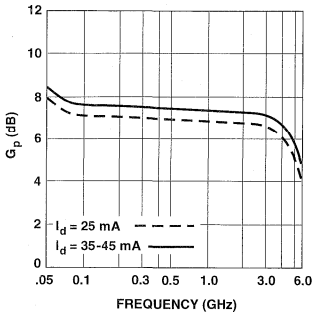


Figure 1. Typical Power Gain vs. Frequency.

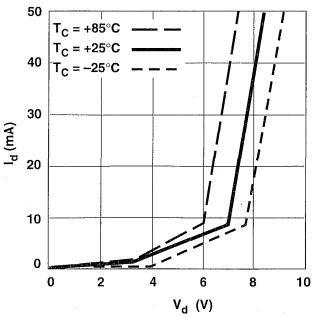


Figure 2. Device Current vs. Voltage.

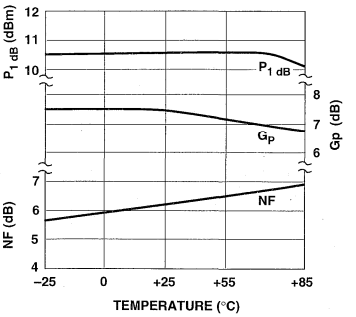


Figure 3. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 2.0 GHz, I_d = 35 mA.

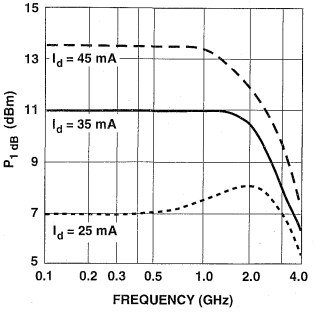


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

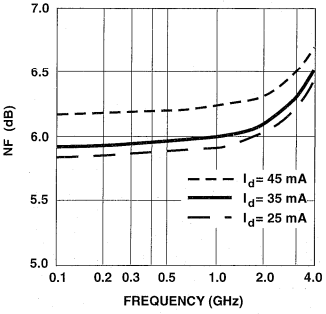
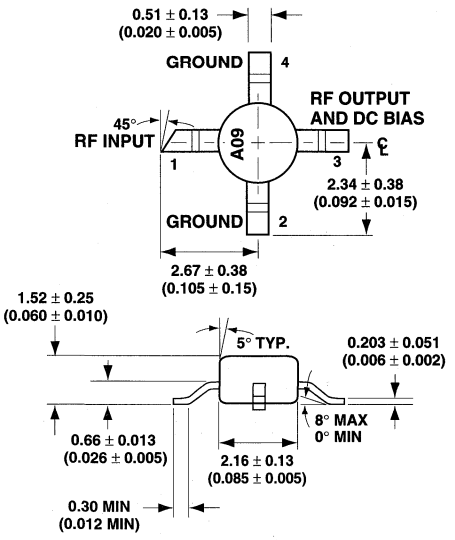


Figure 5. Noise Figure vs. Frequency.

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-1000

Features

- **High Output Power:** +27 dBm Typical P_{1dB} at 1.0 GHz
- **Low Distortion:** 37 dBm Typical IP_3 at 1.0 GHz
- **8.5 dB Typical Gain at 1.0 GHz**
- **Impedance Matched to 25 Ω for Push-Pull Configurations**

Description

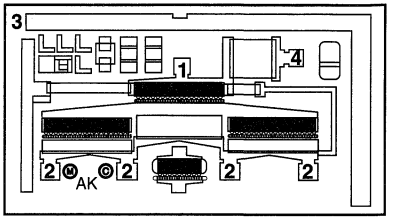
The MSA-1000 is a high performance, medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for use in a push-pull configuration in a 25 Ω system. The MSA-1000 can also be used as single-ended amplifier in a 50 Ω system with slightly reduced performance. Typical applications include narrow and broadband RF amplifiers in industrial and military systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.

This chip is intended to be used with an external blocking capacitor completing the shunt feedback path (closed loop). Data sheet characterization is given for a 80 pF capacitor. Low frequency performance can be extended by using a larger valued capacitor.[1]

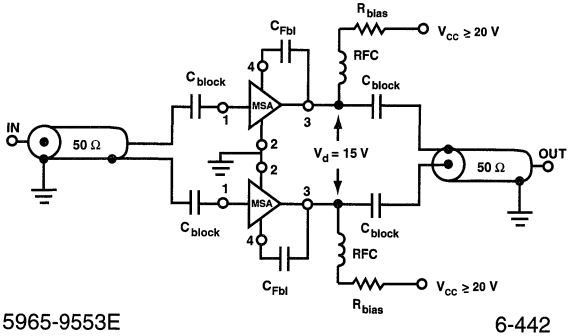
Chip Outline[1]



Note:

1. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Push-Pull Biasing Configuration



MSA-1000 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	425 mA
Power Dissipation[2,3]	7.0 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 10°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 100 mW/°C for $T_{Mounting\ Surface}$ > 130°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 325 mA, Z_O = 25 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.0 GHz	dB		8.5	
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.6	
$f_{3\ dB}$	3 dB Bandwidth[3]		GHz		2.6	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.0 GHz			2.5:1	
NF	25 Ω Noise Figure	f = 1.0 GHz	dB		7.0	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm		27.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		37.0	
t_D	Group Delay	f = 1.0 GHz	psec		175	
V_d	Device Voltage		V	13.5	15.0	16.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–18.0	

Notes:
1. The recommended operating current range for this device is 150 to 400 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
3. Referenced from 0.1 GHz gain (G_P).

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-1000-GP4	100

MSA-1000 Typical Scattering Parameters[1,2] (Z = 50 Ω, T_A = 25°C, I_d = 325 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.001	.41	–121	15.5	5.95	149	–17.7	.130	22	.43	–99	0.68
0.005	.52	–167	8.7	2.73	156	–15.7	.164	6	.48	–161	1.02
0.010	.54	–174	7.7	2.41	166	–15.6	.166	3	.46	–171	1.12
0.050	.54	–179	7.3	2.31	174	–15.7	.165	1	.46	–178	1.17
0.100	.55	179	7.2	2.30	173	–15.7	.165	–1	.46	–179	1.17
0.200	.55	178	7.2	2.30	168	–15.7	.165	–1	.47	177	1.16
0.400	.54	176	7.2	2.29	157	–15.7	.165	–3	.48	176	1.16
0.600	.52	174	7.2	2.30	146	–15.8	.163	–4	.48	174	1.16
0.800	.51	174	7.2	2.29	134	–15.8	.161	–5	.48	173	1.15
1.000	.50	172	7.2	2.29	121	–15.9	.160	–5	.49	172	1.12
1.200	.48	173	7.2	2.28	108	–16.0	.158	–6	.49	172	1.10
1.400	.47	175	7.1	2.26	96	–16.2	.155	–7	.50	174	1.05
1.600	.46	178	6.8	2.20	83	–16.3	.153	–7	.51	175	1.00
1.800	.46	179	6.4	2.09	62	–16.5	.150	–8	.53	176	0.94
2.000	.48	–177	6.0	1.99	56	–16.6	.148	–10	.65	–179	0.68
2.500	.56	–170	4.4	1.65	35	–17.0	.141	–1	.54	178	.91
3.000	.61	–171	2.7	1.36	12	–16.7	.147	1	.69	–176	.52

Notes:

1. S-parameters are de-embedded from 100 mil BeO package measured data using the package model found in the DEVICE MODELS section.
2. S-parameter data assumes an external 80 pF capacitor. Low frequency performance can be extended using a larger valued capacitor.

Typical Performance, T_A = 25°C

(unless otherwise noted)

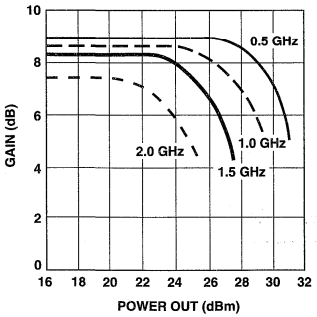


Figure 1. Typical Gain vs. Power Out, Z_O = 25 Ω, I_d = 325 mA.

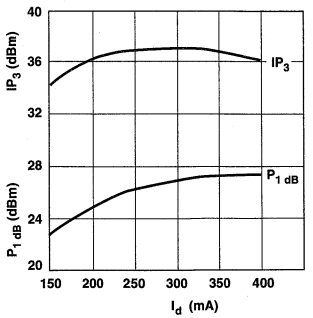


Figure 2. Output Power at 1 dB Gain Compression, Third Order Intercept Point vs. Current, Z_O = 25 Ω, f = 1.0 GHz.

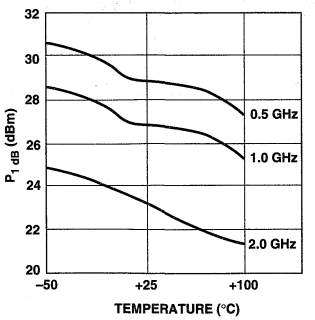


Figure 3. Output Power at 1 dB Gain Compression vs. Case Temperature, Z_O = 25 Ω, I_d = 325 mA.

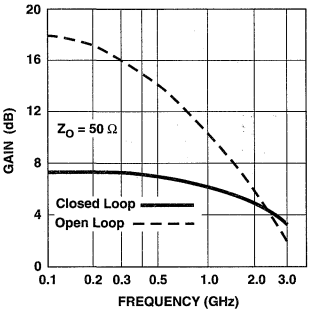
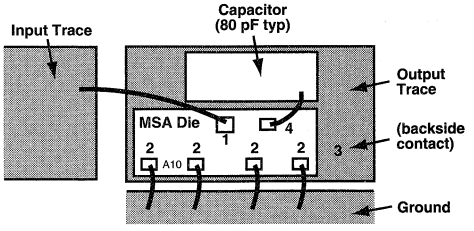


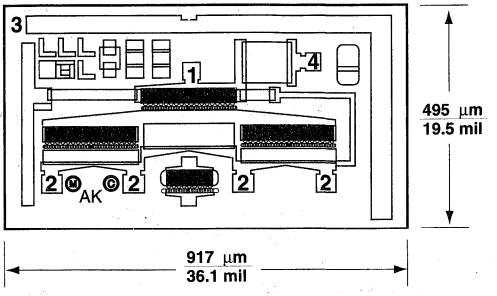
Figure 4. Gain vs. Frequency, I_d = 325 mA.

MSA-1000 Bonding Diagram



Numbers refer to pin contacts listed on the Chip Outline.

MSA-1000 Chip Dimensions



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils. Chip thickness is 114 µm/4.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side.

Note 1: Output contact is made by die attaching the backside of the die.

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-1023

Features

- **High Output Power:** +27 dBm Typical P_{1dB} at 1.0 GHz
- **Low Distortion:** 37 dBm Typical IP_3 at 1.0 GHz
- **8.5 dB Typical Gain at 1.0 GHz**
- **Hermetic, Metal/Beryllia Stripline Package**
- **Impedance Matched to 25 Ω for Push-Pull Configurations**

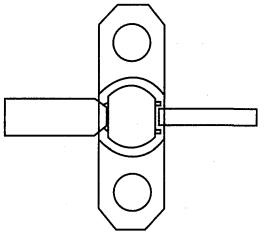
Description

The MSA-1023 is a high performance, medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, BeO flange package for good thermal characteristics.

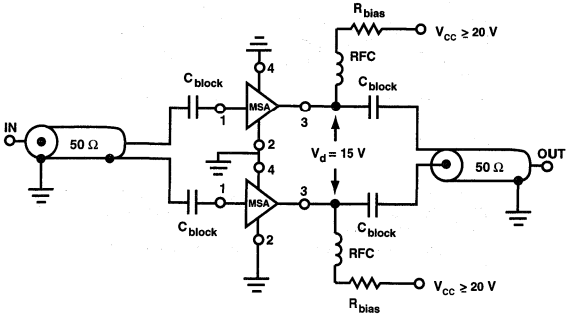
This MMIC is designed for use in a push-pull configuration in a 25 Ω system. The MSA-1023 can also be used as a single-ended amplifier in a 50 Ω system with slightly reduced performance. Typical applications include narrow and broadband RF amplifiers in industrial and military systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

230 mil BeO Flange Package



Typical Push-Pull Biasing Configuration



MSA-1023 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	425 mA
Power Dissipation[2,3]	7.0 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 15°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 66.7 mW/°C for T_C > 95°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 325 mA, Z_O = 25 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.0 GHz	dB	7.5	8.5	9.5
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.0 GHz			2.8:1	
NF	25 Ω Noise Figure	f = 1.0 GHz	dB		7.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz	dBm	25.0	27.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		37.0	
t_D	Group Delay	f = 1.0 GHz	psec		250	
V_d	Device Voltage		V	13.5	15.0	16.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–18.0	

Notes:
1. The recommended operating current range for this device is 150 to 400 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz gain (G_P).

MSA-1023 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 325 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.001	.40	–121	15.3	5.85	149	–17.9	.128	22	.42	–99	0.69
0.005	.51	–167	8.5	2.67	156	–15.9	.160	6	.45	–161	1.05
0.010	.52	–174	7.5	2.36	166	–15.8	.162	3	.45	–171	1.16
0.025	.52	–178	7.2	2.28	172	–15.8	.162	1	.45	–177	1.20
0.050	.52	179	7.1	2.26	173	–15.8	.161	–1	.45	–179	1.21
0.100	.53	176	7.0	2.25	170	–15.8	.161	–3	.45	179	1.21
0.200	.53	172	7.0	2.25	163	–15.8	.161	–5	.46	174	1.21
0.400	.51	164	7.0	2.24	146	–15.8	.161	–11	.46	170	1.22
0.600	.48	157	7.0	2.24	130	–16.0	.159	–16	.45	165	1.23
0.800	.45	151	7.0	2.23	113	–16.1	.157	–21	.44	161	1.24
1.000	.42	146	7.0	2.23	95	–16.2	.155	–26	.44	157	1.24
1.200	.38	144	6.9	2.22	78	–16.4	.151	–31	.44	155	1.24
1.400	.35	145	6.8	2.20	61	–16.7	.146	–36	.45	154	1.24
1.600	.34	149	6.6	2.15	44	–17.0	.141	–41	.46	153	1.22
1.800	.36	152	6.3	2.07	19	–17.3	.136	–45	.49	150	1.18
2.000	.39	153	5.9	1.97	11	–17.7	.130	–49	.62	148	1.13
2.500	.51	148	4.6	1.69	–24	–18.3	.121	–52	.52	140	.91
3.000	.60	133	3.0	1.41	–57	–17.9	.127	–57	.70	128	.59

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

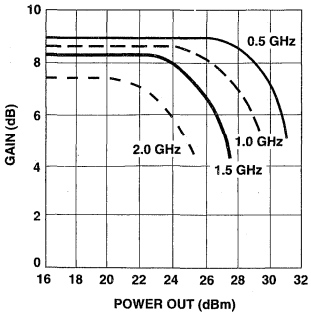


Figure 1. Typical Gain vs. Power Out, Z_O = 25° Ω, I_d = 325 mA.

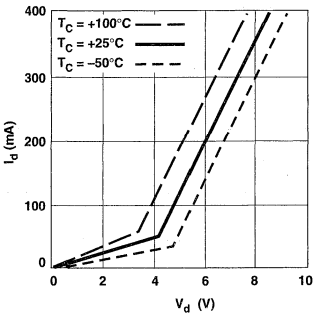


Figure 2. Device Current vs. Voltage.

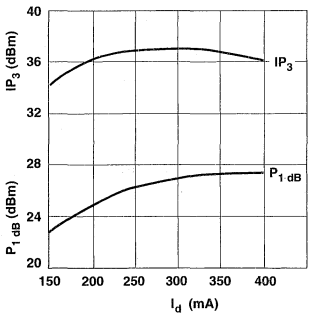


Figure 3. Output Power at 1 dB Gain Compression, Third Order Intercept Point vs. Current, Z_O = 25 Ω, f = 1.0 GHz.

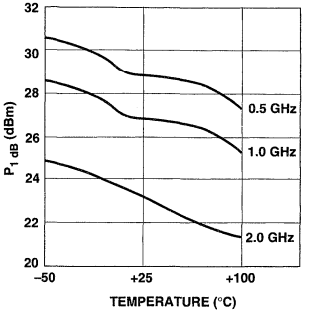


Figure 4. Output Power at 1 dB Gain Compression vs. Temperature, Z_O = 25 Ω, I_d = 325 mA.

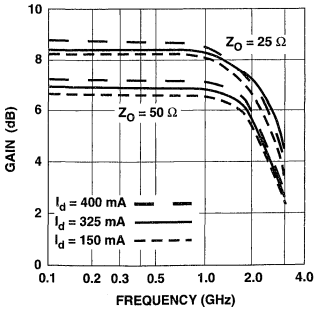


Figure 5. Gain vs. Frequency, I_d = 325 mA.

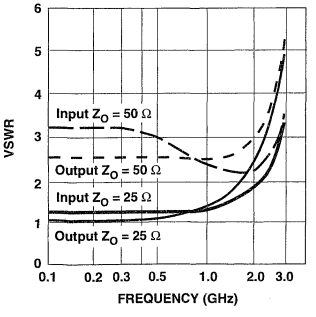
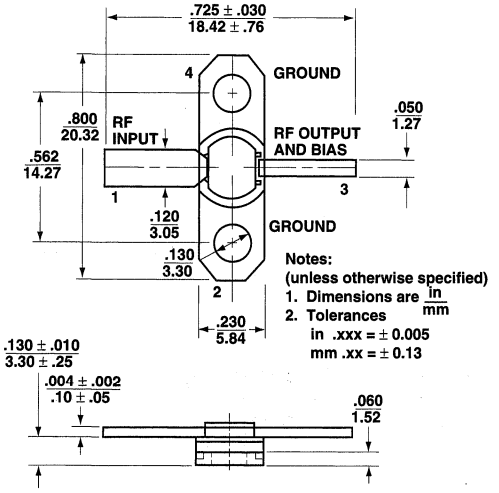


Figure 6. VSWR vs. Frequency, I_d = 325 mA.

230 mil BeO Flange Package



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-1100

Features

- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth:** 50 MHz to 1.6 GHz
- **17.5 dBm Typical P_{1dB} at 0.5 GHz**
- **12 dB Typical 50 Ω Gain at 0.5 GHz**
- **3.5 dB Typical Noise Figure at 0.5 GHz**

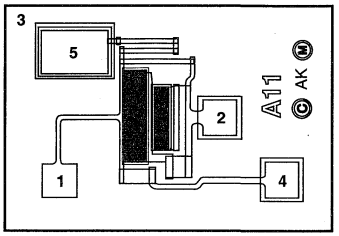
Description

The MSA-1100 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broadband linear amplifiers in industrial and military systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.

Chip Outline[1]

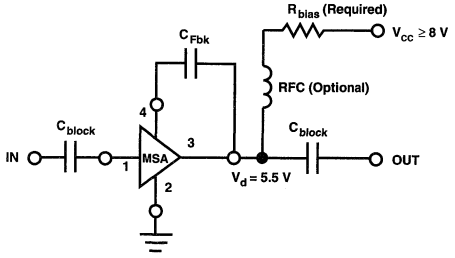


This chip is intended to be used with an external blocking capacitor completing the shunt feedback path (closed loop). Data sheet characterization is given for a 200 pF capacitor. Low frequency performance can be extended by using a larger valued capacitor.[1]

Note:

1. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



MSA-1100 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	100 mA
Power Dissipation[2,3]	650 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc}[2] = 57°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 17.5 mW/°C for $T_{Mounting\ Surface}$ > 163°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 60 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±0.7	
$f_{3\ dB}$	3 dB Bandwidth[3]		GHz		1.6	
VSWR	Input VSWR	f = 0.1 to 1.0 GHz			1.7:1	
	Output VSWR	f = 0.1 to 1.0 GHz			1.9:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		17.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30.0	
t_D	Group Delay	f = 0.5 GHz	psec		125	
V_d	Device Voltage		V	4.5	5.5	6.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 40 to 75 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
3. Referenced from 0.05 GHz gain (G_P).

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-1100-GP4	100

MSA-1100 Typical Scattering Parameters[1,2] (T_A = 25°C, I_d = 60 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.001	.72	–26	19.3	9.23	168	–23.4	.067	46	.72	–27	.52
0.005	.19	–73	14.1	5.09	165	–16.7	.147	11	.19	–77	.96
0.010	.16	–69	13.9	4.97	168	–16.6	.148	9	.16	–79	.99
0.050	.04	–59	12.8	4.39	175	–16.0	.159	3	.04	–102	1.06
0.100	.05	–66	12.8	4.38	175	–16.0	.158	2	.05	–100	1.06
0.200	.07	–78	12.8	4.36	170	–15.9	.161	4	.08	–100	1.05
0.400	.14	–92	12.7	4.31	162	–15.6	.165	7	.14	–105	1.01
0.600	.19	–102	12.5	4.22	153	–15.3	.171	10	.21	–111	.96
0.800	.25	–110	12.3	4.11	144	–14.9	.180	13	.27	–116	.90
1.000	.31	–117	12.0	4.00	137	–14.4	.190	14	.33	–122	.83
1.500	.40	–132	10.9	3.52	117	–13.4	.214	15	.42	–136	.70
2.000	.47	–145	9.6	3.01	100	–12.6	.235	14	.46	–148	.64
2.500	.50	–150	8.3	2.60	89	–12.0	.251	16	.45	–152	.63
3.000	.52	–158	7.0	2.23	77	–11.6	.263	17	.42	–156	.66
3.500	.51	–164	5.7	1.92	68	–11.1	.278	19	.38	–155	.73
4.000	.50	–169	4.6	1.70	61	–10.5	.297	22	.34	–152	.79

Notes:

1. S-parameters are de-embedded from 200 mil BeO package measured data using the package model found in the DEVICE MODELS section.
2. S-parameter data assumes an external 200 pF capacitor. Low frequency performance can be extended using a larger valued capacitor.

Typical Performance, T_A = 25°C

(Unless otherwise noted, performance is for a MSA-1100 used with an external 200 pF capacitor. See bonding diagram.)

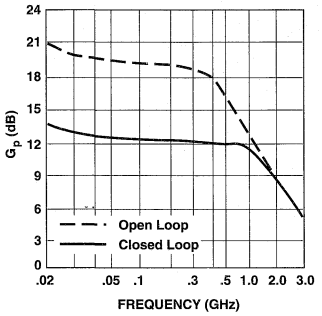


Figure 1. Typical Power Gain vs. Frequency, I_d = 60 mA.

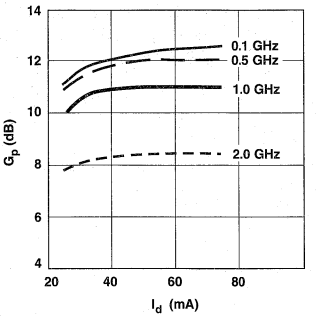


Figure 2. Power Gain vs. Current.

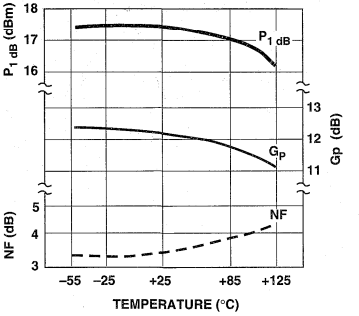


Figure 3. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 60 mA.

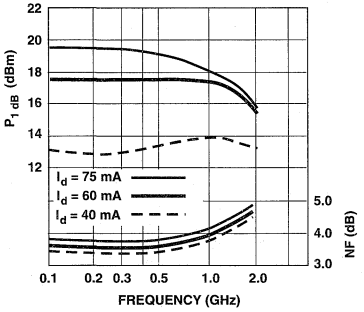
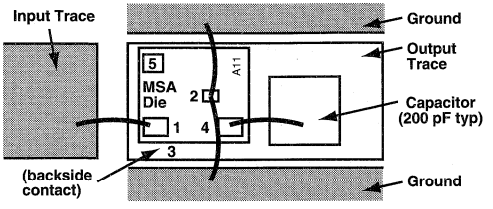


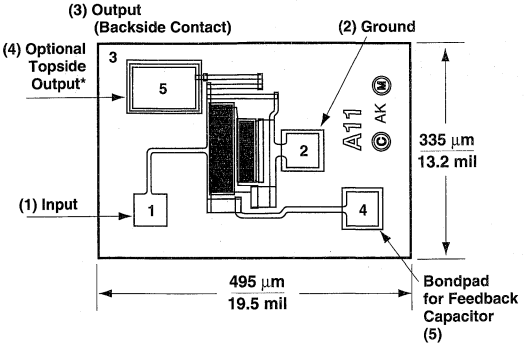
Figure 4. Output Power at 1 dB Gain Compression and Noise Figure vs. Frequency.

MSA-1100 Bonding Diagram



Numbers refer to pin contacts listed on the Chip Outline.

MSA-1100 Chip Dimensions



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils. Chip thickness is 114 µm/4.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side.

*** Output contact is made by die attaching the backside of the die.**

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-1104

Features

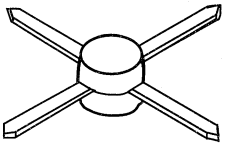
- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth:** 50 MHz to 1.3 GHz
- **17.5 dBm Typical $P_{1\ dB}$ at 0.5 GHz**
- **12 dB Typical 50 Ω Gain at 0.5 GHz**
- **3.6 dB Typical Noise Figure at 0.5 GHz**
- **Low Cost Plastic Package**

Description

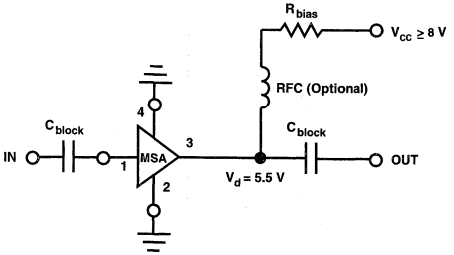
The MSA-1104 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broadband linear amplifiers in commercial and industrial systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package



Typical Biasing Configuration



MSA-1104 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	550 mW
RF Input Power	+1 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 115°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 8.7 mW/°C for T_C > 87°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 60 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.05 GHz	dB		12.7	
		f = 0.5 GHz	dB	10.0	12.0	
		f = 1.0 GHz	dB		10.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±1.0	
$f_{3\ dB}$	3 dB Bandwidth[2]		GHz		1.3	
VSWR	Input VSWR	f = 0.1 to 1.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 1.0 GHz			1.7:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.6	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		17.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30	
t_D	Group Delay	f = 0.5 GHz	psec		200	
V_d	Device Voltage		V	4.4	5.5	6.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 40 to 70 mA. Typical performance as a function of current is on the following page.
2. Referenced from 50 MHz gain (G_P).

MSA-1104 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 60 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
.0005	.76	–22	19.3	9.19	167	–24.4	.060	54	.77	–22	0.48
.005	.20	–79	13.7	4.83	164	–16.5	.149	12	.21	–83	0.96
.025	.05	–78	12.8	4.35	174	–16.2	.154	2	.06	–101	1.07
.050	.04	–75	12.7	4.31	174	–16.4	.151	2	.05	–136	1.09
.100	.04	–81	12.6	4.29	171	–16.4	.152	2	.05	–137	1.09
.200	.04	–93	12.6	4.24	164	–16.3	.153	3	.07	–135	1.09
.300	.06	–105	12.4	4.18	156	–16.2	.155	4	.10	–136	1.08
.400	.07	–115	12.3	4.11	148	–16.0	.158	5	.12	–139	1.07
.500	.09	–124	12.1	4.01	141	–15.8	.162	6	.15	–144	1.06
.600	.11	–132	11.8	3.91	134	–15.6	.166	7	.17	–150	1.06
.700	.13	–140	11.6	3.80	126	–15.4	.170	7	.19	–156	1.05
.800	.15	–147	11.3	3.68	120	–15.2	.174	7	.22	–161	1.04
.900	.16	–154	11.0	3.56	113	–14.9	.180	7	.24	–168	1.03
1.000	.18	–161	10.7	3.43	106	–14.7	.184	6	.26	–173	1.03
1.500	.28	171	9.1	2.85	77	–13.5	.211	2	.35	163	0.99
2.000	.37	149	7.6	2.39	52	–13.0	.224	–5	.43	140	0.99
2.500	.45	133	6.1	2.02	33	–12.7	.231	–10	.47	125	1.02
3.000	.52	118	4.6	1.69	14	–12.6	.234	–16	.50	112	1.05

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C, Z_O = 50 Ω

(unless otherwise noted)

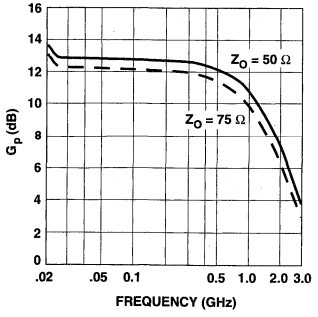


Figure 1. Typical Power Gain vs. Frequency, I_d = 60 mA.

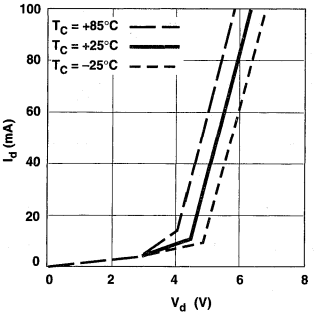


Figure 2. Device Current vs. Voltage.

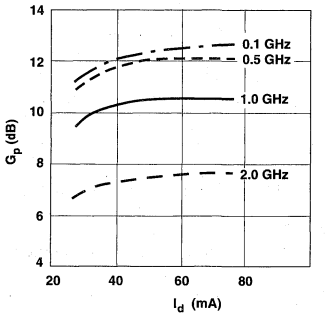


Figure 3. Power Gain vs. Current.

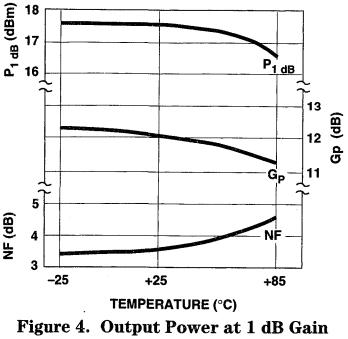


Figure 4. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 60 mA.

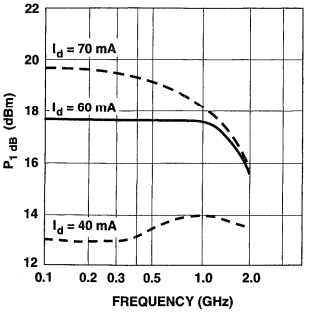


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

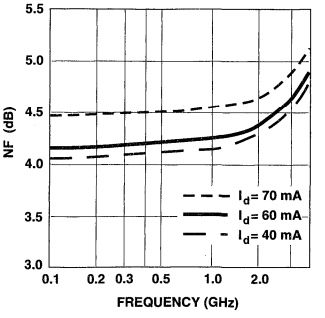
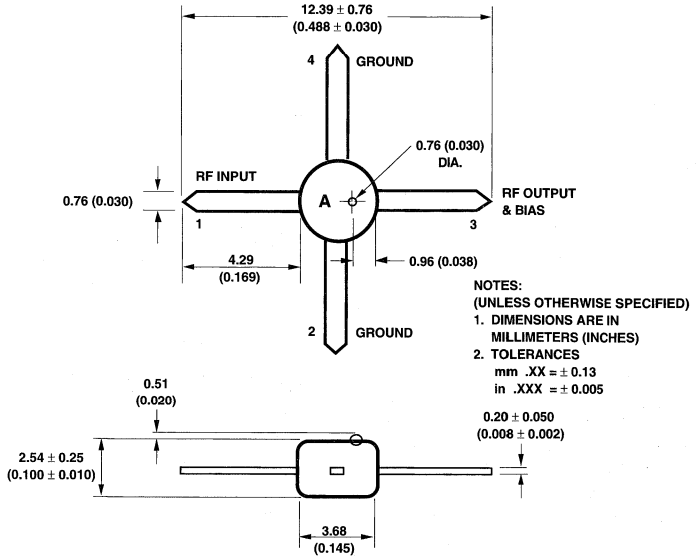


Figure 6. Noise Figure vs. Frequency.

04A Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES).

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-1105

Features

- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth:** 50 MHz to 1.3 GHz
- **17.5 dBm Typical $P_{1\ dB}$ at 0.5 GHz**
- **3.6 dB Typical Noise Figure at 0.5 GHz**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Note:

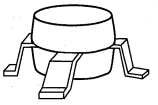
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."

Description

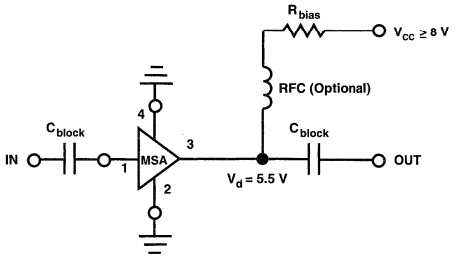
The MSA-1105 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broadband linear amplifiers in commercial and industrial systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

05 Plastic Package



Typical Biasing Configuration



MSA-1105 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	550 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
θ_{jc} = 125°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 8 mW/°C for T_C > 124°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 60 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.05 GHz f = 0.5 GHz f = 1.0 GHz	dB dB dB	 10.0	12.7 12.0 10.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±1.0	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		1.3	
VSWR	Input VSWR	f = 0.1 to 1.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 1.0 GHz			1.7:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.6	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		17.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30.0	
t_D	Group Delay	f = 0.5 GHz	psec		200	
V_d	Device Voltage		V	4.4	5.5	6.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 40 to 70 mA. Typical performance as a function of current is on the following page.
2. Referenced from 50 MHz gain (G_P).

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-1105-TR1	500	7" Reel
MSA-1105-STR	10	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-1105 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 60 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
.0005	.80	–17	19.0	8.94	171	–26.0	.050	51	.81	–16	0.53
.005	.26	–62	13.9	4.98	163	–16.8	.144	15	.26	–64	0.93
.025	.07	–48	12.8	4.36	174	–16.4	.151	4	.08	–52	1.08
.050	.06	–38	12.7	4.33	174	–16.3	.153	2	.06	–48	1.08
.100	.05	–41	12.7	4.31	170	–16.4	.152	3	.06	–52	1.09
.200	.06	–58	12.6	4.26	162	–16.2	.155	5	.08	–73	1.08
.300	.07	–74	12.4	4.19	154	–16.1	.157	7	.10	–91	1.07
.400	.09	–91	12.2	4.10	146	–15.8	.163	8	.12	–105	1.06
.500	.10	–105	12.0	4.00	138	–15.6	.166	8	.14	–116	1.05
.600	.11	–116	11.8	3.88	131	–15.4	.171	10	.17	–126	1.04
.700	.13	–128	11.5	3.76	123	–15.0	.178	11	.18	–135	1.03
.800	.15	–136	11.2	3.63	116	–14.7	.184	11	.21	–144	1.01
.900	.16	–145	10.9	3.49	109	–15.5	.188	11	.22	–151	1.01
1.000	.18	–152	10.5	3.37	102	–14.1	.197	11	.24	–159	1.00
1.500	.28	174	8.8	2.75	72	–13.2	.219	7	.31	170	1.00
2.000	.38	150	7.1	2.28	48	–12.1	.248	0	.34	151	0.99
2.500	.46	133	5.6	1.90	28	–11.9	.254	–4	.38	134	1.02
3.000	.53	118	4.2	1.62	11	–11.6	.262	–8	.40	122	1.04

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C, Z_O = 50 Ω

(unless otherwise noted)

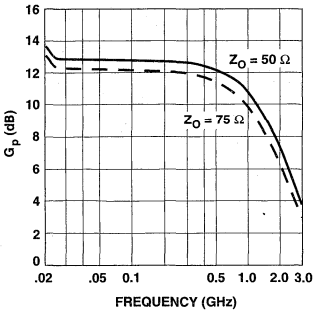


Figure 1. Typical Power Gain vs. Frequency, I_d = 60 mA.

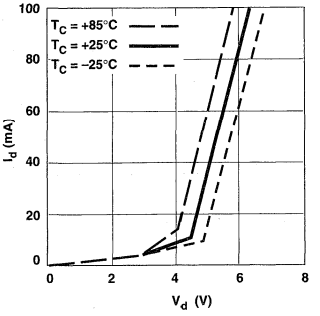


Figure 2. Device Current vs. Voltage.

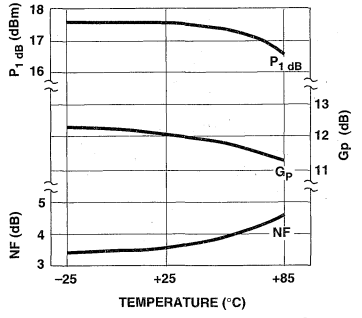


Figure 3. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 60 mA.

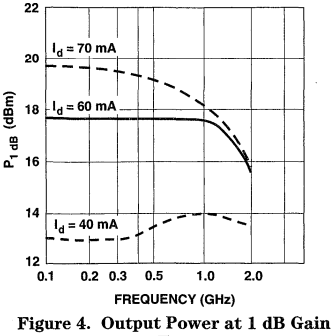


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

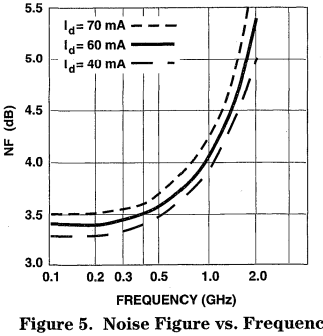
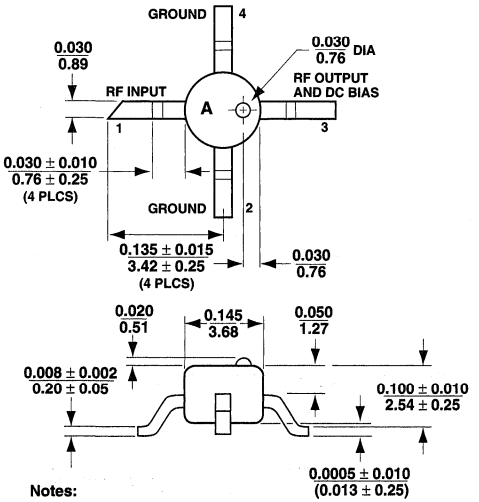


Figure 5. Noise Figure vs. Frequency.

05 Plastic Package Dimensions



Notes:
(unless otherwise specified)
1. Dimensions are $\frac{\text{in}}{\text{mm}}$
2. Tolerances
   in .xxx = ± 0.005
   mm .xx = ± 0.13

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-1110

Features

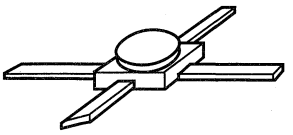
- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth:** 50 MHz to 1.6 GHz
- **17.5 dBm Typical $P_{1\,dB}$ at 0.5 GHz**
- **12 dB Typical 50 Ω Gain at 0.5 GHz**
- **3.5 dB Typical Noise Figure at 0.5 GHz**
- **Hermetic Gold-ceramic Microstrip Package**

Description

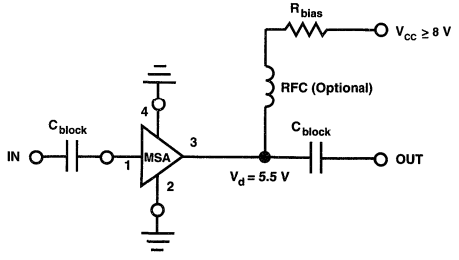
The MSA-1110 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic high reliability package. This MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broadband linear amplifiers in industrial and military systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

100 mil Package



Typical Biasing Configuration



MSA-1110 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	90 mA
Power Dissipation[2,3]	560 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 135°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 7.4 mW/°C for T_C > 124°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 60 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±0.7	±1.0
$f_{3\ dB}$	3 dB Bandwidth[2]		GHz		1.6	
VSWR	Input VSWR	f = 0.1 to 1.0 GHz			1.7:1	
	Output VSWR	f = 0.1 to 1.0 GHz			1.9:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.5	4.5
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm	16.0	17.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30.0	
t_D	Group Delay	f = 0.5 GHz	psec		160	
V_d	Device Voltage		V	4.5	5.5	6.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 40 to 75 mA. Typical performance as a function of current is on the following page.
2. Referenced from 50 MHz gain (G_P).

MSA-1110 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 60 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
.0005	.83	–7	19.5	9.44	176	–31.9	.025	39	.84	–7	0.77
.005	.54	–50	16.8	6.92	158	–18.7	.116	34	.55	–50	0.60
.025	.15	–78	13.0	4.47	167	–16.6	.148	9	.15	–79	1.03
.050	.10	–64	12.6	4.26	171	–16.5	.149	5	.10	–67	1.08
.100	.08	–63	12.5	4.23	171	–16.5	.150	4	.08	–66	1.09
.200	.09	–74	12.4	4.17	166	–16.4	.152	4	.09	–78	1.09
.300	.11	–85	12.3	4.10	160	–16.2	.154	5	.12	–89	1.07
.400	.13	–94	12.3	4.10	154	–16.1	.157	6	.15	–98	1.05
.500	.16	–102	12.1	4.04	148	–15.9	.161	7	.18	–106	1.02
.600	.18	–108	12.0	3.98	143	–15.6	.165	8	.20	–113	1.00
.700	.21	–114	11.8	3.89	137	–15.4	.169	8	.23	–120	0.97
.800	.23	–120	11.6	3.80	131	–15.2	.173	8	.25	–126	0.95
.900	.25	–126	11.4	3.71	126	–15.0	.178	8	.28	–132	0.92
1.000	.27	–131	11.1	3.60	120	–14.8	.182	8	.30	–137	0.91
1.500	.36	–153	9.8	3.10	96	–13.8	.203	4	.37	–160	0.83
2.000	.42	–171	8.4	2.64	74	–13.3	.217	1	.40	–178	0.82
2.500	.47	177	7.2	2.29	59	–12.5	.236	–2	.41	172	0.80
3.000	.47	159	5.9	1.97	43	–13.2	.220	–10	.38	157	0.95

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C, Z_O = 50 Ω

(unless otherwise noted)

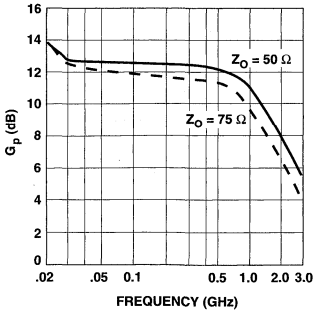


Figure 1. Typical Power Gain vs. Frequency, I_d = 60 mA.

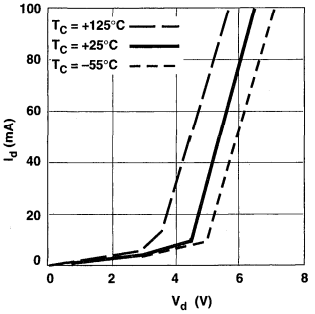


Figure 2. Device Current vs. Voltage.

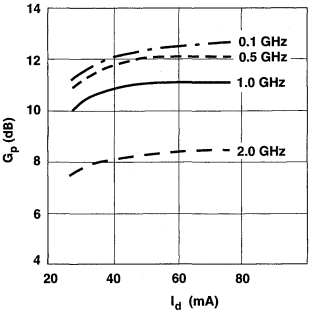


Figure 3. Power Gain vs. Current.

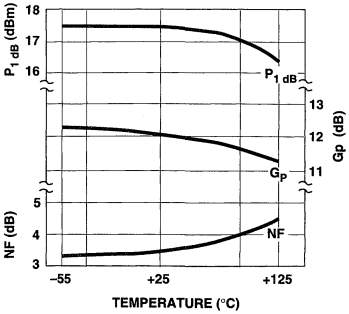


Figure 4. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 60 mA.

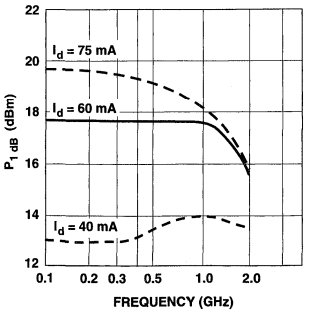


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

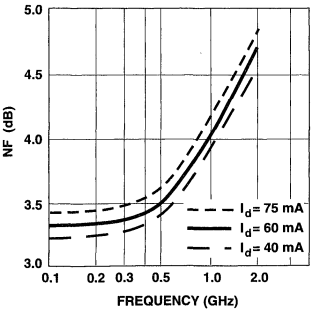
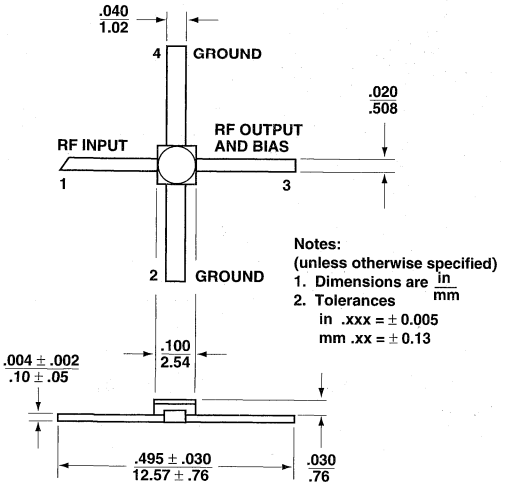


Figure 6. Noise Figure vs. Frequency.

100 mil Package Dimensions



HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-1120

Features

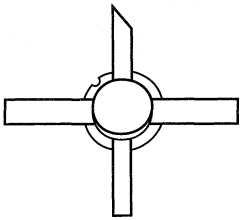
- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth:** 50 MHz to 1.6 GHz
- **17.5 dBm Typical $P_{1\ dB}$ at 0.5 GHz**
- **12 dB Typical 50 Ω Gain at 0.5 GHz**
- **3.5 dB Typical Noise Figure at 0.5 GHz**
- **Hermetic Metal/Beryllia Microstrip Package**

Description

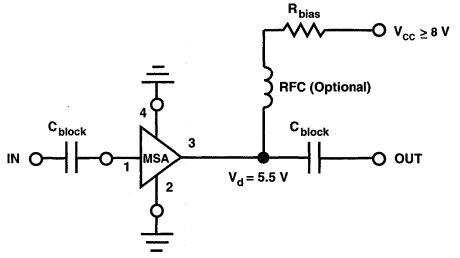
The MSA-1120 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic BeO disk package for good thermal characteristics. This MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broadband linear amplifiers in industrial and military systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

200 mil BeO Package



Typical Biasing Configuration



MSA-1120 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	100 mA
Power Dissipation[2,3]	650 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 60°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 16.7 mW/°C for T_C > 161°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 60 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±0.7	±1.0
$f_{3\ dB}$	3 dB Bandwidth[2]		GHz		1.6	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.9:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.5	4.5
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm	16.0	17.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30.0	
t_D	Group Delay	f = 0.5 GHz	psec		200	
V_d	Device Voltage		V	4.5	5.5	6.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 40 to 75 mA. Typical performance as a function of current is on the following page.
2. Referenced from 50 MHz gain (G_P).

MSA-1120 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 60 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
.0005	.78	–21	19.6	9.53	168	–25.1	.057	50	.79	–21	0.51
.005	.19	–72	13.8	4.91	165	–16.8	.144	11	.19	–72	0.98
.025	.05	–56	12.9	4.44	174	–16.5	.149	3	.06	–75	1.08
.050	.04	–52	12.5	4.23	174	–16.1	.156	2	.04	–79	1.08
.100	.04	–56	12.5	4.22	172	–16.2	.155	1	.04	–78	1.09
.200	.05	–72	12.4	4.19	165	–16.1	.157	1	.06	–91	1.08
.300	.07	–84	12.4	4.15	158	–16.0	.159	2	.09	–101	1.07
.400	.09	–96	12.3	4.10	151	–15.9	.161	2	.11	–109	1.06
.500	.10	–105	12.1	4.04	144	–15.8	.163	3	.13	–117	1.05
.600	.12	–113	12.0	3.98	137	–15.6	.166	3	.16	–124	1.04
.700	.14	–120	11.8	3.89	131	–15.4	.169	2	.18	–130	1.03
.800	.15	–127	11.6	3.80	124	–15.2	.173	2	.20	–136	1.01
.900	.17	–134	11.4	3.71	118	–15.0	.178	1	.22	–142	1.00
1.000	.19	–140	11.1	3.60	112	–14.8	.181	2	.24	–148	0.99
1.500	.25	–167	9.8	3.10	83	–14.0	.200	–3	.31	–174	0.95
2.000	.31	171	8.4	2.64	58	–13.3	.216	–10	.35	163	0.95
2.500	.35	157	7.3	2.31	39	–12.8	.228	–16	.36	148	0.96
3.000	.40	140	6.1	2.02	19	–12.5	.236	–23	.36	134	0.99

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C, Z_O = 50 Ω

(unless otherwise noted)

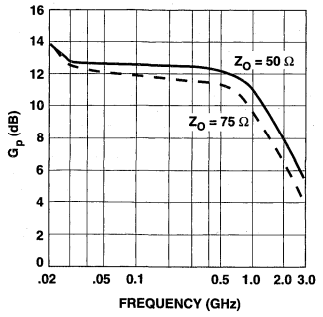


Figure 1. Typical Power Gain vs. Frequency, I_d = 60 mA.

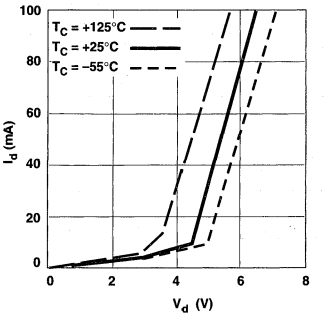


Figure 2. Device Current vs. Voltage.

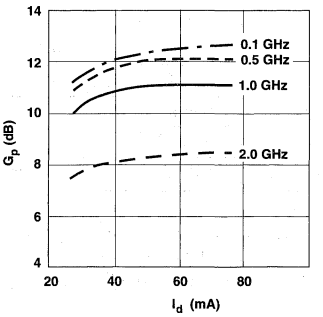


Figure 3. Power Gain vs. Current.

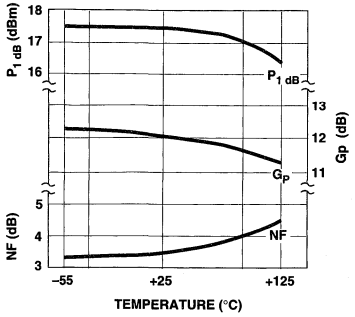


Figure 4. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 60 mA.

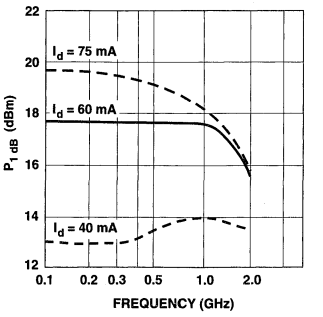


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

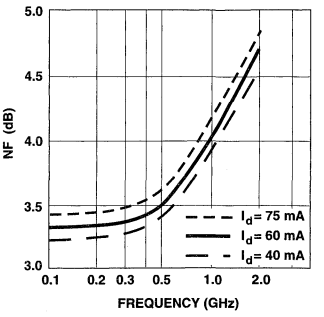
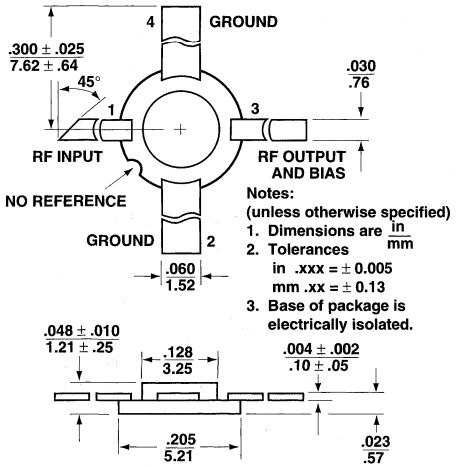


Figure 6. Noise Figure vs. Frequency.

200 mil BeO Package Dimensions



Package marking code is "A11"

HEWLETT® PACKARD

Silicon Bipolar RFIC Amplifiers

Technical Data

MSA-20XX Series

Features

MSA-2011

- **Surface Mount SOT-143 Package**
- **3 dB Bandwidth:** DC to 1.0 GHz
- **16.2 dB Gain at 1 GHz**
- **4.3 dB NF at 1 GHz**

MSA-2035

- **Hermetic Ceramic Package**
- **3 dB Bandwidth:** DC to 1.1 GHz
- **17.3 dB Gain at 1 GHz**
- **3.7 dB NF at 1 GHz**

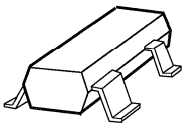
MSA-2085

- **Plastic Microstrip Package**
- **3 dB Bandwidth:** DC to 1.1 GHz
- **16.6 dB Gain at 1 GHz**
- **3.7 dB NF at 1 GHz**

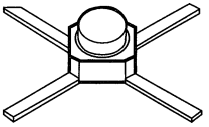
MSA-2086

- **Surface Mount Plastic Microstrip Package**
- **3 dB Bandwidth:** DC to 1.1 GHz
- **16.6 dB Gain at 1 GHz**
- **3.7 dB NF at 1 GHz**

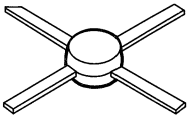
MSA-2011



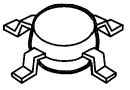
MSA-2035



MSA-2085



MSA-2086



Description

The MSA-20XX series are high performance silicon bipolar RFIC amplifiers designed to be cascadable in 50 Ω systems. The stability factor of K > 1 contributes to easy cascading in numerous narrow and broadband IF and RF commercial and industrial applications.

The MSA series is fabricated using a 10 GHz f_T, 25 GHz F_{MAX}, silicon bipolar RFIC process which utilizes nitride self-alignment, ion implantation, and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

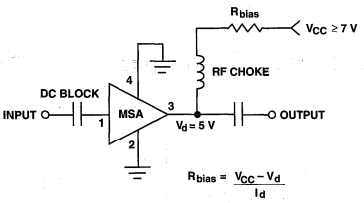
Package options include the industry standard plastic surface mount SOT-143 package, the 100 mil surface mountable hermetic ceramic package, the 85 mil plastic microstripline package, and the 85 mil surface mountable plastic microstripline package.

Absolute Maximum Ratings[1]

Parameter	MSA-2011	MSA-2035	MSA-2085, -2086
Device Current	50 mA	60 mA	60 mA
Power Dissipation[2,3]	250 mW[3a]	325 mW[3b]	325 mW[3c]
RF Input Power	+13 dBm	+13 dBm	+13 dBm
Junction Temperature	150°C	200°C	150°C
Storage Temperature	-65 to 150°C	-65 to 200°C	-65 to 150°C
Thermal Resistance: θ_{jc}	500°C/W	155°C/W	115°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3a. Derate at 2.0 mW/°C for T_C > 25°C.
b. Derate at 6.5 mW/°C for T_C > 149°C.
c. Derate at 8.7 mW/°C for T_C > 112°C.

Typical Biasing Configuration



Electrical Specifications, T_A = 25°C

I_D = 32 mA, Z_o = 50 Ω

Symbol	Parameters and Test Conditions	Units	MSA-2011 Min.	MSA-2011 Typ.	MSA-2011 Max.	MSA-2035 Min.	MSA-2035 Typ.	MSA-2035 Max.	MSA-2085, -2086 Min.	MSA-2085, -2086 Typ.	MSA-2085, -2086 Max.
G_P	Power Gain ($\|S_{21}\|^2$)										
	f = 0.1 GHz	dB		18.9		17.8	19.2	19.8		19.2	
	f = 0.5 GHz			18.1			18.7			18.3	
	f = 1.0 GHz		15.0	16.2			17.3		15.0	16.6	
ΔG_P	Gain Flatness f = 0.1 to 0.6 GHz	dB		±0.6			±0.4	±1.0		±0.6	
f_{3dB}	3 dB Bandwidth	GHz		1.0			1.1			1.1	
VSWR	Input VSWR f = 0.1 to 3.0 GHz			1.3:1			1.3:1			1.2:1	
	Output VSWR f = 0.1 to 3.0 GHz			1.4:1			1.4:1			1.5:1	
P_{1dB}	Power Output @ 1 dB Gain Compression: f = 1.0 GHz	dBm		9.0			9.5			9.0	
NF	50 Ω Noise Figure f = 1.0 GHz	dB		4.3			3.7			3.7	
IP_3	Third Order Intercept Point f = 1.0 GHz	dBm		22			22			22	
t_d	Group Delay f = 1.0 GHz	psec		143			143			143	
V_D	Device Voltage T_C = 25°C	V	4.0	5.0	6.0	4.5	5.0	5.5	4.3	5.0	6.3
dV/dT	Device Voltage Temperature Coefficient	mV/°C		-9.3			-9.3			-9.3	

Note:
1. Refer to "Tape and Reel Packaging for Surface Mount Devices."

Typical Performance for MSA-2011

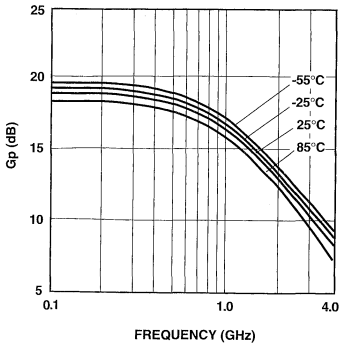


Figure 1. Power Gain vs. Frequency at Four Temperatures, I_D = 32 mA.

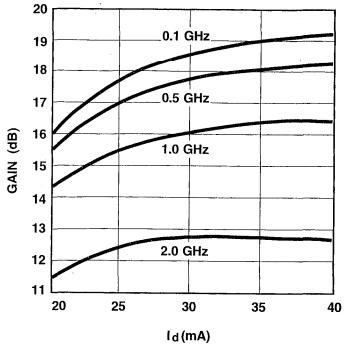


Figure 2. Power Gain vs. Current at 25°C.

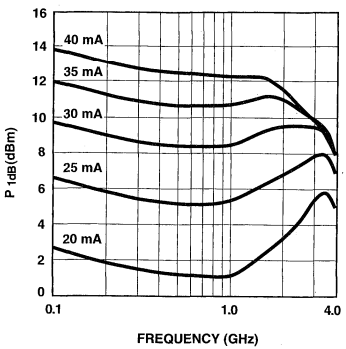


Figure 3. Typical P_{1dB} vs. Frequency at 25°C.

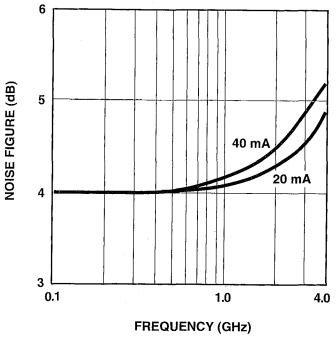


Figure 4. Noise Figure vs. Frequency at I_D = 32 mA.

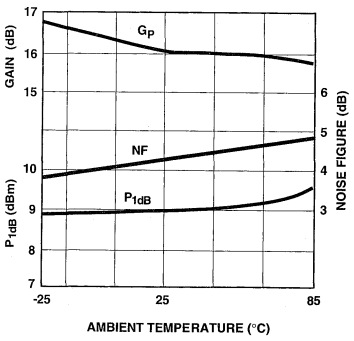


Figure 5. Power Gain, Noise Figure, and P_{1dB} vs. Temperature at 1 GHz and I_D = 32 mA.

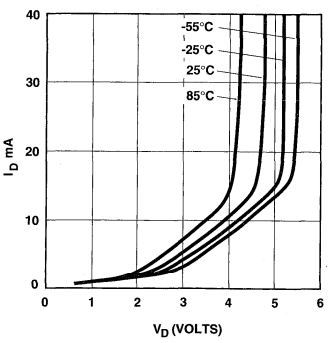


Figure 6. I_D vs. V_D at Four Temperatures.

Typical Performance for MSA-2035

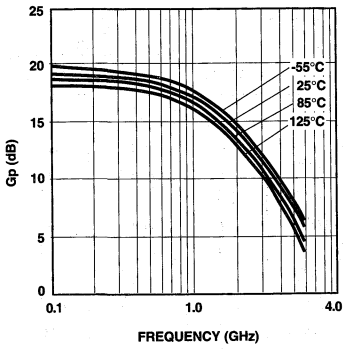


Figure 1. Power Gain vs. Frequency at Four Temperatures, I_D = 32 mA.

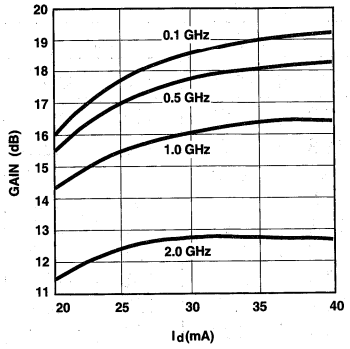


Figure 2. Power Gain vs. Current at 25°C.

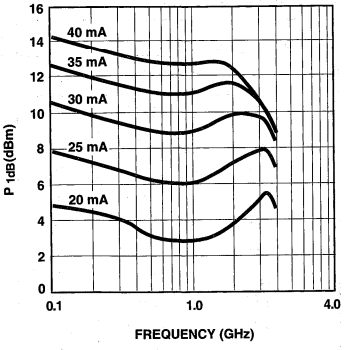


Figure 3. Typical P_{1dB} vs. Frequency at 25°C.

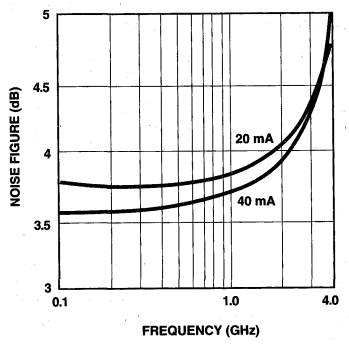


Figure 4. Noise Figure vs. Frequency at I_D = 32 mA.

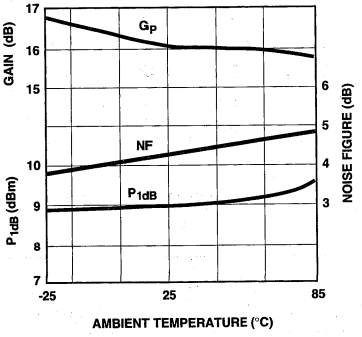


Figure 5. Power Gain, Noise Figure, and P_{1dB} vs. Temperature at 1 GHz and I_D = 32 mA.

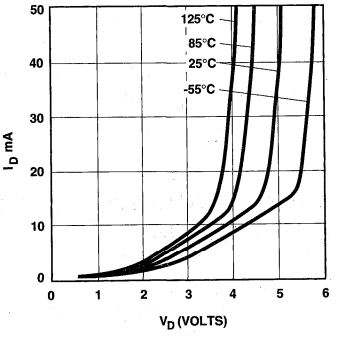


Figure 6. I_D vs. V_D at Four Temperatures.

Typical Scattering Parameters at T_A = 25°C, for MSA-2011

I_D = 32 mA, Z_o = 50 Ω

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.1	0.05	7	18.9	8.81	172	-22.6	0.074	4	0.17	-13
0.2	0.05	9	18.8	8.73	165	-22.4	0.076	8	0.17	-23
0.3	0.06	3	18.6	8.52	157	-22.2	0.077	11	0.17	-34
0.4	0.06	1	18.3	8.25	150	-22.0	0.079	15	0.17	-43
0.5	0.06	0	18.1	8.00	143	-21.7	0.082	17	0.17	-52
0.6	0.07	-5	17.7	7.65	137	-21.4	0.085	20	0.17	-61
0.7	0.07	-8	17.3	7.33	131	-21.1	0.088	22	0.17	-68
0.8	0.08	-12	16.9	7.02	125	-20.7	0.092	24	0.17	-74
0.9	0.08	-18	16.3	6.70	120	-20.3	0.096	26	0.18	-80
1.0	0.08	-22	16.2	6.43	115	-20.0	0.100	28	0.18	-85
1.5	0.09	-46	14.3	5.16	93	-18.2	0.123	31	0.18	-102
2.0	0.11	-69	12.6	4.26	75	-16.7	0.146	31	0.17	-109
2.5	0.11	-93	11.2	3.64	59	-15.6	0.167	29	0.17	-111
3.0	0.12	-118	10.1	3.18	45	-14.7	0.185	26	0.18	-112
3.5	0.12	-152	9.1	2.85	31	-13.9	0.202	24	0.19	-116
4.0	0.15	174	8.1	2.55	18	-13.3	0.216	21	0.20	-124
4.5	0.22	147	7.4	2.33	5	-12.8	0.231	19	0.22	-133
5.0	0.30	127	6.5	2.11	-8	-12.2	0.246	17	0.25	-145
5.5	0.39	113	5.6	1.90	-20	-11.4	0.268	14	0.30	-157
6.0	0.45	100	4.5	1.68	-32	-10.7	0.292	10	0.35	-168

Typical Scattering Parameters at T_A = 25°C, for MSA-2035

I_D = 32 mA, Z_o = 50 Ω

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.1	0.05	-2	19.2	9.13	174	-22.8	0.072	3	0.18	-11
0.2	0.06	-3	19.1	9.05	167	-22.7	0.073	6	0.18	-20
0.3	0.06	-7	19.0	8.94	160	-22.6	0.075	9	0.18	-29
0.4	0.06	-10	18.9	8.77	154	-22.4	0.076	11	0.18	-38
0.5	0.06	-14	18.7	8.58	147	-22.2	0.078	14	0.18	-47
0.6	0.07	-22	18.4	8.35	141	-21.9	0.080	16	0.17	-55
0.7	0.07	-27	18.2	8.10	135	-21.6	0.083	17	0.17	-63
0.8	0.07	-32	17.9	7.86	130	-21.3	0.086	19	0.17	-71
0.9	0.07	-37	17.6	7.59	124	-21.0	0.089	20	0.17	-79
1.0	0.07	-42	17.3	7.33	119	-20.7	0.092	22	0.16	-86
1.5	0.08	-74	15.7	6.11	96	-19.1	0.111	24	0.16	-117
2.0	0.09	-108	14.2	5.15	76	-17.8	0.130	23	0.16	-140
2.5	0.12	-136	12.9	4.42	59	-16.6	0.148	20	0.15	-155
3.0	0.15	-162	11.7	3.86	43	-15.7	0.164	16	0.15	-169
3.5	0.19	176	10.7	3.41	27	-15.1	0.176	11	0.16	-178
4.0	0.25	158	9.7	3.04	12	-14.6	0.187	7	0.17	177
4.5	0.30	141	8.7	2.71	-1	-14.1	0.196	3	0.19	171
5.0	0.37	126	7.8	2.44	-16	-13.8	0.204	-1	0.22	161
5.5	0.43	112	6.8	2.17	-29	-13.5	0.212	-5	0.29	154
6.0	0.49	100	5.7	1.92	-42	-13.1	0.222	-9	0.35	148

Typical Performance for MSA-2085 and MSA-2086

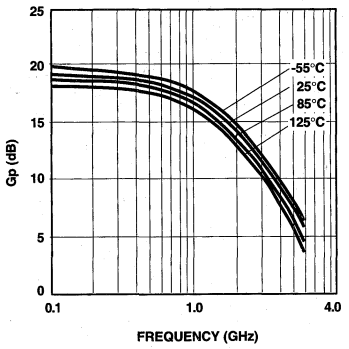


Figure 1. Power Gain vs. Frequency at Four Temperatures, I_D = 32 mA.

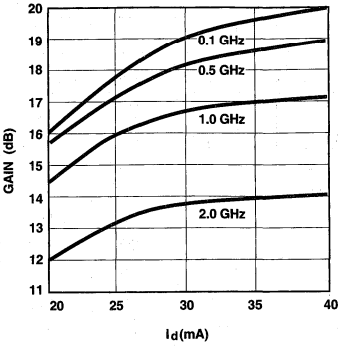


Figure 2. Power Gain vs. Current at 25°C.

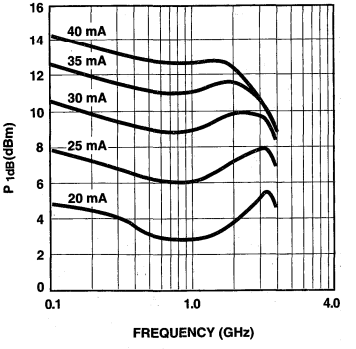


Figure 3. Typical P_{1dB} vs. Frequency at 25°C.

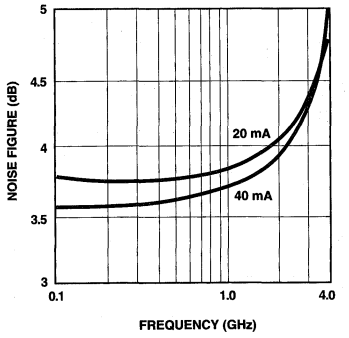


Figure 4. Noise Figure vs. Frequency at I_D = 32 mA.

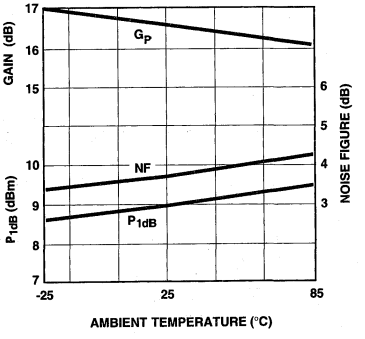


Figure 5. Power Gain, Noise Figure, and P_{1dB} vs. Temperature at 1 GHz and I_D = 32 mA.

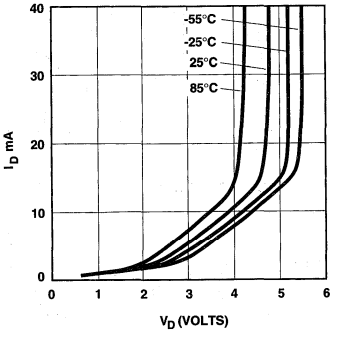


Figure 6. I_D vs. V_D at Four Temperatures.

Typical Scattering Parameters at T_A = 25°C, for MSA-2085

I_D = 32 mA, Z_o = 50 Ω

Frequency	S_{11}		S_{21}			S_{12}			S_{22}	
(GHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.1	0.05	4	19.2	9.11	173	-22.7	0.073	4	0.18	-14
0.2	0.05	-6	19.1	9.00	166	-22.6	0.075	8	0.18	-27
0.3	0.05	-14	18.9	8.79	159	-22.4	0.076	11	0.18	-38
0.4	0.07	-13	18.6	8.53	152	-22.2	0.078	14	0.19	-45
0.5	0.09	-17	18.3	8.26	146	-21.9	0.080	17	0.20	-51
0.6	0.08	-33	18.0	7.98	140	-21.6	0.083	19	0.21	-59
0.7	0.09	-44	17.7	7.71	135	-21.3	0.086	22	0.22	-68
0.8	0.09	-47	17.4	7.41	130	-20.9	0.090	24	0.22	-77
0.9	0.09	-54	17.0	7.06	125	-20.5	0.094	26	0.22	-85
1.0	0.10	-60	16.6	6.77	120	-20.2	0.098	27	0.22	-90
1.5	0.10	-78	14.9	5.58	99	-18.5	0.119	31	0.23	-116
2.0	0.13	-96	13.4	4.67	82	-17.1	0.140	31	0.21	-126
2.5	0.13	-113	12.0	3.97	67	-16.0	0.159	30	0.20	-137
3.0	0.14	-129	10.8	3.48	54	-15.0	0.177	27	0.20	-140
3.5	0.15	-153	9.8	3.10	41	-14.4	0.192	24	0.21	-143
4.0	0.18	-177	8.9	2.77	29	-13.9	0.202	22	0.22	-148
4.5	0.22	163	7.9	2.49	17	-13.5	0.212	19	0.24	-151
5.0	0.27	147	7.0	2.24	6	-13.2	0.218	17	0.28	-154
5.5	0.32	134	6.1	2.02	-5	-12.9	0.225	15	0.31	-159
6.0	0.37	123	5.2	1.82	-15	-12.6	0.235	14	0.35	-164

Typical Scattering Parameters at T_A = 25°C, for MSA-2086

I_D = 32 mA, Z_o = 50 Ω

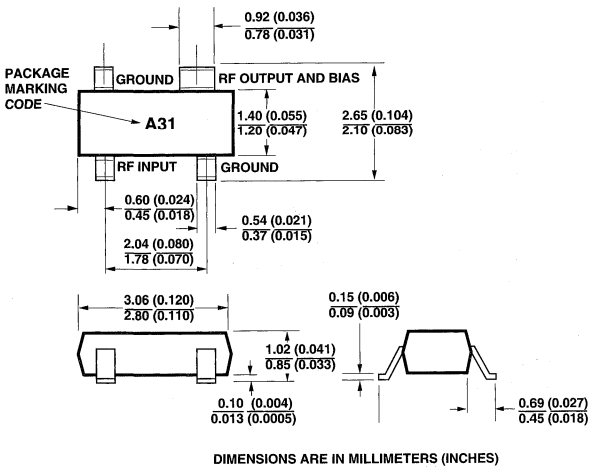
Frequency	S_{11}		S_{21}			S_{12}			S_{22}	
(GHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.1	0.06	1	19.2	9.08	172	-22.8	0.073	4	0.18	-15
0.2	0.05	-5	19.1	8.98	165	-22.6	0.074	7	0.17	-26
0.3	0.05	-10	18.9	8.80	157	-22.4	0.076	10	0.17	-37
0.4	0.07	-15	18.7	8.57	150	-22.2	0.078	13	0.19	-45
0.5	0.09	-18	18.4	8.29	143	-21.9	0.081	15	0.19	-53
0.6	0.09	-22	18.1	7.99	136	-21.6	0.084	18	0.20	-62
0.7	0.08	-23	17.7	7.66	130	-21.2	0.087	20	0.20	-71
0.8	0.08	-31	17.4	7.37	124	-20.8	0.091	21	0.20	-80
0.9	0.08	-34	17.0	7.07	118	-20.5	0.095	23	0.20	-87
1.0	0.08	-44	16.6	6.78	112	-20.1	0.099	23	0.19	-94
1.5	0.07	-71	14.8	5.49	88	-18.2	0.123	24	0.19	-125
2.0	0.06	-99	13.3	4.60	68	-16.7	0.146	22	0.17	-145
2.5	0.07	-176	11.9	3.93	50	-15.5	0.167	17	0.18	-174
3.0	0.14	151	10.7	3.42	31	-14.7	0.185	10	0.20	172
3.5	0.20	125	9.5	2.98	15	-14.2	0.196	3	0.24	153
4.0	0.29	106	8.3	2.61	-1	-13.8	0.204	-3	0.28	139
4.5	0.39	96	7.3	2.31	-15	-13.6	0.210	-8	0.32	129
5.0	0.51	90	6.3	2.08	-29	-13.3	0.217	-12	0.36	124
5.5	0.62	83	5.4	1.85	-43	-13.0	0.225	-16	0.40	119
6.0	0.69	75	4.3	1.64	-58	-12.7	0.233	-22	0.47	113

Tape and Reel Part Number Ordering Information

Part Number	Devices per Reel	Reel Size
MSA-2011-TR1	3000	7"
MSA-2086-TR1	1000	7"

Outline Drawings

SOT-143



DIMENSIONS ARE IN MILLIMETERS (INCHES)

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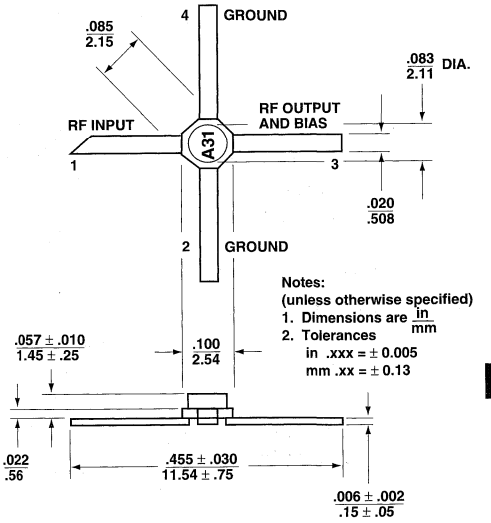

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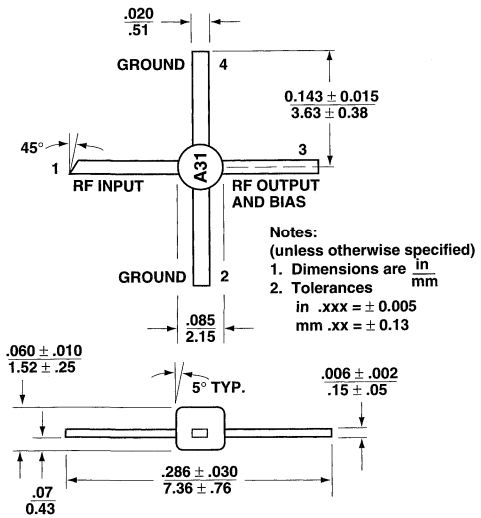

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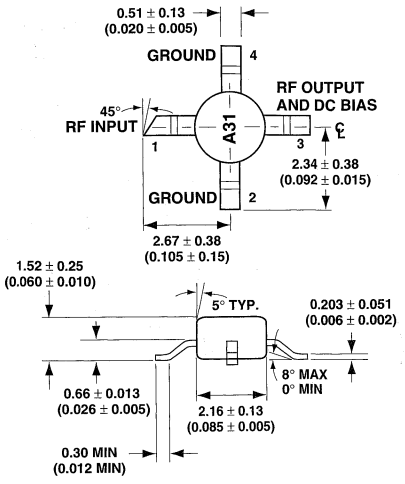


DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-2111

Features

- **Cascadable 50 Ω Gain Block**
- **Medium Power:** 10 dBm at 900 MHz
- **High Gain:** 16.5 dB Typical at 900 MHz
- **Low Noise Figure:** 3.3 dB Typical at 900 MHz
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Note:

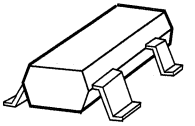
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."

Description

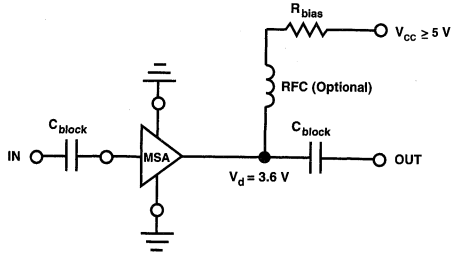
The MSA-2111 is a low cost silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a surface mount plastic SOT-143 package. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

SOT-143 Package



Typical Biasing Configuration



MSA-2111 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	125 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2]:
θ_{jc} = 505°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 2.0 mW/°C for T_C > 85°C.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 29 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 900 MHz	dB	16.0	17.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.3 GHz	dB		±0.5	
$f_{3\,dB}$	3 dB Bandwidth		GHz		0.5	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.8:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.8:1	
NF	50 Ω Noise Figure	f = 900 MHz	dB		3.3	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 900 MHz	dBm		10	
IP_3	Third Order Intercept Point	f = 900 MHz	dBm		20	
t_D	Group Delay	f = 900 MHz	psec		158	
V_d	Device Voltage		V	2.9	3.6	4.3
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 12 to 35 mA. Typical gain performance as a function of current is on the following page.

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-2111-TR1	3000	7" Reel
MSA-2111-BLK	100	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-2111 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 29 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.28	171	23.0	14.1	167	–26.0	.050	9	.27	177	1.03
0.2	.26	163	22.5	13.4	156	–25.5	.053	18	.27	175	1.03
0.3	.24	156	21.9	12.5	145	–24.9	.057	25	.26	173	1.03
0.4	.21	152	21.2	11.5	136	–24.0	.063	30	.26	171	1.03
0.5	.18	149	20.5	10.6	128	–23.4	.068	35	.24	170	1.03
0.6	.15	148	19.7	9.7	120	–22.6	.074	38	.24	169	1.03
0.7	.13	148	19.0	8.9	114	–21.8	.081	40	.22	169	1.04
0.8	.11	152	18.3	8.2	108	–21.1	.088	42	.21	169	1.04
0.9	.09	158	17.6	7.6	102	–20.4	.095	43	.20	168	1.04
1.0	.07	169	16.9	7.0	98	–19.9	.101	44	.19	169	1.05
1.5	.08	–123	14.0	5.0	79	–17.3	.136	45	.10	179	1.06
2.0	.11	–124	11.8	3.9	63	–15.5	.167	42	.06	–147	1.08
2.5	.15	–167	10.1	3.2	56	–14.3	.193	43	.06	–177	1.10
3.0	.27	158	8.3	2.6	43	–13.5	.211	38	.12	149	1.13
3.5	.38	145	6.8	2.2	32	–13.1	.222	34	.16	145	1.14
4.0	.46	135	5.6	1.9	21	–12.6	.234	30	.17	144	1.14

Typical Performance, T_A = 25°C

(unless otherwise noted)

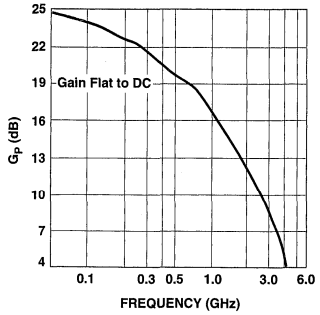


Figure 1. Power Gain vs. Frequency, I_d = 29 mA.

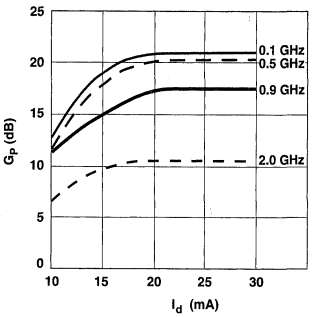


Figure 2. Power Gain vs. Current.

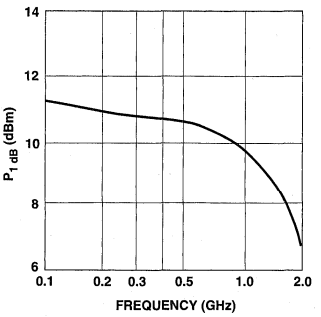


Figure 3. Output Power at 1 dB Gain Compression vs. Frequency, I_d = 29 mA.

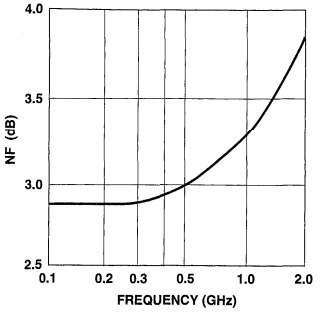
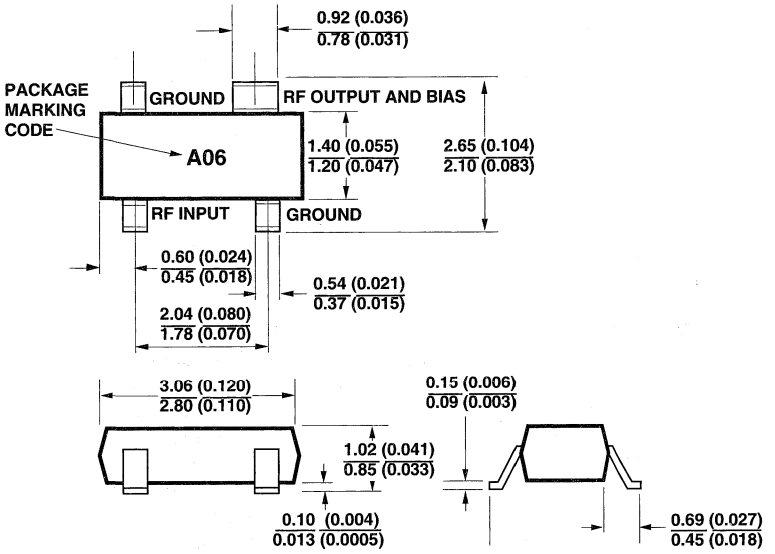


Figure 4. Noise Figure vs. Frequency, I_d = 29 mA.

SOT-143 Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Silicon Bipolar RFIC Amplifiers

Technical Data

MSA-31XX Series

Features

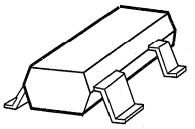
MSA-3111
- **Surface Mount SOT-143 Package**
- **3 dB Bandwidth: DC to 0.5 GHz**
- **18.4 dB Gain at 1 GHz**
- **3.5 dB NF at 1 GHz**

MSA-3135
- **Hermetic Ceramic Package**
- **3 dB Bandwidth: DC to 0.6 GHz**
- **19.6 dB Gain at 1 GHz**
- **3.2 dB NF at 1 GHz**

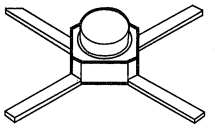
MSA-3185
- **Plastic Microstrip Package**
- **3 dB Bandwidth: DC to 0.5 GHz**
- **18.7 dB Gain at 1 GHz**
- **3.5 dB NF at 1 GHz**

MSA-3186
- **Surface Mount Plastic Microstrip Package**
- **3 dB Bandwidth: DC to 0.5 GHz**
- **18.7 dB Gain at 1 GHz**
- **3.5 dB NF at 1 GHz**

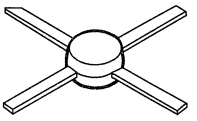
MSA-3111



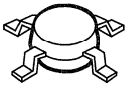
MSA-3135



MSA-3185



MSA-3186



Description

The MSA-31XX series are high performance silicon bipolar RFIC amplifiers designed to be cascadable in 50 Ω systems. The stability factor of K > 1 contributes to easy cascading in numerous narrow and broadband IF and RF commercial and industrial applications.

The MODAMP MSA series is fabricated using a 10 GHz f_T, 25 GHz F_{MAX}, silicon bipolar RFIC process which utilizes nitride self-alignment, ion implantation, and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Package options include, the industry standard plastic surface mount SOT-143 package, the 100 mil surface mountable hermetic ceramic package, the 85 mil plastic microstripline package, and the 85 mil surface mountable plastic microstripline package.

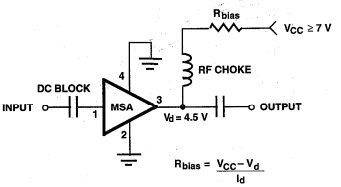
Absolute Maximum Ratings[1]

Parameter	MSA-3111	MSA-3135	MSA-3185, -3186
Device Current	50 mA	60 mA	60 mA
Power Dissipation[2,3]	250 mW[3a]	325 mW[3b]	325 mW[3c]
RF Input Power	+13 dBm	+13 dBm	+13 dBm
Junction Temperature	150°C	200°C	150°C
Storage Temperature	-65 to 150°C	-65 to 200°C	-65 to 150°C

Thermal Resistance: θ_{jc}	500°C/W	155°C/W	115°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3a. Derate at 2.0 mW/°C for T_C > 25°C.
b. Derate at 6.5 mW/°C for T_C > 149°C.
c. Derate at 8.7 mW/°C for T_C > 112°C.

Typical Biasing Configuration



Electrical Specifications, T_A = 25°C

I_D = 29 mA, Z_o = 50 Ω

Symbol	Parameters and Test Conditions	Units	MSA-3111			MSA-3135			MSA-3185, -3186		
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$) f = 0.1 GHz f = 0.5 GHz f = 1.0 GHz	dB	23.5	24.4 22.4 18.4		23.5	24.5 22.8 19.6	26.5	23.5	24.6 22.3 18.7	
ΔG_P	Gain Flatness f = 0.1 to 0.3 GHz	dB		±0.5			±0.4	±1.0		±0.5	
f_{3dB}	3 dB Bandwidth	GHz		0.5			0.6			0.5	
VSWR	Input VSWR f = 0.1 to 3.0 GHz			1.2:1			1.2:1			1.2:1	
	Output VSWR f = 0.1 to 3.0 GHz			1.2:1			1.2:1			1.4:1	
P_{1dB}	Power Output @ 1 dB Gain Compression: f = 1.0 GHz	dBm		9.0			9.3			9.0	
NF	50 Ω Noise Figure f = 1.0 GHz	dB		3.5			3.2			3.5	
IP_3	Third Order Intercept Point f = 1.0 GHz	dBm		23			22			21	
t_d	Group Delay f = 1.0 GHz	psec		130			130			130	
V_D	Device Voltage T_C = 25°C	V	4.0	4.5	6.0	4.5	4.7	5.5	4.0	4.7	6.0
dV/dT	Device Voltage Temperature Coefficient	mV/°C		-9.6			-9.6			-9.6	

Note: 1. Refer to "Tape and Reel Packaging for Surface Mount Devices."

Typical Performance for MSA-3111

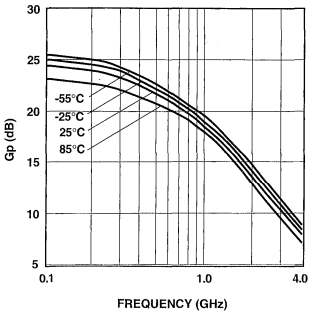


Figure 1. Power Gain vs. Frequency at Four Temperatures, I_D = 29 mA.

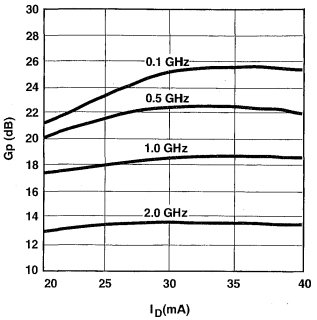


Figure 2. Power Gain vs. Current at 25°C.

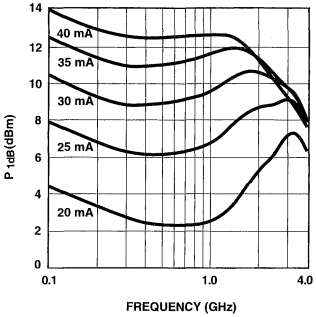


Figure 3. Typical P_{1dB} vs. Frequency at 25°C.

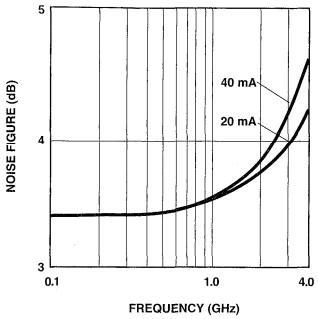


Figure 4. Noise Figure vs. Frequency at I_D = 29 mA.

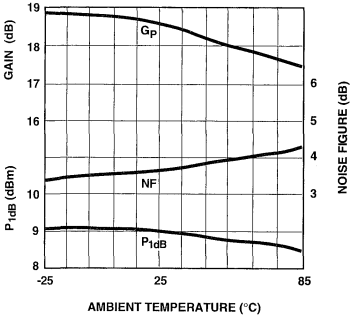


Figure 5. Power Gain, Noise Figure, and P_{1dB} vs. Temperature at 1 GHz and I_D = 29 mA.

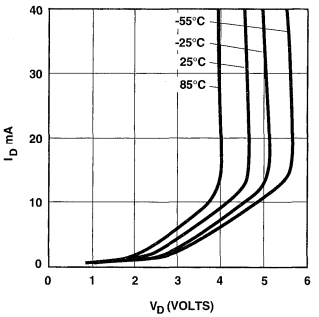


Figure 6. I_D vs. V_D at Four Temperatures.

Typical Scattering Parameters at T_A = 25°C, for MSA-3111

I_D = 29 mA, Z_o = 50 Ω

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.1	0.05	3	24.4	16.53	167	-27.0	0.045	9	0.10	-23
0.2	0.06	4	24.0	15.83	156	-26.5	0.047	16	0.10	-41
0.3	0.07	-4	23.4	14.78	146	-26.0	0.050	23	0.10	-59
0.4	0.07	-8	22.7	13.59	136	-25.3	0.054	28	0.11	-72
0.5	0.07	-12	22.0	12.53	128	-24.6	0.059	33	0.11	-84
0.6	0.07	-18	21.1	11.41	121	-23.9	0.064	36	0.11	-94
0.7	0.07	-22	20.4	10.47	114	-23.1	0.070	39	0.11	-100
0.8	0.08	-26	19.7	9.63	109	-22.4	0.076	41	0.11	-106
0.9	0.08	-32	19.0	8.89	104	-21.7	0.082	42	0.11	-111
1.0	0.08	-35	18.4	8.27	99	-21.1	0.088	43	0.11	-114
1.5	0.08	-59	15.6	5.99	80	-18.5	0.118	44	0.11	-123
2.0	0.10	-79	13.4	4.69	65	-16.6	0.148	42	0.10	-122
2.5	0.10	-104	11.8	3.88	52	-15.2	0.175	38	0.11	-118
3.0	0.10	-129	10.4	3.31	39	-14.1	0.198	33	0.12	-114
3.5	0.12	-163	9.3	2.91	27	-13.2	0.219	28	0.12	-117
4.0	0.15	164	8.2	2.58	16	-12.6	0.236	23	0.13	-125
4.5	0.21	140	7.4	2.34	4	-12.1	0.250	18	0.13	-136
5.0	0.29	121	6.5	2.10	-7	-11.7	0.260	14	0.14	-148
5.5	0.36	109	5.6	1.90	-18	-11.3	0.271	10	0.17	-158
6.0	0.42	98	4.6	1.70	-28	-11.0	0.282	7	0.21	-165

Typical Performance for MSA-3135

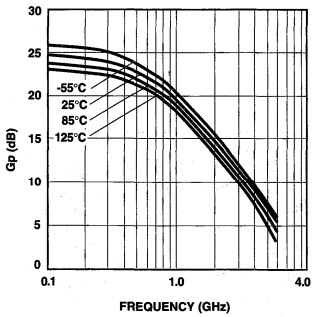


Figure 1. Power Gain vs. Frequency at Four Temperatures, I_D = 29 mA.

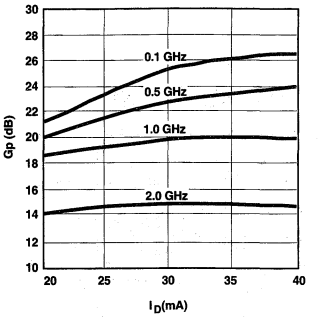


Figure 2. Power Gain vs. Current at 25°C.

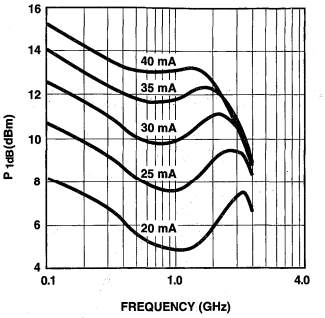


Figure 3. Typical P_{1dB} vs. Frequency at 25°C.

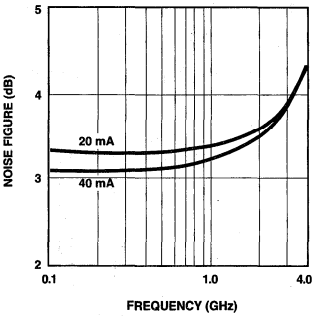


Figure 4. Noise Figure vs. Frequency at I_D = 29 mA.

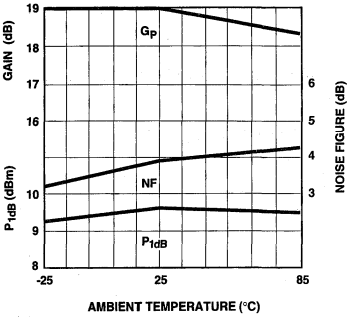


Figure 5. Power Gain, Noise Figure, and P_{1dB} vs. Temperature at 1 GHz and I_D = 29 mA.

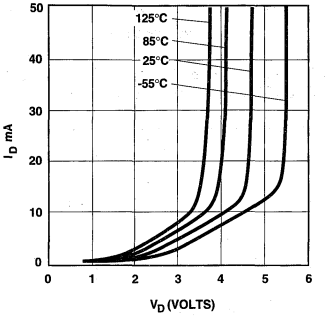


Figure 6. I_D vs. V_D at Four Temperatures.

Typical Scattering Parameters at T_A = 25°C, for MSA-3135

I_D = 29 mA, Z_o = 50 Ω

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.1	0.05	1	24.7	17.11	169	-27.3	0.043	7	0.09	-19
0.2	0.06	2	24.4	16.52	158	-27.0	0.045	14	0.09	-37
0.3	0.07	-2	23.9	15.72	149	-26.5	0.047	20	0.09	-52
0.4	0.07	-7	23.4	14.77	139	-26.0	0.050	24	0.09	-67
0.5	0.07	-12	22.8	13.77	131	-25.4	0.054	29	0.09	-80
0.6	0.07	-21	22.1	12.79	124	-24.7	0.058	32	0.09	-92
0.7	0.07	-27	21.5	11.86	117	-24.1	0.063	34	0.09	-102
0.8	0.07	-33	20.9	11.03	111	-23.4	0.037	36	0.09	-111
0.9	0.08	-39	20.2	10.25	106	-22.8	0.072	38	0.09	-119
1.0	0.08	-44	19.6	9.55	101	-22.2	0.078	39	0.09	-127
1.5	0.08	-79	16.9	7.03	80	-19.7	0.104	39	0.10	-155
2.0	0.09	-116	14.8	5.52	63	-17.7	0.130	36	0.10	-171
2.5	0.11	-145	13.2	4.55	49	-16.3	0.153	31	0.09	176
3.0	0.15	-172	11.7	3.86	35	-15.2	0.175	25	0.10	162
3.5	0.19	166	10.5	3.34	22	-14.3	0.192	19	0.11	154
4.0	0.24	149	9.4	2.94	9	-13.7	0.207	13	0.12	152
4.5	0.29	134	8.3	2.61	-3	-13.2	0.219	7	0.13	148
5.0	0.35	120	7.4	2.34	-16	-12.8	0.228	1	0.15	141
5.5	0.41	107	6.4	2.08	-27	-12.5	0.236	-5	0.19	138
6.0	0.46	95	5.4	1.87	-39	-12.3	0.243	-10	0.24	137

Typical Performance for MSA-3185, MSA-3186

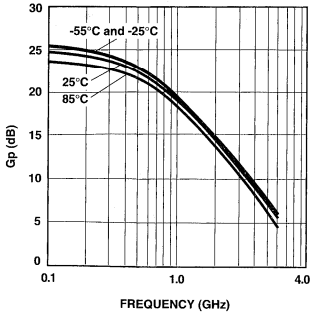


Figure 1. Power Gain vs. Frequency at Four Temperatures, I_D = 29 mA.

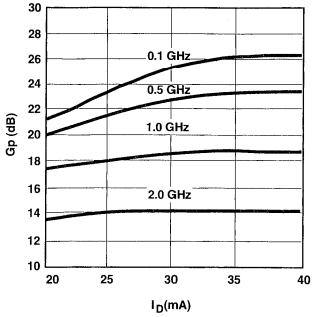


Figure 2. Power Gain vs. Current at 25°C.

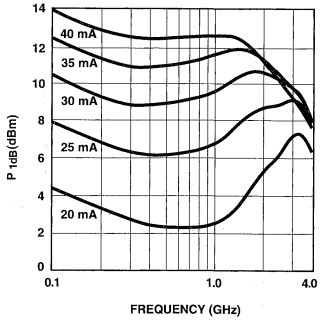


Figure 3. Typical P_{1dB} vs. Frequency at 25°C.

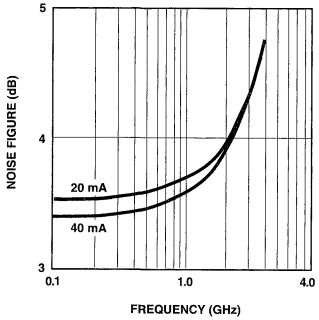


Figure 4. Noise Figure vs. Frequency at I_D = 29 mA.

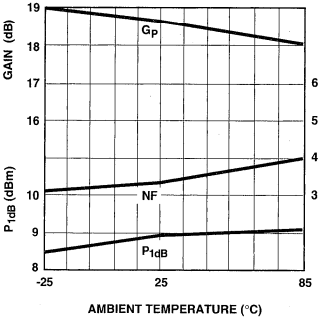


Figure 5. Power Gain, Noise Figure, and P_{1dB} vs. Temperature at 1 GHz and I_D = 29 mA.

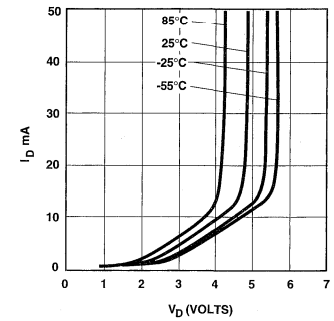


Figure 6. I_D vs. V_D at Four Temperatures.

Typical Scattering Parameters at T_A = 25°C, for MSA-3185

I_D = 29 mA, Z_o = 50 Ω

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.1	0.05	-3	24.6	17.04	167	-27.2	0.044	8	0.09	-32
0.2	0.04	-13	24.2	16.22	156	-26.8	0.046	16	0.09	-57
0.3	0.04	-22	23.6	15.18	145	-26.2	0.049	22	0.10	-76
0.4	0.06	-25	23.0	14.07	135	-25.5	0.053	27	0.11	-84
0.5	0.07	-27	22.2	12.95	127	-24.7	0.058	31	0.12	-91
0.6	0.07	-31	21.5	11.85	119	-24.0	0.063	34	0.12	-102
0.7	0.07	-33	20.7	10.85	112	-23.3	0.068	36	0.12	-110
0.8	0.06	-41	20.0	10.01	106	-22.6	0.074	38	0.13	-120
0.9	0.06	-45	19.3	9.27	101	-21.9	0.080	39	0.13	-126
1.0	0.06	-57	18.7	8.59	96	-21.3	0.086	40	0.13	-134
1.5	0.05	-89	15.9	6.23	74	-18.6	0.118	38	0.13	-157
2.0	0.05	-122	13.9	4.93	57	-16.6	0.147	33	0.12	-173
2.5	0.08	167	12.2	0.07	41	-15.1	0.175	26	0.16	-163
3.0	0.16	143	10.7	3.44	25	-14.1	0.197	17	0.18	-154
3.5	0.21	120	9.4	2.95	11	-13.5	0.212	9	0.24	-138
4.0	0.30	102	8.2	2.56	-3	-13.0	0.223	2	0.28	-124
4.5	0.40	93	7.1	2.26	-16	-12.7	0.231	-5	0.31	-114
5.0	0.51	87	6.1	2.03	-28	-12.4	0.240	-11	0.34	-109
5.5	0.61	80	5.2	1.82	-40	-12.2	0.247	-17	0.36	-105
6.0	0.67	72	4.3	1.64	-53	-12.0	0.251	-23	0.40	-101

Typical Scattering Parameters at T_A = 25°C, for MSA-3186

I_D = 29 mA, Z_o = 50 Ω

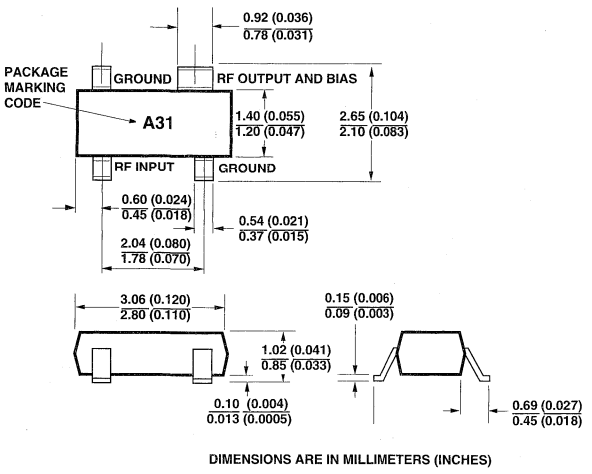
Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.1	0.05	1	24.7	17.11	169	-27.3	0.043	7	0.09	-19
0.2	0.06	2	24.4	16.52	158	-27.0	0.045	14	0.09	-37
0.3	0.07	-2	23.9	15.72	149	-26.5	0.047	20	0.09	-52
0.4	0.07	-7	23.4	14.77	139	-26.0	0.050	24	0.09	-67
0.5	0.07	-12	22.8	13.77	131	-25.4	0.054	29	0.09	-80
0.6	0.07	-21	22.1	12.79	124	-24.7	0.058	32	0.09	-92
0.7	0.07	-27	21.5	11.86	117	-24.1	0.063	34	0.09	-102
0.8	0.07	-33	20.9	11.03	111	-23.4	0.037	36	0.09	-111
0.9	0.08	-39	20.2	10.25	106	-22.8	0.072	38	0.09	-119
1.0	0.08	-44	19.6	9.55	101	-22.2	0.078	39	0.09	-127
1.5	0.08	-79	16.9	7.03	80	-19.7	0.104	39	0.10	-155
2.0	0.09	-116	14.8	5.52	63	-17.7	0.130	36	0.10	-171
2.5	0.11	-145	13.2	4.55	49	-16.3	0.153	31	0.09	176
3.0	0.15	-171	11.7	3.86	35	-15.2	0.175	25	0.10	162
3.5	0.19	166	10.5	3.34	22	-14.3	0.192	19	0.11	154
4.0	0.24	149	9.4	2.94	9	-13.7	0.207	13	0.12	152
4.5	0.29	134	8.3	2.61	-3	-13.2	0.219	7	0.13	148
5.0	0.35	120	7.4	2.34	-16	-12.8	0.228	1	0.15	141
5.5	0.41	107	6.4	2.08	-27	-12.5	0.236	-5	0.19	138
6.0	0.46	95	5.4	1.87	-39	-12.3	0.243	-10	0.24	137

Tape and Reel Part Number Ordering Information

Part Number	Devices per Reel	Reel Size
MSA-3111-TR1	3000	7"
MSA-3186-TR1	1000	7"

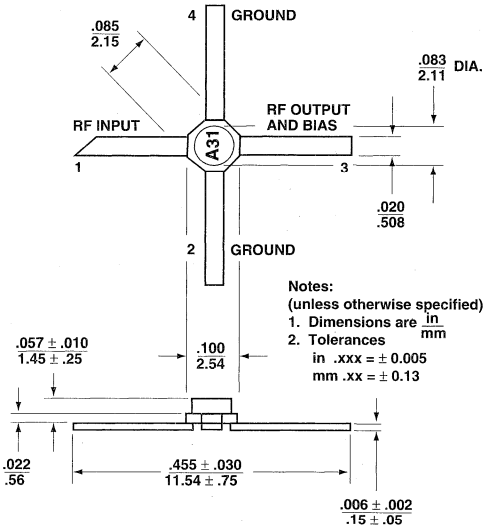
Outline Drawings

SOT-143



DIMENSIONS ARE IN MILLIMETERS (INCHES)

35



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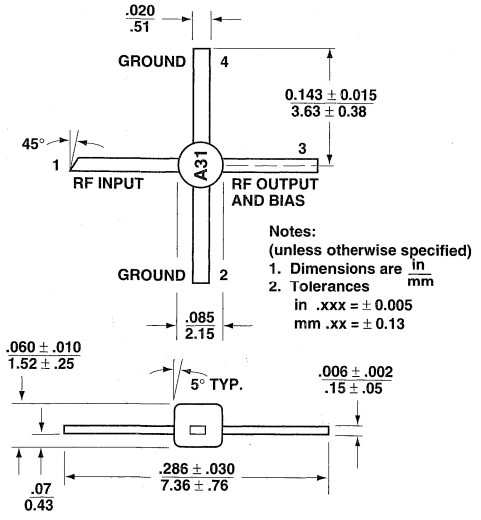

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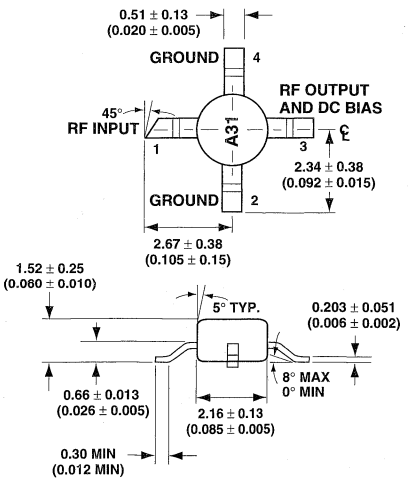


DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-9970

Features

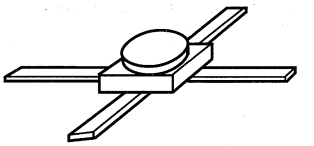
- **Open Loop Feedback Amplifier**
- **Performance Flexibility with User Selected External Feedback for:**
  - Broadband Minimum Ripple Amplifiers
  - Low Return Loss Amplifiers
  - Negative Gain Slope Amplifiers
- **Usable Gain to 6.0 GHz**
- **16.0 dB Typical Open Loop Gain at 1.0 GHz**
- **14.5 dBm Typical $P_{1\,dB}$ at 1.0 GHz**
- **Hermetic Gold-ceramic Microstrip Package**

Description

The MSA-9970 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic high reliability package. This MMIC is designed with high open loop gain and is intended to be used with external resistive and reactive feedback elements to create a variety of special purpose gain blocks.

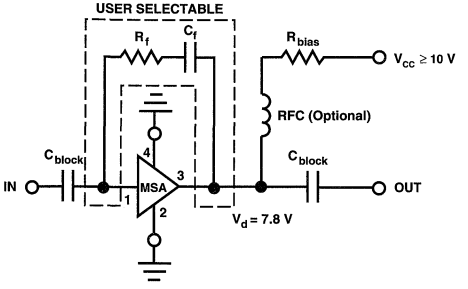
Applications include very broadband, minimum ripple amplifiers with extended low frequency performance possible through the use of a high valued external feedback blocking capacitor; extremely well matched (–20 dB return loss) amplifiers; and negative gain slope amplifiers for flattening MMIC cascades.

70 mil Package



The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Typical Biasing Configuration



5965-9668E

MSA-9970 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]:
θ_{jc} = 150°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.7 mW/°C for T_C > 88°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain[2] ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		17.5	
		f = 1.0 GHz		14.5	16.0	17.5
		f = 4.0 GHz		8.0	9.0	10.0
$P_{1\,dB}$	Output Power at 1 dB Gain Compression[2]	f = 1.0 GHz	dBm		14.5	
IP_3	Third Order Intercept Point[2]	f = 1.0 GHz	dBm		25.0	
V_d	Device Voltage		V	7.0	7.8	8.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16.0	

Notes:
1. The recommended operating current range for this device is 25 to 45 mA. Typical performance as a function of current is on the following page.
2. Open loop value. Adding external feedback will alter device performance.

MSA-9970 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.02	.89	–1	17.5	7.51	179	–37.2	.014	4	.93	–1	1.01
0.05	.90	–3	17.5	7.47	177	–35.6	.017	34	.92	–3	.83
0.1	.90	–6	17.4	7.45	174	–33.2	.022	43	.93	–6	.70
0.2	.89	–12	17.4	7.43	168	–29.6	.033	61	.93	–13	.39
0.4	.87	–24	17.2	7.27	156	–24.4	.061	63	.91	–27	.24
0.6	.85	–36	17.0	7.06	145	–20.8	.091	58	.90	–40	.21
0.8	.82	–47	16.6	6.78	134	–18.8	.115	52	.87	–53	.21
1.0	.79	–59	16.2	6.49	124	–17.0	.141	44	.84	–66	.24
1.5	.72	–86	15.3	5.79	100	–14.6	.186	29	.74	–96	.28
2.0	.65	–113	14.2	5.10	77	–13.4	.215	16	.64	–123	.34
2.5	.59	–133	13.0	4.45	61	–12.9	.227	7	.57	–143	.39
3.0	.54	–155	11.6	3.79	42	–12.5	.236	–3	.51	–163	.46
3.5	.53	–174	10.3	3.28	26	–12.4	.239	–14	.45	178	.53
4.0	.52	168	9.2	2.87	10	–12.5	.238	–22	.39	164	.59
4.5	.53	152	8.0	2.51	–4	–12.6	.234	–30	.34	155	.66
5.0	.55	140	6.9	2.21	–17	–12.8	.228	–37	.31	153	.72
5.5	.55	130	5.8	1.94	–31	–13.2	.220	–44	.30	154	.80
6.0	.55	121	4.6	1.70	–43	–13.6	.209	–48	.32	157	.88
6.5	.56	114	3.5	1.50	–53	–13.8	.203	–54	.37	158	.94
7.0	.56	107	2.6	1.34	–63	–14.0	.201	–59	.42	157	.97

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C

(unless otherwise noted)

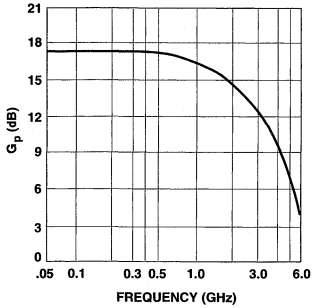


Figure 1. Open Loop Power Gain vs. Frequency, I_d = 35 mA.

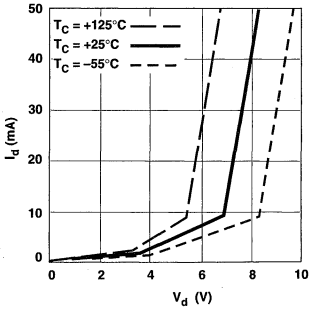


Figure 2. Device Current vs. Voltage.

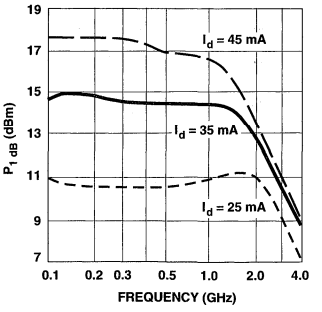


Figure 3. Open Loop Output Power at 1 dB Gain Compression vs. Frequency.

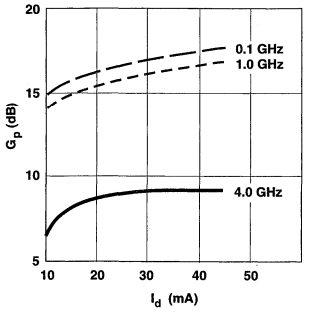


Figure 4. Open Loop Power Gain vs. Current.

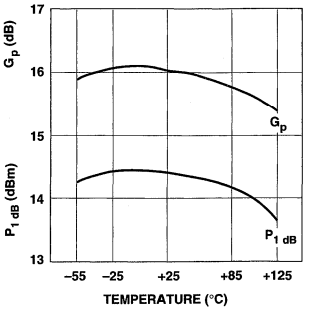
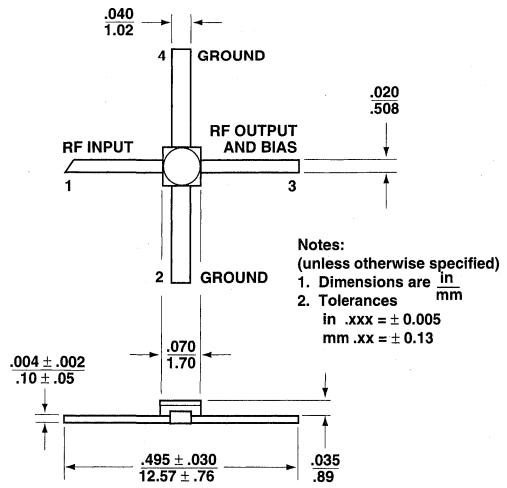


Figure 5. Open Loop Output Power at 1 dB Gain Compression and Open Loop Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 35 mA.

70 mil Package Dimensions



HEWLETT® PACKARD

Silicon Bipolar RFIC 900 MHz Driver Amplifier

Reliability Data

HPMX-3002

Description

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the relevant MIL-STD-883 or HP internal GSS methods. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Hewlett-Packard Communications Components Designer's Catalog, except that for Autoclave a failure is defined as a part which fails catastrophically.

1. Life Test

A. Demonstrated Performance

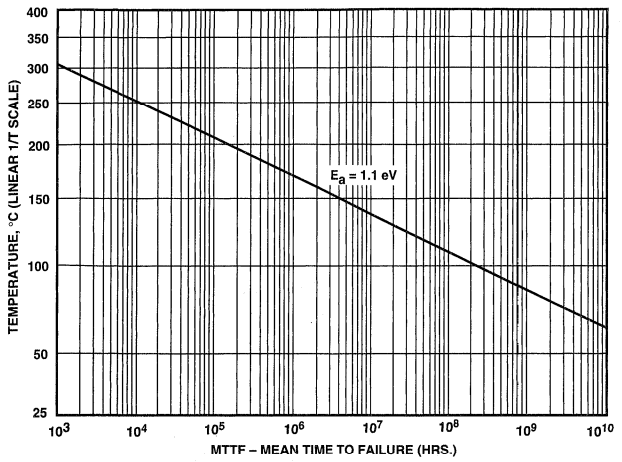
Test Name	Test Conditions	Units Tested	Total Device Hrs.	Total Failed
High Temperature Operating Life (O.L.)	$T_{J(max.)}$ = 150° C	90	180,000	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1 eV, and is listed in the following table.

Junction Temp. T_J(°C)	Point(1)		90% Confidence Level(2)	
	MTTF* (hours)	MTTF FIT(3)	MTTF (hours)	FIT(3)
150	3.8×10^6	260	2.9×10^6	341
125	2.6×10^7	39	2.0×10^7	51
100	2.2×10^8	5	1.7×10^8	6
75	2.6×10^9	<1	2.0×10^9	<1

*MTTF data calculated from high temperature Operating Life tests.



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hours/day) x (5 days/week) / (168 hours/week) ≅ 25%

Then the point failure rate per year is:

$(4.55 \times 10^{-9}) \times (25\%) \times (8760 \text{ hours/year}) \cong 1.0 \times 10^{-3}$ % per year

Likewise, the 90% confidence level failure rate per year is:

$(5.88 \times 10^{-9}) \times (25\%) \times (8760 \text{ hours/year}) \cong 1.3 \times 10^{-3}$ % per year

2. Environmental Tests

Test Name	Reference	Test Conditions	Units Tested	Units Failed
Temperature Cycle	M1010	-65°C to +150°C; 10 min. dwell; 200 cycles	116	0
Thermal Shock	M1011	-65°C to +150°C; 5 min. dwell; 100 cycles	178	0
Autoclave, unbiased	HP GSS 12-109	121°C; 15 PSIG, 96 hrs.	76	0
Resistance to Solvents	M2015	3 solvent groups	15	0
Solderability	M2003	260°C, 5 sec. dwell; 8 hours steam age	22	0

3. Flammability Test

(MIL-STD-202, Method 111):
Meets Needle Flame test per UL Category D (Flaming Time <3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD

Classification: Class I

HEWLETT® PACKARD

Silicon Bipolar Monolithic Amplifier

Reliability Data

INA Series

Description

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-883. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

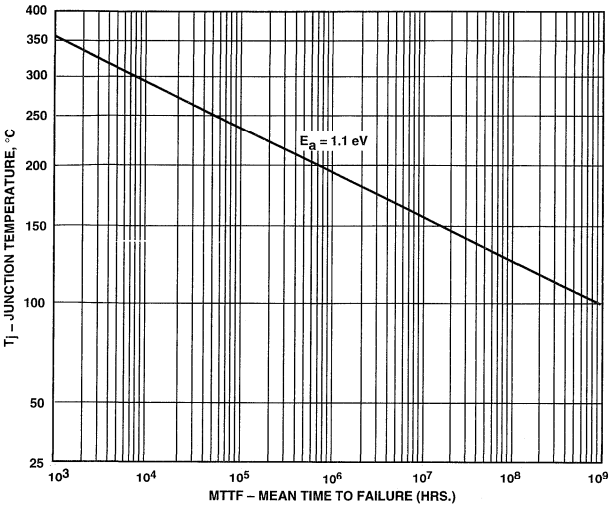
Test Name	Test Conditions	Units Tested	Total Device Hrs.	Total Failed
High Temperature Operating Life (O.L.)	T_J = 175° C	78	78,000	0
High Temperature Operating Life (O.L.)	T_J = 150° C	344	344,000	0
High Temperature Storage (HTS)*	T_A = 150° C	78	78,000	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1 eV, and is listed in the following table.

Junction Temp. T_J(°C)	Point(1)		90% Confidence Level(2)	
	MTTF* (hours)	MTTF FIT(3)	MTTF (hours)	FIT(3)
150	1.5×10^7	66	6.6×10^6	152
125	1.0×10^8	10	4.4×10^7	22.7
100	8.6×10^8	1.17	3.8×10^8	2.64
55	6.0×10^{10}	0.017	2.6×10^{10}	0.038

*MTTF data calculated from high temperature Operating Life tests.



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hours/day) x (5 days/week) ÷ 168 hours/week ≅ 25%

Then the point failure rate per year is:

$(1.17 \times 10^{-9}) \times (25\%) \times (8760 \text{ hours/year}) \cong 2.6 \times 10^{-4}$ % per year

Likewise, the 90% confidence level failure rate per year is:

$(2.64 \times 10^{-9}) \times (25\%) \times (8760 \text{ hours/year}) \cong 5.8 \times 10^{-4}$ % per year

2. Environmental Tests

Test Name	MIL-STD-883 Method	Test Conditions	Units Tested	Units Failed
Thermal Shock	1011	-65°C to +150°C; 200 cycles	56	0
Temperature Cycle	1010	-65°C to +150°C; 1000 cycles	52	0
Thermal Shock	1011	-55°C to +125°C; 100 cycles	115	0
Temperature Cycle	1010	-55°C to +125°C; 1000 cycles	115	0
85/85	HP GSS 12-107	85°C/85% RH; 1000 hrs., min.	142	1
Autoclave	HP GSS 12-109	121°C; 15 PSIG, 96 hrs., min.	139	0
Solderability	2003	Solder temp 245°C ±5°C; Dwell time 5.5 sec.	22	0
Solder Heat	2031	260°C ±5°C for 10 secs ±0.5 sec.	22	0

3. Flammability Test

(MIL-STD-202, Method 111):
Meets Needle Flame test per UL Category D (Flaming Time <3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD

Classification: Class I

1 GHz Low Noise Silicon MMIC Amplifiers

Reliability Data

INA-30311
INA-50311

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-883. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

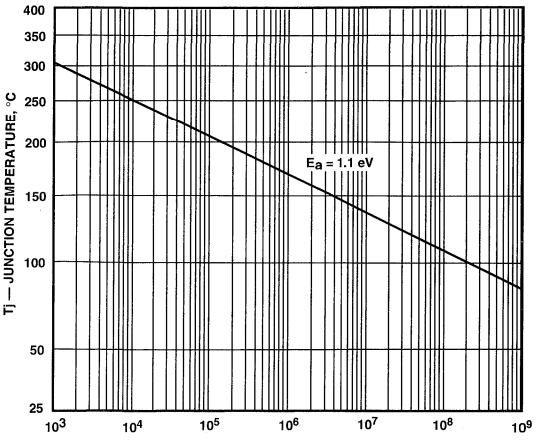
Test Name	Test Condition	Units Tested	Total Device Hrs.	Total Failed	Failure Rate (%/1K Hours)
High Temperature Operating Life (O.L.)	V_d = 5 V (I_d = 20 mA) T_J = 150°C 1000 hrs.	115	115,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1eV, and is listed in the following table.

Junction Temp. T_J (°C)	Point(1) MTTF* (hours)	Point(1) FIT(3)	90% Confidence Level(2) MTTF (hours)	90% Confidence Level(2) FIT(3)
150	3.8×10^6	260	2.9×10^6	341
125	2.6×10^7	39	2.0×10^7	51
100	2.2×10^8	5	1.7×10^8	6
75	2.6×10^9	<1	2.0×10^9	<1

*MTTF data calculated from high temperature Operating Life tests.



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows:
   FIT = 10^9/(MTTF)

C. Example of Failure Rate Calculation:

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day) × (5 days/wk) ÷ 168 hrs/wk ≅ 25%

Then the point failure rate per year is:

$(4.55 \times 10^{-9}) \times (25\%) \times (8760 \text{ hrs/yr}) \cong 1.0 \times 10^{-3}$ % per year

Likewise, the 90% confidence level failure rate per year is:

$(5.88 \times 10^{-9}) \times (25\%) \times (8760 \text{ hrs/yr}) \cong 1.3 \times 10^{-3}$ % per year

2. Environmental and Mechanical Tests

Test Name	MIL-STD-883 Reference	Test Conditions	Units Tested	Total Failed
Thermal Shock	M1011	-65°C to 150°C, 5 min. dwell, 200 cycles	76	0
85°C/85%RH	M1004	85°C/85%RH Biased, 1000 hrs.	73	0
Temperature Cycles	M1010	-65°C to 150°C, 10 min. dwell, 200 cycles	74	0
Autoclave	HP GSS	121°C, 15 PSIG, 96 hrs	74	0

3. Flammability Test (MIL-STD-202, Method 111):

Meets Needle Flame test per UL Category D (Flaming Time <3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD Classification: Class I

HEWLETT® PACKARD

Low Noise Silicon MMIC Amplifiers

Reliability Data

INA-51063
INA-52063

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-883. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

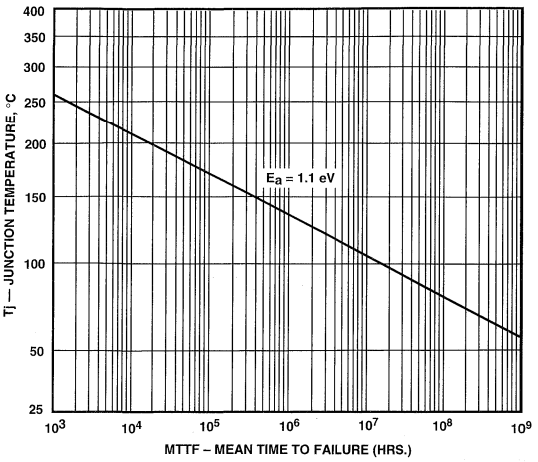
Test Name	Test Condition	Units Tested	Total Device Hrs.	Total Failed
High Temperature Operating Life (O.L.)	V_d = 5 V (I_d = 11 mA) T_J = 150°C 1000 hrs.	56	56,000	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1eV, and is listed in the following table.

Junction Temp. T_J (°C)	Point(1)		90% Confidence Level(2)	
	MTTF* (hours)	FIT(3)	MTTF (hours)	FIT(3)
150	3.9×10^5	2564	2.01×10^5	4975
125	2.6×10^6	385	1.34×10^6	746
100	2.0×10^7	50.0	1.03×10^7	97.0
55	2.0×10^9	0.5	1.03×10^9	0.97

*MTTF data calculated from high temperature Operating Life tests.



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows:
   FIT = 10^9/(MTTF)

C. Example of Failure Rate Calculation:

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day) × (5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

$(50 \times 10^{-9}) \times (25\%) \times (8760 \text{ hrs/yr}) = 1.10 \times 10^{-2}$ % per year

Likewise, the 90% confidence level failure rate per year is:

$(97 \times 10^{-9}) \times (25\%) \times (8760 \text{ hrs/yr}) = 2.12 \times 10^{-2}$ % per year

2. Environmental and Mechanical Tests

Test Name	MIL-STD-883 Reference	Test Conditions	Units Tested	Total Failed
Thermal Shock	M1011	-65°C to 150°C, 5 min. dwell, 200 cycles	66	0
85°C/85%RH	M1004	85°C/85%RH biased, 500 hrs.	56	0
Temperature Cycles	M1010	-65°C to 150°C, 10 min. dwell, 200 cycles	69	0
Autoclave	HP GSS 12-109	121°C, 15 PSIG, 96 hrs	58	0
Solderability	M2003	8 hrs. steam aging, 245°C, 5 sec. dwell	22	0
Popcorning	HP-GSS	125°C, 24 hrs. bake, 85°C/85%RH 168 hrs, IR reflow	22	0
Solder Heat	MIL-STD 750 M2031	260°C, 10 sec. dwell	17	0

3. Flammability Test (MIL-STD-202, Method 111):

Meets Needle Flame test per UL Category D (Flaming Time <3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD Classification: Class I

HEWLETT® PACKARD

Silicon Bipolar Variable Gain Amplifiers

Reliability Data

IVA Series

Description

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-883. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

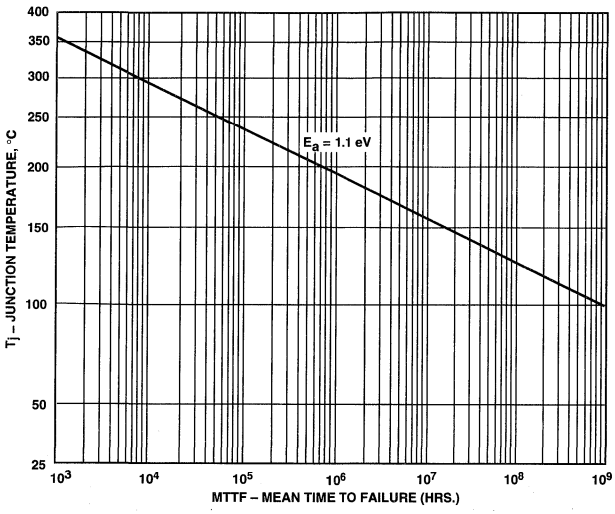
Test Name	Test Conditions	Units Tested	Total Device Hrs.	Total Failed
High Temperature Operating Life (O.L.)	T_J = 150° C	217	217,000	1
High Temperature Storage (HTS)*	T_J = 150° C	43	43,000	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1 eV, and is listed in the following table.

Junction Temp. T_J(°C)	Point(1)		90% Confidence Level(2)	
	MTTF* (hours)	MTTF FIT(3)	MTTF (hours)	FIT(3)
200	1.6×10^5	6319	1.2×10^5	8278
175	7.1×10^5	1402	5.4×10^5	1836
150	3.8×10^6	260	2.9×10^6	341
125	2.6×10^7	39	2.0×10^7	51
100	2.2×10^8	5	1.7×10^8	6
75	2.6×10^9	<1	2.0×10^9	<1
50	4.4×10^{10}	<1	3.3×10^{10}	<1

*MTTF data calculated from high temperature Operating Life tests.



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hours/day) x (5 days/week) ÷ 168 hours/week ≅ 25%

Then the point failure rate per year is:

(4.55 x 10^{-9}) x (25%) x (8760 hours/year) ≅ 1.0 x 10^{-3} % per year

Likewise, the 90% confidence level failure rate per year is:

(5.88 x 10^{-9}) x (25%) x (8760 hours/year) ≅ 1.3 x 10^{-3} % per year

2. Environmental Tests

Test Name	MIL-STD-883 Method	Test Conditions	Units Tested	Units Failed
Temperature Cycle	1010	-65°C to +150°C; 10 min. dwell; 200 cycles, min.	450	1
Thermal Shock	1011	-65°C to +150°C; 5 min. dwell; 200 cycles, min.	448	0
Autoclave, unbiased	HP GSS 12-109	121°C; 15 PSIG, 96 hrs., min.	327	1
Temperature Humidity, biased	HP GSS 12-107	85°C/85% RH; 1000 hrs., min.	131	0
Resistance to solvents	2015	3 solvent groups	15	0
Solderability	2003	260°C, 5 sec. dwell; Post 8 hours steam aging	82	0

3. Flammability Test

(MIL-STD-202, Method 111):
Meets Needle Flame test per UL Category D (Flaming Time <3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD

Classification: Class I

HEWLETT® PACKARD

GaAs MMIC Amplifiers

Reliability Data

MGA-81563
MGA-82563
MGA-86563
MGA-87563
IAM-91563

Description

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-883. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Hewlett-Packard Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

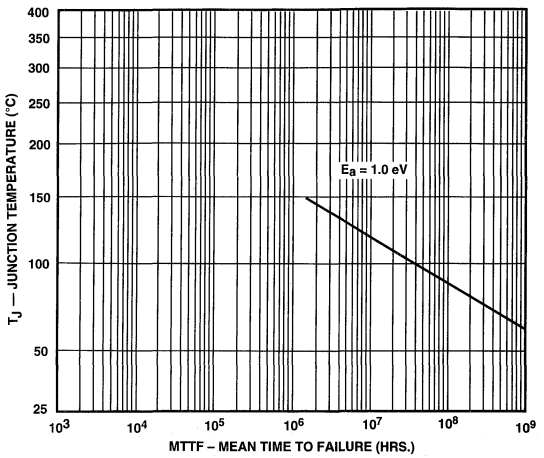
Test Name	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate (%/1K Hours)
High Temperature Operating Life (O.L.)	V_d = 5.0 V (I_d = 10 mA) T_J = 150 °C 1000 hrs.	76	76,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.0 eV, and the device thermal resistance of the stress board is 130 °C/W, and is listed in the following table.

Junction Temp. T_J (°C)	Point[1]		90% Confidence Level[2]	
	MTTF* (hours)	FIT[3]	MTTF (hours)	FIT[3]
150	1.0×10^6	1000	4.4×10^5	2272
125	8.0×10^6	125	3.5×10^6	285
100	5.0×10^7	20	2.2×10^7	45
55	4.0×10^9	0.25	1.7×10^9	0.58

*MTTF data calculated from high temperature Operating Life tests.



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows:
   FIT = 10^9/(MTTF)

C. Example of Failure Rate Calculation:

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

$(20 \times 10^{-9}) \times (25\%) \times (8760 \text{ hrs/yr}) = 4.3 \times 10^{-5}$ % per year

Likewise, the 90% confidence level failure rate per year is:

$(45 \times 10^{-9}) \times (25\%) \times (8760 \text{ hrs/yr}) = 9.85 \times 10^{-5}$ % per year

2. Environmental Tests

Test Name	MIL-STD-883 Reference	Test Conditions	Units Tested	Units Failed
Thermal Shock	M1011	-65°C to 150°C, 10 min dwell, 200 cycles	306	0
Autoclave	HP GSS 12-109	121°C, 15 PSIG, 96 hrs	152	0
85°C/85% RH	M1004	85°C/85% RH biased, 1000 hrs	64	0
Solder Heat	MIL-STD-750 M2031	260°C, 10 sec dwell	17	0
Solderability	M2003	8 hrs steam aging, 245°C, 5 sec dwell	22	0
Terminal Strength	M2004	8 ounce pull/pin	22	0
Popcorning	HP GSS	24 hrs bake at 125°C, 168 hrs 85/85, IR-REFLOW	17	0

3. Flammability Test (MIL-STD-202, Method 111):

Meets Needle Flame Test per UL Category D (Flaming Time < 3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD Classification:

Class I

HEWLETT® PACKARD

Silicon Bipolar Monilithic Amplifiers

Reliability Data

MSA Series

Description

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

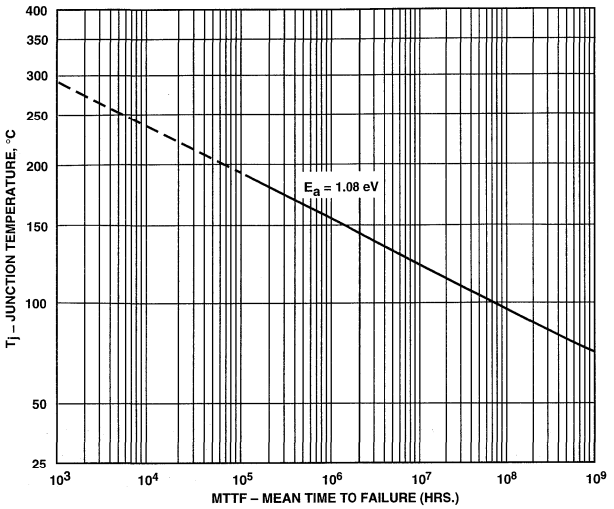
Test Name	Test Condition	Units Tested	Total Device Hrs.	Total Failed	Failure Rate (%/1K Hours)
High Temperature Operating Life (O.L.)	T_A = 125°C, (T_J = 160)	258	516,000	0	0
High Temperature Operating Life (O.L.)	T_A = 150°C, (T_J = 183)	190	188,000	2	1.06
High Temperature Storage (HTS)*	T_A = 150°C	350	350,912	1	0.28

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1eV, and the device thermal resistance of the stress board is 130°C/W, and listed in the following table.

Junction Temp. TJ (°C)	Point(1)		90% Confidence Level(2)	
	MTTF* (hours)	MTTF FIT(3)	MTTF (hours)	FIT(3)
183	9.5×10^4	1.05×10^4	3.57×10^4	2.80×10^4
160	7.4×10^5	1.35×10^3	3.21×10^5	3.11×10^3
125	9.9×10^6	1.0×10^2	4.3×10^6	2.3×10^2
100	8.0×10^7	12.5	3.5×10^7	28

*MTTF data calculated from high temperature Operating Life tests.



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF)

C. Example of Failure Rate Calculation:

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk ≅ 25%

Then the point failure rate per year is:

(12.5 x 10^{-9}/hr) x (25%) x (8760 hrs/yr) = 2.7 x 10^{-3} % per year

Likewise, the 90% confidence level failure rate per year is:

(8.0 x 10^{-7}/hr) x (25%) x (8760 hrs/yr) = 1.8 x 10^{-1}% per year

2. Environmental Tests

Test Name	MIL-STD 750 Reference	Test Conditions	Units Tested	Units Failed
Solderability	2026	215°C, 5 seconds post 8 hr steam aging	22	0
Solder Heat	2031	260°C, 10 seconds	22	0
Resistance to Solvents	1022	4 Solvent Groups	15	0
Autoclave	HP GSS 12-109	121°C, 16 PSIG, 96 hrs	549	0
Thermal Shock	1056	-65/150°C, 5 min dwell, 200 cycles	460	0
Temperature Cycle	1051	-55 to 150°C min dwell, 200 cycles	643	0
Lead Integrity		2.0 Pounds Minimum	15	0

3. Flammability Test

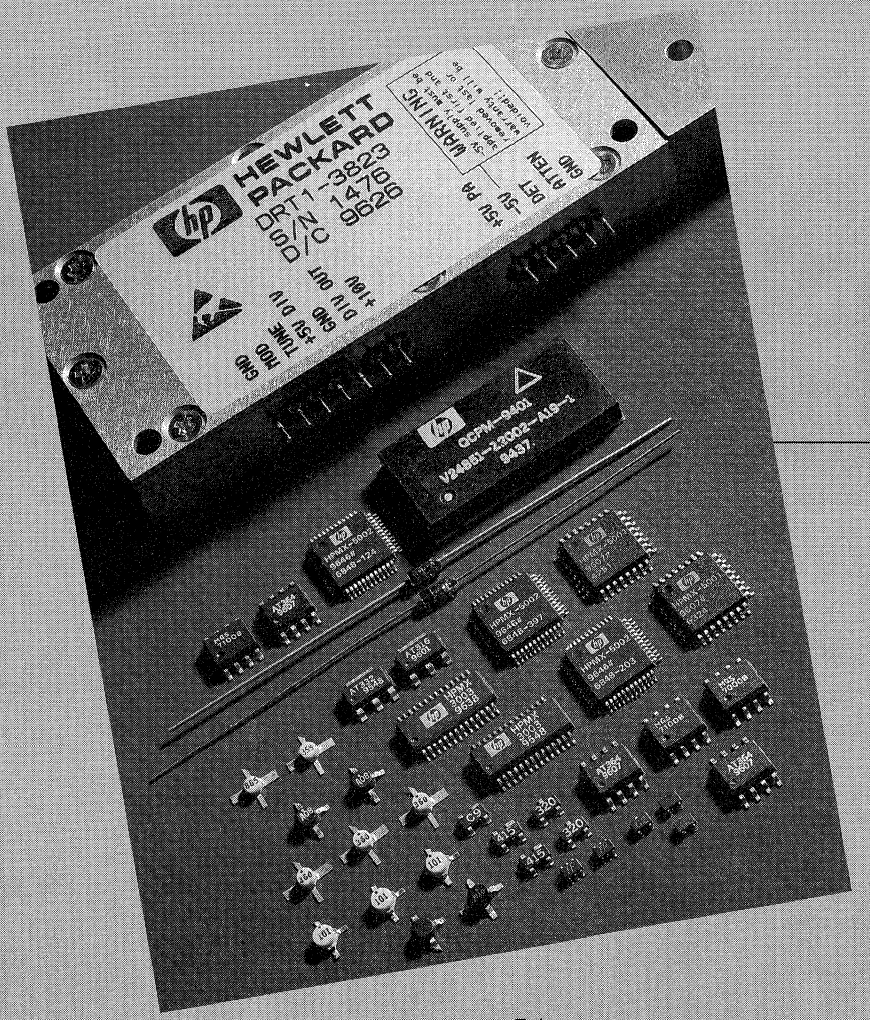
(MIL-STD-202, Method 111):
Meets Needle Flame test per UL Category D (Flaming Time <3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD

Classification: Class I

HEWLETT® PACKARD

RFICs for Mixers, Modulators, Switches, Attenuators, Frequency Dividers, and Other Functions



RFIC Mixers, Modulators, Switches, Attenuators, Frequency Dividers, and Other Functions

Characteristics

Hewlett-Packard manufactures a broad line of innovative microwave and RF integrated circuits for use in the communications marketplace. Our product offering includes general purpose devices as well as products specifically optimized for use in mobile communications handsets, base stations, and TV distribution equipment. Combining HP's technology leadership, the appropriate choice of silicon or GaAs processes, and the smallest size surface mount packages on the market, our engineers create semiconductor solutions that achieve the highest value to you, our customer. Our world-wide manufacturing facilities allow us to produce products with HP's proven quality, in high volumes, at competitive prices.

Processes

A number of processes are used to manufacture these devices.

SAT process:
Hewlett-Packard's state-of-the-art 10 GHz f_T 25 GHz f_{MAX} silicon bipolar process is also used to manufacture the AT line of discrete bipolar transistors. Diffused resistors are added to this joined-backside-collector process to allow the creation of simple ICs such as the MSF self-oscillating mixers.

ISOSAT Process:
Trench isolation is coupled with the SAT transistor engine to create a process optimized for high speed analog integrated circuits. Material and processing enhancements raise the nominal f_T of this process to above 15 GHz. Design flexibility is enhanced through the addition of second metal capability, and by the availability of such on-chip elements such as capacitors, diodes, and high valued resistors. This process also utilizes polyimide as an inter-metal dielectric and scratch protection.

HP-25:
This process results from enhancements to Hewlett-Packard's high speed digital silicon processes, to make it suitable for microwave applications. It has a nominal f_T of 25 GHz.

MESFET processes:
Hewlett-Packard has a number of Gallium Arsenide MESFET processes, variously optimized for gain, noise performance, or power.

PHEMT process:
MMICs processed using this technology are targeted for markets putting a premium on low noise figure and improved device-to-device consistency.

Control Process:
For devices such as switches and attenuators, a special GaAs process is used that provides more robust gate structures for higher power handling capability.

Product families

The HMMC product line offers a variety of high performance chip products for use at microwave and millimeter wave frequencies. The HMMC-1002 is a voltage variable attenuator operational from DC to 50 GHz. The HMMC-2006 and HMMC-2007 are reflective and absorptive SPDT switches operating to 8 GHz, while the HMMC-2027 is a reflective SPDT switch operating to 26.5 GHz.

The HPMX series products are designed for transmitter applications. The HPMX-2xxx series are modulator products, and include both BPSK and QPSK modulators. The HPMX-3xxx series are power amplifier products, and include both an integrated driver amplifier

with power control as well as a multi-function LNA-switch-power amplifier IC. The HPMX-5001 and HPMX-5002 and HPMX-3003 form a chipset for use in either Digital European Cordless Telephone (DECT) or the 2.4 GHz band.

The IAM family are mixer circuits. The IAM-8x series are silicon Gilbert cell multiplier-based frequency converters. This structure works well as an active mixer in functions requiring load insensitive conversion gain, good spurious signal suppression, low LO power and moderate dynamic range. The IAM-9x series are GaAs FET based mixer ICs with functionality similar to that provided by dual-gate mixers. These devices have an advantage in applications requiring low noise figures or higher frequencies.

The IFD series products are silicon prescalers with operation to 5 GHz.

The MGS family are single-pole double-throw switches designed for commercial applications. Both an absorptive version (MGS-71 series) and a reflective version (MGS-70 series) are offered. The very low current draw of these MMIC switches makes them a superior choice in applications where power consumption is a major concern. Operation is from DC to 6 GHz depending on the package.

Application Information

The following application information is either published in this catalog or available from your local Hewlett-Packard sales office, authorized distributor, or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

Application Notes

Abstracts

Evaluation of Vector Modulator IC Performance

Application Note—1126

The following brief discussion describes some of the tests used to evaluate the performance of vector modulator ICs.

Power Output

Power output of a vector modulator IC can be specified in different ways. The most common way is the single sideband (SSB) output power level. An alternative way that is easier to test is the peak output power. The SSB output power will be 3 dB lower than the peak power.

Peak power output can be measured by simply applying DC voltages to the I and Q modulation inputs with appropriate reference voltages applied to Iref and Qref. If the normal reference voltage is 2.5 VDC, a 1.2 Vp-p I, Q signal can be simulated by applying 0.6VDC + 2.5VDC = 3.1VDC to both the Imod and Qmod inputs. The resulting output power read on a spectrum analyzer will be about 3 dB above the SSB output power.

The LO leakage section of this discussion describes a method of directly measuring the SSB output power.

LO Leakage

There are two main causes of LO leakage through a QPSK modulator. The first is the basic performance of the IC with no external signals other than required bias voltages and LO signal applied. The second is LO leakage that is due to externally applied signals.

The inherent LO suppression of the IC is the result of the variability of the electrical properties of the transistors and resistors that make up the IC. Random variations IC components can lead to DC offsets at the I and Q inputs. These DC offsets are multiplied by the LO signal and appear at the output as LO leakage. The larger the offset, the greater the LO leakage.

The LO leakage of an IC can be measured by connecting all four I and Q inputs to a bias source (typically Vcc/2 = 2.5 VDC). Apply the LO signal that is standard for the IC (the level used in the data sheet measurements) and observe the output on a spectrum analyzer with the sweep centered on the LO frequency. Subtract the power output indicated from the peak power output (measurement described above) to determine the LO suppression relative to the peak output. The LO suppression relative to a SSB output will be 3 dB lower because the peak power reading is 3 dB higher than the SSB power output.

The most common way of specifying the LO leakage is to specify the LO suppression relative to SSB output power. An SSB test can be performed by applying sine and cosine signals to the I and Q inputs, along with any appropriate DC biases required, and the LO signal. The spectrum analyzer will show a classic SSB output spectrum making it very easy to calculate the LO suppression-simply subtract the LO leakage level from the unsuppressed sideband level.

A third alternative is to use the DSB output obtained by applying in-phase sine wave signals to both I and Q inputs along with appropriate DC biases and the LO signal. The two sidebands will read 3 dB lower in power than the SSB peak output so the LO suppression relative to the sidebands will be 3 dB lower than the value obtained from the SSB

test (and 6 dB lower than the value obtained from the peak power test).

When performing the SSB and DSB measurements, you must be extremely careful to ensure that the average level of the AC signals applied to the I and Q inputs are exactly equal to the DC bias applied to the Iref and Qref inputs. You should try to match the DC levels within 1 or 2 millivolts.

Modulation Error (Sideband Suppression)

The QPSK modulator's purpose is to modulate the phase of a carrier signal with equal amplitude at each of four or eight possible data points. Real modulators do not shift the phase to the exact theoretical value, and there is always some variation in the amplitude of the output signal.

Modulation error can be expressed in terms of rms or peak levels of amplitude error, phase error, and /or percent error. One common but flawed technique for estimating rms (average) phase error is to use the SSB suppression in the following formula:

SSB suppression (dBc) =

$$10 \log \frac{(1 + \cos f)}{(1 - \cos f)}$$

where ϕ is the average phase error in degrees.

The sideband suppression can be obtained from the above described test for SSB power output/LO suppression. Note that the sideband suppression obtained is critically dependent on matching the peak to peak amplitudes of the I and Q signals.

Though our measured data follows the general shape of the theoretical curve, it rarely meets the curve. The actual data varies by as much as ±10 dB about the theoretical curve. Also, applications such as GSM telephones have definite limits on the peak phase error, a value that cannot be obtained from the formula. For these reasons, a direct measurement is the best way to evaluate modulator error performance.

The amplitude and phase error can easily be measured by using a vector network analyzer to perform an S21 measurement. The LO signal for the modulator is provided by port 1 of the analyzer (set the output to an appropriate value) with the output of the modulator connected to port 2 of the analyzer (an attenuator at the output of the IC may be needed. The Iref and Qref pins should be biased normally (≈2.5 VDC) and the Imod and Qmod pins connect to precise DC sources such as HP-6626A system power supply. The Imod and Qmod voltages are set to values that should give predictable phase shifts (at 15° intervals, for example) and an S21 reading is performed at each point as the voltages are changed, until a full 360° phase rotation has been achieved. Table 1 shows a sequence of voltages to apply to a vector modulator for 15° steps around the I, Q circle.

Table 1.

Voltage at Imod (VDC)	Voltage at Qmod (VDC)	Relative Vector Angle (degrees)
3.750	2.500	0
3.707	2.824	15
3.583	3.125	30
3.384	3.384	45
3.125	3.583	60
2.824	3.707	75
2.500	3.750	90
2.176	3.707	105
1.875	3.583	120
1.616	3.384	135
1.417	3.125	150
1.293	2.824	165
1.250	2.500	180
1.293	2.176	195
1.417	1.875	210
1.616	1.616	225
1.875	1.417	240
2.176	1.293	255
2.500	1.250	270
2.824	1.293	285
3.125	1.417	300
3.384	1.616	315
3.583	1.875	330
3.707	2.176	345

Notes to Table 1:

1. voltages applied to Imod and Qmod inputs always fit the following formula:
   $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2} = 1.25$ which is simply the equation of the I, Q circle in the V_{Imod}, V_{Qmod} coordinate axes shown in Figure 1.
2. $V_{Imod} = 2.5 + 1.25 \cos \theta$ where θ is the vector angle from the I axis.
3. $V_{Imod} = 2.5 + 1.25 \sin \theta$ where θ is the vector angle from the I axis.

The average value of the magnitude of the S21 readings will be the reference for amplitude error calculations. Since the phase value read will depend upon the analysis frequency, the cables used and the fixture or test board, the phase readings will be relative. The first phase measurement is normally chosen as the reference to which all the other phase readings will be compared. The average amplitude error is just the numerical average of the difference between each amplitude reading and the reference value (the average value of all the readings). The average phase error is the average of the differences between each phase value and the reference value. The peak phase error is the highest magnitude value of difference between the input phase (corrected to the reference) value and each measured value.

Modulation error can be expressed as a percentage by using the instantaneous amplitude error and phase error values. The modulation error percentage is 100 times the ratio of the error vector (the line between the actual modulation point and the average modulation point) and average vector magnitudes (the average value of magnitude at all points measured). The magnitude of the error vector is determined by following the formulas presented below.

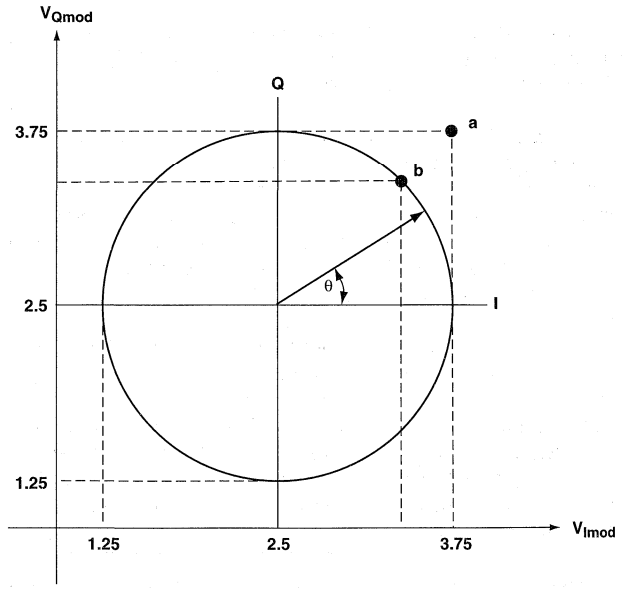


Figure 1. I and Q coordinate axes. "a" is the point where peak output power is measured. "b" is the point where the SSB output power is measured.

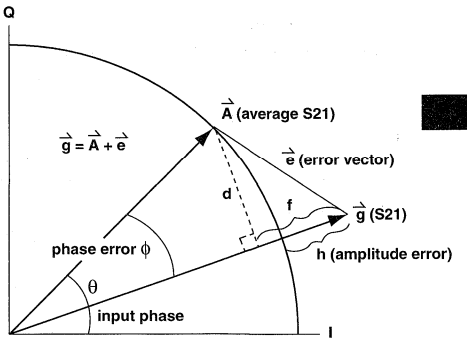


Figure 2. Illustration of error vector magnitude for calculating percent modulation error.

Amplitude error, $h = |\vec{A}| - |\vec{g}|$ where $|\vec{A}|$ is the average S21 magnitude and $|\vec{g}|$ is the magnitude of the S21 reading at the specific point where we want to calculate the modulation error percentage. Note: S21 magnitude readings must be in linear terms, not decibels. Phase readings should be in degrees.

$$\text{percent modulation error} = 100 \frac{|\vec{e}|}{|\vec{A}|}$$

$$|e| = \sqrt{d^2 + f^2}$$

$$d = |\vec{A}| \sin\left(\phi \frac{\pi}{80}\right) \approx |\vec{A}|\, \phi\, \frac{\pi}{180} \text{ for small values of phase error, } \phi$$

$$f = |\vec{g}| - |\vec{A}| \cos\left(\phi \frac{\pi}{180}\right) \approx h \text{ for small values of phase error, } \phi$$

$$\therefore |e| = \sqrt{\left(|A|\phi \frac{\pi}{180}\right)^2 + h^2}$$

$$\text{percent modulation error} \approx 100 \frac{\sqrt{\left(|\vec{A}|\phi \frac{\pi}{180}\right)^2 + h^2}}{|\vec{A}|}$$

Summary

The old computer adage about GIGO (garbage-in, garbage-out) is especially applicable to IC modulator tests. Measuring the performance of a vector modulator IC requires a thorough understanding and careful control of all the input signals. The table below summarizes the common problems and their causes.

Symptom	Probable Cause/Solution
Power output below spec	Test conditions (SSB, DSB, peak) should match data sheet conditions- any of the following conditions may lead to low output power: 1) insufficient LO power 2) I and Q signal levels too low or the wrong type 3) Vcc too low 4) LO frequency too high 5) blocking caps at LO input or RF output too small at low frequencies 6) quality of solder connections—especially at RFout pin
LO leakage above spec (poor carrier suppression)	DC offset between Imod and Iref and/or Qmod and Qref. Check for offsets with DMM, make adjustments to average Imod, Qmod signal levels, or adjust bias voltages at Iref and/or Qref for 0 offset. Use **sine wave** LO drive! Using signals with harmonics above about -20 dBc will degrade performance of the modulator.
Sideband suppression above spec	Amplitude imbalance between Imod and Qmod. Adjust for equal amplitude with an oscilloscope or a true-rms voltmeter. This problem can also be the result of a non 90° phase shift between the I and Q signals or an improperly functioning LO phase shifter. Use **sine wave** LO drive! Using signals with harmonics above about -20 dBc will degrade performance of the modulator.
Harmonics of I, Q signals in output spectrum	Probably using too high an I, Q level—check peak-to-peak levels using an oscilloscope or wide bandwidth true-RMS voltmeter. This problem can also be the result of using a distorted sine-wave signals (GIGO)- check I and Q signals for harmonic content with a low frequency spectrum analyzer or distortion analyzer.
Other poor performance	Be sure you are using a "clean" LO signal. You should be using a sine-wave source with harmonics at least 20 dB below the fundamental frequency. Square wave sources will not work!

Applications

The application notes represented by these abstracts are available from your local Hewlett-Packard sales office or nearest Hewlett-Packard authorized distributor or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

AN-A004R
Electrostatic Discharge and Damage Control
identifying and preventing ESD damage

Publication No. 5091-8803E

AN-A006
Mounting Considerations for Packaged Microwave Semiconductors
Mechanical, thermal, and soldering information

Publication No. 5091-8696E

AN-G007
MGS Series Monolithic GaAs Switches
DC to 6 GHz packaged switch use, including information on driver circuits.

Publication No. 5091-3746E

AN-S010
A 5.0 GHz Bipolar Active Mixer
This application note contrasts the features and performance of an active bipolar Gilbert cell based mixer with conventional passive diode mixers.

Publication No. 5966-0453E

AN-S013
MagIC Active Mixers
The what, why, and how-to for IAM-8x series active mixers including a demonstration circuit.

Publication No. 5091-6488E

DesignPak
DesignPak is a comprehensive data library of s-parameter and noise parameter data for Hewlett Packard RF and microwave semiconductors. It includes data for the MSF series self-oscillating mixers, the MGS series switches, the HMMC series attenuators, and the HPMX-3x series ICs.

Publication No. 5963-2301E

RFIC Mixers, Modulators, Switches, Attenuators, Frequency Dividers, and Other Functions Selection Guides

Mixers

Part Number	Description	Package	F in (GHz)	F out (GHz)	IP_3 (dBm)	V_{cc} (V)	I_c (mA)	Page No.
HPMX-2006	double balanced upconverter	SSOP-16	DC-0.9	0.8-2.5	+2	3	15	7-66
	(with integrated post amplifier)				+14	3	38	
IAM-81008	3-port double balanced mixer	SO-8	.05-5.0	up to 2.4	+3	5	12.5	7-119
IAM-81028	3-port double balanced mixer	hermetic	.05-5.0	up to 2.4	+3	5	12.5	7-123
IAM-82008	3-port double balanced mixer	SO-8	.05-5.0	up to 3	+18	10	55	7-127
IAM-82028	3-port double balanced mixer	hermetic	.05-5.0	up to 3	+18	10	55	7-131
IAM-91563	unbalanced downconverter with adjustable bias	SC-70	0.8-6.0	.05-0.7	+3/+7.5	3	9/16	7-135

For discrete implementation, see also Schottky diodes

Modulators

Part Number	Description	Package	F out (GHz)	P_{1dB} (dBm)	V_{cc} (V)	I_c (mA)	Page No.
HPMX-2003	QPSK with power match	SO-16	0.8-1.0	+3	5	39	7-38
HPMX-2005	QPSK	SO-16	0.05-0.25	-5	5	15	7-54
HPMX-2006	BPSK (modulator only)	SSOP-16	0.8-2.5	-8.5	3	15	7-66
	BPSK (with post-amplifier)			+4.5	3	38	
HPMX-2007	QPSK (modulator only)	SSOP-16	0.04-0.4	-23	3	10	7-74
	QPSK (with upconverting mixer)		0.005-4	-15	3	25	

Multi-Function RFICs

Part Number	Description	Package	V_{cc} (V)	I_c (mA)	Page No.
HPMX-3002	900 MHz integrated driver amplifier	SO-8	6	160	6-76
HPMX-3003	1.5 - 2.5 GHz LNA / switch/PA	SSOP-28	3	5 / - / 450	7-82
HPMX-5001	1.5 - 2.5 GHz Upconverter -Downconverter	TQFP-32	3	39, 60	7-90
HPMX-5002	DECT IF Modulator/Demodulator	TQFP-48	3	21	7-105

Selection Guide, continued

Switches

Part Number	Description	Package	Frequency Range (GHz)	Power (dBm)	$V_{control}$ (V)	Page No.
HMMC-2006	SPDT reflective switch	chip	DC-6	+27 P_{1dB}	-10	7-20
HMMC-2007	SPDT absorptive switch	chip	DC-8	+27 P_{1dB}	-10/+10	7-26
HMMC-2027	SPDT reflective switch	chip	DC-26	+27 P_{1dB}	-10	7-32
HPMX-3003	LNA/Switch/PA	SSOP-28	1.5-2.5	+55 IP_3	-5	7-82
MGS-70008	SPDT reflective switch	SO-8	DC-3	+45 IP_3	-5	7-156
MGS-71008	SPDT absorptive switch	SO-8	DC-3	+45 IP_3	-5	7-161

For discrete implementation, see also PIN diodes

Other ICs

Part Number	Description	Package	V_{cc} (V)	I_c (mA)	Page No.
IFD-53010	5 GHz Divide by 4 prescaler	100 mil stripline	5 or -5	43	7-151
IFD-53011	3 GHz Divide by 4 prescaler	100 mil stripline	5 or -5	43	7-151
HMMC-1002	DC-50 GHz Variable Attenuator	chip	0, -4	-	7-12

HEWLETT® PACKARD

DC – 50 GHz Variable Attenuator

Technical Data

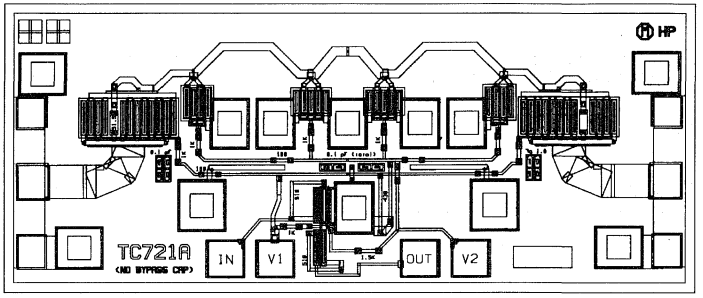
HMMC-1002

Features

- **Specified Frequency Range:** DC - 26.5 GHz
- **Return Loss:** 10 dB
- **Minimum Attenuation:** 2.0 dB
- **Maximum Attenuation:** 30.0 dB

Description

The HMMC-1002 is a monolithic, voltage variable, GaAs IC attenuator that operates from DC to 50 GHz. It is fabricated using MWTC's MMICB process which features an MBE epitaxial layer, backside ground vias, and FET gate lengths of approximately 0.4 mm. The variable resistive elements of the HMMC-1002 are two 750 mm wide series FETs and four 200 mm wide shunt FETs. The distributed topology of the HMMC-1002 minimizes the parasitic effects of its series and shunt FETs, allowing the HMMC-1002 to exhibit a wide dynamic range across its full bandwidth. An on-chip DC reference circuit may be used to maintain optimum VSWR for any attenuation setting or to improve the attenuation versus voltage linearity of the attenuator circuit.



Chip Size:	1470 x 610 µm (57.9 x 24.0 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
RF Pad Dimensions:	60 x 70 µm (2.4 x 2.8 mils), or larger
DC Pad Dimensions:	75 x 75 µm (3.0 x 3.0 mils), or larger

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{DC-RF}	DC Voltage to RF Ports	V	-0.6	+1.6
V_1	V_1 Control Voltage	V	-5.0	+0.5
V_2	V_1 Control Voltage	V	-5.0	+0.5
V_{DC}	DC In/DC Out	V	-0.6	+1.0
P_{in}	RF Input Power	dBm		17
T_{mina}	Minimum Ambient Operating Temperature	°C	-55	
T_{maxa}	Maximum Ambient Operating Temperature	°C		+125
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp.	°C		+300

Note:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.

DC Specifications/Physical Properties, $T_A = 25°C$

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{V1}	V_1 Control Current, (V_1 = -4V)	mA	5.3	9.3	12
I_{V2}	V_2 Control Current, (V_2 = -4V)	mA	5.3	9.3	12
V_p	Pinch-off Voltage (V_2, with V_1 = 0 V) Four 200 µm wide shunt FETs, V_{DD} = 1 V @ RF_{in}, I_{DD} = 5 mA	V	-0.6	-1.3	-2.5

Electrical Specifications[1], $T_A = 25°C$, $Z_O = 50\ \Omega$

Parameters and Test Conditions	Units	Freq. (GHz)	Min.	Typ.	Max.
Minimum Attenuation, $\|S_{21}\|$ V_1 = 0 V, V_2 = -4 V	dB	1.5		1.0	2.4
		8.0		1.4	2.4
		20.00		1.7	2.4
		26.5		2.0	2.4
		50.0		3.9	
Input/Output Return Loss @ Min. Attenuation Setting, V_1 = 0 V, V_2 = -4 V	dB	<26.5	10	16	
		<50.0		8	
Maximum Attenuation, $\|S_{21}\|$ V_1 = -4 V, V_2 = 0 V	dB	1.5	27	30	
		8.0	27	38	
		20.0	27	38	
		26.5	27	40	
		50.0		35	
Input/Output Return Loss @ Max. Attenuation Setting, V_1 = -4 V, V_2 = 0 V	dB	<26.5	8	10	
		<50.0		10	
DC Power Dissipation (does not include input signals) V_1 = -5 V, V_2 = -5 V	mW				152

Applications

The HMMC-1002 is designed to be used as a gain control block in an AGC assembly. Because of its wide dynamic range and return loss performance, the HMMC-1002 may also be used as a broadband pulse modulator or single-pole single-throw, non-reflective switch.

Operation

The attenuation of the HMMC-1002 is adjusted by applying negative voltages to V1 and V2. V1 controls the drain-to-source resistances of the series FETs while V2 controls the drain-to-source resistances of the shunt FETs. For any HMMC-1002 the values of V1 may be adjusted so that the device attenuation versus voltage is monotonic for both V1 and V2; however, this will slightly degrade the input and output return loss.

The attenuation of the HMMC-1002 may also be controlled using only a single input voltage by utilizing the on-chip DC reference circuit and the driver circuit shown in Figure 4. This circuit optimizes VSWR for any attenuation setting. Because of process variations, the values of V_{REF}, R_{REF}, and R_L are different for each wafer if optimum performance is required. Typical values for these elements are given. The ratio of the resistors R1 and R2 determines the sensitivity of the attenuation versus voltage performance of the attenuator. For more information on the performance of the HMMC-1002 and the driver circuits previously mentioned see MWTC's Application Note #37, "HMMC-1002 Attenuator: Attenuation Control." For more S-parameter information, see MWTC's Application Note #44, "HMMC-1002 Attenuator: S-Parameters."

Assembly Techniques

Solder die attach using a AuSn solder preform is the recommended assembly method; however, an epoxy die attach method using ABLEBOND® 71-1LM1 or ABLEBOND® 36-2 may also be employed. Gold thermosonic wedge bonding with 0.7 mil wire is the recommended method for bonding to the device. Tool force should be 22 grams ± 1 gram, stage temperature is 150 ± 2°C, and ultrasonic power and duration of 64 ± 1 dB and 76 ± 8 msec, respectively. The top and bottom metallization is gold.

For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

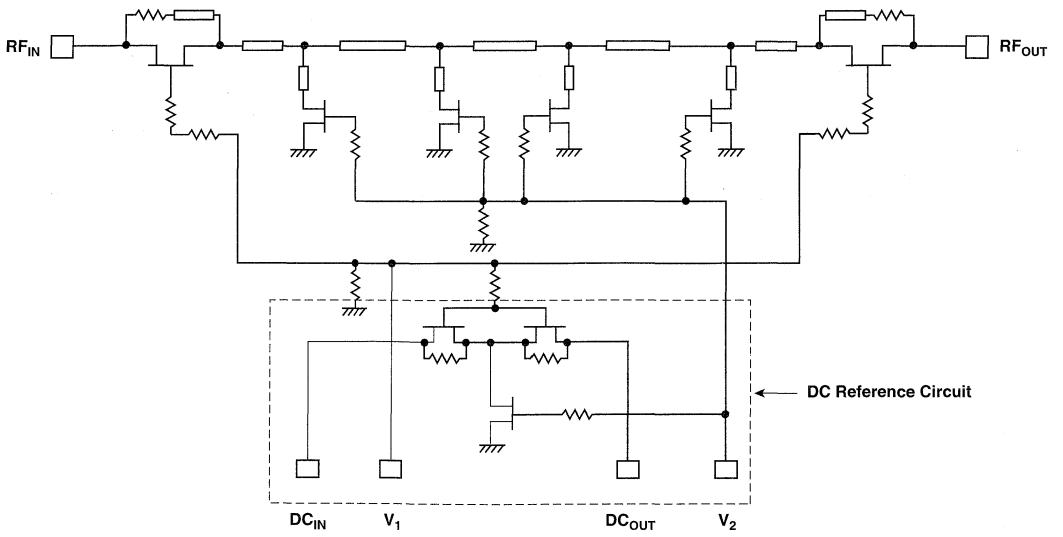
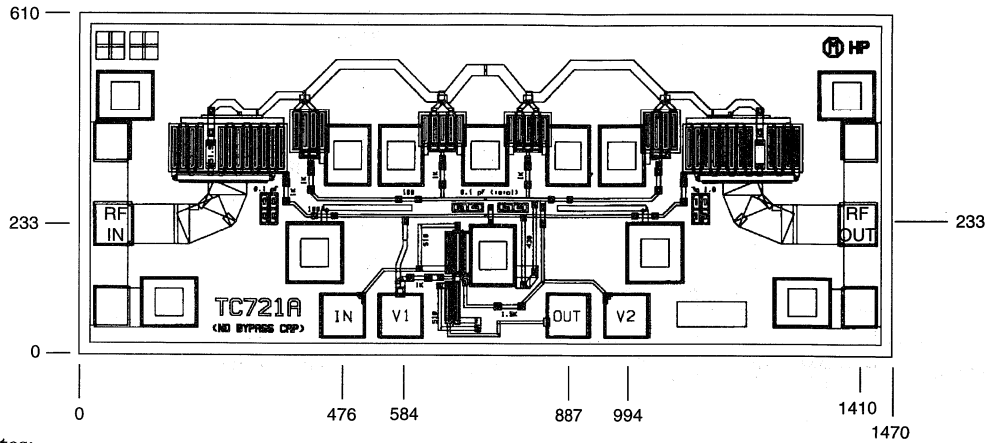


Figure 1. HMMC-1002 Schematic.



Notes:

1. All dimensions in microns and shown to center of bond pad.
2. DC_{in}, V1, DC_{out}, and V_2 bonding pads are 75 x 75 microns.
3. RF input and output bonding pads are 60 x 70 microns.
4. Chip thickness: 127 ± 15 µm.

Figure 2. HMMC-1002 Bonding Pad Locations.

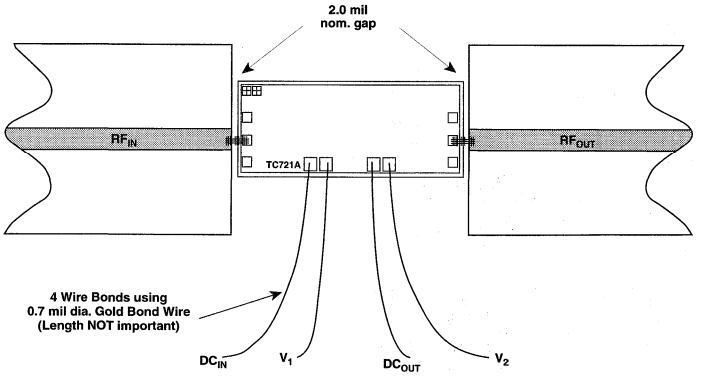


Figure 3. HMMC-1002 Assembly Diagram.

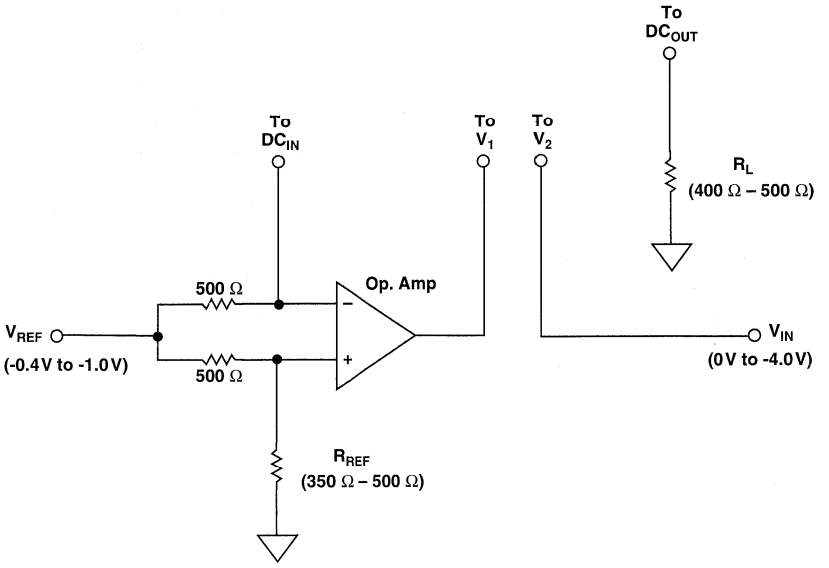


Figure 4. Attenuator Driver.

HMMC-1002 Typical Performance

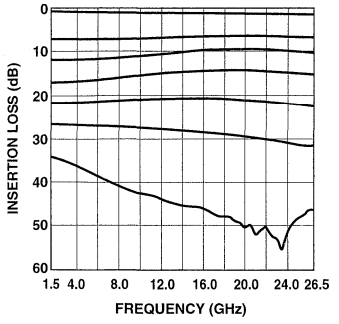


Figure 5. Attenuation vs. Frequency[1].

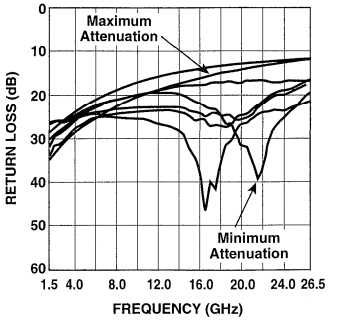


Figure 6. Output Return Loss vs. Frequency[1].

Note:

1. Data obtained from on-wafer measurements. T_{chuck} = 25°C.

HMMC-1002 Typical Power Performance

All Attenuation Settings were done at 1 GHz.

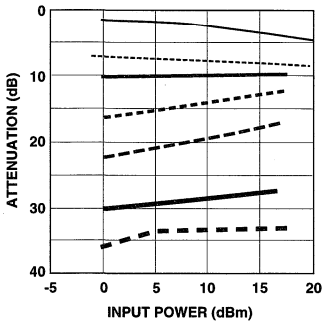


Figure 7. Attenuation vs. Input Power @ 50.0 MHz.[1].

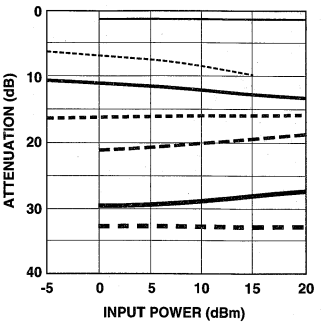


Figure 8. Attenuation vs. Input Power @ 2.0 GHz.[1].

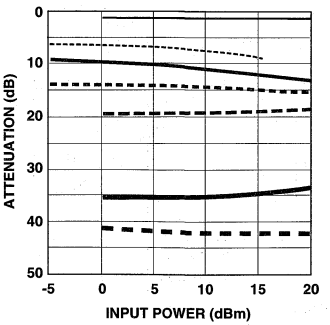


Figure 9. Attenuation vs. Input Power @ 10.0 GHz.[1].

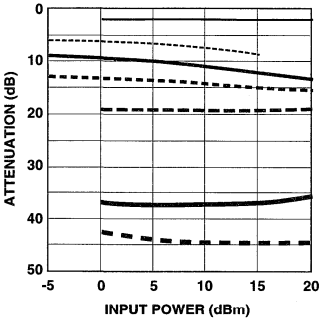


Figure 10. Attenuation vs. Input Power @ 14.0 GHz.[1].

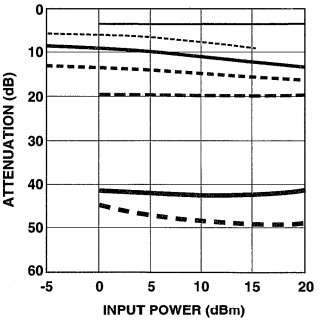


Figure 11. Attenuation vs. Input Power @ 18.0 GHz.[1].

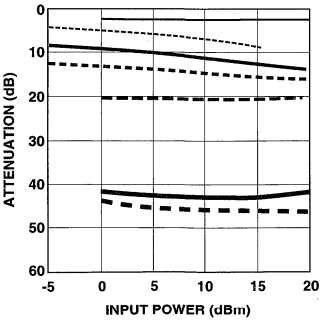


Figure 12. Attenuation vs. Input Power @ 22.0 GHz.[1].

Note:

1. Data taken with the device mounted in connectorized package.

Key for Attenuation Settings:

- Min.
- Min. + 5 dB
- Min. + 10 dB
- Min. + 15 dB
- Min. + 20 dB
- Min. + 30 dB
- Max.

HMMC-1002 Typical Harmonic Performance

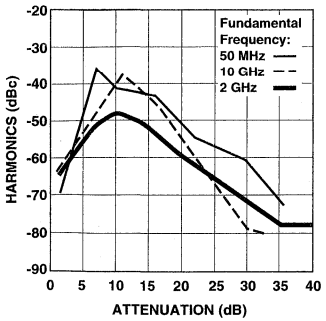


Figure 13. Second Harmonic Suppression vs. Attenuation. Input Power = 0 dBm[1].

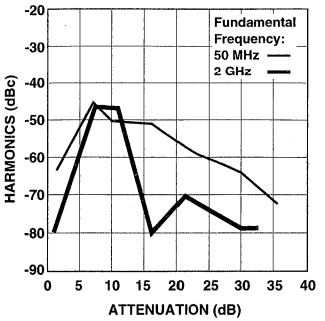


Figure 14. Third Harmonic Suppression vs. Attenuation. Input Power = 0 dBm[1].

Note:

1. Data taken with the device mounted in connectorized package.

HMMC-1002 Typical Temperature Performance

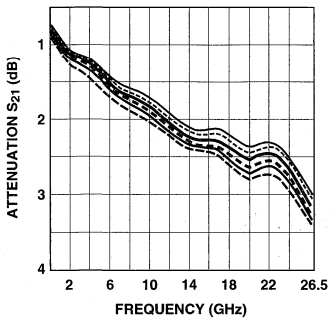


Figure 15. Attenuation vs. Temperature @ Minimum Attenuation.[2].

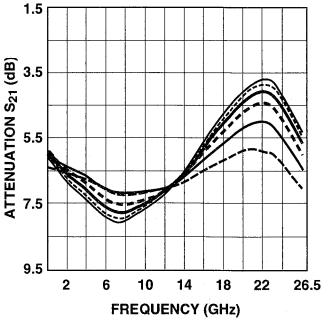


Figure 16. Attenuation vs. Temperature @ 5 dB Attenuation.[2].

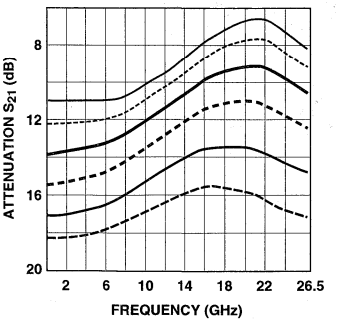


Figure 17. Attenuation vs. Temperature @ 10 dB Attenuation.[2].

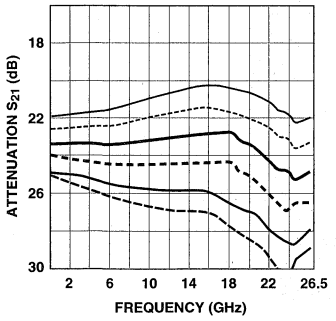


Figure 18. Attenuation vs. Temperature @ 20 dB Attenuation.[2].

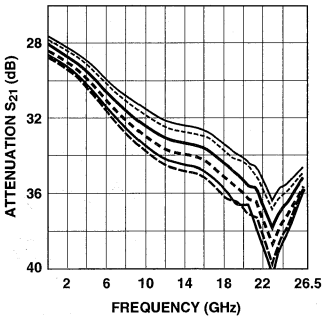


Figure 19. Attenuation vs. Temperature @ 30 dB Attenuation.[2].

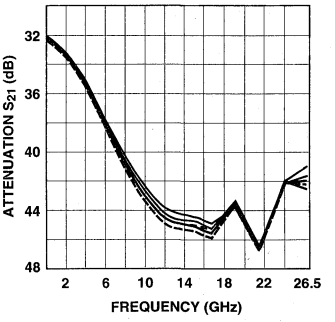


Figure 20. Attenuation vs. Temperature @ Max. Attenuation.[2].

Note:

1. Data taken with the device mounted in connectorized package.

Key for Temperature Settings:

- —— -55°C
- ------- -25°C
- —— 0° C
- - - - +25°C
- —— +55°C
- - - - +85°C

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

HEWLETT® PACKARD

DC – 6 GHz Unterminated SPDT Switch

Technical Data

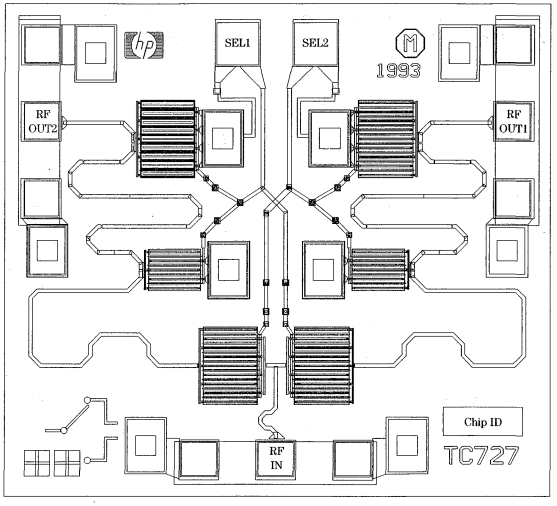
HMMC-2006

Features

- **Frequency Range:** DC-6 GHz
- **Insertion Loss:**
  <1dB @ 6 GHz
- **Isolation:**
  >70 dB @ 45 MHz
  >35 dB @ 6 GHz
- **Return Loss:** >12 dB
  (Both Input & Output)
- **Switching Speed:** <1 ns
- **P_{-1dB}:**
  23 dBm @ 50 MHz
  >27dBm @ 6 GHz
- **Harmonics:** <-25 dBc @
  20 dBm (DC coupled)

Description

The HMMC-2006 is a GaAs monolithic microwave integrated circuit (MMIC) designed for low insertion loss and high isolation from DC to 6 GHz. It is intended for use as a general-purpose, singlepole, double-throw (SPDT) switch. One series and two shunt MESFETs per throw provide 1.2 dB maximum insertion loss and 35 dB minimum isolation at 6 GHz. HMMC-2006 chips use through-substrate vias to provide ground connections to the chip backside and minimize the number of wire bonds required. The HMMC-2006 is also available in an 8-lead flatpack (1GG7-4201).



Chip Size:	960 x 1070 µm (37.8 x 42.1 mils)
Chip Size Tolerance:	+0, -10 µm (+0, -0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	80 x 80 µm (3.2 x 3.2 mils), or larger

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{sel}	Select Voltages 1 and 2	V	-12	+3
P_{in}	RF Input Power	dBm		30
T_{op}	Operating Temperature	°C	-55	+125
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp. (for 60 seconds max.)	°C		+300

Note:

1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A = 25°C except for T_{ch}, T_{STG}, and T_{max}.

DC Specifications/Physical Properties, T_A = 25°C

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_l	Leakage Current @ -10 V	µA			100
V_p	Pinch-off Voltage @ 8 mA	V	-6.75		-3.25
BV_{gss}	Breakdown Voltage Total	V	-18.0		-12.5

RF Specifications, T_A = 25°C, Z_O = 50 Ω, V_{sel} high = 0 V, V_{sel} low = -10 V

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
BW	Guaranteed Operating Bandwidth		GHz	DC		6
IL	Insertion Loss, RF_{in} to RF_{out},	f = 6 GHz, ON throw	dB		1	1.2
ISO	Isolation, RF_{in} to RF_{out},	f = 6 GHz, OFF throw	dB	35	40	
RL_{in}	Input Return Loss		dB	12	14	
RL_{out}	Output Return Loss		dB	12	15	
$P_{1\,dB}$	Input Power where IL increases by 1 dB	f = 50 MHz	dBm	18	23	
t_s	Switching Speed, 10%–90% RF Envelope,	f = 2 GHz	ns		1	

Applications

The HMMC-2006 can be used in instrumentation, communications, radar, ECM, EW, and many other systems requiring SPDT switching. It can be used for pulse modulation, port isolation, transfer switching, high-speed switching, replacement of mechanical switches, and so on. It can also be used as a terminated SPST (single-pole-single-throw) switch by placing a 50 Ω load on either RF output port.

Assembly Techniques

Die attach may be done with either a AuSn solder preform or conductive epoxy. Gold thermosonic bonding is recommended for all bonds. The top and bottom metallization is gold. For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

S-Parameters[1], T_A = 25°C, Z_O = 50 Ω, V_{sel} high = 0 V, V_{sel} low = -10 V

Frequency GHz	S_{11}		S_{21} (Insertion Loss)		S_{31} (Isolation)	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
0.1	0.93	-8	4.26	172	0.01	86
0.5	0.0365	-27.03	0.9366	-11.32	0.0010	78.03
1.0	0.0372	-41.81	0.9336	-17.35	0.0017	76.84
1.5	0.0448	-63.14	0.9311	-23.47	0.0026	76.05
2.0	0.0542	-80.60	0.9286	-27.67	0.0033	75.66
2.5	0.0631	-88.46	0.9271	-29.73	0.0039	77.4
3.0	0.0715	-93.98	0.9242	-33.03	0.0049	81.14
3.5	0.0795	-101.90	0.9199	-38.93	0.0059	82.09
4.0	0.0872	-108.90	0.9164	-45.14	0.0063	78.90
4.5	0.0951	-114.40	0.9123	-50.49	0.0068	78.94
5.0	0.1022	-120.90	0.9054	-56.36	0.0078	84.68
5.5	0.1074	-123.50	0.9032	-62.07	0.0084	84.71
6.0	0.1138	-132.70	0.9058	-69.04	0.0115	91.24

Note:

1. 3-port-wafer-probed data.

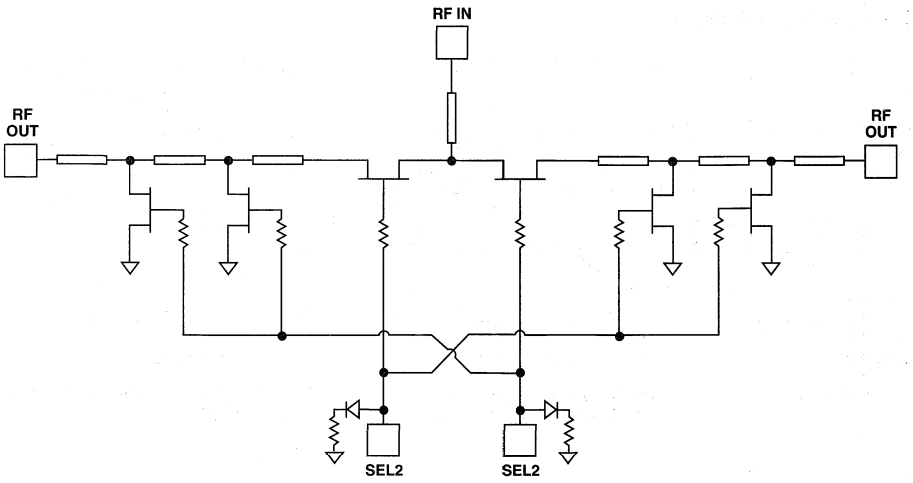


Figure 1. HMMC-2006 Schematic.

Recommended Operating Conditions, $T_A = 25°C$

Select Line		RF Path	
SEL1	**SEL2**	**RF IN to RF OUT1**	**RF IN to RF OUT2**
-10 V	0 V	Isolated	Low Loss
0 V	-10 V	Low Loss	Isolated

HMMC-2006 Typical Performance

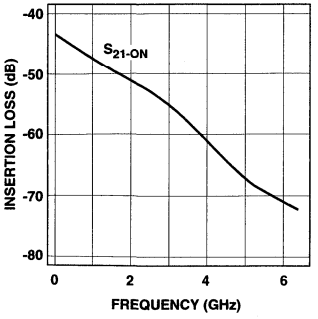


Figure 2. Insertion Loss[1] vs. Frequency.

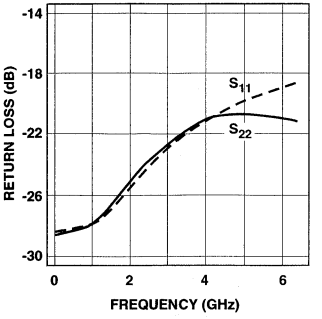


Figure 3. Input and Output (On Throw) Return Loss[1] vs. Frequency.

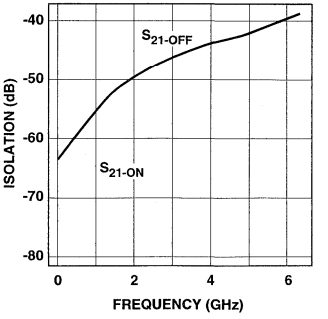


Figure 4. Input-to-Output Isolation[1] vs. Frequency.

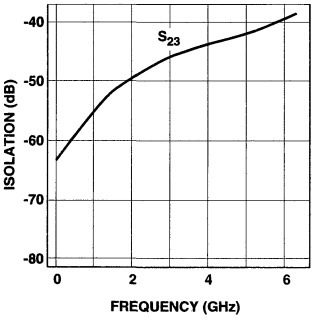


Figure 5. Output-to-Output Isolation[2] vs. Frequency.

Notes:

1. Wafer-probed measurements
2. Calculated from wafer-probed measurements

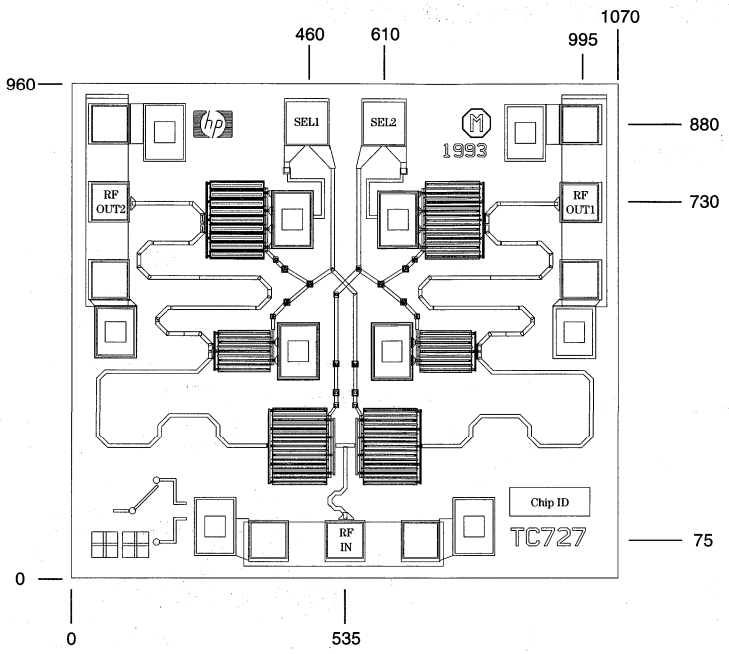


Figure 6. HMMC-2006 Bonding Pad Locations. (Dimensions in micrometers)

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

DC – 8 GHz Terminated SPDT Switch

Technical Data

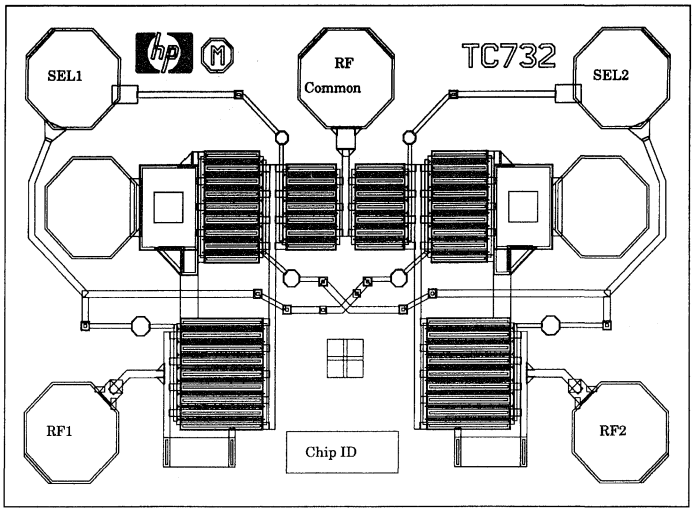
HMMC-2007

Features

- **Outputs Terminated in 50 Ω When Off**
- **Frequency Range:** DC-8 GHz
- **Insertion Loss:** 1.2 dB @ 8 GHz
- **Isolation:** >70 dB @ 45 MHz >35 dB @ 8 GHz
- **Return Loss:** 25 dB (Both Input and Selected Output) 18 dB Unselected Output
- **Switching Speed:** <20 µs (10%-90% RF)
- **P_{-1dB}:** 27 dBm
- **Harmonics (DC Coupled):** <-80 dBc @ 10 dBm

Description

The HMMC-2007 is a GaAs monolithic microwave integrated circuit (MMIC) designed for low insertion loss and high isolation from DC to 8 GHz. It is intended for use as a general-purpose, single-pole, double-throw (SPDT), absorptive switch. Two series and two shunt MESFETs per throw provide 1.4 dB maximum insertion loss and 38 dB typical isolation at 6 GHz. HMMC-2007 chips use through-substrate vias to provide ground connections to the chip backside and minimize the number of wire bonds required.



Chip Size:	660 x 960 µm (25.9 x 37.8 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	120 x 120 µm (4.7 x 4.7 mils)

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{sel}	Select Voltages 1 and 2	V	-10.5	+10.5
P_{in}	RF Input Power	dBm		27
T_{op}	Operating Temperature	°C	-55	+125
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp.	°C		+200
P_{unsel}	Power into Unselected Output	dBm		27

Note:

1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A = 25°C except for T_{op}, T_{STG}, and T_{max}.

DC Specifications/Physical Properties, T_A = 25°C

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
$I_{SEL\ -10V}$	Leakage Current @ -10 V	µA			200
$I_{SEL\ +10V}$	Leakage Current @ +10 V	µA			20
V_p	Pinch-Off Voltage ($V_{SEL2} = V_p$, V_{RFout2} = +2 V, I_{RFout2} = 4 mA, V_{SEL1} = -10 V, V_{RFout1} = open circuit, V_{RFin} = GND	V	-6.75		-3.00
BV_{gss}	Breakdown Voltage (Test FET w/$V_D = V_S$ = GND, I_G = -50 µA)	V			-13.0

RF Specifications, T_A = 25°C, Z_O = 50 Ω, $V_{sel\text{-}high}$ = +10 V, $V_{sel\text{-}low}$ = -10 V

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
BW	Guaranteed Operating Bandwidth	GHz	DC		8.0
IL	Insertion Loss, RF_{in} to Selected RF_{out}, f = 6 GHz, OFF throw	dB		1.1	1.4
ISO	Isolation, RF_{in} to Unselected RF_{out}, f = 6 GHz, OFF throw	dB		38	
RL_{in}	Input Return Loss @ 6 GHz	dB		25	
$RL_{out\text{-}ON}$	Output Return Loss, ON throw @ 6 GHz	dB		25	
$RL_{out\text{-}OFF}$	Output Return Loss, OFF throw @ 6 GHz	dB		18	
$P_{1\ dB}$	Input Power where IL increases by 1 dB f_{in} = 2 GHz	dBm		27	
t_s	Switching Speed, 10%–90% RF Envelope f_{in} = 2 GHz	µs		20	

Applications

The HMMC-2007 can be used in instrumentation, communications, radar, ECM, EW, and many other systems requiring SPDT switching. It can be used for pulse modulation, port isolation, transfer switching, high-speed switching, replacement of mechanical switches, and so on.

Assembly Techniques

Die attach should be done with conductive epoxy. Gold thermosonic bonding is recommended for all bonds. The top and bottom metallization is gold. For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

S-Parameters[1], $T_A = 25°C$, $Z_O = 50\ \Omega$, V_{sel} high = 0 V, V_{sel} low = -10 V

Freq. GHz	S_{11}			S_{21} (Insertion Loss)			S_{31} (Isolation)	S_{22} (ON Throw)			S_{33} (OFF Throw)		
	dB	Mag.	Ang.	dB	Mag.	Ang.	dB	dB	Mag.	Ang.	dB	Mag.	Ang.
0.5	-26.41	0.048	-57.11	-1.08	0.88	-49.06	-67.74	-28.40	0.03	-47.94	-32.26	0.024	47.18
1.0	-27.53	0.042	-113.83	-1.13	0.88	-93.69	-60.55	-24.74	0.05	-117.54	-30.79	0.029	-38.11
1.5	-30.69	0.029	-176.73	-1.18	0.87	-138.08	-56.17	-31.91	0.02	168.76	-30.35	0.030	-64.68
2.0	-32.37	0.024	115.57	-1.21	0.87	177.39	-53.18	-31.31	0.02	119.22	-26.21	0.049	-134.70
2.5	-31.79	0.026	61.35	-1.25	0.87	133.00	-50.38	-28.90	0.03	68.41	-26.38	0.048	151.66
3.0	-30.60	0.030	4.27	-1.30	0.86	88.53	-47.63	-32.95	0.02	-11.68	-25.66	0.052	103.24
3.5	-28.53	0.037	-58.32	-1.33	0.86	44.08	-45.67	-29.26	0.03	-44.21	-22.99	0.071	38.61
4.0	-27.14	0.044	-124.01	-1.34	0.86	-0.53	-44.12	-30.61	0.02	-113.40	-22.41	0.076	-21.25
4.5	-26.46	0.048	172.69	-1.37	0.85	-45.16	-42.68	-32.21	0.02	165.53	-21.68	0.082	-75.25
5.0	-27.03	0.045	107.19	-1.40	0.85	-89.79	-41.45	-36.49	0.01	141.98	-19.88	0.101	-133.81
5.5	-28.64	0.037	32.44	-1.42	0.85	-134.56	-40.28	-34.51	0.01	4.26	-19.89	0.101	167.02
6.0	-29.55	0.033	-59.18	-1.45	0.85	-179.46	-39.16	-32.44	0.02	-100.27	-19.03	0.112	115.49
6.5	-26.88	0.045	-156.32	-1.51	0.84	135.54	-38.12	-27.18	0.04	176.54	-18.28	0.122	56.80
7.0	-23.24	0.069	130.95	-1.56	0.84	90.76	-37.13	-23.83	0.06	122.00	-18.67	0.117	-2.63
7.5	-21.53	0.084	70.91	-1.52	0.84	46.04	-36.36	-21.48	0.08	51.31	-18.61	0.117	-60.32
8.0	-21.21	0.087	15.06	-1.62	0.83	0.47	-35.64	-21.73	0.08	-15.06	-17.65	0.131	-124.25
8.5	-20.92	0.090	-41.26	-1.64	0.83	-44.44	-34.83	-22.22	0.07	-81.88	-16.95	0.142	172.46
9.0	-19.88	0.101	-104.30	-1.66	0.83	-90.23	-34.13	-20.42	0.09	-145.01	-16.07	0.157	115.03
9.5	-18.65	0.117	-175.05	-1.84	0.81	-135.81	-33.62	-18.17	0.12	145.14	-14.94	0.179	59.82
10.0	-17.04	0.141	116.96	-1.90	0.80	179.24	-34.14	-16.31	0.15	85.15	-14.31	0.193	3.39

Note:

1. Three-port-wafer-probed data: Port 1 = RF Input, Port 2 = Selected RF Output (i.e., ON throw), and Port 3 = Unselected RF Output (i.e., OFF throw).

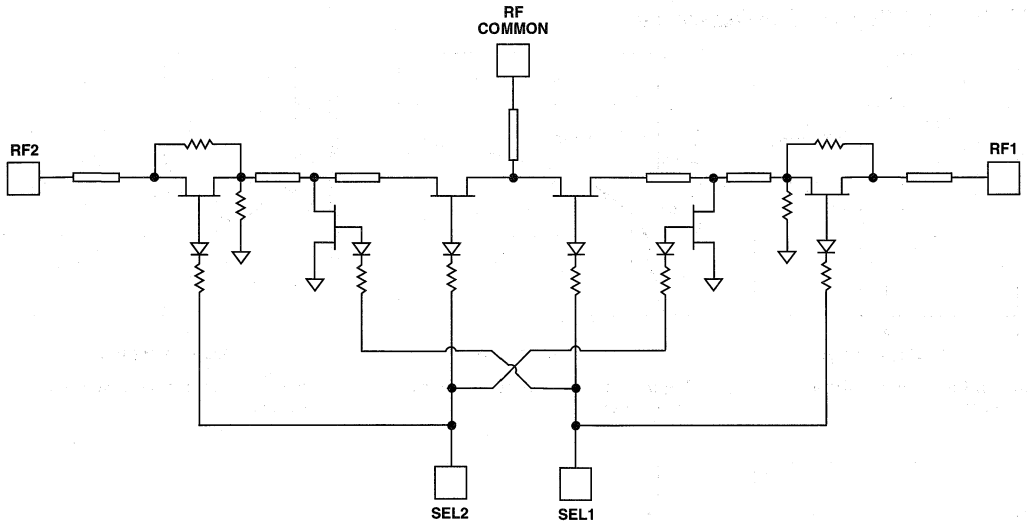


Figure 1. HMMC-2007 Schematic.

Recommended Operating Conditions, $T_A = 25°C$

Select Line		RF Path	
SEL1	**SEL2**	**RF IN to RF OUT2**	**RF IN to RF OUT1**
+10 V	-10 V	Isolated	Low Loss
-10 V	+10 V	Low Loss	Isolated

HMMC-2007 Typical Performance

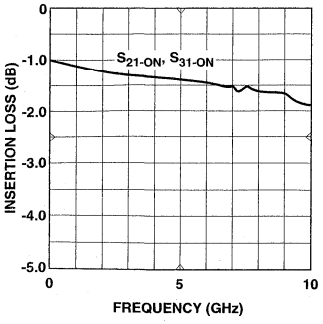


Figure 2. Insertion Loss[1] vs. Frequency.

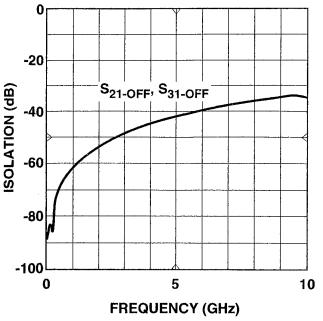


Figure 3. Input-to-Output Isolation[1] vs. Frequency.

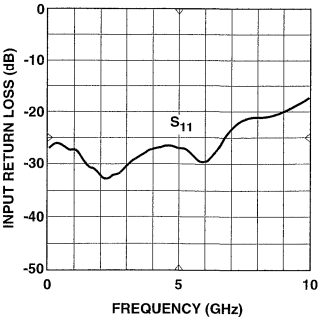


Figure 4. Input Return Loss[1] vs. Frequency.

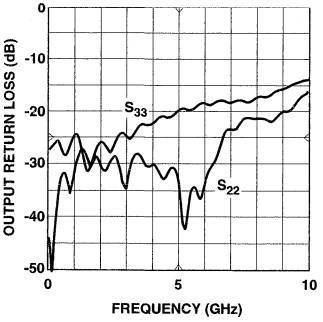


Figure 5. Output Return Loss[1] vs. Frequency.

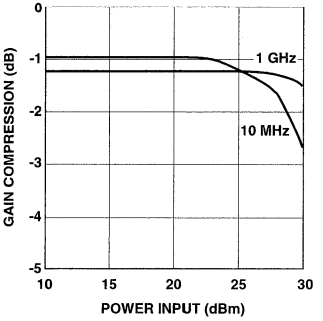


Figure 6. Gain Compression vs. Power Input.

Note:

1. Data taken with the device mounted in modular breadboard package.

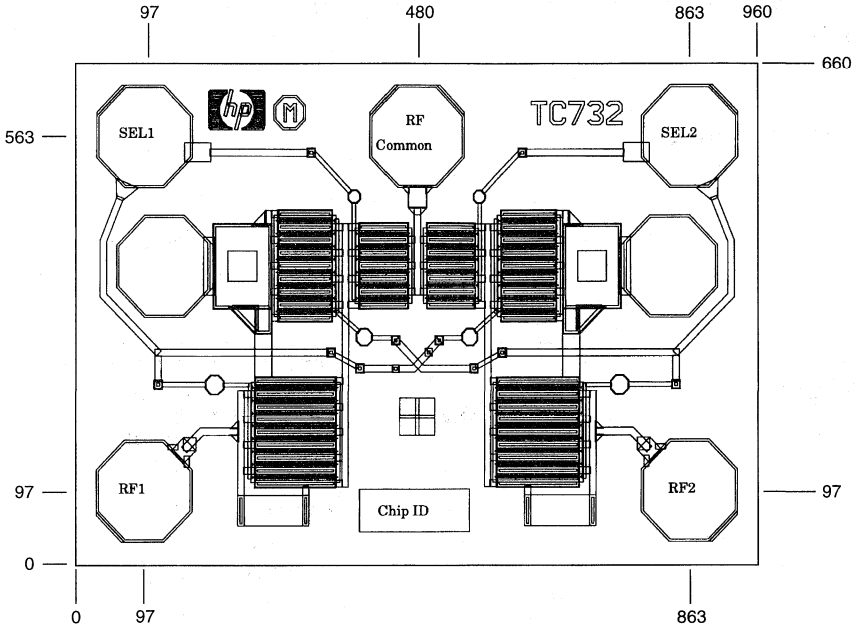


Figure 6. HMMC-2007 Bonding Pad Locations. (Dimensions in micrometers)

Note:
All compression data measured in an individual device mounted in an HP83040 Series Modular Microcircuit Package @ T_{case} = 25°C.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

HEWLETT® PACKARD

DC – 26.5 GHz SPDT GaAs MMIC Switch

Technical Data

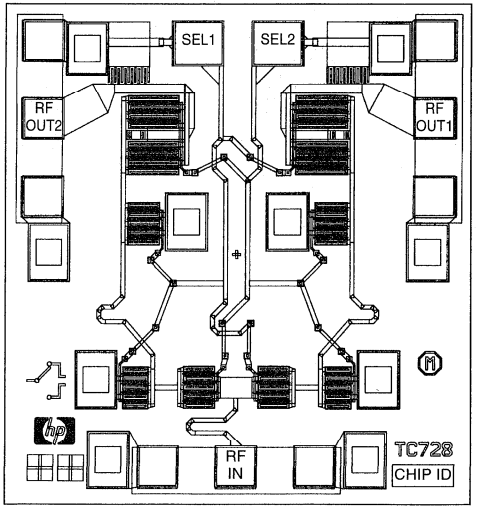
HMMC-2027

Features

- **Outputs Terminated in 50 Ω When Off**
- **Frequency Range:** DC-26.5 GHz
- **Insertion Loss:** 2.5dB @ 26.5 GHz
- **Isolation:** >70 dB @ 45 MHz
  30 dB @ 26.5 GHz
- **Return Loss:**
  15 dB (Both Input and Selected Output)
  12 dB Unselected Output
- **Switching Speed:** <1 ns (10%-90% RF)
- **P_{-1dB}:** 18 dBm @ 10 MHz
  27 dBm @ 2 GHz
- **Harmonics (DC Coupled):**
  <-45 dBc @ 10 MHz and 5 dBm
  <-65 dBc @ 2 GHz and 5 dBm

Description

The HMMC-2027 is a GaAs monolithic microwave integrated circuit (MMIC) designed for low insertion loss and high isolation from DC to 26.5 GHz. It is intended for use as a general-purpose, single-pole, double-throw (SPDT), absorptive switch. Two series and two shunt MESFETs per throw provide 3 dB maximum insertion loss and 30 dB minimum isolation at 26.5 GHz. HMMC-2027 chips use through-substrate vias to provide ground connections to the chip backside and minimize the number of wire bonds required.



Chip Size:	900 x 960 µm (35.4 x 37.8 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	80 x 80 µm (3.2 x 3.2 mils), or larger

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{sel}	Select Voltages 1 and 2	V	-10.5	+3
P_{in}	RF Input Power	dBm		25
T_{op}	Operating Temperature	°C	-55	+125
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp.	°C		+200
P_{unsel}[2]	Power into Unselected Output	dBm		15

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A = 25°C except for T_{op}, T_{STG}, and T_{max}.
2. Operation in excess of these @ $T_{op\text{-}max}$ may result in permanent damage.

DC Specifications/Physical Properties, T_A = 25°C

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_l	Leakage Current @ -10 V	µA			200
V_p	Pinch-Off Voltage (V_{SEL2} = V_p, V_{RFout2} = +2 V, I_{RFout2} = 2 mA, V_{SEL1} = -10 V, V_{RFout1} = open circuit, V_{RFin} = GND	V	-6.75		-3.00
BV_{gss}	Breakdown Voltage (Test FET w/V_D = V_S = GND, I_G = -50 µA)	V			-13.0

RF Specifications, T_A = 25°C, Z_O = 50 Ω, $V_{sel\text{-}high}$ = 0 V, $V_{sel\text{-}low}$ = -10 V

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
BW	Guaranteed Operating Bandwidth	GHz	DC		26.5
IL	Insertion Loss, RF_{in} to Selected RF_{out},f = 26.5 GHz, ON throw	dB		2.5	3.0
ISO	Isolation, RF_{in} to Unselected RF_{out},f = 26.5 GHz, OFF throw	dB	27	30	
ISO	Isolation, RF_{in} to Unselected RF_{out}, f = 18 GHz, OFF throw	dB	40	43	
RL_{in}	Input Return Loss	dB	12	15	
$RL_{out\text{-}ON}$	Output Return Loss, ON throw	dB	13	16	
$RL_{out\text{-}OFF}$	Output Return Loss, OFF throw	dB	9	12	
$P_{1\ dB}$	Input Power where IL increases by 1 dB f_{in} = 2 GHz	dBm		27	
t_s	Switching Speed, 10%–90% RF Envelope f_{in} = 2 GHz	ns		1	

Applications

The HMMC-2027 can be used in instrumentation, communications, radar, ECM, EW, and many other systems requiring SPDT switching. It can be used for pulse modulation, port isolation, transfer switching, high-speed switching, replacement of mechanical switches, and so on.

Assembly Techniques

Die attach should be done with conductive epoxy. Gold thermosonic bonding is recommended for all bonds. The top and bottom metallization is gold. For more detailed information see HP application note #999, "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

S-Parameters[1], $T_A = 25°C$, $Z_O = 50\ \Omega$, V_{sel} high = 0 V, V_{sel} low = -10 V

Freq. GHz	S_{11}			S_{21} (Insertion Loss)			S_{31} (Isolation)	S_{22} (ON Throw)			S_{33} (OFF Throw)		
	dB	Mag.	Ang.	dB	Mag.	Ang.	dB	dB	Mag.	Ang.	dB	Mag.	Ang.
0.5	-26.41	0.048	-57.11	-1.08	0.88	-49.06	-67.74	-28.40	0.03	-47.94	-32.26	0.024	47.18
0.5	-18.28	0.12	-7.04	-1.33	0.86	-8.52	-71.40	-18.44	0.12	-9.89	-16.79	0.14	173.87
1.5	-18.53	0.12	-13.70	-1.35	0.86	-14.62	-61.02	-18.46	0.12	-19.75	-16.47	0.15	171.75
4.0	-18.92	0.11	-27.64	-1.41	0.85	-24.53	-51.67	-18.75	0.12	-38.78	-15.36	0.17	168.03
6.5	-19.43	0.11	-45.02	-1.47	0.84	-39.56	-49.50	-19.10	0.11	-63.22	-14.55	0.19	152.55
9.0	-20.57	0.09	-64.07	-1.56	0.84	-55.13	-46.87	-19.72	0.10	15.79	-14.28	0.19	136.68
11.5	-21.85	0.08	-2.59	-1.62	0.83	-71.03	-44.71	-20.91	0.09	243.63	-13.84	0.20	121.81
14.0	-23.10	0.07	258.44	-1.74	0.82	-29.63	-42.30	-22.41	0.08	217.48	-13.53	0.21	106.44
16.5	-24.05	0.06	235.82	-1.88	0.81	258.60	-41.74	-24.17	0.06	179.74	-12.95	0.23	92.94
19.0	-24.59	0.06	224.56	-1.99	0.80	242.13	-37.07	-27.09	0.04	133.20	-12.76	0.23	74.01
21.5	-25.42	0.05	206.39	-2.10	0.79	227.84	-40.39	-28.85	0.04	68.10	-13.12	0.22	68.84
24.0	-24.66	0.06	209.77	-2.10	0.78	209.72	-34.46	-24.31	0.06	6.26	-12.11	0.25	54.32
26.5	-21.90	0.08	223.86	-2.39	0.76	191.82	-31.38	-19.43	0.11	-33.31	-12.03	0.25	38.26

Note:

1. Three-port-wafer-probed data: Port 1 = RF Input, Port 2 = Selected RF Output (i.e., ON throw), and Port 3 = Unselected RF Output (i.e., OFF throw).

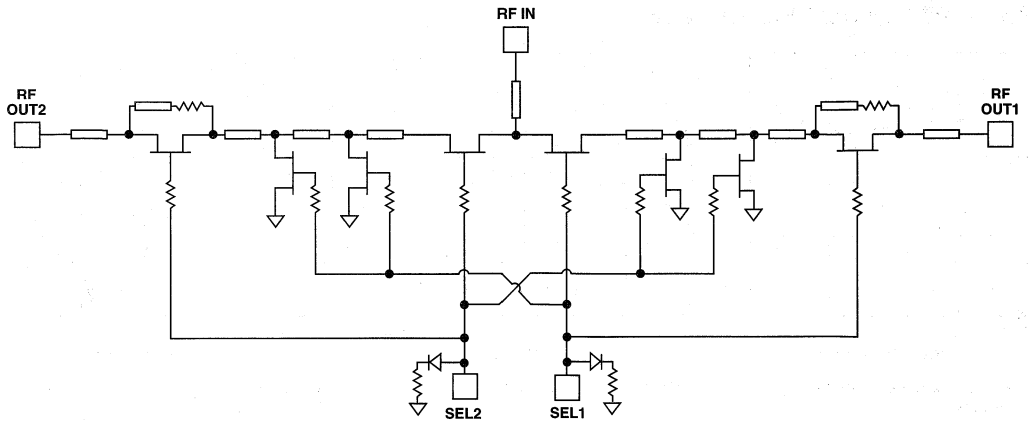


Figure 1. HMMC-2027 Schematic.

Recommended Operating Conditions, $T_A = 25°C$

Select Line		RF Path	
SEL1	**SEL2**	**RF IN to RF OUT1**	**RF IN to RF OUT2**
-10 V	0 V	Isolated	Low Loss
0 V	-10 V	Low Loss	Isolated

HMMC-2027 Typical Performance

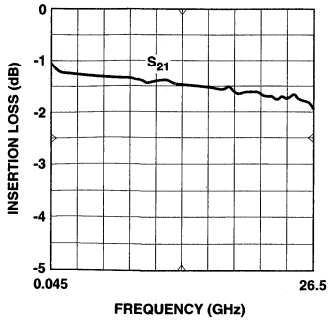


Figure 2. Insertion Loss[1] vs. Frequency.

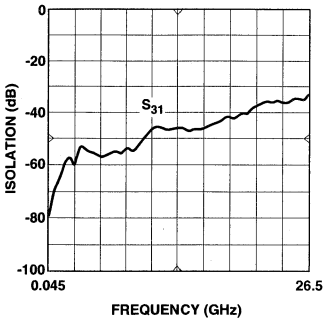


Figure 3. Input-to-Output Isolation[1] vs. Frequency.

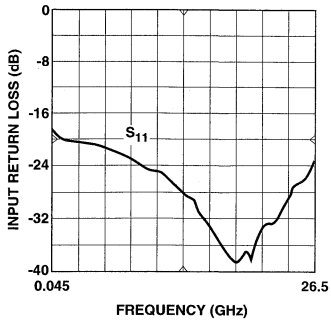


Figure 4. Input Return Loss[1] vs. Frequency.

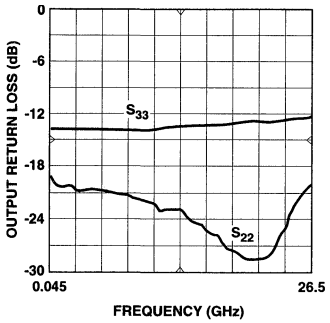


Figure 5. Output Return Loss[1] vs. Frequency.

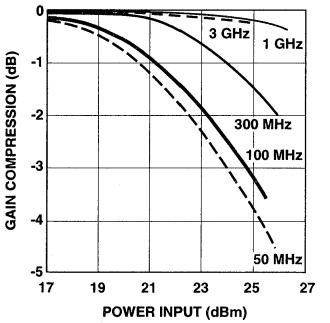


Figure 6. Gain Compression[2] vs. Power Input.

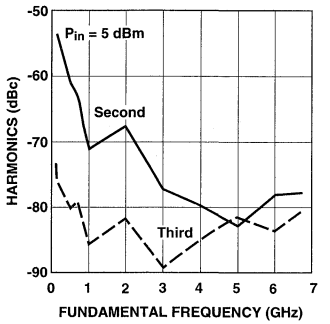


Figure 7. Harmonics vs. Fundamental Frequency[2,3].

Notes:

1. Data obtained from wafer-probed measurements.
2. All compression and harmonic data measured on individual device mounted in an HP83040 Series Modular Microcircuit Package @ T_{case} = 25°C.
3. Harmonic data points below -80 dBc are at or near the noise floor of the measurement system.

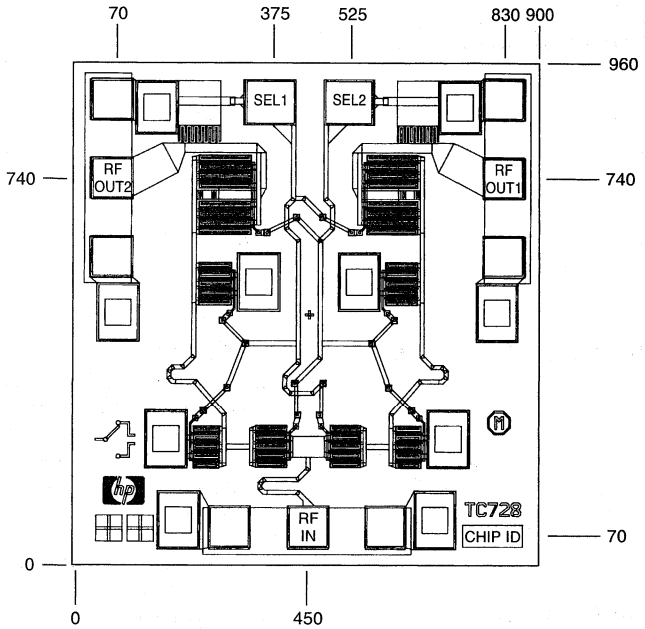


Figure 8. HMMC-2027 Bonding Pad Locations. (Dimensions in micrometers)

Note:
All compression data measured in an individual device mounted in an HP83040 Series Modular Microcircuit Package @ T_{case} = 25°C.

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

HEWLETT® PACKARD

Silicon Bipolar RFIC 900 MHz Vector Modulator

Technical Data

HPMX-2003

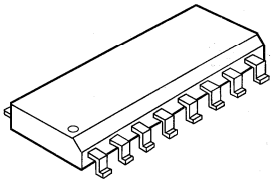
Features

- **800–1000 MHz Output Frequency Range**
- **+6 dBm Peak P_{out}**
- **Unbalanced 50 Ω Output**
- **Internal 90° Phase Shifter**
- **5 Volt, 36 mA Bias**
- **SO-16 Surface Mount Package**

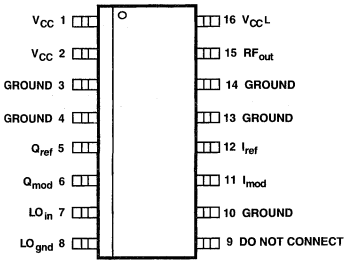
Applications

- **Direct Modulator for 900 MHz Cellular Telephone Handsets, Including GSM, JDC, and NADC**
- **Direct Modulator for 900 MHz ISM Band Spread-Spectrum Transmitters and LANs**

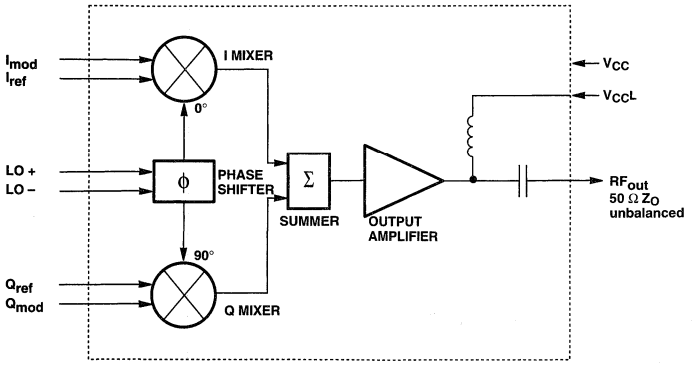
Plastic SO-16 Package



Pin Configuration



Functional Block Diagram



Description

Hewlett Packard's HPMX-2003 is a Silicon RFIC direct conversion vector modulator designed for use at output frequencies between 800 MHz and 1 GHz. Housed in a SO-16 surface mount plastic package, the IC contains two matched Gilbert cell mixers, an RC phase shifter, a summer, and an output amplifier complete with 50 Ω impedance match and DC block.

This device is suitable for use in direct and offset-loop modulated portable and mobile telephone handsets for cellular systems such as GSM, North American Digital Cellular and Japan Digital Cellular. It can also be used in digital transmitters operating in the 900 MHz ISM (Industrial-Scientific-Medical) band, including use in Local Area Networks (LANs).

The HPMX-2003 is fabricated with Hewlett-Packard's 25 GHz ISOSAT-II process, which combines stepper lithography, ion-implantation, self-alignment techniques, and gold metallization to produce RFICs with superior performance, uniformity and reliability.

HPMX-2003 Absolute Maximum Ratings, T_A = 25°C

Symbol	Parameter	Units	Absolute Maximum[1]
P_{diss}	Power Dissipation[2,3]	mW	500
LO_{in}	LO Input Power	dBm	15
V_{CC}	Supply Voltage	V	10
ΔV_{Imod}, ΔV_{Qmod}	Swing of V_{Imod} about V_{Iref}[4] or V_{Qmod} about V_{Qref}	V_{p-p}	5[4]
V_{Iref}, V_{Qref}	Reference Input Levels[4]	V	5[4]
T_{STG}	Storage Temperature	°C	-65 to +150
T_j	Junction Temperature	°C	150

Thermal Resistance[2]:
θ_{jc} = 125°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_C = 25°C (T_C is defined to be the temperature at the end of pin 3 where it contacts the circuit board).
3. Derate at 8 mW/°C for T_C > 88°C.
4. Do not exceed V_{CC} by more than 0.8 V.

HPMX-2003 Guaranteed Electrical Specifications, T_A = 25°C, Z_O = 50 Ω

V_{CC} = 5 V, LO= -12 dBm at 900 MHz (Unbalanced Input), V_{Iref} = V_{Qref} = 2.5 V (Unless Otherwise Noted).

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_d	Device Current	mA		36	44
P_{out}	Output Power V_{Imod} = V_{Qmod} = 3.75 V	dBm	+4.0	+6	
LO_{leak}	P_{out} - LO at Output V_{Imod} = V_{Qmod} = 2.5 V	dBc	+30	+37	
ε_{mod}	Average Modulation Error $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 1.25 V	%		4	7

HPMX-2003 Summary Characterization Information, T_A = 25°C, Z_O = 50 Ω

V_{CC} = 5 V, LO = -12 dBm at 900 MHz (Unbalanced Input), V_{Iref} = V_{Qref} = 2.5 V (Unless Otherwise Noted).

Symbol	Parameters and Test Conditions	Units	Typ.
R_{in}	Input Resistance (I_{mod} to I_{ref} or Q_{mod} to Q_{ref})	Ω	10 k
R_{in-gnd}	Input Resistance to Ground (Any I, Q Pin to Ground)	Ω	10 k
$VSWR_{LO}$	LO VSWR (50 Ω) GSM: 890-915 MHz Bandwidth NADC: 824-850 MHz Bandwidth JDC: 940-960 MHz Bandwidth		1.5:1 1.5:1 1.5:1
$VSWR_O$	Output VSWR (50 Ω) (Tuned by Placement of V_{ccL} Capacitor – See Figures 22, 32, and 42) GSM: 890-915 MHz Bandwidth NADC: 824-850 MHz Bandwidth JDC: 940-960 MHz Bandwidth		1.2:1 1.1:1 1.2:1
	Output Noise Floor V_{Imod} = V_{Qmod} = 3.75 V	dBm/Hz	-134
IM_3	DSB Third Order Intermodulation Products	dBc	+34
A_i	RMS Amplitude Error	dB	0.3
P_i	RMS Phase Error	degrees	2

HPMX-2003 Pin Description

V_{CC} (pins 1,2)

These two pins provide DC power to the mixers in the RFIC, and are connected together internal to the package. They should be connected to a 5 V supply, with appropriate AC bypassing (1000 pF typ.) used near the pins, as shown in figures 1 and 2. **The voltage on these pins should always be kept *at least 0.8 V more positive* than the DC level on any of pins 5, 6, 11, or 12.** Failure to do so may result in the modulator drawing sufficient current through the data or reference inputs to damage the IC.

Ground (pins 3, 4, 10, 13 & 14)

These pins should connect with minimal inductance to a solid ground plane (usually the backside of the PC board). Recommended assembly employs multiple plated through via holes where these leads contact the PC board.

I_{ref} (pin 12) and Q_{ref} (pin 5), I (pin 11) and Q (pin 6) Inputs

The I and Q inputs are designed for unbalanced operation but can be driven differentially with similar performance. The recommended level of unbalanced I and Q signals is 2.5 V_{p-p} with an average level of 2.5 V above ground. The reference pins should be DC biased to this average data signal level (V_{CC}/2 or 2.5 V typ.). For single ended drive, pins 5 and 12 can be tied together. For balanced operation, 2.5 V_{p-p} signals may be applied across the I_{mod}/I_{ref} and the Q_{mod}/Q_{ref} pairs. The average level of all four signals should be about 2.5 V above ground. The impedance between any I or Q and ground is typically 10 K Ω and the impedance between I_{mod} and I_{ref} or Q_{mod} and Q_{ref} is typically 10 KΩ. The input bandwidth typically cxcccds 40 MHz. It is possiblc to reduce LO leakage through the IC by applying slight DC imbalances between I_{mod} and I_{ref} and/or Q_{mod} and Q_{ref} (see section entitled "HPMX-2003 Using Offsets to Improve Lo Leakage"). All performance data shown on this data sheet was taken with unbalanced I/Q inputs.

LO Input (pins 7 and 8)

The LO input of the HPMX-2003 is balanced and matched to 50 For drive from an unbalanced LO, pin 7 should be AC coupled to the LO using a 50 Ω transmission line and a blocking capacitor (1000 pF typ.), and pin 8 should be AC grounded (1000 pF capacitor typ.), as shown in figure 1. For drive from a balanced LO source, 50 Ω transmission lines and blocking capacitors (1000 pF typ.) are used on both pins 7 and 8, as shown in figure 2. The internal phase shifter allows operation from 800 - 1000 MHz. The recommended LO input level is -12 dBm. All performance data shown on this data sheet was taken with unbalanced LO operation.

RF Output (pin15)

The RF output of the HPMX-2003 is configured for unbalanced operation. The output is internally DC blocked and matched to 50 Ω, so a simple 50 Ω microstrip line is all that is required to connect the modulator to other circuits.

V_{CCL} (pin 16)

Pin 16 is the V_{CC} input for the output stage of the IC. It is **not** internally connected to the other V_{CC} pins. The external connection allows the addition of a small inductor (0 - 6 nH) to tune the output for minimum VSWR, depending upon the operating frequency.

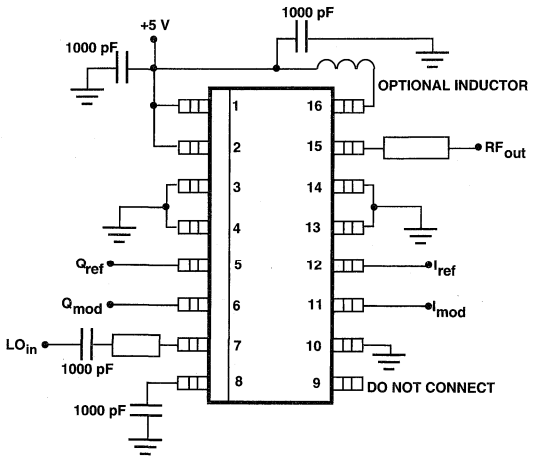


Figure 1. HPMX-2003 Connections Showing Unbalanced LO and I, Q Inputs.

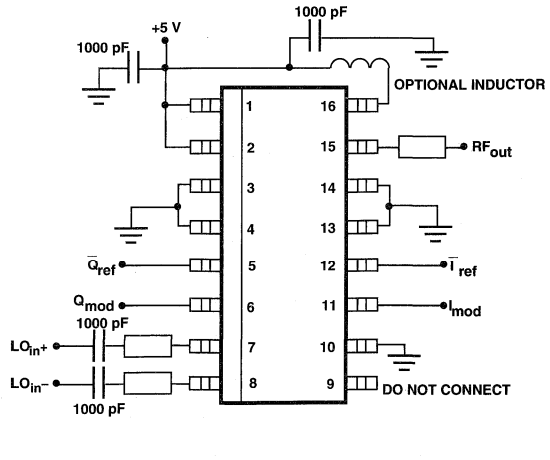


Figure 2. HPMX-2003 Connections Showing Balanced LO and I, Q Inputs.

HPMX-2003 Typical Data Measurement

Direct measurement of the amplitude and phase error at the output is an accurate way to evaluate modulator performance. By measuring the error directly, all the harmonics, LO leakage, etc. that show up in the output signal are accounted for. Figure 3, below, shows the test setup that was used to create the amplitude and phase error plots (figures 12 and 13).

Amplitude and phase error are measured by using the four channel power supply to simulate I and Q input signals. Real 2.5 V_{p-p} I and Q signals would swing 1.25 volts above and below an average 2.5 V level, therefore, a "high" level input is simulated by applying 3.75 V, and a "low" level by applying 1.25 V to the I and/or Q inputs.

Amplitude and phase are measured by setting the network analyzer for an S_{21} measurement at frequency of choice. Set the port 1 stimulus level to the LO level you intend to use in your circuit (-12 dBm for the data sheet). A 6-10 dB attenuator can be placed in the line to port 2 to prevent network analyzer overload, depending upon the network analyzer you are using.

By adjusting the V_{Imod} and V_{Qmod} settings you can step around the I, Q vector circle, reading magnitude and phase at each point. The relative values of phase and amplitude at the various points will indicate the accuracy of the modulator. Note: you must use very low ripple power supplies for the reference, V_{Imod}, and V_{Qmod} supplies. Ripple or noise of only a few millivolts will appear as wobbling phase readings on the network analyzer.

The same test setup shown below is used to measure input and output VSWR, reverse isolation, and power vs. frequency. V_{Imod} and V_{Qmod} are set to 3.75 V and the appropriate frequency ranges are swept. S_{11} provides input VSWR data, S_{22} provides output VSWR data. S_{21} provides power output (add source power to S_{21} derived gain).

LO leakage data shown in figures 18, and 19 is generated by setting $V_{Imod} = V_{Qmod} = V_{Iref} = V_{Qref} = 2.5$ V then performing an S_{21} sweep. Since phase is not important for these measurements, a scalar network analyzer or a signal generator and spectrum analyzer could be used.

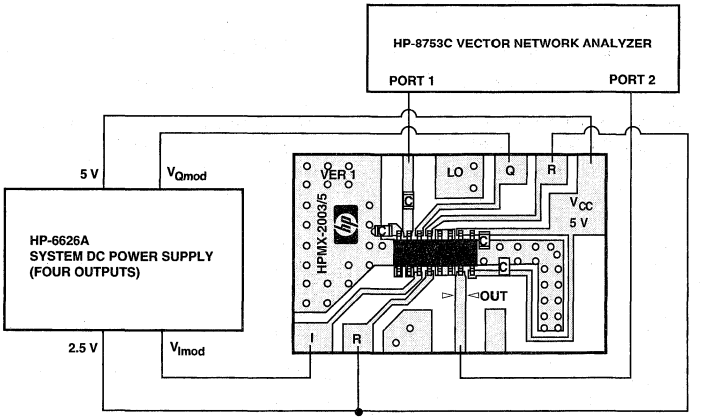


Figure 3. Test Setup for Measuring Amplitude and Phase Error, Input and Output VSWR, Power Output and LO Leakage of the Modulator.

HPMX-2003 Typical Performance

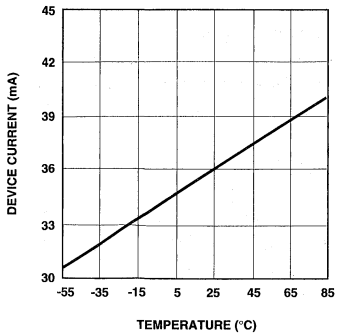


Figure 4. HPMX-2003 Device Current vs. Temperature, V_{CC} = 5 V.

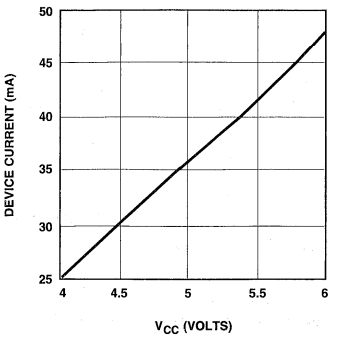


Figure 5. HPMX-2003 Device Current vs. V_{CC}, T_A = 25°C.

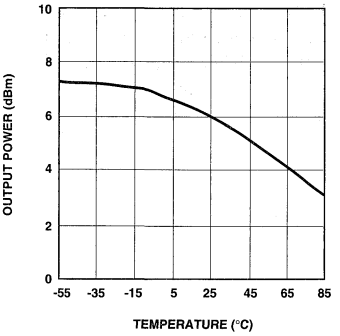


Figure 6. HPMX-2003 Power Output vs. Temperature at 900 MHz, LO = -12 dBm, V_{Imod} = V_{Qmod} = 3.75 V, V_{Iref} = V_{Qref} = 2.5 V, V_{CC} = 5 V.

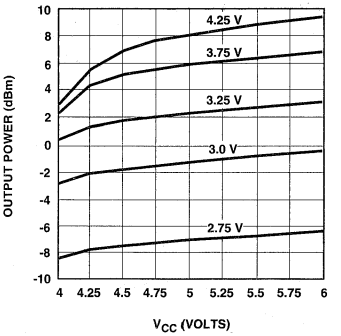


Figure 7. HPMX-2003 Power Output vs. V_{CC} and I, Q Level at 900 MHz, LO = -12 dBm, V_{Imod} = V_{Qmod}, T_A = 25°C.

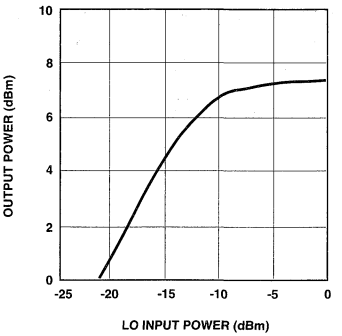


Figure 8. HPMX-2003 Power Output vs. LO Level at 900 MHz, V_{CC} = 5 V, V_{Imod} = V_{Qmod} = 3.75 V, T_A = 25°C.

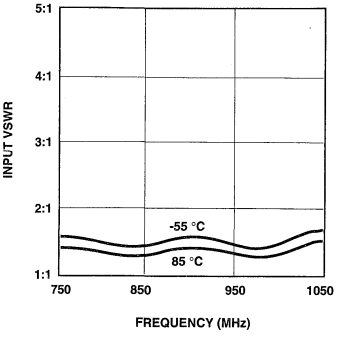


Figure 9. HPMX-2003 LO Input VSWR vs. Frequency and Temperature, V_{CC} = 5 V.

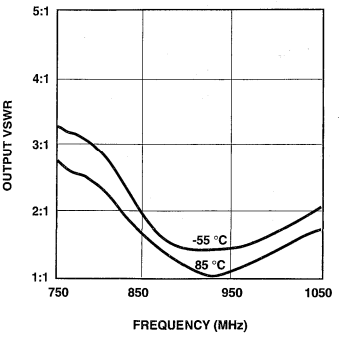


Figure 10. HPMX-2003 Output VSWR vs. Frequency and Temperature.

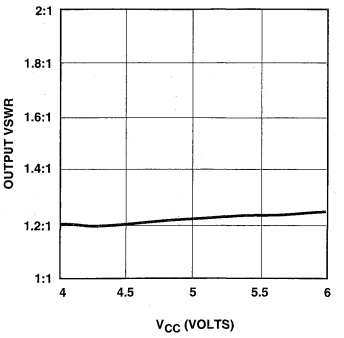


Figure 11. HPMX-2003 Output VSWR vs. V_{CC} at 900 MHz, T_A = 25°C.

HPMX-2003 Modulation Accuracy (Sample Part)

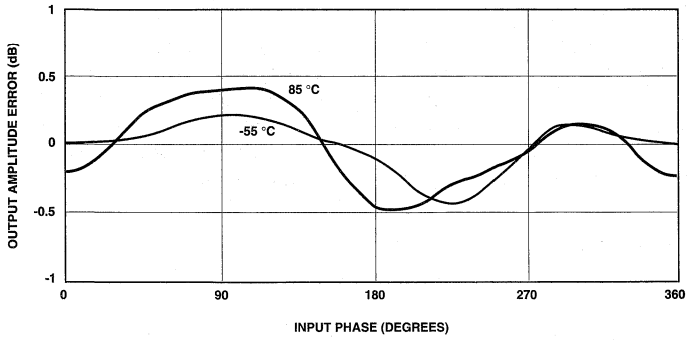


Figure 12. HPMX-2003 Amplitude Error vs. Input Phase at 900 MHz, V_{CC} = 5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 1.25 V, LO = -12 dBm. 25°C Curve Deleted for Clarity.

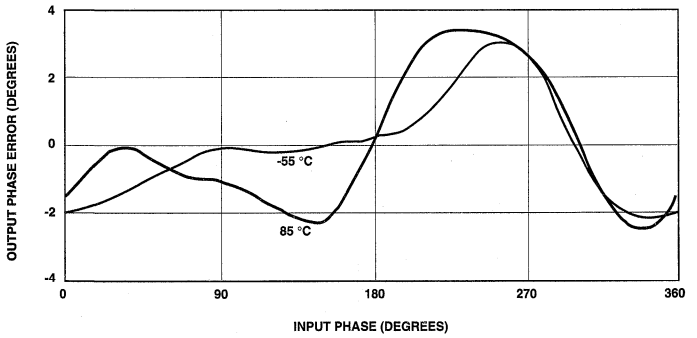


Figure 13. HPMX-2003 Output Phase Error vs. Input Phase at 900 MHz, V_{CC} = 5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 1.25 V, LO = -12 dBm. 25°C Curve Deleted for Clarity.

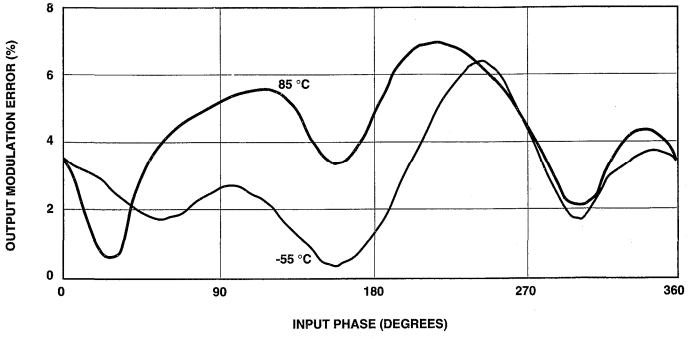


Figure 14. Modulation Error vs. Input Phase at 900 MHz, V_{CC} = 5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 1.25 V, LO = -12 dBm. Percent Modulation Error is Calculated from the Values of Amplitude and Phase Error.

HPMX-2003 Single and Double Sideband Performance

Single sideband (SSB) and double sideband (DSB) tests are sometimes used to evaluate modulator performance. Figure 17, below, shows the test equipment setup that was used to create the SSB and DSB output spectrum graphs (figures 15 and 16).

The phase shift provided by the I and Q signal generators must be very close to 90 degrees and the amplitude of the two signals must be matched within a few millivolts or results will not accurately reflect the performance of the modulator IC.

The I, Q signal generator must put out low distortion signals or the output spectrum will show high harmonic levels that reflect the performance of the signal generator, not the modulator.

HPMX-2003 Typical Sideband Performance Data

SSB: $V_{Iref} = V_{Qref} = 2.5$ V, $V_{Imod} = V_{Iref} + 1.25 \sin(2\pi f t)$, $V_{Qmod} = V_{Qref} + 1.25 \cos(2\pi f t)$, f = 25 kHz
DSB: $V_{Iref} = V_{Qref} = 2.5$ V, $V_{Imod} = V_{Iref} + 1.25 \cos(2\pi f t)$, $V_{Qmod} = V_{Qref} + 1.25 \cos(2\pi f t)$, f = 25 kHz

Symbol	Parameters and Test Conditions	Units	SSB	DSB
P_{LSB}	Lower Sideband Power Output	dBm	+3	0
LO_{leak}	LO Suppression	dBc	34	31
P_{USB}	Upper Sideband Power Output	dBm	-32	0
IM_3	Third Order Intermodulation Products	dBm	NA	-34

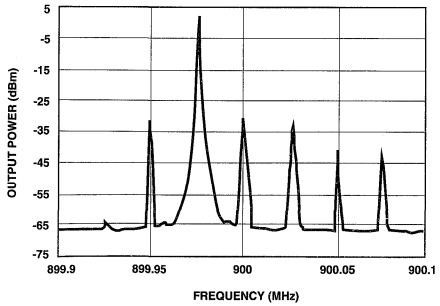


Figure 15. Single Sideband Output Spectrum. LO = -12 dBm at 900 MHz. The Test Setup is Shown in Figure 17.

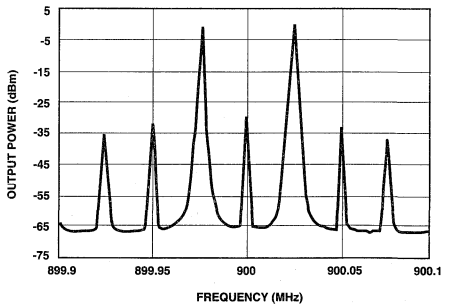


Figure 16. Double Sideband Output Spectrum. LO = -12 dBm at 900 MHz. The Test Setup is Shown in Figure 17.

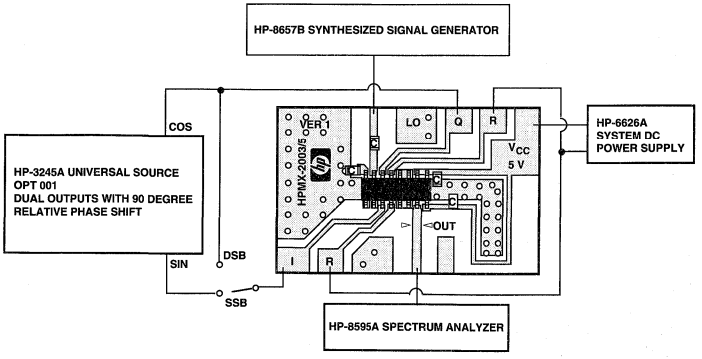


Figure 17. HPMX-2003 Single/Double Sideband Test Setup.

HPMX-2003 Using Offsets to Improve LO Leakage

It is possible to improve on the excellent performance of the HPMX-2003 for applications that are particularly sensitive to LO leakage. The nature of the improvement is best understood by examining figures 18 and 19, below.

LO leakage results when normal variations in the wafer fabrication process cause small shifts in the values of the modulator IC's internal components. These random variations create an effect equivalent to slight DC imbalances at the input of each (I and Q) mixer. The DC imbalances at the mixer inputs are multiplied by ±1 at the LO frequency and show up at the output of the IC as LO leakage.

It is possible to externally apply small DC signals to the I and Q inputs and exactly cancel the internally generated DC offsets. This will result in sharply decreased LO leakage at precisely the frequency and temperature where the offsets were applied (see figure 18).

This improvement is not very useful if it doesn't hold up over frequency and temperature changes. The lower curve in figure 18 shows how the offset-adjusted LO leakage varies versus frequency. Note that it remains below -45 dBm over most of the frequency range shown. In the 20 MHz range centered at 900 MHz, the level is closer to -55 dBm.

Figure 19 shows the performance of the offset adjusted LO leakage over temperature. Note that the adjusted curve is at a level below -50 dBm over most of the temperature range.

The net result of using externally applied offsets with the HPMX-2003 is that an LO leakage level below -40 dBm can typically be achieved over both frequency and temperature.

The magnitude of the required external offset varies randomly from part to part and between the I and Q mixers on any given IC. Offsets can range from -56 mV to +56 mV. External offsets may be applied either by varying the average level of the I and Q modulating signals, or by varying the voltages at the I_{ref} and Q_{ref} pins of the modulator.

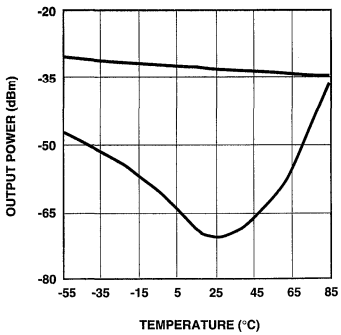


Figure 18. LO Leakage vs. Frequency Without DC Offsets (Upper Curve) and LO Leakage vs. Frequency With DC Offsets (Adjusted for Minimum LO Leakage at 900 MHz). T_A = 25°C, V_{CC} = 5 V, V_{Iref} = V_{Qref} = 2.5 V, LO = -12 dBm.

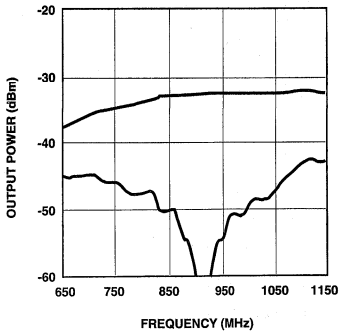


Figure 19. LO Leakage With No DC Offsets vs. Temperature (Upper Curve) and LO Leakage With DC Offsets (Adjusted for Minimum Leakage at 25°C) vs. Temperature (Lower Curve). Frequency = 900 MHz, V_{CC} = 5 V, V_{Iref} = V_{Qref} = 2.5 V, LO = -12 dBm.

HPMX-2003 Modulation Spectrum Diagrams

Figure 20, below, shows the test setup that was used to generate the modulation spectrum diagrams that appear on the GSM, JDC and NADC applications pages of this data sheet. The major differences between the tests are summarized in the table below.

The modulation spectra are created by setting the function generator to the appropriate bit-clock frequency. The pattern generator is set to produce a pseudorandom serial bit stream (n = 20) that is NRZ coded. The pseudorandom bit stream which simulates the serial data in a digital phone is fed to the base-band processor that splits it into a two bit parallel stream (I and Q) and then filters each according to the requirements of the digital telephone system being simulated. The I and Q signals from the baseband filter are then DC offset by 2.5 V using the op-amp circuit. The output of the modulator is monitored using a spectrum analyzer.

System	Bit Clock Frequency	Baseband Filter	Channel (LO) Frequency
GSM	270 kHz	0.3 GMSK (HP 8657B)	900 MHz
JDC	42 kHz	α = 0.5 π/4 DQPSK (HP 8657D)	950 MHz
NADC	48.6 kHz	α = 0.35 π/4 DQPSK (HP 8657D)	835 MHz

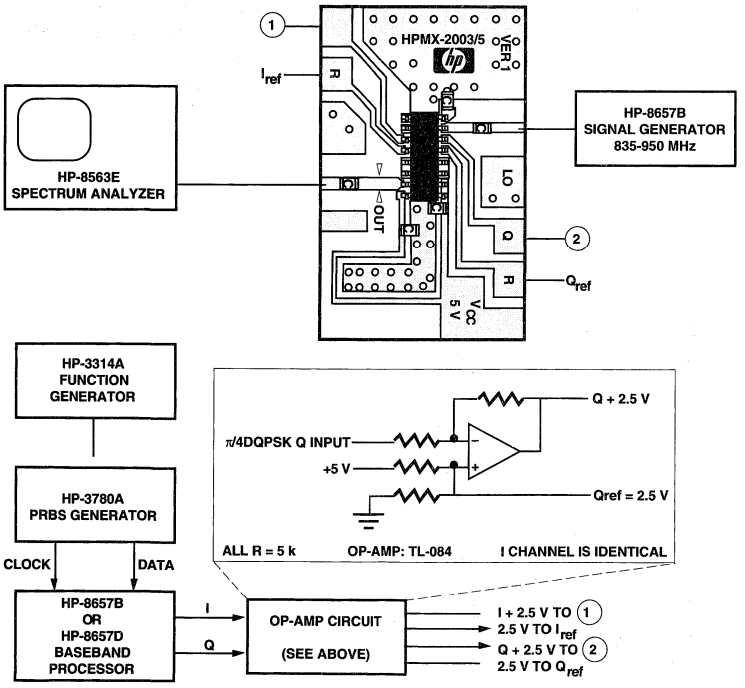


Figure 20. Test Equipment Setup for Modulation Spectrum Diagrams.

HPMX-2003 GSM Applications

The GSM System

GSM (Group Speciale Mobile) commonly refers to the European digital cellular telephone system standard. Digital cellular phones for the European market must conform to this standard. The GSM system is characterized by 200 kHz channel spacing and mobile to base transmit frequencies of 890 - 915 MHz. The primary modulation characteristics include 0.3 GMSK filtering of the I and Q signals and 270 kbps transmission rate.

Critical Performance Parameters

GSM standards require that the telephone exhibit RMS phase error ≤5° and peak phase error <20°. The modulated output spectrum of the phone must lie within a "spectral mask" which defines maximum allowable radiation levels into adjacent and alternate channels. Specifically, 200 kHz from the channel center frequency (f_0), the output of the phone must be at least 30 dB below the peak output at f_0. 400 kHz from f_0 the output must be 50-60 dB below the peak output at f_0 depending upon the class of radio. Refer to the GSM900 specifi-cations for more detailed information.

HPMX-2003 Performance

Typical RMS phase error level of 2° and typical peak levels of 8° makes the HPMX-2003 an excellent choice for GSM applications. The output spectrum falls easily within the GSM spectral mask, and the high power and simple output configuration mean lower components count, reduced size and higher system efficiency.

Particulars of Use

Many of the GSM application performance graphs shown in this data sheet were created using the test board shown in figure 21, below.

The only external components required by this IC are four chip capacitors. One capacitor is used as a DC block on the input transmission line. The second capacitor (at pin 8) provides an AC ground to one side of the differential LO input. The third and fourth capacitors (at pins 1 and 16) are for V_{CC} bypass.

The circuit board includes an inductive trace that can optionally be used to minimize output VSWR by placing a bypass capacitor at various points along the inductive line. Minimum VSWR for GSM applications is achieved by placing the capacitor as shown in the circle (inductance ≈2 nH).

The IC has an internal blocking capacitor so the output is a simple 50 Ω transmission line. An enlarged scale layout of the test board can be found on the last page of this data sheet.

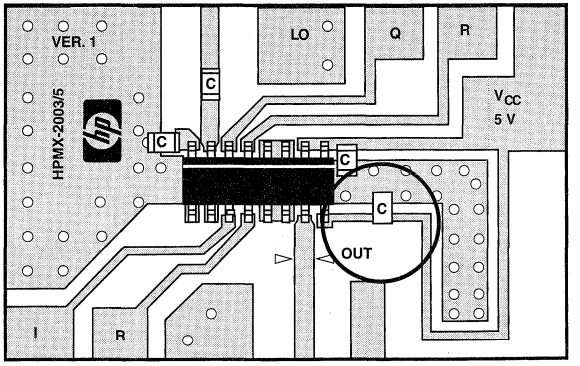


Figure 21. HPMX-2003 GSM Test Board.

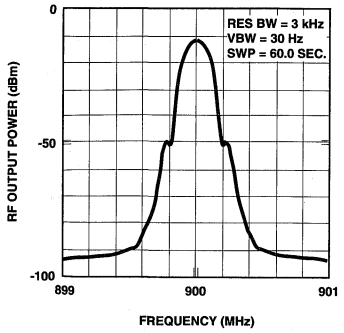


Figure 22. HPMX-2003 GSM Modulation Spectrum at -40°C.

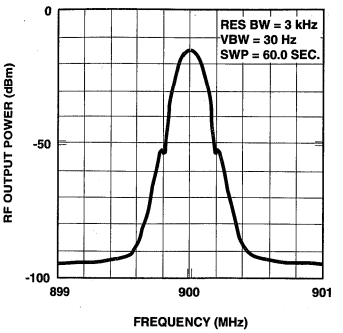


Figure 23. HPMX-2003 GSM Modulation Spectrum at 25°C.

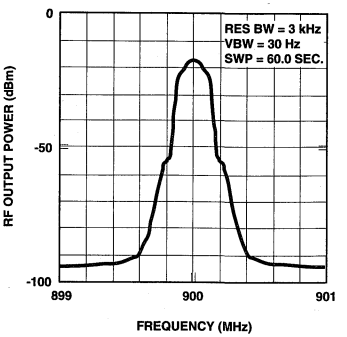


Figure 24. HPMX-2003 GSM Modulation Spectrum at 85°C.

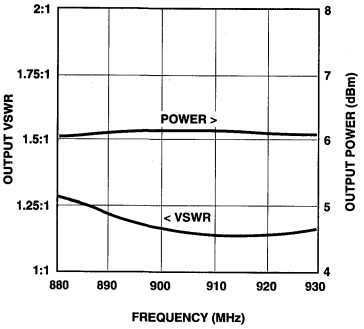


Figure 25. HPMX-2003 Output VSWR and Power vs. Frequency, V_{CC} = 5 V, LO = -12 dBm, V_{Imod} = V_{Qmod} = 3.75 V, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

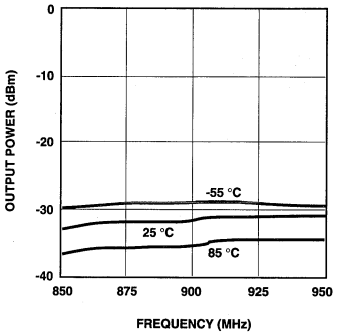


Figure 26. HPMX-2003 LO Leakage vs. Frequency and Temperature (Without Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, V_{Imod} = V_{Qmod} = V_{Iref} = V_{Qref} = 2.5 V.

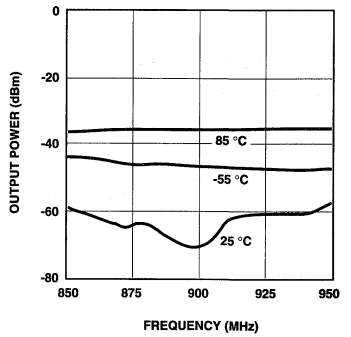


Figure 27. LO leakage vs. Frequency and Temperature (With 25°C Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V.

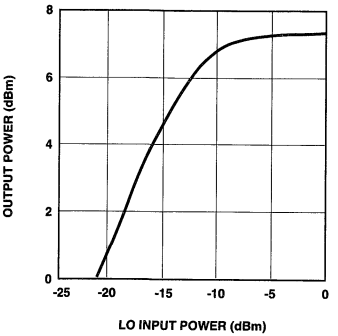


Figure 28. HPMX-2003 Power Output vs. LO Input Power at 900 MHz, V_{CC} = 5 V, V_{Imod} = V_{Qmod} = 3.75 V, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

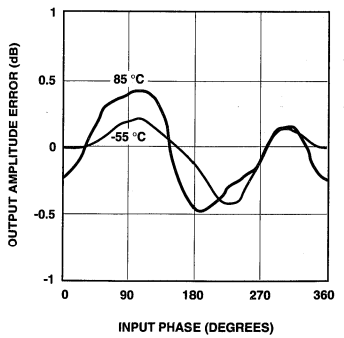


Figure 29. HPMX-2003 Vector Amplitude Error vs. Input Phase and Temperature at 900 MHz, V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V.

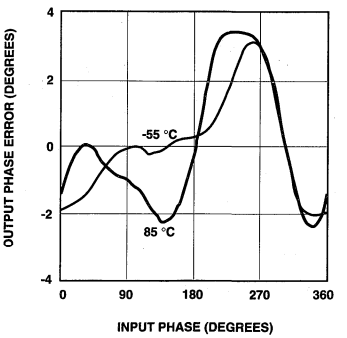


Figure 30. HPMX-2003 Vector Phase Error vs. Input Phase and Temperature at 900 MHz, V_{CC} = 5 V, LO = -12 dBm, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V.

Note: Modulation spectrum test conditions as follows: V_{CC} = 5 V, LO = -12 dBm at 900 MHz, V_{Imod} = V_{Qmod} = 2.5 V_{p-p}, unbalanced, average level = 2.5 V, V_{Iref} = V_{Qref} = 2.5 V, bit clock rate: 270 kHz, baseband filter: α = 0.3 GMSK.

HPMX-2003 NADC Applications

The NADC System

NADC (North American Digital Cellular) commonly refers to the digital sections of the IS-55 cellular telephone system standard. Dual mode (FM/TDMA) cellular phones for the North American market must conform to this standard. The NADC system is characterized by 30 kHz channel spacing and mobile to base transmit frequencies of 824 - 849 MHz. The primary modulation characteristics include $\pi/4$ DQPSK filtering of the I and Q signals and 48.6 kbps transmission rate.

Critical Performance Parameters

System specifications require that the telephone exhibit RMS modulation error under 12% in the digital mode. The modulated output spectrum of the phone must lie within a "spectral mask" which defines maximum allowable radiation levels into adjacent and alternate channels. Specifically, total power radiated into the either adjacent channel must be at least 26 dB below the mean output power. Total power radiated into either alternate channel must be at least 45 dB below the mean output power. Refer to the IS-55 specifications for more detailed information.

HPMX-2003 Performance

The typical RMS modulation error level of 4% makes the HPMX-2003 an excellent choice for NADC applications. The output falls easily within the NADC spectral requirements, and the high power and simple output configuration mean lower components count, reduced size and higher system efficiency.

Particulars of Use

Many of the NADC application performance graphs shown in this data sheet were created using the test board shown in figure 31, below.

The only external components required by this IC are four chip capacitors. One capacitor is used as a DC block on the input transmission line. The second capacitor (at pin 8) provides an AC ground to one side of the differential LO input. The third and fourth capacitors (at pins 1 and 16) are for V_{CC} bypass.

The circuit board includes an inductive trace that can optionally be used to minimize output VSWR by placing a bypass capacitor at various points along the inductive line. Minimum VSWR for NADC applications is achieved by placing the capacitor as shown in the circle (inductance ≈ 6 nH).

The IC has an internal blocking capacitor so the output is a simple 50 Ω transmission line. An enlarged scale layout of the test board can be found on the last page of this data sheet.

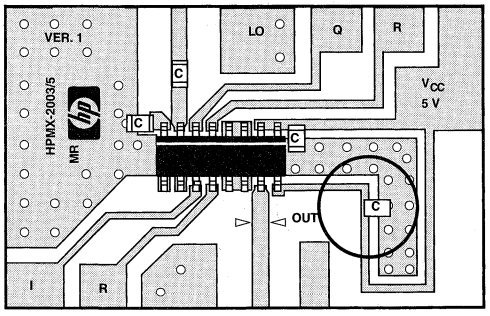


Figure 31. HPMX-2003 NADC Test Board.

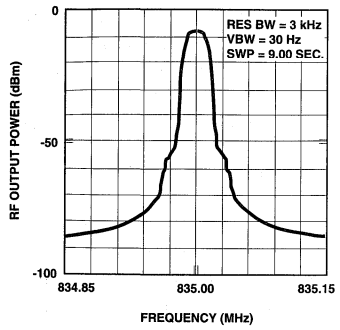


Figure 32. HPMX-2003 NADC Modulation Spectrum at -40°C.

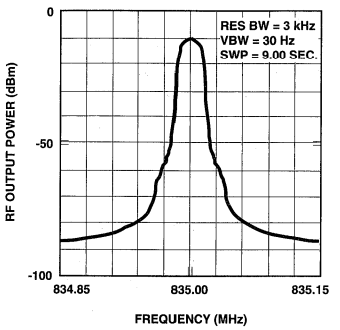


Figure 33. HPMX-2003 NADC Modulation Spectrum at 25°C.

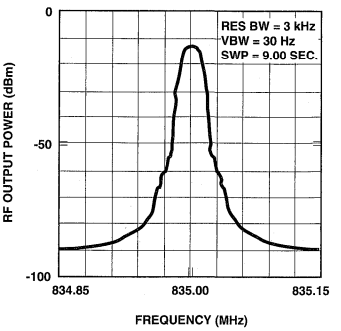


Figure 34. HPMX-2003 NADC Modulation Spectrum at 85°C.

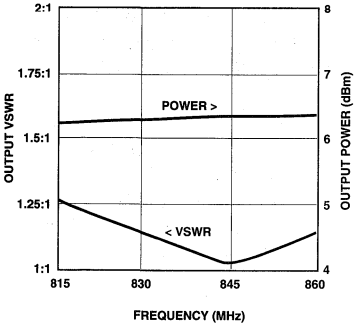


Figure 35. HPMX-2003 Output VSWR and Power vs. Frequency, V_{CC} = 5 V, LO = -12 dBm, V_{Imod} = V_{Qmod} = 3.75 V, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

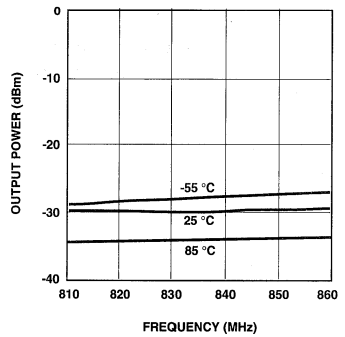


Figure 36. HPMX-2003 LO Leakage vs. Frequency and Temperature (Without Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, V_{Imod} = V_{Qmod} = V_{Iref} = V_{Qref} = 2.5 V.

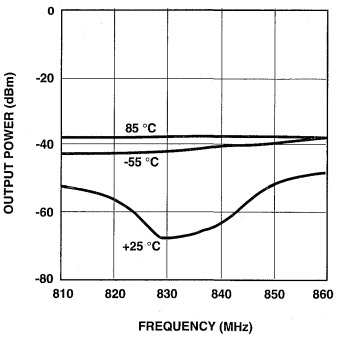


Figure 37. LO Leakage vs. Frequency and Temperature (With 25°C Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V.

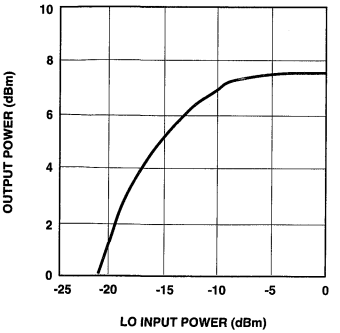


Figure 38. HPMX-2003 Power Output vs. LO Input Power at 900 MHz, V_{CC} = 5 V, LO = -12 dBm, V_{Imod} = V_{Qmod} = 3.75 V, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

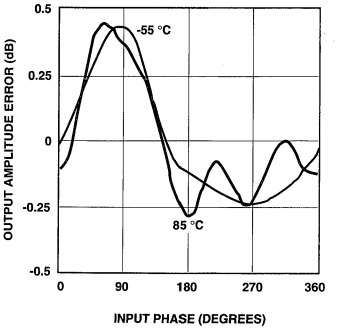


Figure 39. HPMX-2003 Vector Amplitude Error vs. Input Phase and Temperature at 900 MHz, V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V.

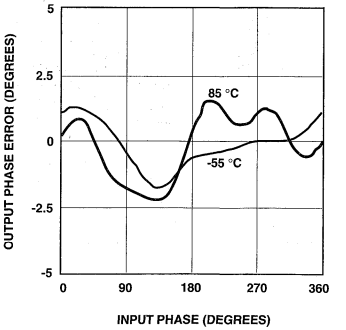


Figure 40. HPMX-2003 Vector Phase Error vs. Input Phase and Temperature at 900 MHz, V_{CC} = 5 V, LO = -12 dBm, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V.

Note: Modulation spectrum test conditions as follows: LO = -12 dBm at 835 MHz, V_I = V_Q = 2.5 V_{p-p}, unbalanced, average level = 2.5 V, V_{Iref} = V_{Qref} = 2.5 V, bit clock rate: 48.6 kHz, baseband filter: α = 0.35, $\pi/4$ DQPSK, V_{CC} = 5 V.

HPMX-2003 JDC Applications

The JDC System

JDC (Japan Digital Cellular) commonly refers to the Japanese digital cellular telephone system standard. Digital cellular phones for the Japanese market must conform to this standard. The JDC system is characterized by 25 kHz channel spacing and mobile to base transmit frequencies of 940 – 960 MHz. The primary modulation characteristics include $\pi/4$ DQPSK filtering of the I and Q signals and 42 kbps transmission rate.

Critical Performance Parameters

JDC standards require that the telephone exhibit RMS modulation error ≤12.5%. The modulated output spectrum of the phone must lie within a "spectral mask" which defines maximum allowable radiation levels into adjacent and alternate channels. Specifically, 50 kHz from the channel center frequency (f_0), the output of the phone must be at least 45 dB below the peak output at f_0. 100 kHz from f_0, the output must be at least 60 dB below the peak output at f_0. Refer to the JDC specifications for more detailed information.

HPMX-2003 Performance

The typical RMS modulation error level of 4% makes the HPMX-2003 an excellent choice for JDC applications. The output spectrum falls easily within the JDC spectral mask, and the high power and simple output configuration mean lower components count, reduced size and higher system efficiency.

Particulars of Use

Many of the JDC application performance graphs shown in this data sheet were created using the test board shown in figure 41,below.

The only external components required by this IC are four chip capacitors. One capacitor is used as a DC block on the input transmission line. The second capacitor (at pin 8) provides an AC ground to one side of the differential LO input. The third and fourth capacitors (at pins 1 and 16) are for V_{CC} bypass.

The circuit board includes an inductive trace that can optionally be used to minimize output VSWR by placing a bypass capacitor at various points along the inductive line. Minimum VSWR for JDC applications is achieved by placing the capacitor as shown in the circle (inductance ≈ 0 nH).

The IC has an internal blocking capacitor so the output is a simple 50 Ω transmission line. An enlarged scale layout of this board can be found on the last page of this data sheet.

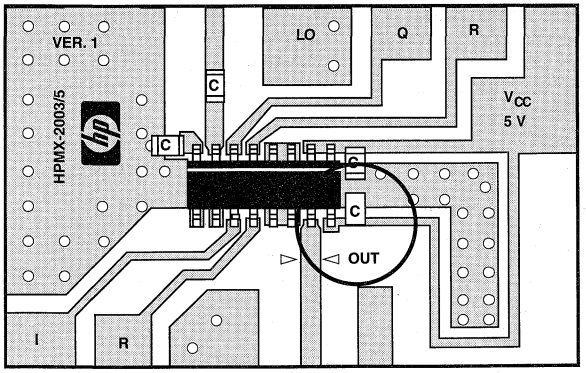


Figure 41. HPMX-2003 JDC Test Board.

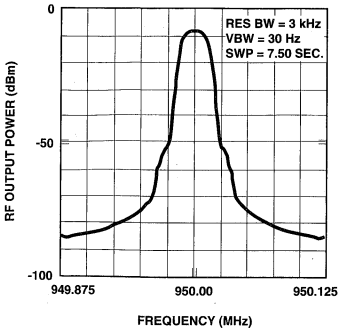


Figure 42. HPMX-2003 JDC Modulation Spectrum at -40°C.

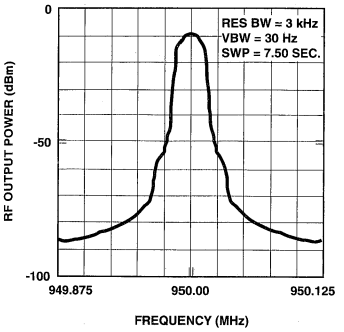


Figure 43. HPMX-2003 JDC Modulation Spectrum at 25°C.

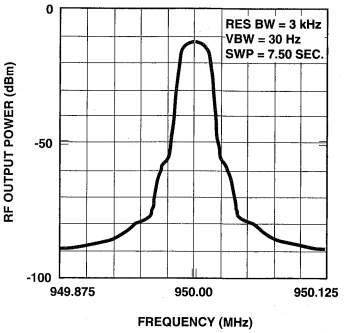


Figure 44. HPMX-2003 JDC Modulation Spectrum at 85°C.

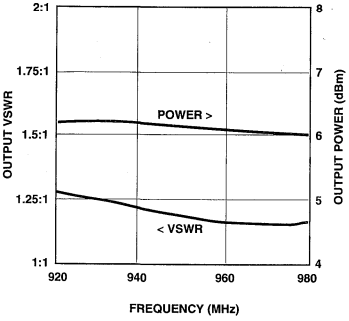


Figure 45. HPMX-2003 Output VSWR and Power vs. Frequency, V_{CC} = 5 V, LO = -12 dBm, V_{Imod} = V_{Qmod} = 3.75 V, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

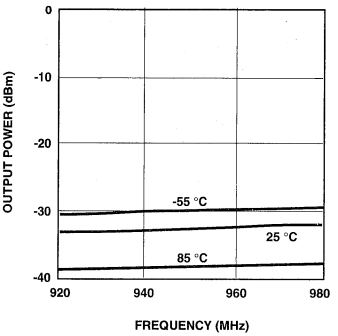


Figure 46. HPMX-2003 LO Leakage vs. Frequency and Temperature (Without Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, V_{Imod} = V_{Qmod} = V_{Iref} = V_{Qref} = 2.5 V.

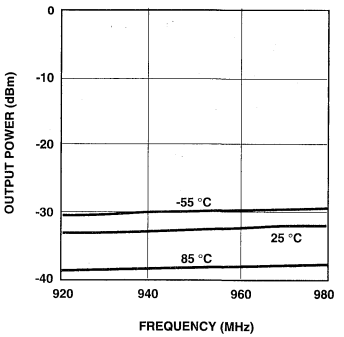


Figure 47. LO Leakage vs. Frequency and Temperature (With 25°C Offset Adjustment), V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V.

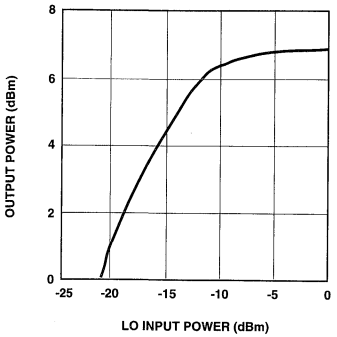


Figure 48. HPMX-2003 Power Output vs. LO Input Power at 950 MHz, V_{CC} = 5 V, V_{Imod} = V_{Qmod} = 3.75 V, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

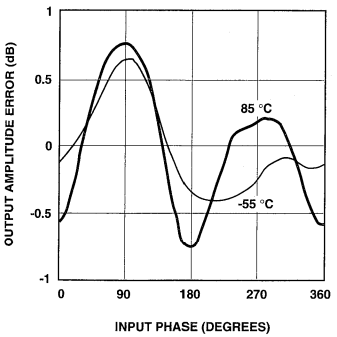


Figure 49. HPMX-2003 Vector Amplitude Error vs. Input Phase and Temperature at 950 MHz, V_{CC} = 5 V, LO = -12 dBm, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V.

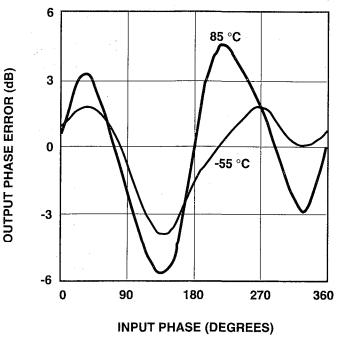


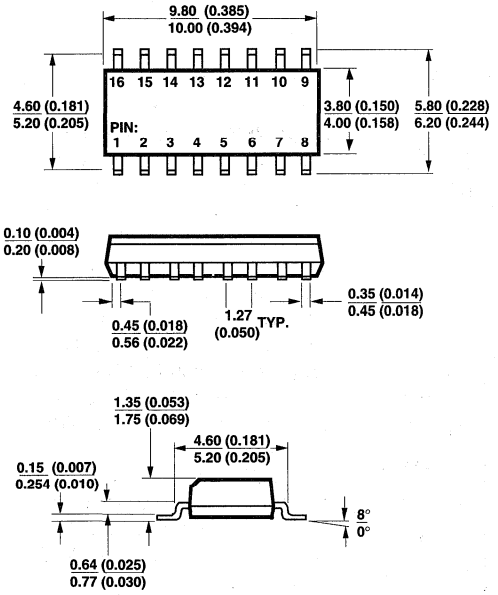
Figure 50. HPMX-2003 Vector Phase Error vs. Input Phase and Temperature at 950 MHz, V_{CC} = 5 V, LO = -12 dBm, Unbalanced, V_{Iref} = V_{Qref} = 2.5 V.

Note: Modulation spectrum test conditions as follows: LO = -12 dBm at 950 MHz, V_{Imod} = V_{Qmod} = 2.5 V_{p-p}, unbalanced, average level = 2.5 V, V_{Iref} = V_{Qref} = 2.5 V, bit clock rate: 42 kHz, baseband filter: α = 0.5, π/4 DQPSK, V_{CC} = 5 V.

HPMX-2003
Part Number Ordering Information

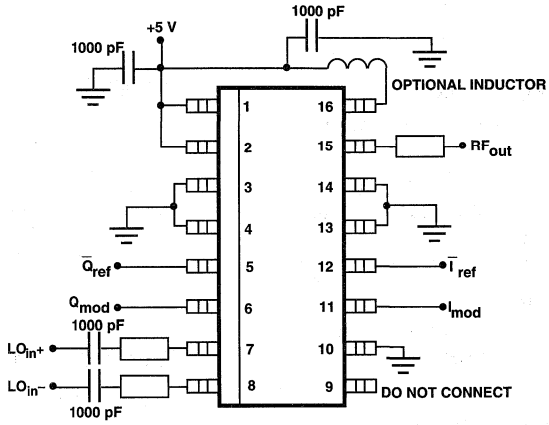
Part Number	Option	No. of Devices	Reel Size
HPMX-2003		25 min.	tube
HPMX-2003	T10	1000	7"

Package Dimensions
SO-16 Package



NOTE: DIMENSIONS ARE IN MILLIMETERS (INCHES).

HPMX-2003 Test Board Layout



Finished board size: 1.5" x 1" x 1/32" Material: 1/32" epoxy/fiberglass, 1 oz. copper, both sides, tin/lead coating, both sides.

Note: white "+" marks indicate drilling locations for plated-through via holes to the groundplane on the bottom side of the board.

HEWLETT® PACKARD

Silicon Bipolar RFIC 100 MHz Vector Modulator

Technical Data

HPMX-2005

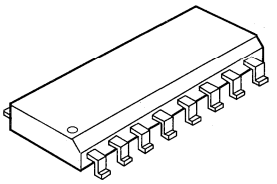
Features

- **25 - 250 MHz Output Frequency**
- **-5 dBm Peak P_{out}**
- **Unbalanced 50 Ω Ouptut Match**
- **Internal 90° Phase Shifter**
- **5 V, 15 mA Bias**
- **SO-16 Surface Mount Package**

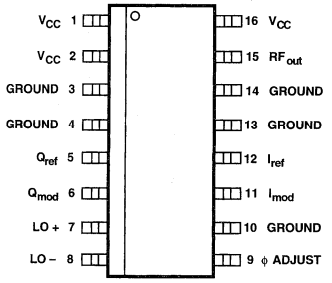
Applications

- **Dual Conversion Cellular Telephone and PCS Handsets**
- **Dual Conversion ISM Band Transmitters and LANs**
- **Direct Conversion Digital Transmitters for 25-250 MHz**

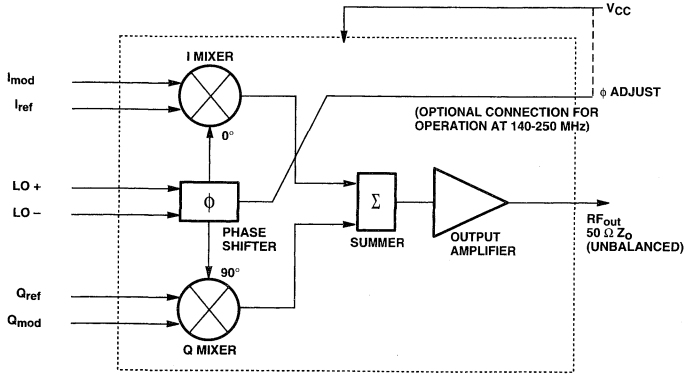
Plastic SO-16 Package



Pin Configuration



Functional Block Diagram



Description

Hewlett Packard's HPMX-2005 is a silicon RFIC vector modulator housed in a SO-16 surface mount plastic package. This IC can be used for direct modulation at output frequencies from 25 to 250 MHz, or, in combination with an up-converting mixer, for dual or multiple conversion modulation to higher frequencies. The IC contains two matched Gilbert cell mixers, an RC phase shifter, a summer, and an output amplifier.

This RFIC is well suited to portable and mobile cellular telephone applications such as North American Digital Cellular, GSM, and Japan Digital Cellular, and to Personal Communications Systems such as DCS-1800 or handyphones. It is also useful for applications in 900 MHz, 2.4 GHz and 5.7 GHz ISM (Industrial-Scientific-Medical) bands requiring digital modulation, such as Local Area Networks (LANs).

The HPMX-2005 is fabricated with Hewlett-Packard's 25 GHz ISOSAT-II process, which combines stepper lithography, self-alignment, ion-implantation techniques, and gold metallization to produce state of the art RFICs.

HPMX-2005 Absolute Maximum Ratings, T_A = 25°C

Symbol	Parameter	Units	Absolute Maximum[1]
P_{diss}	Power Dissipation [2,3]	mW	500
LO_{in}	LO Input Power	dBm	15
V_{CC}	Supply Voltage	V	10[4]
ΔV_{Imod}, ΔV_{Qmod}	Swing of V_{Imod} about V_{Iref} or V_{Qmod} about V_{Qref}	V_{p-p}	5[4]
V_{Iref}, V_{Qref}	Reference Input Levels	V	5
T_{STG}	Storage Temperature	°C	-65 to 150
T_j	Junction Temperature	°C	150

Thermal Resistance[2]:
θ_{jc} = 125°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_C = 25°C (T_C is defined to be the temperature at the ends of pin 3 where it contacts the circuit board).
3. Derate at 8 mW/°C for T_C > 87°C.
4. This voltage must not exceed V_{CC} by more than 0.8 V.

HPMX-2005 Guaranteed Electrical Specifications, T_A = 25°C, Z_O = 50 Ω

V_{CC} = 5 V, LO = -12 dBm @ 100 MHz (Unbalanced Input), V_{Iref} = V_{Qref} = 2.5 V (unless otherwise noted).

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_d	Device Current	mA		14	17
P_{out}	Output Power V_{Imod} = V_{Qmod} = 3.25 V	dBm	-7	-5	
LO_{leak}	P_{out} - LO at Output V_{Imod} = V_{Qmod} = 2.5 V	dBc	30	36	
ε_{mod}	Average Modulation Error $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2} = 0.75$ V	%		2.5	5

HPMX-2005 Summary Characterization Information. T_A = 25°C, Z_O = 50 Ω

V_{CC} = 5 V, LO = -12 dBm @ 100 MHz (Unbalanced Input), V_{Iref} = V_{Qref} = 2.5 V (unless otherwise noted).

Symbol	Parameters and Test Conditions	Units	Typ.
R_{in}	Input Resistance (I_{mod} to I_{ref} or Q_{mod} to Q_{ref})	Ω	10 k
$R_{in\text{-}gnd}$	Input Resistance to Ground (Any I, Q Input to Ground)	Ω	10 k
$VSWR_{LO}$	LO VSWR (50 Ω) 25 - 200 MHz Bandwidth		1.5:1
$VSWR_O$	Output VSWR (50 Ω) 25 - 200 MHz Bandwidth		2.5:1
-	Output Noise Floor V_{Imod} = V_{Qmod} = 3.25 V	dBm/Hz	-134
IM_3	DSB Third Order Intermodulation Products	dBc	33
A_i	RMS Amplitude Error	dB	0.15
P_i	RMS Phase Error	degrees	1.0

HPMX-2005 Pin Descriptions

V_{CC} (pins 1, 2 & 16)

These three pins provide DC power to the RFIC, and are connected together internal to the package. They should be connected to a 5 V supply, with appropriate AC bypassing (1000 pF typ.) used near the pins, as shown in figures 1 and 2.**The voltage on these pins should always be kept *at least 0.8 V more positive* than the DC level on any of pins 5, 6, 11, or 12.** Failure to do so may result in the modulator drawing sufficient current through the data or reference inputs to damage the IC (see also Figure 5).

Ground (pins 3, 4, 10, 13 & 14)

These pins should connect with minimal inductance to a solid ground plane (usually the backside of the PC board). Recommended assembly employs multiple plated through via holes where these leads contact the PC board.

I_{ref} (pin 12) and Q_{ref} (pin 5) I_{mod} (pin 11) and Q_{mod} (pin 6) Inputs

The I and Q inputs are designed for unbalanced operation but can be driven differentially with similar performance. The recommended level of unbalanced I and Q signals is 1.5 V_{p-p} with an average level of 2.5 V above ground. The reference pins should be DC biased to this average data signal level (V_{CC}/2 or 2.5 V typ.). For single ended drive, pins 5 and 12 can be tied together. For differential operation, 0.75 V_{p-p} signals may be applied across the I_{mod}/I_{ref} and the Q_{mod}/Q_{ref} pairs. The average level of all four signals should be about 2.5 V above ground. The impedance between I_{in} or Q_{in} and ground is typically 10 kΩ and the impedance between I_{mod} and I_{ref} or Q_{mod} and Q_{ref} is typically 10 kΩ. The input bandwidth typically exceeds 40 MHz. It is possible to reduce LO leakage through the IC by applying slight DC imbalances between I_{mod} and I_{ref} and/or Q_{mod} and Q_{ref} (see page 9). All performance data shown on this data sheet was taken with unbalanced I/Q inputs.

LO Input (pins 7 and 8)

The LO input of the HPMX-2005 is balanced (differential) and matched to 50 Ω. For drive from a unbalanced LO, pin 7 should be AC coupled to the LO using a 50 Ω transmission line and a blocking capacitor (1000 pF typ.), and pin 8 should be AC grounded (1000 pF capactitor typ.), as shown in figure 1. For drive from a differential LO source, 50 Ω transmission lines and blocking capacitors (1000 pF typ.) are used on both pins 7 and 8, as shown in figure 2. The internal phase shifter allows operation from 25 to 200 MHz (or to 250 MHz by using pin 9 — see below). The recommended LO input level is -12 dBm. All performance data shown on this data sheet was taken with unbalanced LO operation.

Phase Adjust (pin 9)

Applying a DC bias to this pin alters the frequency range of the internal RC phase shifter. In normal operation, this pin is not connected. (Do not ground this pin!) For operation at LO frequencies above 140 MHz, superior modulation error can be achieved by connecting pin 9 to V_{CC} (5 V). The resulting changes in performance are shown in figures 13 through 18. Use of pin 9 extends the operating range to beyond 250 MHz.

RF Output (pin 15)

The RF output of the HPMX-2005 is configured for unbalanced operation, and connects directly to an emitter follower in the output stage of the IC. The output impedance is appropriate for connection without further impedance matching to transmission lines of characteristic impedance between 50 Ω and 150 Ω. The reflection coefficients are given in figure 11. A DC blocking capacitor (1000 pF typ.) is required on this pin.

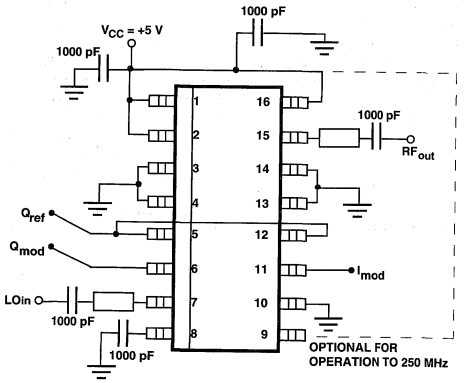


Figure 1. HPMX-2005 Connections Showing Unbalanced LO and I/Q Inputs.

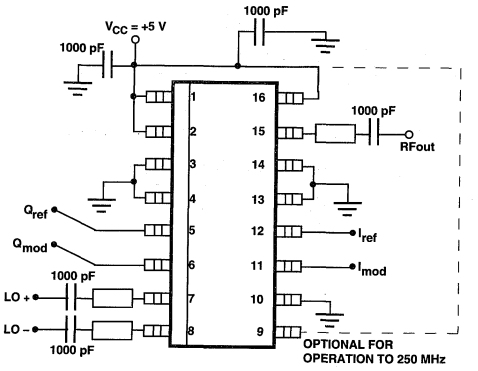


Figure 2. HPMX-2005 Connections Showing Differential LO and I/Q Inputs.

HPMX-2005 Typical Data Measurement

Direct measurement of the amplitude and phase error at the output is the most accurate way to evaluate modulator performance. By measuring the error directly, all the harmonics, LO leakage, etc. that show up in the output signal are accounted for. Figure 3 below shows the test setup that was used to create the amplitude and phase error plots (figures 19 and 21).

Amplitude and phase error are measured by using the four channel power supply to simulate I and Q input signals. Real 1.5 V_{p-p} I and Q signals would swing 0.75 volts above and below an average 2.5 V level, therefore, a logic "high" level input is simulated by applying 3.25 V, and a logic "low" level by applying 1.75 V to the I and/or Q inputs.

Amplitude and phase are measured by setting the network analyzer for an S_{21} measurement at the center frequency of choice. Set the port 1 stimulus level to the LO level you intend to use in your circuit (-12 dBm for the data sheet).

By adjusting the V_i and V_q settings you can step around the I/Q vector circle, reading magnitude and phase at each point. The relative values of phase and gain (amplitude) at the various points will indicate the accuracy of the modulator. Note: you must use very low ripple power supplies for the reference, V_{Imod}, and V_{Qmod} supplies. Ripple or noise of only a few millivolts will appear as wobbling phase readings on the network analyzer.

The same test setup shown below is used to measure input and output VSWR, reverse isolation, and power vs. frequency. V_{Imod} and V_{Qmod} are set to 3.25 V and the appropriate frequency ranges are swept. S_{11} provides input VSWR data, S_{22} provides output VSWR data and S_{12} provides reverse isolation data. S_{21} provides power output (add the source power to the S_{21} derived gain).

LO leakage data shown in figure 17 is generated by setting V_{Imod} = V_{Qmod} = V_{Iref} = V_{Qref} = 2.5 volts then performing an S_{21} sweep. Since phase is not important for these measurements, a scalar network analyzer or a signal generator and spectrum analyzer could be used.

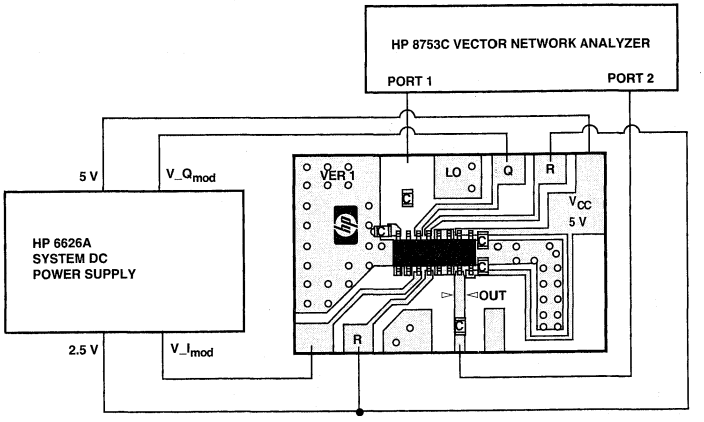


Figure 3: Test Setup for Measuring Amplitude and Phase Error, Input and Output VSWR, Reverse Isolation and LO Leakage of the Modulator.

HPMX-2005 Typical Performance

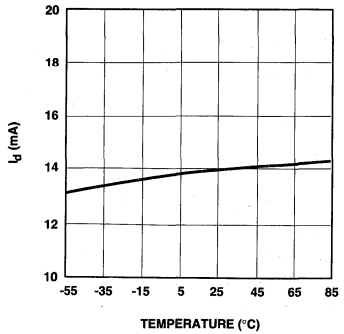


Figure 4. HPMX-2005 Device Current vs. Temperature. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod} = 3.25 V, T_A = 25°C.

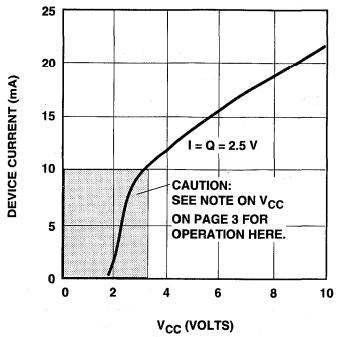


Figure 5. HPMX-2005 Device Current vs. Voltage. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod} = 3.25 V, T_A = 25°C.

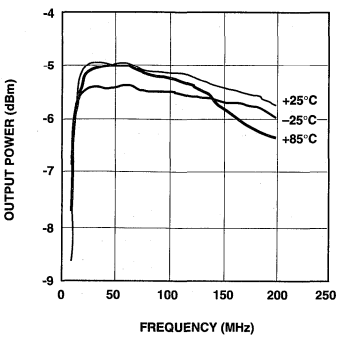


Figure 6. HPMX-2005 Power Output vs. Frequency and Temperature. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod} = 3.25 V.

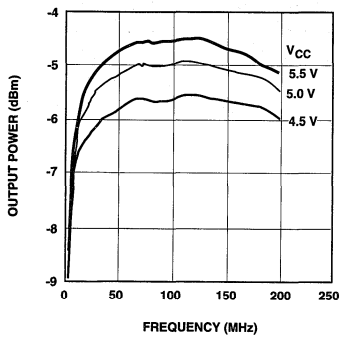


Figure 7. HPMX-2005 Power Output vs. Frequency and Supply Voltage. LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod} = 3.25 V, T_A = 25°C.

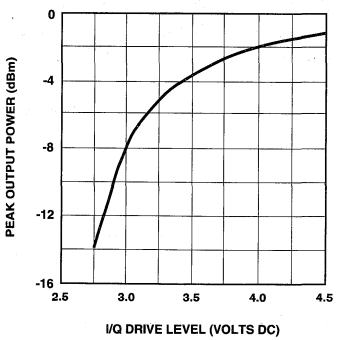


Figure 8. HPMX-2005 Power Output vs. I/Q Drive Level at 100 MHz. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod}, T_A = 25°C.

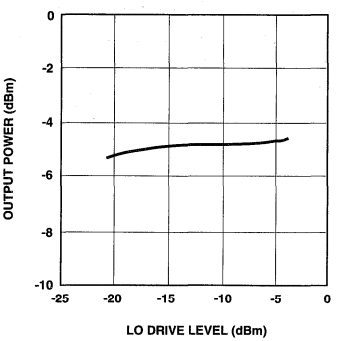


Figure 9. HPMX-2005 Power Output vs. LO Drive Level at 100 MHz. V_{CC} = 5 V, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod} = 3.25 V, T_A = 25°C.

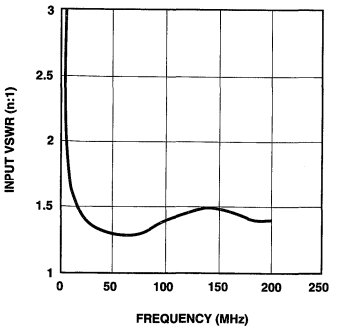


Figure 10. HPMX-2005 LO VSWR vs. Frequency. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

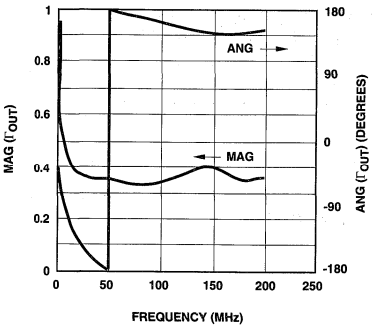


Figure 11. HPMX-2005 Output Reflection Coefficient vs. Frequency. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

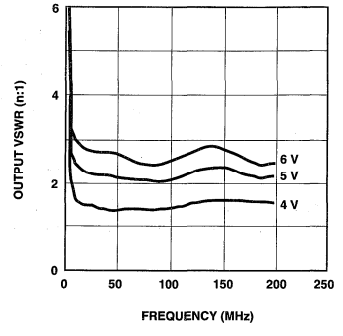


Figure 12. HPMX-2005 Output VSWR vs. Frequency and Supply Voltage. LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

HPMX-2005 Typical Performance Using Phase Adjust

The HPMX-2005 has an internal phase shifter that in normal use (pin 9 open circuited) operates over a frequency range of 25 to 200 MHz. By applying 5 volts to pin 9, this frequency range can be raised to beyond 250 MHz. This page shows HPMX-2005 modulator performance with pin 9 tied to V_{CC} = 5 V for higher frequency operation. Using the Φ adjust has minimal effect on the VSWRs at the LO port.

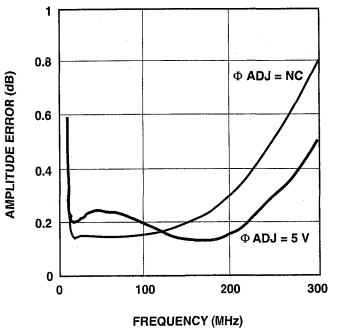


Figure 13. HPMX-2005 RMS Amplitude Error vs. Frequency and Φ Adjust. V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 0.75 V, T_A = 25°C.

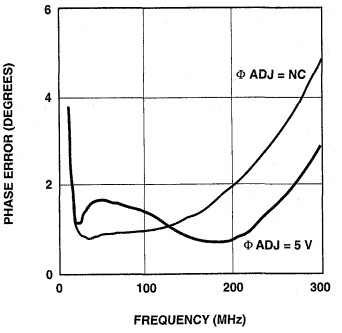


Figure 14. HPMX-2005 RMS Phase Error vs. Frequency and Φ Adjust. V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 0.75 V, T_A = 25°C.

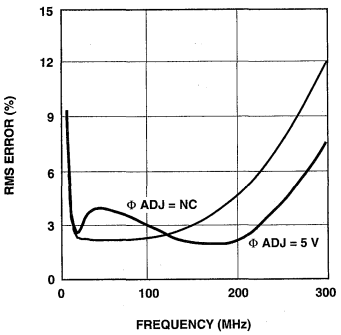


Figure 15. HPMX-2005 RMS Modulation Error vs. Frequency and Φ Adjust. V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 0.75 V, T_A = 25°C.

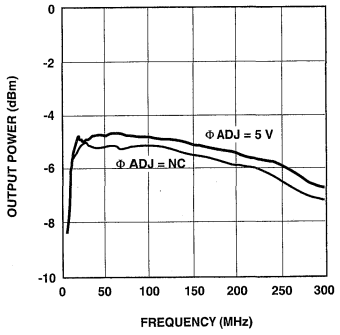


Figure 16. HPMX-2005 Output Power vs. Frequency and Φ Adjust. V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $V_{Imod} = V_{Qmod}$ = 3.25 V, T_A = 25°C.

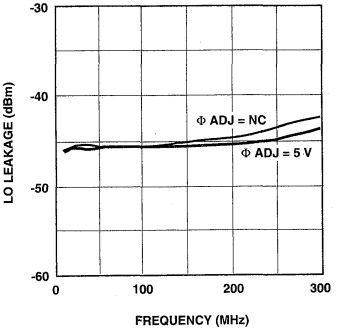


Figure 17. HPMX-2005 LO Leakage vs. Frequency and Φ Adjust. V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref} = V_{Imod} = V_{Qmod}$ = 2.5 V, T_A = 25°C.

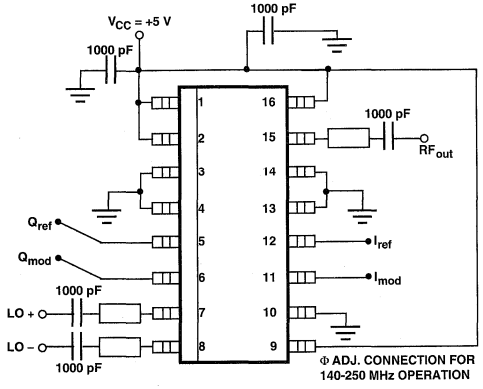


Figure 18. Connection of Pin 9 for Operation of the HPMX-2005 at Frequencies Between 140 MHz and 250 MHz.

HPMX-2005 Modulation Accuracy (Sample Part)

V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 0.75 V, T_A = 25°C (unless otherwise noted).

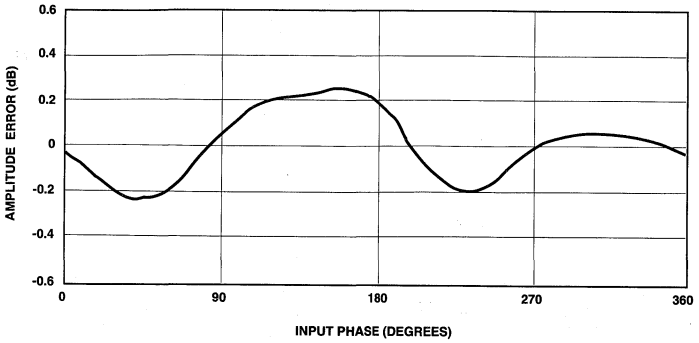


Figure 19. HPMX-2005 RMS Amplitude Error vs. Input Phase at 100 MHz.

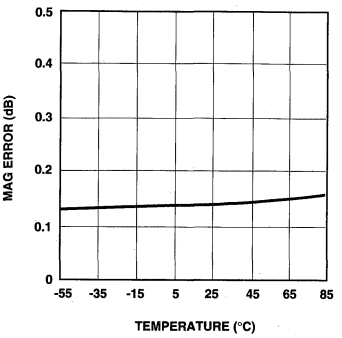


Figure 20. HPMX-2005 RMS Amplitude Error at 100 MHz vs. Temperature.

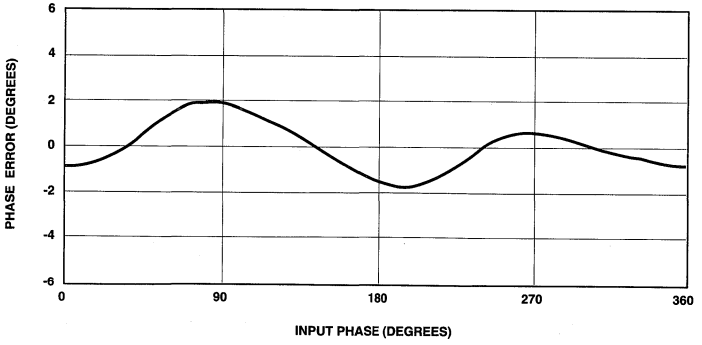


Figure 21. HPMX-2005 Phase Error vs. Input Phase at 100 MHz.

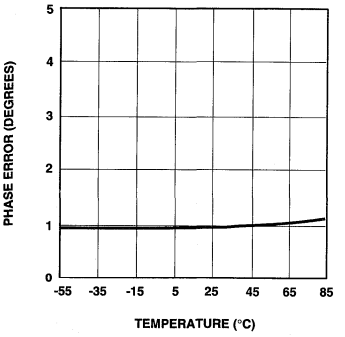


Figure 22. HPMX-2005 RMS Phase Error at 100 MHz vs. Temperature.

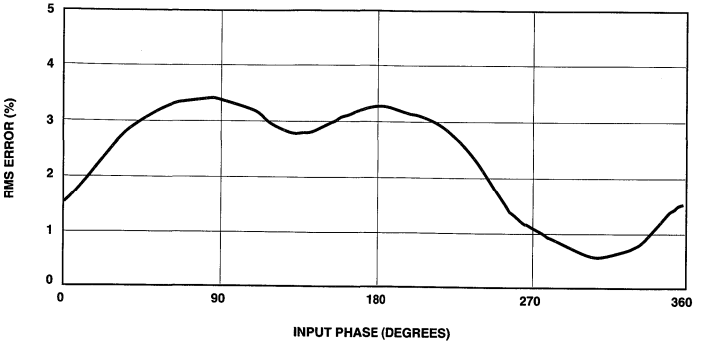


Figure 23. HPMX-2005 RMS Modulation Error vs. Input Phase at 100 MHz. This value is calculated from the values of amplitude and phase error.

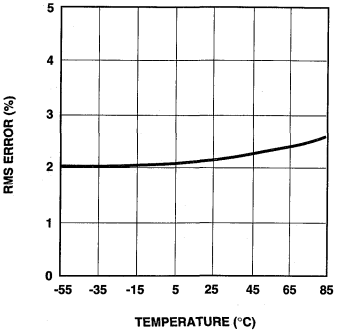


Figure 24. HPMX-2005 RMS Modulation Error at 100 MHz vs. Temperature.

HPMX-2005 Single and Double Sideband Performance

Single sideband (SSB) and double sideband (DSB) tests are sometimes used to evaluate modulator performance. Typical SSB and DSB output spectrum graphs for the HPMX-2005 are shown in figures 25 and 26 below. Figure 27 shows the test equipment setup used to generate this information.

For accurate measurements of modulator performance and LO suppression, the phase shift provided by the I and Q signal generators must be very close to 90 degrees and the amplitude of the two signals must be matched to within a few millivolts. The I,Q signal generator must put out low distortion signals or the spectrum analyzer will show high harmonic levels that reflect the performance of the signal generator, not the modulator.

HPMX-2005 Typical Sideband Performance Data

V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $V_{Imod} = V_{Iref} + 0.75\ V \sin(2\pi f_n t)$, $V_{Qmod} = V_{Qref} + 0.75\ V \cos(2\pi f_n t)$ for SSB, $V_{Imod} = V_{Qmod} = V_{Qref} + 0.75\ V \cos(2\pi f_n t)$ for DSB, f_n = 25 kHz, T_A = 25°C

Symbol	Parameters and Test Conditions	Units	SSB	DSB
P_{LSB}	Lower Sideband Power Output	dBc	-8	-11
LO_{leak}	LO Suppression	dBc	33	30
P_{USB}	Upper Sideband Power Output	dBm	-38	-11
IM_3	3rd Order Intermodulation Distortion Level	dBc	NA	33

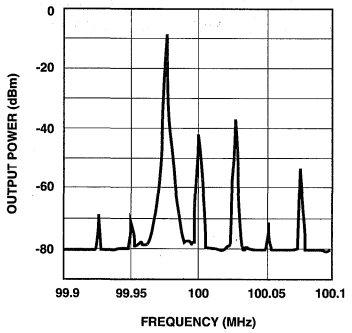


Figure 25. Single Sideband Output Spectrum.

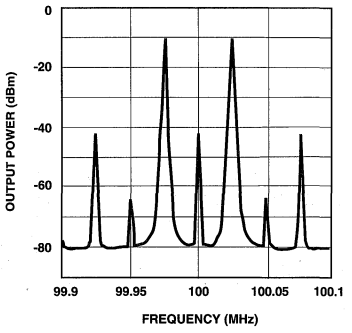


Figure 26. Double Sideband Output Spectrum.

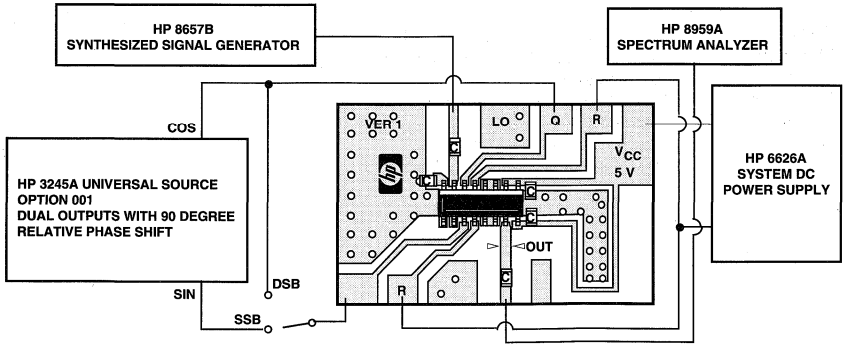


Figure 27. HPMX-2005 Single/Double Sideband Test Setup.

HPMX-2005 Using Offsets to Improve LO Leakage

It is possible to improve on the excellent performance of the HPMX-2005 for applications that are particularly sensitive to LO leakage. The amount and nature of the improvement are best understood by examining figures 28 and 29, below.

LO leakage results when normal variations in the wafer fabrication process cause small shifts in the values of the modulator IC's internal components. These random variations create an effect equivalent to slight DC imbalances at the input of each (I and Q) mixer. The DC imbalances at the mixer inputs are multiplied by ±1 at the LO frequency and show up at the output of the IC as LO leakage.

It is possible to externally apply small DC signals to the I and Q inputs and exactly cancel the internally generated DC offsets. This will result in sharply decreased LO leakage at precisely the frequency and temperature where the offsets were applied (see figure 28).

This improvement is not very useful if it doesn't hold up over frequency and temperature changes. The lower curve in figure 28 shows how the offset-adjusted LO leakage varies versus frequency. Note that it remains below -60 dBm over most of the frequency range shown. In the 20 MHz range centered at 100 MHz, the level is closer to -70 dBm.

Figure 29 shows the performance of the offset adjusted LO leakage over temperature. Note that the adjusted curve is at a level near -70 dBm over the entire temperature range.

The net result of using externally applied offsets with the HPMX-2005 is that an LO leakage level below -50 dBm can typically be achieved over both frequency and temperature.

The magnitude of the required external offset varies randomly from part to part and between the I and Q mixers on any given IC. Offsets can range from -35 mV to +35 mV. External offsets may be applied either by varying the average level of the I and Q modulating signals, or by varying the voltages at the I_{ref} and Q_{ref} pins of the modulator.

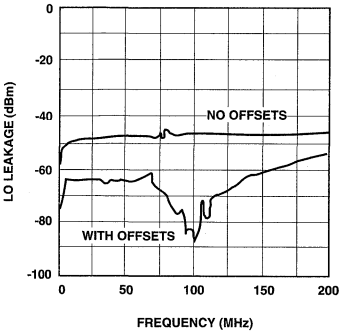


Figure 28. LO Leakage vs. Frequency Without DC Offsets and LO Leakage vs. Frequency with DC Offsets Adjusted for Minimum LO Leakage at 100 MHz. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

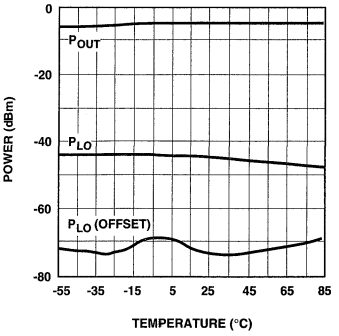


Figure 29. LO Leakage with No DC Offsets at 100 MHz vs. Temperature (Upper Curve) and LO Leakage with DC Offsets Adjusted for Minimum Leakage at 25°C vs. Temperature (Lower Curve). V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V.

HPMX-2005 Modulation Spectrum Diagrams

Figure 30, below, shows the test set-up that was used to generate the GSM, JDC and NADC modulation spectrum diagrams that appear on the following page. The major differences between these tests are summarized in the table below.

The modulation spectra are created by setting the function generator to the appropriate bit-clock frequency. The pattern generator is set to produce a pseudorandom serial bit stream (n = 20) that is NRZ coded. The pseudorandom bit stream which simulates the serial data in a digital phone is fed to the base-band processor that splits it into a two bit parallel stream (I and Q) and then filters each according to the requirements of the digital telephone system being simulated. The I and Q signals from the baseband filter are then DC offset by 2.5 V using the op-amp circuit. The output of the modulator is monitored using a spectrum analyzer.

System	Bit Clock Frequency	Baseband Filter	Channel (LO) Frequency
GSM	270 kHz	0.3 GMSK (HP-8657B)	900 MHz
JDC	42 kHz	α = 0.5 π/4 DQPSK (HP-8657D)	950 MHz
NADC	48.6 kHz	α = 0.35 π/4 DQPSK (HP-8657D)	835 MHz

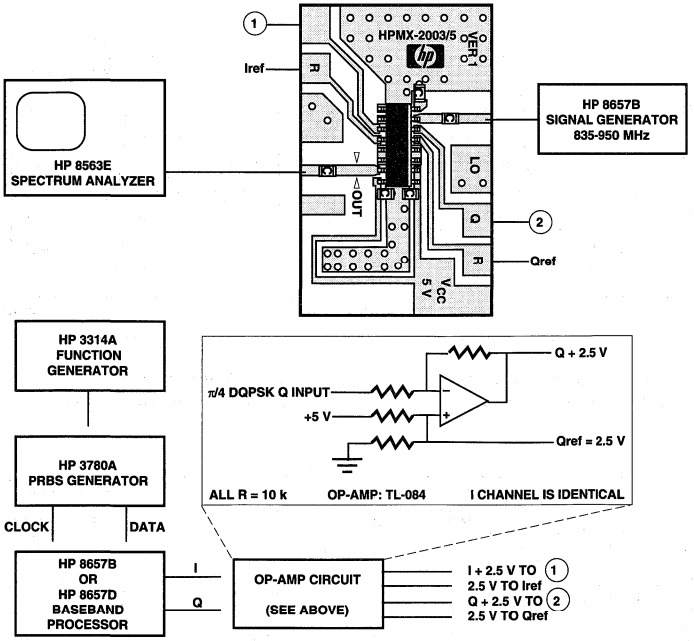


Figure 30. Test Equipment Setup for Modulation Spectrum Diagrams.

HPMX-2005 Cellular Telephone Modulation Spectrum Performance

T_A = 25°C (unless otherwise noted)

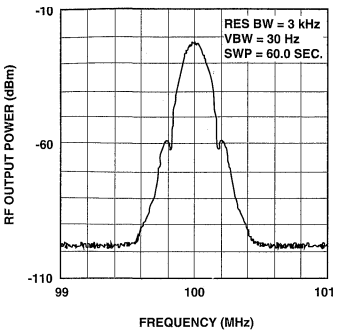


Figure 31. HPMX-2005 GSM Modulation Spectrum at -40°C.

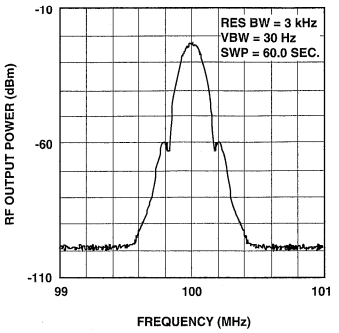


Figure 32. HPMX-2005 GSM Modulation Spectrum at 25°C.

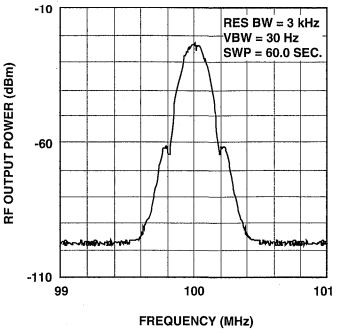


Figure 33. HPMX-2005 GSM Modulation Spectrum at 85°C.

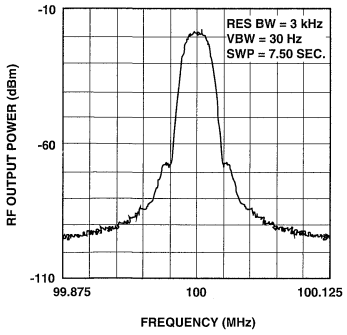


Figure 34. HPMX-2005 JDC Modulation Spectrum at -40°C.

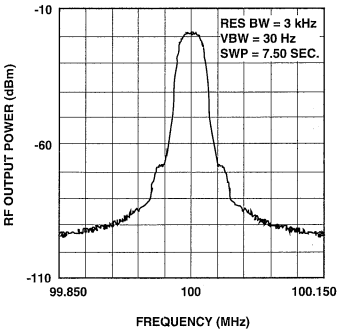


Figure 35. HPMX-2005 JDC Modulation Spectrum at 25°C.

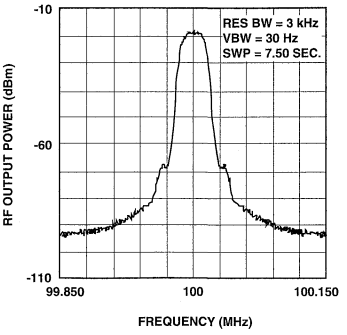


Figure 36. HPMX-2005 JDC Modulation Spectrum at 85°C.

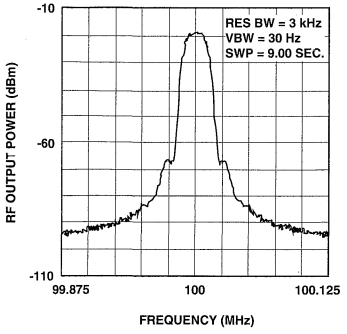


Figure 37. HPMX-2005 NADC Modulation Spectrum at -40°C.

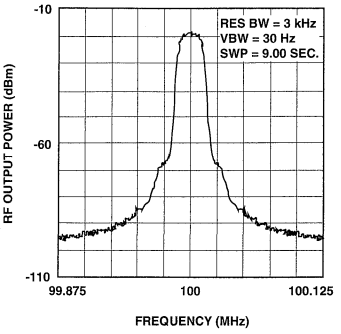


Figure 38. HPMX-2005 NADC Modulation Spectrum at 25°C.

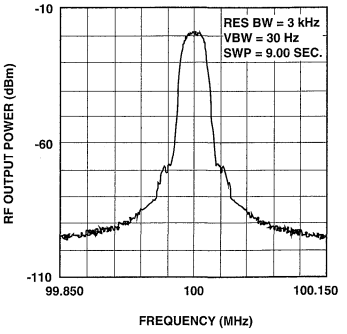
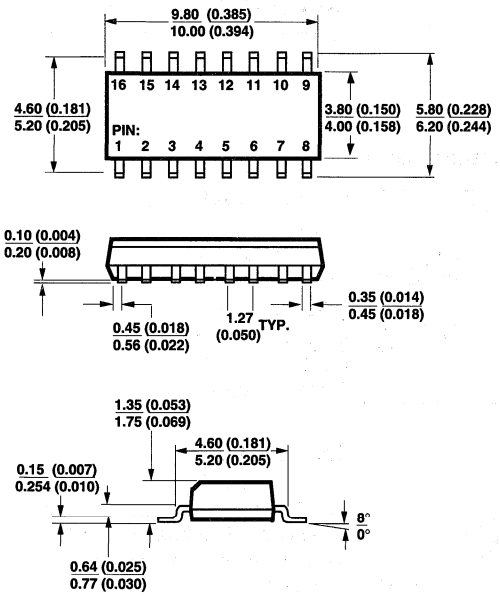


Figure 39. HPMX-2005 NADC Modulation Spectrum at 85°C.

Part Number Ordering Information

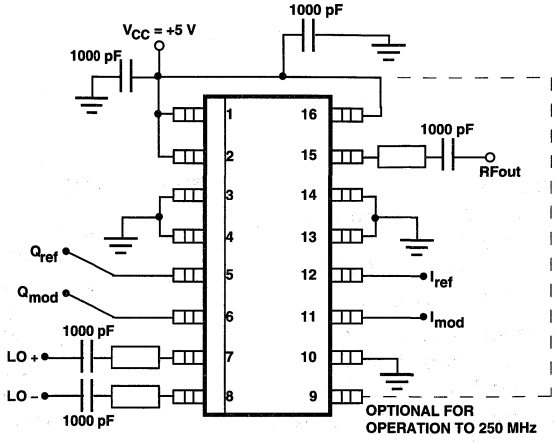
Part Number	Option	No. of Devices	Container
HPMX-2005		25 Min.	Tube
HPMX-2005	T10	1000	7" Reel

Package Dimensions
SO-16 Package



NOTE: DIMENSIONS ARE IN MILLIMETERS (INCHES).

HPMX-2005 Test Board Layout



Finished board size 1.5" x 1" x 1/32"

Material: 1/32" epoxy/fiberglass, 1 oz. copper, both sides, fused tin/lead coating, both sides.

Note: white "+" marks indicate drilling locations for plated-through via holes to the groundplane on the bottom side of the board.

0.8 – 2.5 GHz Upconverter/Amplifier

Technical Data

HPMX-2006

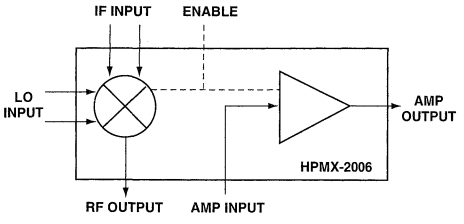
Features

- **Wide Band Operation**
  RF Output: 800-2500 MHz
  IF Input: DC-900 MHz
- **2.7- 5.5 V Operation**
- **Mixer + Amplifier:** 38 mA
  Mixer only: 15 mA
  Standby Mode: <40 µA
- **Differential LO and High Impedance IF Inputs**
- **-8.5 dBm Mixer and +4.5 dBm Amplifier Output Power at 1900 MHz**
- **JEDEC Standard SSOP-16 Surface Mount Package**

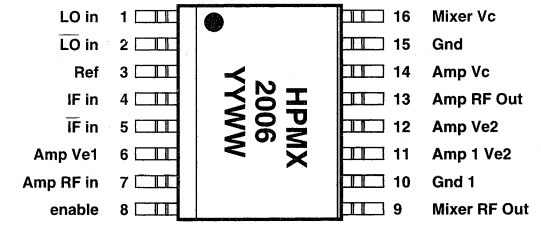
Applications

- **Cordless Handsets and Base Stations**
- **Wireless Data Terminals**
- **Cellular/PCS Handsets and Base Stations**

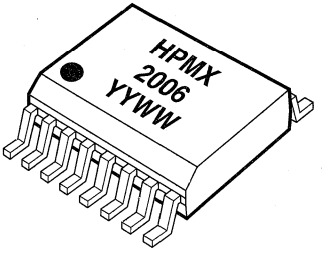
Functional Block Diagram



Package Pin Configuration



Plastic SSOP-16



Description

The HPMX-2006 upconverter/ amplifier IC is designed to meet the needs of cellular and PCS telephone and wireless LAN applications.

The IC consists of a Gilbert Cell mixer optimized for upconversion followed by a post-amplifier. The mixer and amplifier are independent allowing the insertion of a sideband filter between the two.

The mixer is double balanced. Both LO and IF inputs may be run either single-endedly, or in differential mode to reduce LO leakage. LO inputs are matched near 50 Ω; high impedance IF inputs allow the mixer to be used as a BPSK modulator. An integrated transformer on the mixer RF port creates a single-ended, matched to 50 Ω output at 1900 MHz, and also reduces common mode noise.

The amplifier features a single-ended 50 Ω match on the input port. The open collector output is easily matched with a simple 2 element network, providing flexible use and good power added efficiency. The amplifier can be disabled to allow use of the mixer alone, reducing the current draw to around 15 mA. The entire IC can be put into a standby mode reducing current consumption to under 40 μA from a 3V source.

The SSOP-16 package insures that the IC occupies a minimal amount of printed circuit board space.

The HPMX-2006 is manufactured using Hewlett-Packard's 30 GHz ISOSAT-II process which combines stepper lithography, self alignment, ion implantation techniques and gold metalization to produce state-of-the-art RFICs.

HPMX-2006 Absolute Maximum Ratings[1]

			Mixer		Amplifier	
Symbol	**Parameter**	**Units**	**Min.**	**Max.**	**Min.**	**Max.**
V_{CC}	Supply Voltage	V	-0.2	8	-0.2	8
P_{diss}	Power Dissipation[2,3]	mW		174		274
	Single-Ended Input Mixer LO Voltage	V		V_C + 0.2		
	Single-Ended Input Mixer IF Voltage	V		V_C + 0.2		
	Amplifier Input RF Power	dBm				+5
T_j	Junction Temperature	°C	-40	+150	-40	+150
T_{STG}	Storage Temperature	°C	-40	+150	-40	+150

Notes:
1. Operation of this device in excess of any of these parameters may cause permanent damage.
2. T_{CASE} = 25°C
3. Derate at 7 mW/°C for T_{CASE} >82°C.

Thermal Resistance[2]:
θ_{jc} = 150°C/W

Recommended operating range of V_{cc} = 2.7 to 5.5 V, T_a = -40 to + 85°C

Standard Test Conditions

Unless otherwise stated, all test data was taken on packaged parts under the following conditions:
V_{cc} = +3.0 VDC, Z_{out} = 50 Ω, ambient temperature T_a = 25°C
LO input: 1750 MHz, -3 dBm, single-ended
IF input: 150 MHz, 300 mV_{p-p}, single-ended, terminated in a 50 Ω pull-up resistor (R1R2 in Figure 11)
$Z_{out\ mixer}$ = $Z_{in\ amp}$ = 50 Ω, $Z_{out\ amp}$ per Figure 11 ((L=2.8 nH, C=2.2 pF)
See Figure 11 for test set-up schematic diagram.

HPMX-2006 Guaranteed Electrical Specifications

Standard test conditions apply unless otherwise noted.

Symbol	**Parameters and Test Conditions**	**Units**	**Min.**	**Typ.**	**Max.**
I_C mix	Sleep Mode Current, Mixer	μA			20
I_C amp	Sleep Mode Current, Amplifier	μA			20
I_C mix	Mixer Transmit Current	mA		15	18
I_C amp	Amplifier Transmit Current	mA		23	28
P_{out}	SSB Output Power, Mixer Only	dBm	-11	-9	
P_{out}	Output Power, Amplifier Only (-9.5 dBm in)	dBm	+2.5	+3.8	

HPMX-2006 Summary Characterization Information

Standard test conditions apply unless otherwise noted. Table 2 applies for 900 and 2500 MHz.
IF remains 150 MHz for all frequencies.

Performance vs. Frequency	900 MHz	1900 MHz	2500 MHz	Units
Mixer RF Output Power, V_{if} = 300 mV_{pp}	-8	-9	-12.5	dBm
Mixer RF Output Power, V_{if} = 30 mV_{pp}	-28	-28	-32	dBm
Mixer RF Output Power at 1 dB Gain Compression	-7	-8.5	-12	dBm
Mixer Output Third Order Intercept Point	+3	+2	-4	dBm
Mixer LO Suppression	25	21	18.5	dBc
Mixer Phase Noise (4 MHz offset)	-143	-144	-146	dBm/Hz
Amplifier RF Output Power at P_{in} = -9.5 dBm	+9	+3.8	-2	dBm
Amplifier RF Output Power at 1 dB Gain Compression	+9	+4.5	+2.5	dBm
Amplifier Output Third Order Intercept Point	+19	+14	+12	dBm
Small Signal Amplifier Gain	21	14.5	9.5	dB
Amplifier Noise Figure	8.5	9	9.5	dB
Amplifier Input Return Loss	10.5	9.5	10.5	dB
Amplifier Output Return Loss	9.5	6.5	12	dB
Isolation, Mixer Output to Amplifier Input	32	30	30	dB

HPMX-2006 Pin Description Table

No.	Mnemonic	Description	Typical Signal	Notes
1	LO	differential mi≤xer LO	-3 dBm from single-ended,	LO identical to LObar.
2	LObar	input	50 Ω source	DC present (needs Cbl).
3	Ref	internal voltage reference		Supplies base bias for AC-coupled IF.
4	IF	differential mixer IF	-6 dBm from single-ended,	IF identical to IFbar.
5	IFbar	input	50 W source	Must bias per Table 3.
6	AmpVe1	ground	0 V or unconnected	Disconnect for mixer only
7	AmpRFin	amplifier input	-9.5 dBm from 50 Ω source	DC present (needs Cbl)
8	Enable	chip (amp and mixer) enable input	<0.4V disables >2.5V enables IC	
9	MxRFout	mixer RF output	-9.0 dBm into 50 Ω load	At DC ground
10	gnd1	ground	0 V	
11	Amp1Ve2	ground	0 V or unconnected	Disconnect for mixer only
12	AmpVe2	ground	0 V or unconnected	Disconnect for mixer only
13	AmpRFout	amplifier output	+3 dBm into 50 Ω load	DC present (needs Cbl). RF match required.
14	AmpVc	amplifier Vcc input	3 V, 23 mA	
15	gnd	ground	0 V	
16	MxVc	mixer Vcc input	3 V, 15 mA	

HPMX-2006 Typical Performance

Standard test conditions apply unless otherwise noted.

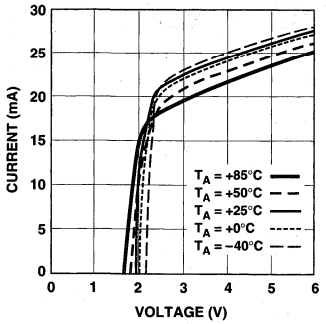


Figure 1. Mixer Device Current vs. Device Voltage over Temperature.

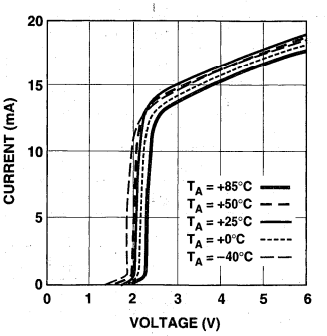


Figure 2. Mixer Device Current vs. Device Voltage over Temperature.

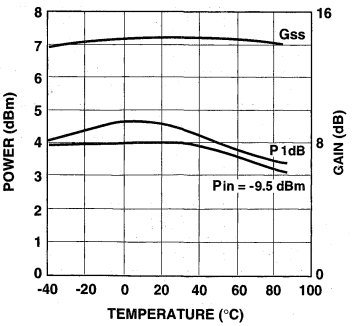


Figure 3. Amp. Output at P_{in} = 9.5 dBm and at 1 dB Compression and Small Signal Gain vs. Temperature.

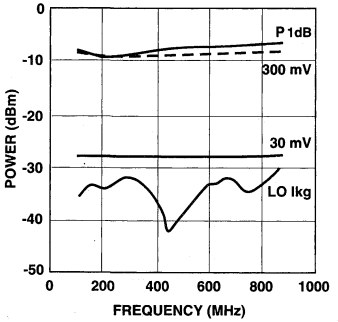


Figure 4. Mixer Output at V_{if} = 30 mV_{pp} and 300 mV_{pp}, at P_{1dB}, and LO Suppression at V_{if} = 300 mV_{pp} vs. IF Frequency.

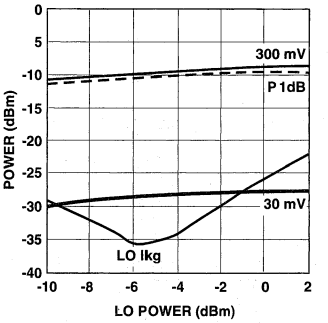


Figure 5. Mixer Output at V_{if} = 30 mV_{pp} and 300 mV_{pp}, at P_{1dB}, and LO Suppression at V_{if} = 300 mV_{pp} vs. LO Power.

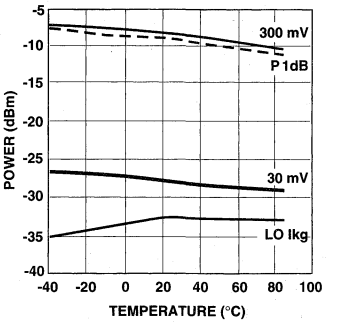


Figure 6. Mixer Output at V_{if} = 30 mV_{pp} and 300 mV_{pp}, at P_{1dB}, and LO Suppression at V_{if} = 300 mV_{pp} vs. Temperature.

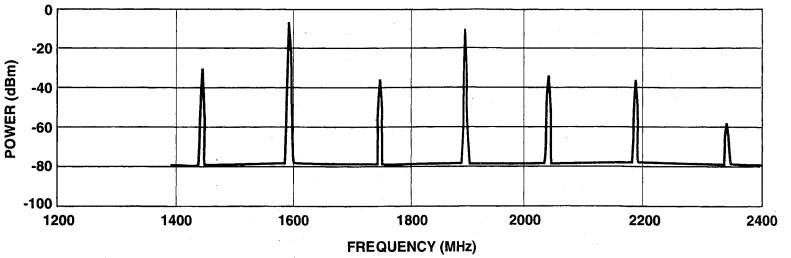


Figure 7. Mixer Output Spectrum for 1 GHz Bandwidth, Centered at 1900 MHz.

Table 1. Typical Output Spurs for 0 – 6 GHz, Standard Test Conditions.

	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8	9	10
0											-	-38.9	-32.2	-44.1	-49.3	-67.2	-64.4	<-80	-73.6	<-80	<-80
1	<-80	<-80	<-80	-70	-78.5	-52.1	-58.8	-33.2	-38.9	-10.1	-31.7	-8.7	-38.3	-38.3	-59.0	-50.1	-39.2	-50.1	-50.2	<-60	<-60
2	<-80	<-60	<-60	<-60	<-60	<-60	-49.5	-50.0	-33.2	-39.1	-42.1	-50.4	-36.1	-48.8	-58.8	<-60	<-60	<-60	<-60	<-60	<-60
3	<-60	<-60	-38.4	-58.6	<-60	<-60	<-60	-52.7	<-60	<-60	-45.6	-37.1	-52	<-60	<-60						
4	<-60	-45.5	-52.0	<-60																	

HPMX-2006 Mixer Port Impedances

GHz	Mag.	Deg.
0.05	0.86	-4
0.10	0.81	-3
0.15	0.84	-1
0.20	0.88	-3
0.25	0.93	-9
0.30	0.91	-15
0.40	0.80	-19
0.50	0.81	-23
0.60	0.80	-28
0.70	0.80	-30
0.80	0.85	-34
0.90	0.84	-39

Figure 8. Impedance of Mixer IF Port.

Circuit of Figure 11 with 1 k Pull up Resistors for the IFs and LO and RF Ports Terminated in 50 Ω.

GHz	Mag.	Deg.
0.50[1]	0.49	-49
0.75	0.48	-63
1.00	0.46	-73
1.25	0.42	-82
1.50	0.40	-102
1.75	0.31	-114
1.75[2]	0.24	-131
2.00	0.20	147
2.25	0.20	87
2.50	0.16	15
2.75	0.37	-131
3.00	0.53	168

Figure 9. Impedance of Mixer LO Port.

[1] Circuit of Figure 11 with IF and RF Ports Terminated in 50 Ω.
[2] As above but LO RC combination in Figure 11 changed from 12 Ω and 12 pF to 0 Ω and 2.7 pF (recommended use for >1.75 GHz).

GHz	Mag.	Deg.
0.50	0.60	82
0.75	0.55	38
1.00	0.52	-5
1.25	0.36	-35
1.50	0.18	-44
1.75	0.17	-17
2.00	0.20	5
2.25	0.24	13
2.50	0.28	17
2.75	0.34	12
3.00	0.37	3

Figure 10. Impedance of Mixer RF Port.

Circuit of Figure 11 with IF and LO Ports Terminated in 50 Ω.

Typical Scattering Parameters, Common Emitter, Z_O = 50 Ω, V_{CC} = 3 V, I_C = 23 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	0.51	149	19.72	9.68	-26	-37.08	0.014	-43	0.91	-3
0.5	0.37	144	17.42	7.43	-49	-39.17	0.011	11	0.78	-16
0.8	0.37	120	16.56	6.73	-76	-43.10	0.007	1	0.80	-22
0.9	0.37	113	16.24	6.49	-85	-36.48	0.015	25	0.83	-23
1.0	0.39	104	15.99	6.30	-94	-40.00	0.010	22	0.84	-26
1.1	0.39	96	15.55	5.99	-101	-41.94	0.008	28	0.84	-29
1.2	0.40	88	15.16	5.73	-112	-47.96	0.004	118	0.84	-32
1.3	0.41	81	15.07	5.67	-120	-38.42	0.012	68	0.85	-33
1.4	0.40	75	14.50	5.31	-125	-40.92	0.009	85	0.87	-36
1.5	0.40	67	13.37	4.66	-134	-46.02	0.005	147	0.84	-40
1.6	0.38	62	12.69	4.31	-145	-33.98	0.020	99	0.85	-40
1.7	0.37	61	12.46	4.20	-148	-33.15	0.022	102	0.84	-44
1.8	0.36	58	11.64	3.82	-153	-32.77	0.023	102	0.84	-49
1.9	0.33	62	11.17	3.62	-161	-34.42	0.019	88	0.79	-51
2.0	0.33	62	10.81	3.47	-168	-34.89	0.018	91	0.77	-54
2.1	0.31	64	9.99	3.16	-175	-29.37	0.034	96	0.75	-58
2.2	0.31	70	9.37	2.94	178	-30.75	0.029	102	0.72	-62
2.3	0.30	75	8.66	2.71	173	-30.75	0.029	89	0.69	-65
2.4	0.32	79	8.10	2.54	170	-33.15	0.022	90	0.67	-70
2.5	0.32	84	7.16	2.28	166	-32.77	0.023	89	0.65	-76
3.0	0.32	94	4.45	1.67	134	-28.40	0.038	99	0.49	-103

HPMX-2006 Test Circuit

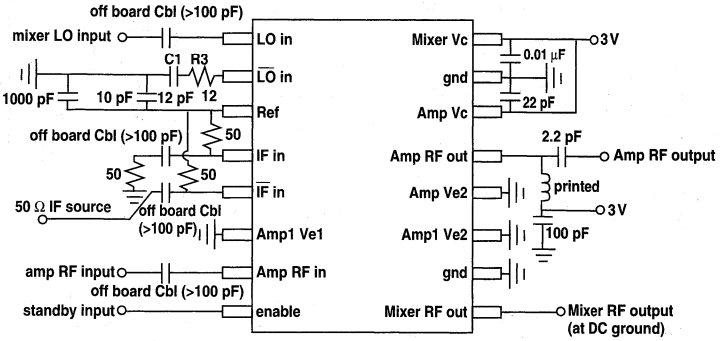


Figure 11. Test Board Configuration.

HPMX-2006 Circuit Use

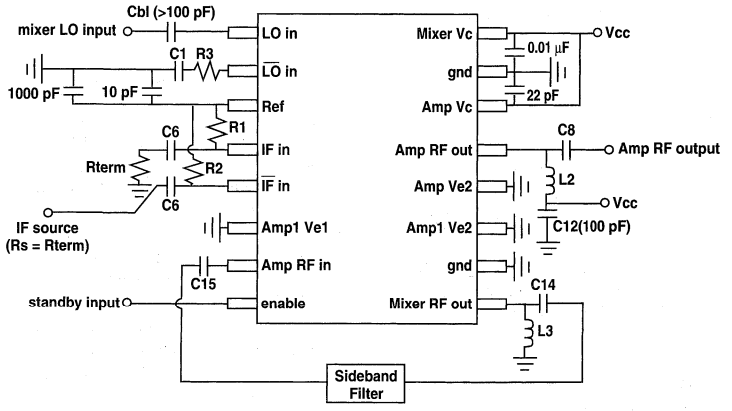


Figure 12. Schematic Diagram of Typical IC Use.

Table 2 lists values for components that change depending on frequency of operation and AC or DC coupling of the IF input. For 2.5 GHz operation, a pre-amplifier may be inserted between the Mixer output and the Amp RF in.

Table 2. Values for Variable Components (see next page for details).

Component	Function	Value	Condition	Value	Condition	Notes
C1, R3	LO AC coupling	12 pF + 12 Ω	F LO < 1.75 GHz	2.7 pF + 0 Ω	F LO > 1.75 GHz	de-Q with R = 12 Ω for broadband operation < 1.75 GHz
C6	IF AC coupling	100 pF typ	AC coupled	short ckt	DC coupled	see also R1,R2
R1,R2	biases IF bases	50 Ω typ	AC coupled	open ckt	DC coupled	also sets load for optimum IF[1]
C8, L2	amp out match	see Table 3 for values vs. frequency				L2 set by position of C12
L3, C14	mixer output match	not used	1900 MHz operation	27 nH 1.3 pF[2]	900 MHz operation	900 MHz operation only
C15	amp input match	not used	1900 MHz operation	3.3 pF[2]	900 MHz operation	900 MHz operation only

Notes:
1. Noise Optimum at R1, R2 = 150 Ω
2. Optional

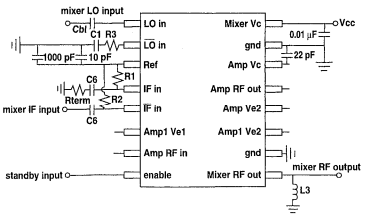


Figure 13. Mixer Only Use (AC Coupled Single-ended Use Shown). Refer to Table 2 for Component Values.

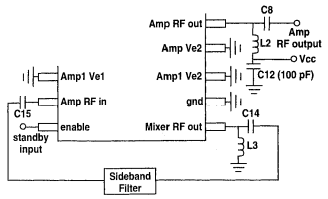


Figure 14. 900 MHz Use. Refer to Table 2 for Component Values.

Frequency, MHz	L2, nH	C8, pF
900	12.5	2.2
1500	5.4	2.2
1800	3.1	2.2
1900	2.8	2.2
2400	1.6	2.2

Table 3. Amp Output Match Component Values vs. Frequency.

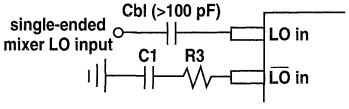


Figure 15. LO Connections for Single-ended Operation.

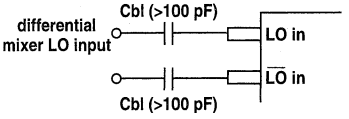


Figure 16. LO Connections for Balanced Operation.

1. LO in and LO bar in are identical; either can be used as the single-ended LO input with the other AC grounded.
2. R3 lowers the Q of the blocking capacitor to remove possible resonances for broadband operation below 1.75 GHz.

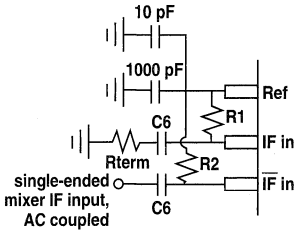


Figure 17. IF Connections for AC Coupled Single-ended Use.

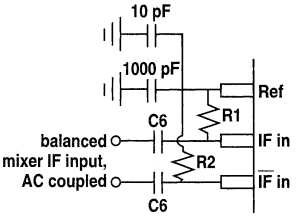


Figure 18. IF Connections for AC Coupled Balanced Use.

1. The IF pins require a bias voltage to operate properly (see Table 4). When the IF is AC coupled, this voltage is supplied from the Ref pin via R1 and R2. When the IF is DC coupled, the voltage is externally generated and the Ref pin is not used.
2. The base current is small, so to 1st order the value of R1, R2 can be selected to set the IF load impedance (50 -200 ohm typ.)
3. IF in and IF bar in are identical; either can be used as as the single-ended IF input with the other AC grounded.
4. R_{term} (optional) should be the same value as the IF source impedance. It improves LO rejection by balancing the IF port and also de-Q's C6.

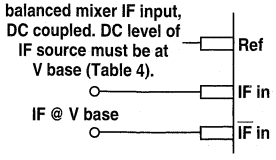


Figure 19. IF Connections for DC Coupled Use.

V_{cc}, V	V_{base}, V
2.7	1.5
3.0	1.5
3.5	1.5-1.75
4.0	1.5-2.0
4.5	1.5-2.25
5.0	1.5-2.5

Table 4. V_{base} vs. V_{cc}. V_{base} is the required bias at the IF ports.

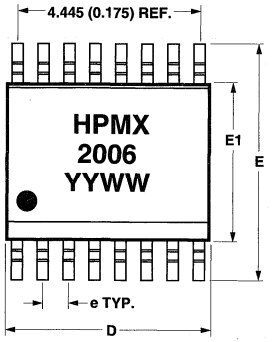
1. For DC coupled operation, the IF input must also supply V_{base} to both IF in and IF in bar, per the values in Table 4. Ref pin is not used.

Part Number Ordering Information

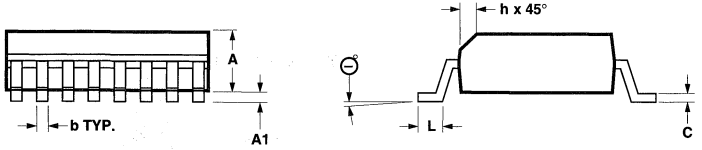
Part Number	No. of Devices	Container
HPMX-2006-TR1	1000	Tape and Reel
HPMX-2006-BLK	25	Tape

Package Dimensions

JEDEC Standard SSOP-16 Package



SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	1.372 (0.054)	1.575 (0.062)
A1	0.127 (0.005)	0.254 (0.010)
b	0.203 (0.008)	0.305 (0.012)
C	0.178 (0.007)	0.254 (0.010)
D	4.801 (0.189)	5.004 (0.197)
E	5.867 (0.231)	6.121 (0.241)
e	0.635 BSC (0.025)	
E1	3.835 (0.151)	3.988 (0.157)
h	0.305 (0.012)	0.457 (0.018)
L	0.533 (0.021)	0.787 (0.031)
θ	0	8



DIMENSIONS IN MILLIMETERS AND (INCHES).

HEWLETT® PACKARD

Vector Modulator/Mixer

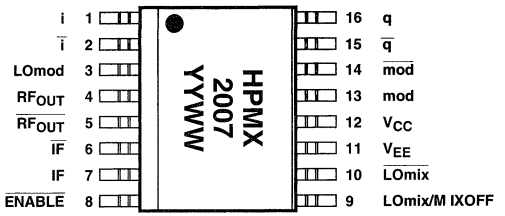
Technical Data

HPMX-2007

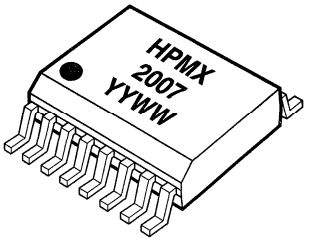
Features

- 5 MHz to 4 GHz Overall Operating Frequency Range
- 40-400 MHz LOmod range
- 2.7 - 5.5 V Operation (3 V, 25 mA)
- Differential High Impedance i, q Inputs
- On-Chip Linear RC Phase Shifter
- -23 dBm Modulator S.E. Output Power into 50 Ω at 150 MHz
- -15 dBm Linear (-11 dBm Saturated) Mixer Output Power into 50 Ω at 1900 MHz
- Mixer Can Be Used for Up/Down Conversion or Disabled (3 V, 10 mA)
- Standby Mode (<1 μA)
- JEDEC Standard SSOP-16 Surface Mount Package

Package Pin Configuration



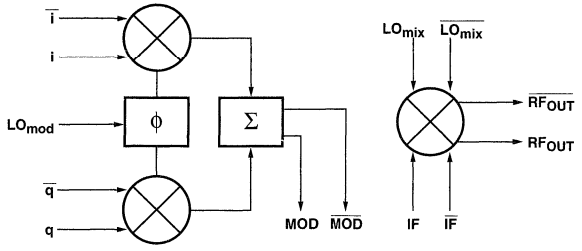
Plastic SSOP-16



Applications

- NADC, PDC, GSM Handsets and Base Stations
- PCS Handsets and Base Stations
- DLMR Handsets
- CDPD Radios
- ISM Band Wireless Links

Functional Block Diagram



General Description

The HPMX-2007 vector modulator/mixer IC is designed to meet the needs of cellular and PCS telephone applications.

The heart of the IC is a vector (or quadrature) modulator followed by a Gilbert cell mixer. The modulator and mixer can be used together, drawing only 25 mA from a 3.0 volt supply. The mixer can be disabled by connecting either LOmix or $\overline{LOmix}$ to V_{CC},

allowing operation of the modulator alone and reducing current drain to only 10 mA.

The i and q signal inputs are balanced to insure high common mode noise rejection.

The output of the mixer is a differential pair of open collectors. One collector can be connected to V_{CC} and the other matched to 50 Ω using a shunt L, series C network. Alternatively, the output can be matched to 50 Ω through a 4:1 balun.

The SSOP-16 package insures that the IC occupies a minimal amount of printed circuit board space.

The HPMX-2007 is manufactured using Hewlett-Packard's 30 GHz ISOSAT-II process which combines stepper lithography, self alignment, ion implantation techniques and gold metallization to produce state-of-the-art RFICs.

HPMX-2007 Absolute Maximum Ratings[1]

Recommended Operating Range of V_{CC} = 2.7 to 5.5 V, T_A = -40 to +85°C.

Parameter	Min.	Max.
V_{CC} Supply Voltage		8 V
Power Dissipation[2,3]		400 mW
RF Input Power		+15 dBm
Junction Temperature		+150°C
Storage Temperature	-65°C	+150°C

Thermal Resistance:[2]
θ_{jc} = 150°C/W

Notes:
1. Operation of this device in excess of any of these parameters may cause permanent damage.
2. T_{case} = 25°C.
3. Derate at 7 mW/°C for T_{case} > 90°C.

Standard Test Conditions

Unless otherwise stated, all test data was taken on packaged parts under the following conditions:

V_{CC} = +3.0 VDC, Z_{out} = 50 Ω, ambient temperature T_A = 25°C
LOmod input: 149.67 MHz, 400 mV_{p-p}, single ended
LOmix input: 1750.33 MHz, -10 dBm, single ended, 50 Ω
Single sideband tests:
i, q input: 10 kHz, 600 mV_{p-p} differential with $V_{CC}/2$ = 1.5 V offset.
See Figure 25 for test setup schematic diagram.

HPMX-2007 Key Guaranteed Electrical Specifications

Standard test conditions apply unless otherwise noted.

Symbol	Parameters and Test Conditions	Min.	Typ.	Max.	Units
P_{out}	SSB Output Power	-17.5	-15		dBm
	Unwanted Sideband Output Level in SSB Mode		-40	-30	dBc
	LOmix + LOmod Leakage Relative to SSB Output Power		-35	-27	dBc
I_d	Device Current ($\overline{ENABLE}$ Open)		25	30	mA
	Device Current, Disabled Mode ($\overline{ENABLE}$ = V_{CC})		5	25	µA

HPMX-2007 Summary Characterization Information

Standard test conditions apply unless otherwise noted.

Modulator-Only Mode	Typ	Units
DC Current Drain	10	mA
i, q Input 3 dB Bandwidth	>90	MHz
LOmod Input Frequency Range (for Sideband Suppression > 30 dBc)	40-400	MHz
SSB Output Current (Open Collectors). See Figure 26.	2	mA pk-pk diff.
SSB LOmod Suppression @ 150 MHz	-35	dBc
DSB 3rd Order IM Products @ 150 MHz	-45	dBc
Output Noise Floor	-160	dBm/Hz

Modulator + Mixer Performance (Output at 1900 MHz)	Typ	Units
Total DC Current Drain (Mixer Cannot Be Used Without Also Turning On the Modulator)	25	mA
Mixer IF Input 3 dB Bandwidth	400	MHz
Differential Output Current (Open Collectors). See Figure 26.	12	mA pk-pk diff.
Linear Output Power. See Figure 25.	-15	dBm
IM_3 Output Power. See Figure 19.	-22	dBc
Output Noise Floor	-153	dBm/Hz
LOmix Leakage to RF Output	-22	dBc

HPMX-2007 Pin Description Table

No.	Mnemonic	Description	Typical Signal
1	i	Balanced modulation input Z = 75 kΩ ‖ 0.5 pF	600 mV pk-pk differential average value of $V_{CC}/2$
2	$\overline{i}$		
3	LOmod	Modulator LO input Z = 5 kΩ ‖ 0.5 pF	40-400 MHz, -10 dBm from 50 Ω source
4	RF	Balanced mixer RF output open collectors Z = current src. ‖ 3 kΩ ‖ 0.7 pF	5-4000 MHz, 12 mA pk-pk differential, with network shown in Figure 25
5	$\overline{RF}$		
6	$\overline{IF}$	Balanced mixer input Z = 5 kΩ ‖ 0.5 pF	40-400 MHz, 350 mV pk-pk diff.
7	IF		
8	$\overline{ENABLE}$	Chip enable input	3 V CMOS logic compatible
9	LOmix/mixoff	Balanced mixer LO input and mixer enable line Z = 1 kΩ ‖ 0.6 pF	-10 dBm from 50 Ω source network shown in Figure 25
10	$\overline{LO1}$		
11	V_{EE}	Chip substrate connection	0 V (DC and AC ground)
12	V_{CC}	Power supply connection	+2.7 - 5.5 V
13	MOD	Balanced modulator RF output open collectors Z = current src. ‖ 35 kΩ ‖ 0.7 pF	40-400 MHz, 2 mA pk-pk differential with network shown in Figure 25
14	$\overline{MOD}$		
15	$\overline{q}$	Balanced modulation input Z = 75 kΩ ‖ 0.5 pF	600 mV pk-pk differential average value of $V_{CC}/2$
16	q		

Note: Impedances shown are AC equivalents at each pin, relative to ground. See Figure 26.

Table 1. Typical Output Spurs.

All values in dBc relative to output at 1900 MHz. f_{LOmix} = 1750.33 MHz, f_{LOmod} = 149.67 MHz, $V_i = V_q$ = 1.65 V, $V_{\bar{i}} = V_{\bar{q}}$ = 1.35 V, $f_{spur} = m*f_{LOmix}+n*f_{LOmod}$

m↓ n→	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6
0	-38.8	-53.4	-47.7	-60.1	-46.7	-72.3	-	-72.2	-46.7	-60.1	-47.6	-53.3	-38.8
1	-51.9	-37.3	-37.7	-23.9	-23.6	0	-21.4	0	-22.1	-17.7	-41.7	-28.7	-35.1
2	-26.6	-32.8	-23.7	-36.3	-16.5	-34.5	-19.5	-21.3	-26.3	-36.8	-29.5	-48.8	-40.6
3	-37.8	-32.7	-57.4	-28.3	-25.9	-21.2	-27.5	-23.8	-38.7	-45.9	-54.3	-41.2	-48.8
4	-45.7	-47.1	-45.3	-47.0	-39.4	-51.1	-43.3	-40.4	-49.7	-54.7	-49.8	-57.8	-57.2
5	-65.0	-67.5	-56.1	-61.7	-57.6	-52.0	-43.5	-54.8	-61.6	-65.4	-59.9	-64.7	-63.7
6	-65.5	-82.2	-65.9	-60.7	-57.4	-62.7	-57.5	-66.2	-64.9	-77.1	-72.0	-83.1	-86.3

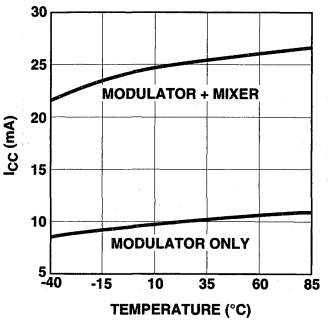


Figure 1. I_{CC} vs. Temperature.

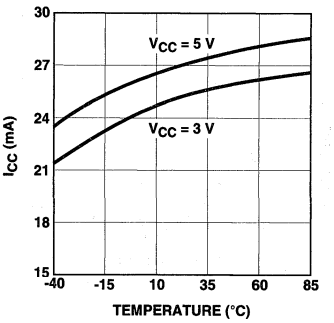


Figure 2. Modulator + Mixer I_{CC} vs. Temperature and V_{CC}.

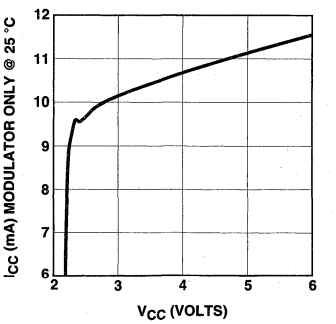


Figure 3. Modulator Only Mode I_{CC} vs. V_{CC} at 25°C.

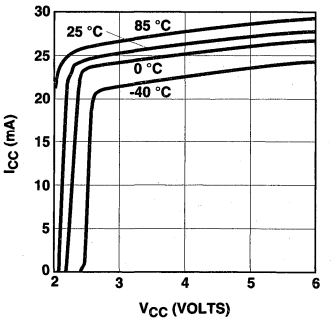


Figure 4. Modulator + Mixer I_{CC} vs. V_{CC} and Temperature.

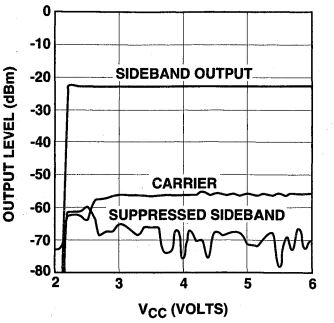


Figure 5. Modulator Only SSB Performance vs. V_{CC}.

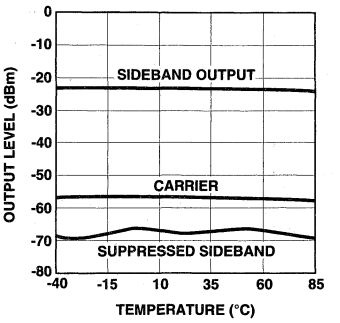


Figure 6. Modulator Only SSB Performance vs. Temperature.

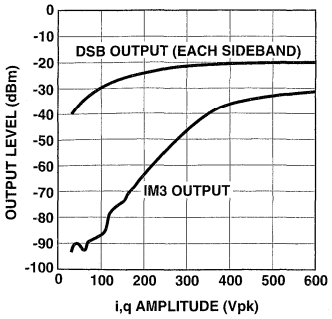


Figure 7. Modulator Only DSB Output Power Level and IM3 Level vs. i,q Input Amplitude (Each Pin, Relative to Ground).

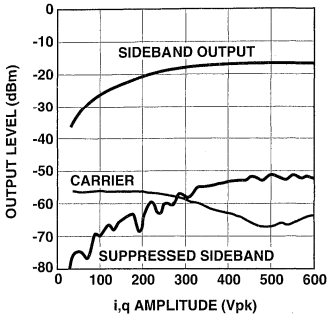


Figure 8. Modulator Only SSB Mode Performance vs. i,q Input Amplitude (Each Pin, Relative to Ground).

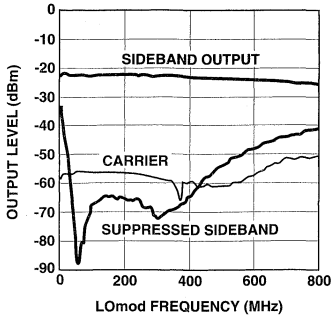


Figure 9. Modulator Only SSB Output Power, Carrier and Sideband Suppression vs. LOmod Frequency.

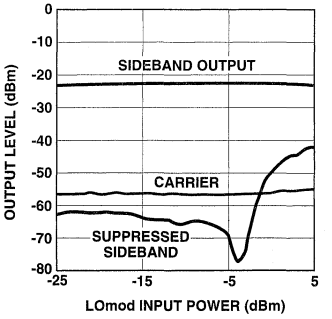


Figure 10. Modulator Only SSB Performance vs. LOmod Input Level.

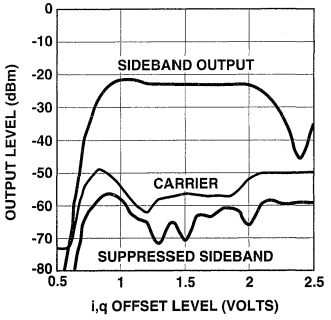


Figure 11. Modulator Only SSB Performance vs. i,q Offset Level (Each Pin, Relative to Ground).

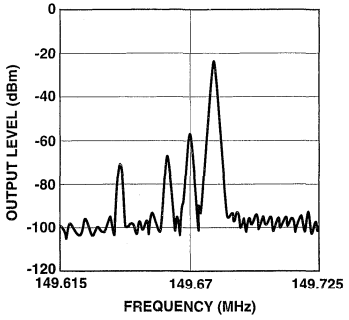


Figure 12. Modulator Only SSB Output Spectrum at 150 MHz.

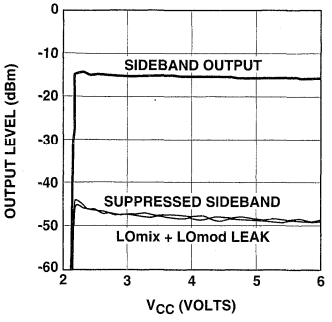


Figure 13. Modulator + Mixer SSB Output Levels vs. V_{CC}.

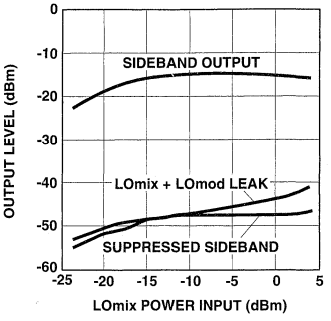


Figure 14. Modulator + Mixer SSB Output Levels vs. LOmix Power Input.

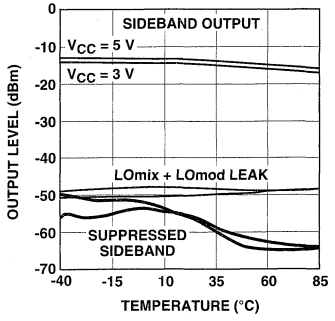


Figure 15. Modulator + Mixer SSB Output Levels vs. Temperature and V_{CC}.

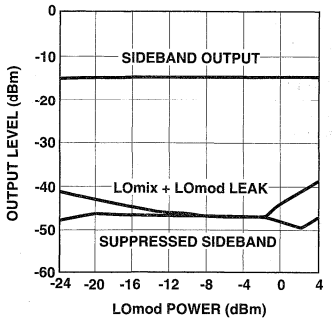


Figure 16. Modulator + Mixer SSB Output Levels vs. LOmod Power Input.

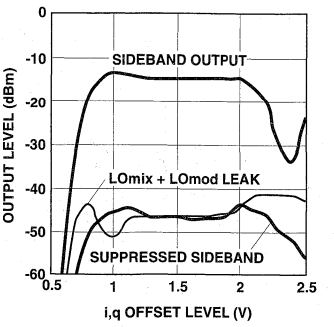


Figure 17. Modulator + Mixer SSB Performance vs. i,q Offset Level (Each Pin, Referenced to Ground).

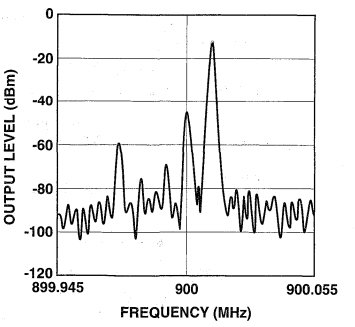


Figure 18. Modulator + Mixer SSB Output Spectrum at 900 MHz.

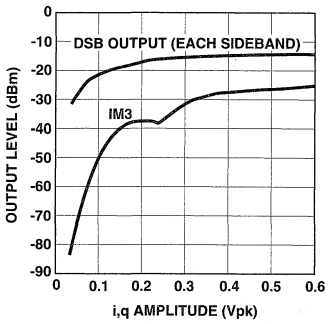


Figure 19. Modulator + Mixer DSB Performance vs. i,q Amplitude (Each Pin, Referenced to Ground).

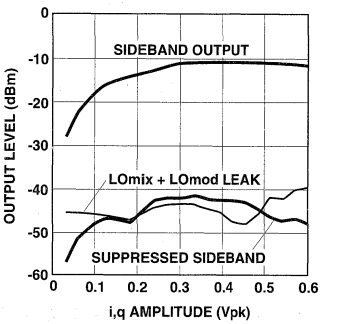


Figure 20. Modulator + Mixer SSB Performance vs. i,q Input Amplitude (Each Pin, Referenced to Ground).

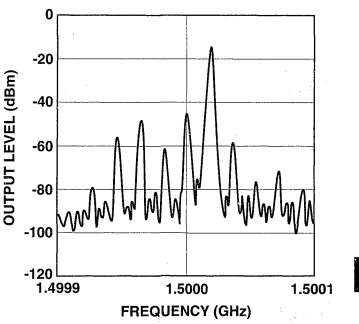


Figure 21. Modulator + Mixer SSB Output Spectrum at 1500 MHz.

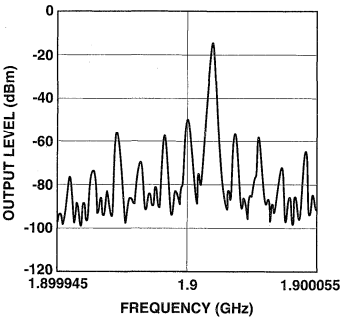


Figure 22. Modulator + Mixer SSB Output Spectrum at 1900 MHz.

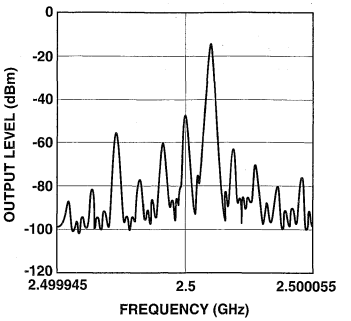


Figure 23. Modulator + Mixer SSB Output Spectrum at 2500 MHz.

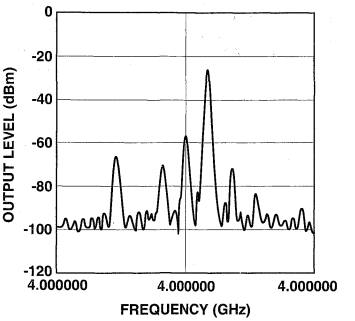


Figure 24. Modulator + Mixer SSB Output Spectrum at 4000 MHz.

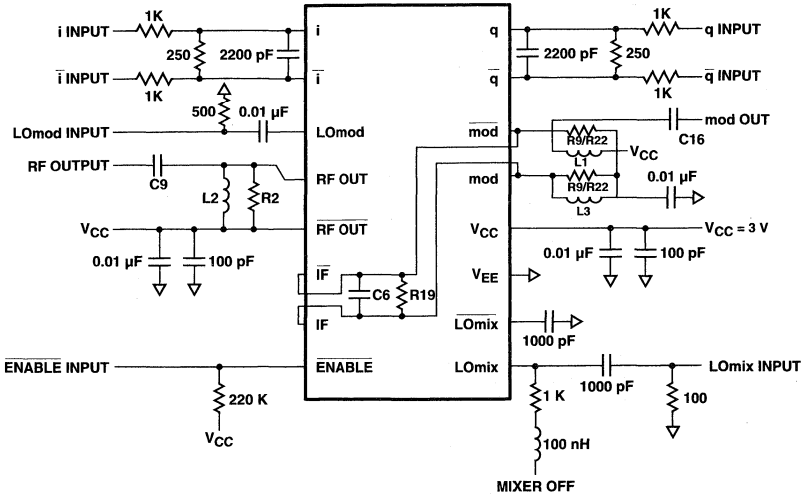


Figure 25. Test Board Schematic Diagram. Connecting the Mixer Off Line to +3 V Turns Off the Mixer. Leave It Open to Allow Mixer to Operate. Component Values that Change with Frequency Are Shown in Table 2.

Table 2. Test Board Component Values that Change with Operating Frequency.

Refer to Figure 25.

$f_{LOmix}+f_{LOmod}$ MHz	f_{LOmix} MHz	f_{LOmod} MHz	R9/R22 Ω	L3 nH	L1 nH	R19 Ω	C6 pF	C16 nF	R2 Ω	L2 nH	C9 pF
900	750.33	149.67	-	100	100	430	3.9		200	12	3.3
1500	1350.33	149.67	-	100	100	300	3.9		120	5.6	1.8
1900	1750.33	149.67	-	100	100	430	3.9		120	3.3	1.2
2500	2350.33	149.67	-	100	100	430	3.9		75	-	-
mod. only	-	149.67	300	0	-	-	-	10	-	-	-

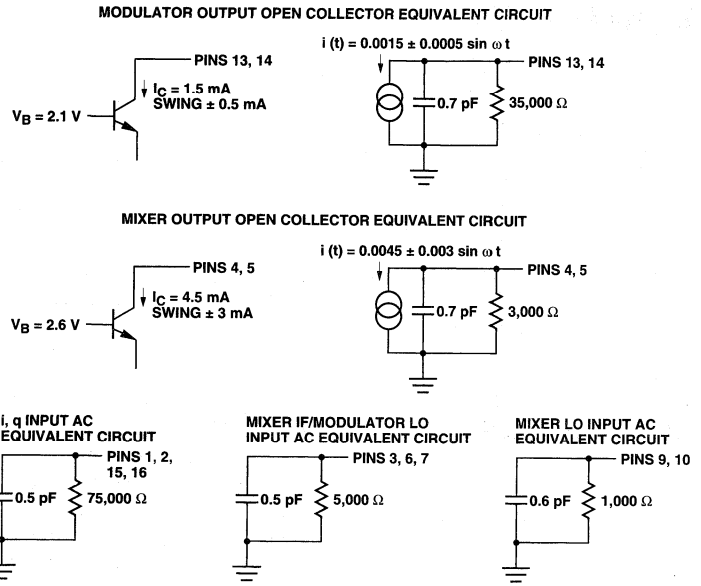


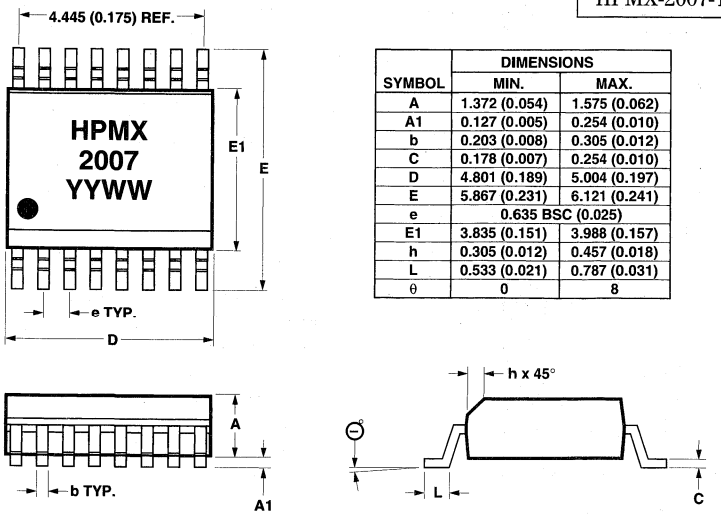
Figure 26. Equivalent Circuits for HPMX-2007 Inputs/Outputs.

Part Number Ordering Information

Part Number	No. of Devices	Container
HPMX-2007-BLK	25	Tape
HPMX-2007-TR1	1000	Tape and Reel

Package Dimensions

JEDEC Standard SSOP-16 Package



SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	1.372 (0.054)	1.575 (0.062)
A1	0.127 (0.005)	0.254 (0.010)
b	0.203 (0.008)	0.305 (0.012)
C	0.178 (0.007)	0.254 (0.010)
D	4.801 (0.189)	5.004 (0.197)
E	5.867 (0.231)	6.121 (0.241)
e	0.635 BSC (0.025)	
E1	3.835 (0.151)	3.988 (0.157)
h	0.305 (0.012)	0.457 (0.018)
L	0.533 (0.021)	0.787 (0.031)
θ	0	8

DIMENSIONS IN MILLIMTERS AND (INCHES).

HEWLETT® PACKARD

1.5 – 2.5 GHz LNA Switch PA

Technical Data

HPMX-3003

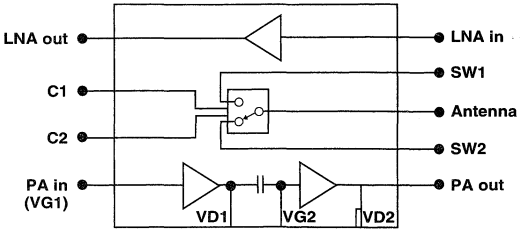
Features

- **GaAs MMIC LNA-Switch-Power Amp for 1.5 – 2.5 GHz Transceiver Use**
- **LNA: 2.2 dB NF, 13 dB G_a @ 1.9 GHz**
- **Switch: 55 dBm OIP @ 1.9 GHz**
- **Power Amp: +4 dBm in, +27.5 dBm out, 23.5 dB Gain, 35% η_{add} @ 1.9 GHz**
- **3 or 5 V Operation**
- **JEDEC Standard SSOP-28 Surface Mount Package**

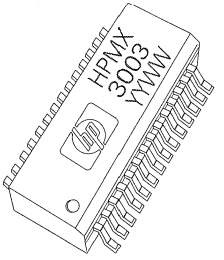
Applications

- **Personal Communications Systems (PCS)**
- **Cordless Telephone Systems**
- **2400 MHz Wireless LANs and ISM Band Spread Spectrum Applications**

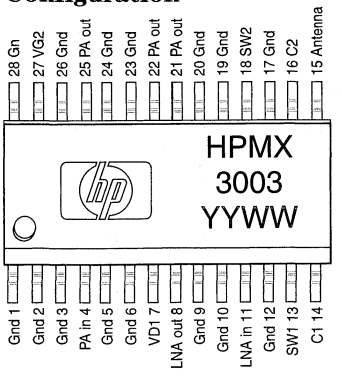
Functional Block Diagram



Plastic SSOP-28



Package Pin Configuration



Description

Hewlett-Packard's HPMX-3003 combines a Low Noise Amplifier, GaAs MMIC switch, and 27.5 dBm power amp in a single miniature 28 lead surface mount plastic package. This RFIC would typically serve as the "front end" and power stage of a battery operated wireless transceiver for PCS or ISM band use. Each section of the RFIC can also be used independently.

The single-supply LNA makes use of the low noise characteristics of GaAs to create a matched, broad-band amplifier with target performance of 13 dB gain and 2.2 dB noise figure. The switch provides +55 dBm IP3 for linear operation. The power amplifier produces up to 820 mW with 35% power added efficiency.

The HPMX-3003 is fabricated with Hewlett-Packard's GaAs MMIC process, and features a nominal 0.5 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to produce MMICs with superior performance, uniformity and reliability.

HPMX-3003 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum[1] LNA	Absolute Maximum[1] Switch	Absolute Maximum[1] Power Amp
P_{diss}	Power Dissipation[2,3]	mW	250[2,3]		1500[2,3]
P_{in}	CW RF Input Power	dBm	+20	+33	+20
V_d	Device Voltage	V	8	—	8
V_{cont}	Control Voltage	V	—	-6	—
T_{ch}	Channel Temperature	°C	175	175	175
T_{STG}	Storage Temperature	°C	-65 to 150	-65 to 150	-65 to 150

Notes:

1. Operation of this device above any of these limits may cause permanent damage.
2. T_{case} = 25°C
3. Derate at 18.2 mW/°C for T_C > 78°C

Thermal Resistance[2]:
θ_{jc} = 55°C/W

Recommended operating range of V_{cc} = 2.7 to 5.5 V, T_a = -40 to + 85 °C

HPMX-3003 Standard Test Conditions

Unless otherwise stated, all test data was taken on packaged parts under the following conditions:

T_a= 25 °C, Z_o = 50 Ω

V_{cc} = +3.0 V DC, $V_{control}$ = -3.0 V DC, V_{D1} = +3.6 V DC

LNA P_{in} = -20 dBm, PA P_{in} = +4 dBm, frequency = 1.9 GHz

Perfomance cited is performance in test circuit shown in Figure 17.

HPMX-3003 Guaranteed Electrical Specifications

Standard test conditions apply unless otherwise noted.

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
G_{test}	LNA gain through switch	dB	9.0	11	
P_{out}	Output power through switch	dBm	24.0	25.5	
I_d LNA	LNA bias current	mA		6.5	9.5

HPMX-3003 Summary Characterization Information

Standard test conditions apply unless otherwise noted. All information tested in 1900 MHz Test Circuit, and reflects performance of test circuit at 1900 MHz.

Symbol	Parameters and Test Conditions		Units	Typ
LNA				
NF	Noise Figure		dB	2.2
$\|S_{21}\|^2$	50 Ω Gain		dB	13
IRL	Input Return Loss		dB	15
ORL	Output Return Loss			12
IIP_3	Input Third Order Intercept		dBm	-1
Switch				
P_{1dB}	Output Power where insertion loss is increased by 1 dB	ΔC1 to C2 = 3 V	dBm	+23
P_{1dB}	Output Power where insertion loss is increased by 1 dB[1]	ΔC1 to C2 = 5 V	dBm	+29
IP_3	Third Order Intercept		dBm	+55
S_{21} on	Insertion Loss, on channel		dB	0.8
S_{21} off	Isolation, off channel		dB	15
IRL_{on}	Return Loss, on channel		dB	26
IRL_{off}	Return Loss, off channel		dB	0.5
Power amp (Vg = -.8 V required)				
GP	Gain	V_{D1} = 3.6 V, P_{in} = +4 dBm	dB	23.5
η_{PAadd}	Power Added Efficiency	V_{D1} = 3.6 V	%	35
P_{out}	Output Power	V_{D1} = 3.6 V, P_{in} = +4 dBm	dBm	+27.5
I_d PA	Transmit Current	V_{D1} = 3.6 V, P_{in} = +4 dBm	mA	450

Note:

1. The P_{1dB} of the switch can be improved by increasing the difference between the values of C1 and C2 from the normal 3 V (+23 dB P_{1dB}) to 5 V (+29 dB P_{1dB}).

HPMX-3003 Pin Description

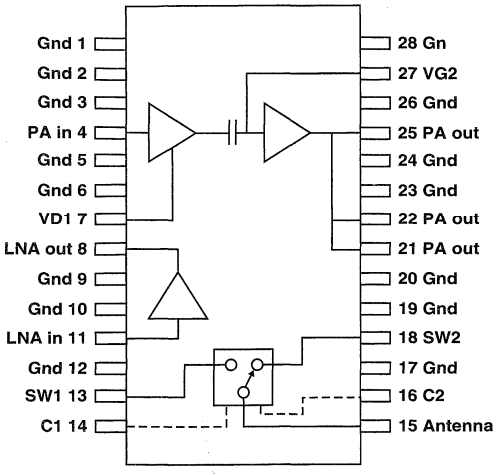


Figure 1. HPMX-3003 Pin Outs and Schematic.

HPMX-3003 Pin Description Table

No.	Mnemonic	Description	Typical Signal	Description
1 2 3	Gnd Gnd Gnd	ground ground ground	0 V 0 V 0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
4	PA_{in}	input to Power Amplifier	DC: -0.75 V RF: +4 dBm	Bias through 500 Ω resistor and 100 pF capacitor. 50 Ω transmission line with DC blocking capacitor (>24 pF) to input. Shunt 2.7 pF used on test board to match input at 1.9 GHz.
5 6	Gnd Gnd	ground ground	0 V 0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
7	VD1	Drain bias of PA stage 1	+3 V, 100 mA	Set drain bias to 3 V (can be tied to same rail as PA out). Bypass with 100 pF capacitor at pin.
8	LNA out	output of LNA	DC: +3 V, 5 mA RF: -7 dBm	Bias through 5 nH choke (printed on PC board) and 100 pF bypass capacitor to 10 Ω resistor and 1000 pF bypass capacitor. Can be operated from 3 to 5 V supply line. 50 Ω transmission line with DC block (>24 pF) to receiver.
9 10	Gnd Gnd	ground ground	0 V 0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
11	LNA in	input of LNA	DC: 0 V RF: -20 dBm	50 Ω transmission line from switch. Input blocking capacitor (24 pF) and shunt 5 nH inductor to ground (noise match at 1.9 GHz) required. Typically a filter is employed between the LNA input and the switch.
12	Gnd	ground	0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
13	SW1	switch terminal 1	DC: 0 V RF: -20 dBm	Switch input or output. Symmetrical with SW2. 50 Ω transmission line to LNA (or PA). Line should not carry DC voltage.
14	C1	switch control 1	closed: 0 V open: -3 to -5 V	High impedance line to control switch, used in conjunction with C2. C2 should be open when C1 is closed.
15	Antenna	switch center pole	DC: 0 V RF: +26 dBm	50 Ω transmisson line to/from antenna. Line should not carry DC voltage.
16	C2	switch control 2	closed: 0 V open: -3 to -5 V	High impedance line to control switch, used in conjunction with C1. C1 should be open when C2 is closed.
17	Gnd	ground	0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
18	SW2	switch terminal 2	DC: 0 V RF: +4 dBm	Switch input or output. Symmetrical with SW1. 50 Ω transmission line to PA (or LNA). Line should not carry DC voltage.
19 20	Gnd Gnd	ground ground	0 V 0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
21 22	PA out PA out	output of PA output of PA	DC: 3 V, 350 mA RF: +27 dBm	2.7 pF chip capacitor to ground provides 1.9 GHz output match for PA. 50 Ω transmission line to switch. LC choke and blocking C used. Typically a filter is employed between the PA output and the switch input.
23 24	Gnd Gnd	ground ground	0 V 0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
25	PA out	output of PA	DC: 3 V, 350 mA RF: +27 dBm	Leave unconnected; use pins 21 & 22 for PA out.
26	Gnd	ground	0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
27	VG2	Gate bias on PA stage 2	-0.75 V	Provide bias through 10 Ω resistor. Bypass to ground at pin with 10 pF capacitor, and on power supply side of resistor with 1000 pF capacitor.
28	Gnd	ground	0V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.

HPMX-3003 Typical Performance

Standard test conditions apply unless otherwise noted. 2.4 GHz performance is performance in test circuit shown in Figure 18. Some aspects of performance are determined by the test circuit impedances.

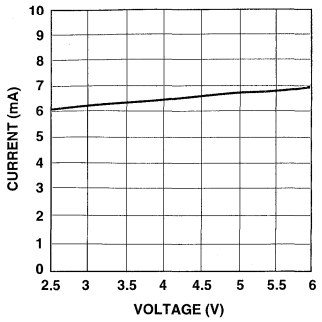


Figure 2. LNA Current vs. Device Voltage at 1900 MHz.

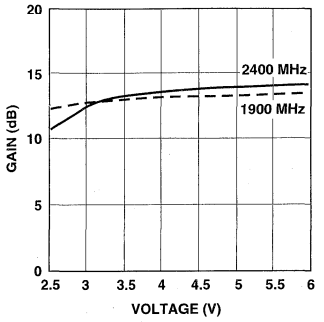


Figure 3. LNA Gain vs. Device Voltage and Frequency.

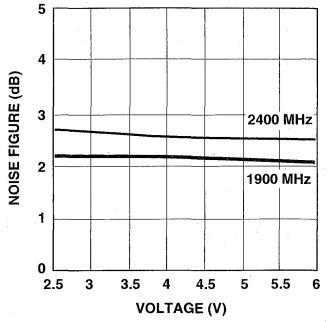


Figure 4. LNA Noise Figure vs. Device Voltage and Frequency.

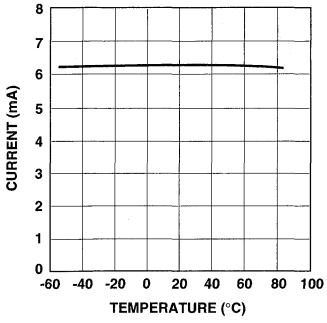


Figure 5. LNA Current vs. Temperature at 1900 MHz.

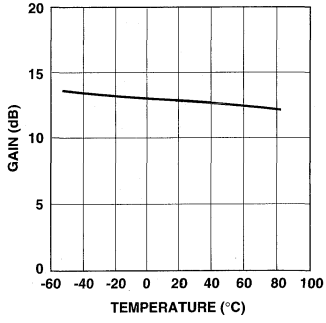


Figure 6. LNA Gain vs. Temperature at 1900 MHz.

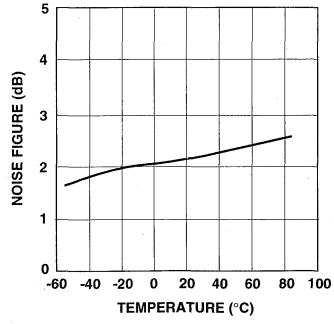


Figure 7. LNA Noise Figure vs. Temperature at 1900 MHz.

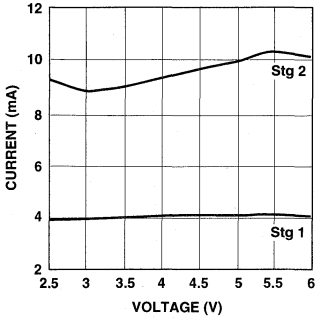


Figure 8. PA Current vs. Device Voltage at 1900 MHz.

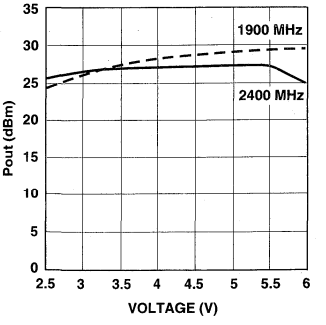


Figure 9. PA Output Power vs. Supply Voltage and Frequency.

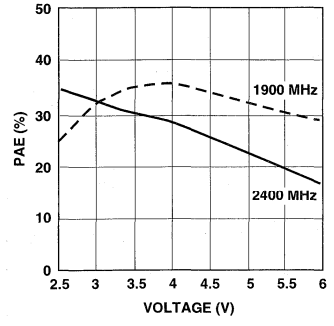


Figure 10. PA Power Added Efficiency vs. Supply Voltage and Frequency.

HPMX-3003 Typical Performance, continued

Standard test conditions apply unless otherwise noted. 2.4 GHz performance is performance in test circuit shown in Figure 18. Some aspects of performance are determined by the test circuit impedances.

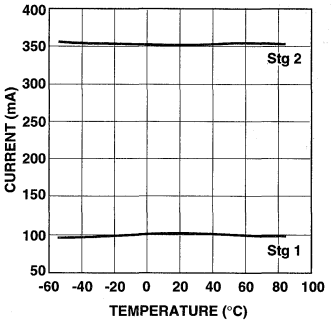


Figure 11. PA Current vs. Temperature at 1900 MHz and VD1 = 3.6V.

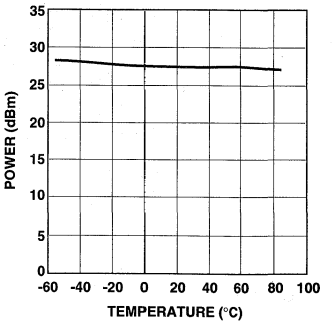


Figure 12. PA Output Power vs. Temperature at 1900 MHz and VD1 = 3.6V.

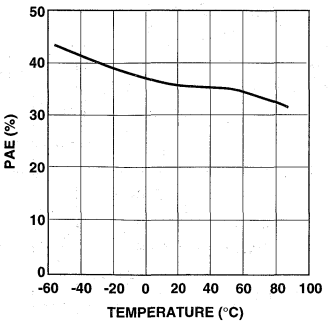


Figure 13. PA Power Added Efficiency vs. Temperature at 1900 MHz and VD1 = 3.6V.

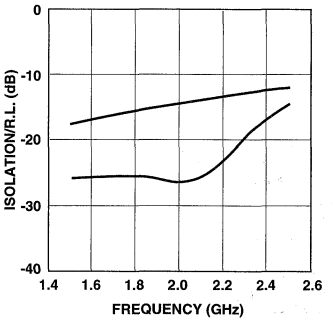


Figure 14. Switch Isolation and "ON" State Return Loss vs. Frequency.

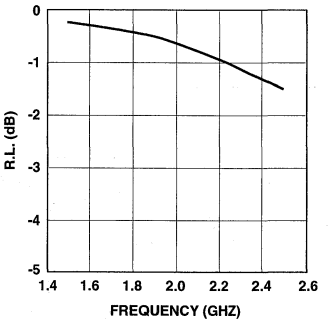


Figure 15. Switch "OFF" State Return Loss vs. Frequency.

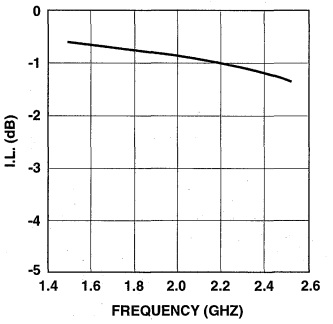


Figure 16. Switch "ON" State Insertion Loss vs. Frequency.

HPMX-3003 Typical Scattering Parameters for the LNA,

Common Source, Z_O = 50 Ω, V_D = 3 V, I_D = 5 mA

Frequency	S_{11}		S_{21}		S_{12}		S_{22}	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
1.0	0.97	-27	2.00	158	0.035	-12	0.91	-22
1.2	0.96	-33	2.06	150	0.036	-17	0.91	-27
1.4	0.95	-40	2.13	142	0.037	-23	0.90	-31
1.6	0.94	-47	2.20	134	0.038	-30	0.88	-36
1.8	0.92	-54	2.28	125	0.038	-39	0.87	-41
2.0	0.90	-62	2.36	117	0.039	-49	0.86	-46
2.2	0.88	-70	2.45	109	0.039	-62	0.84	-50
2.4	0.85	-79	2.54	100	0.040	-77	0.83	-55
2.6	0.82	-89	2.63	90	0.042	-95	0.81	-60
2.8	0.78	-99	2.71	81	0.045	-115	0.79	-65
3.0	0.75	-110	2.79	71	0.050	-135	0.78	-71

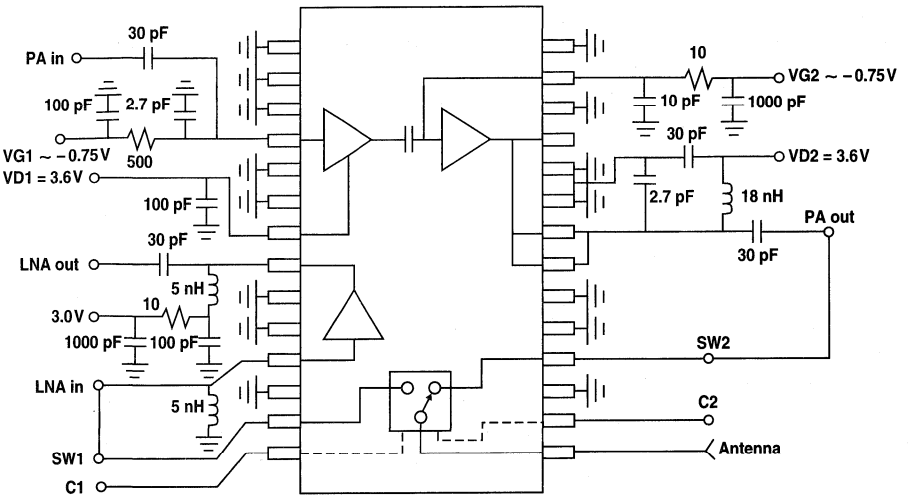


Figure 17. HPMX-3003 Test Circuit (1900 MHz).

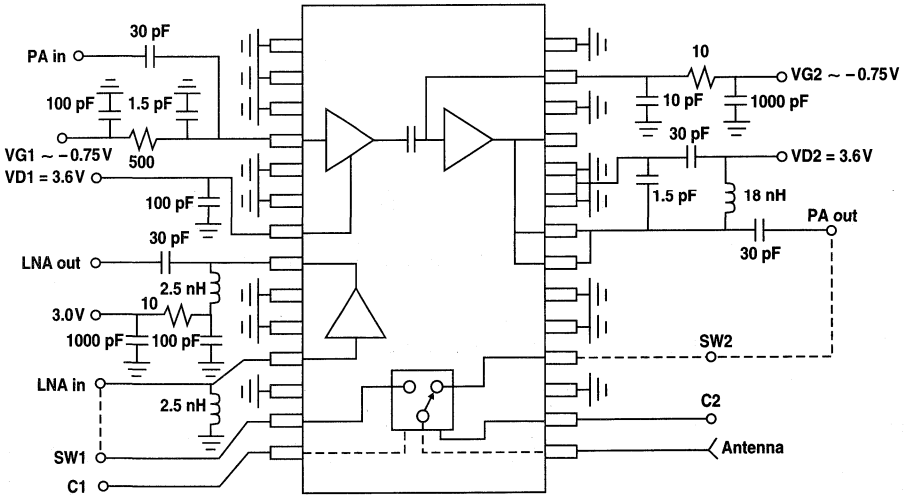
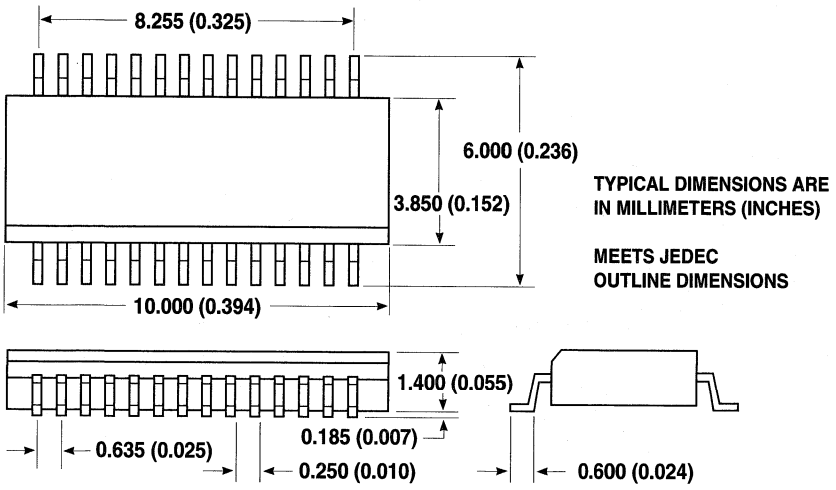


Figure 18. HPMX-3003 Test Circuit (2400 MHz).

JEDEC Standard SSOP-28 Package Outline Drawing



Part Number Ordering Information

Part Number	No. of Devices	Container
HPMX-3003-TR1	1000	Tape and Reel
HPMX-3003-BLK	25	Tape

HEWLETT® PACKARD

1.5–2.5 GHz Upconverter/ Downconverter

Technical Data

HPMX-5001

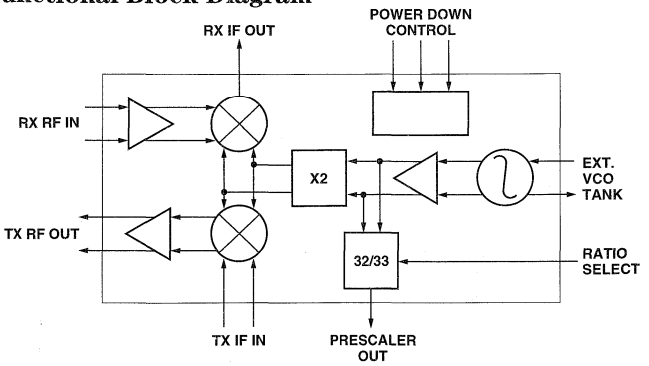
Features

- 2.7 V Single Supply Voltage
- Low Power Consumption (60 mA in Transmit Mode, 39 mA in Receive Mode Typical)
- 2 dBm Typical Transmit Power at 1900 MHz
- Half-Frequency VCO with Frequency Doubler
- 32/33 Dual-Modulus Prescaler
- Flexible Chip Biasing, Including Standby Mode
- TQFP-32 Surface Mount Package
- Operation to 2.5 GHz
- Use with Companion HPMX-5002 IF chip

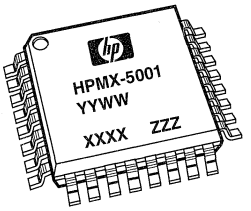
Applications

- DECT, UPCS and ISM Band Handsets and Basestations

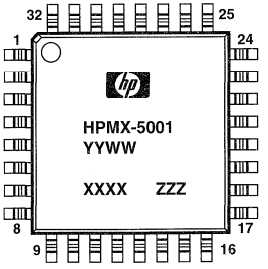
Functional Block Diagram



Plastic TQFP-32 Package



Pin Configuration



General Description

The HPMX-5001 Upconverter/ Downconverter provides RF system designers with all of the necessary features to perform an RF-to-IF downconversion for a receive path, as well as an IF-to-RF upconversion for transmit mode.

Designed to meet the unique needs of portable applications, the HPMX-5001 combines the qualities of flexible chip biasing, low power consumption, and true 2.7 V minimum supply voltage operation to provide superior performance and battery life. By incorporating the active elements of the VCO on-chip, as well as a 32/33 dual-modulus prescaler, overall system component count and costs are decreased. The 32-TQFP package insures that this high level of integration occupies a small amount of printed circuit board space.

The HPMX-5001 can be used in either dual-conversion systems (with the HPMX-5002 IF Demodulator/Modulator) or single-conversion systems. The HPMX-5001 is manufactured using Hewlett-Packard's HP-25 Silicon Bipolar Process with 25 GHz f_T and 30 GHz f_{Max}.

HPMX-5001 Absolute Maximum Ratings[1]

Parameter	Min.	Max.
V_{CC} Supply Voltage	-0.2 V	8 V
Voltage at Any Pin[4]	-0.2 V	V_{CC} + 0.2 V
Power Dissipation[2,3]		600 mW
RF Input Power		15 dBm
Junction Temperature		+150°C
Storage Temperature	-55°C	+125°C

Thermal Resistance[2]:
θ_{jc} = 100°C/W

Notes:
1. Operation of this device in excess of any of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 10 mW/°C for T_{CASE} > 90°C.
4. Except CMOS logic inputs–see Summary Characterization Information table.

HPMX-5001 Guaranteed Electrical Specifications

Unless otherwise noted, all parameters are guaranteed under the following conditions: V_{CC} = 3.0 V. Test results are based upon use of networks shown in test board schematic diagram (see Figure 28). Typical values are for V_{CC} = 3.0 V, T_A = 25° C.

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
G_C	Receive Conversion Gain[1]	dB	12	14	
P_{out}	Transmitter Power Output Input[2]				
	2:1 output VSWR	dBm	0	2	
I_{CC}	Device Supply Current Transmit Mode	mA		64	80
	Receive Mode	mA		43	54
	Synth Mode	mA		15	19
	Standby Mode (with DIVMC Set High)	µA		1	50
V_{DIV}	DIV Single-Ended Swing[3]	V_{PP}	0.7	1	

Notes:
1. 50 Ω RF source, 100 MHz < I_F < 300 MHz, 1.89 GHz RF. There is a 750 Ω resistor on chip between RXIF and RXIFB (pins 3 and 4). A matching network from 750 Ω to 50 Ω is used for this measurement. Insertion loss of the matching network is included in the net conversion gain figure. See Figure 28.
2. Signal injected into P3 in Figure 28 is -12.5 dBm.
3. DIV output AC coupled into a 2 kΩ || 10 pF load. See test board schematic diagram, Figure 28.

HPMX-5001 Summary Characterization Information

Typical values measured on test board shown in Figure 28 at V_{CC} = 3.0 V, T_A = 25°C, RXIF = 110.592 MHz, TXRF = 1.89 GHz, unless otherwise noted.

Symbol	Parameters and Test Conditions	Units	Typical	
V_{IH}	CMOS Input High Voltage (Can Be Pulled up as High as V_{CC} + 7 V)[1]	V	≥ V_{CC} - 0.8	
V_{IL}	CMOS Input Low Voltage	V	≤ V_{CC} - 1.9	
I_{IH}	CMOS Input High Current	µA	< 10	
I_{IL}	CMOS Input Low Current	µA	> -300	
t_s	DIVMC Setup Time[2,8]	ns	4	
t_h	DIVMC Hold Time[2,8]	ns	0	
t_{pd}	DIV Propagation Delay[2,8]	ns	< 7	
	Mode Switching Time[3]	µs	< 1	
Receive Mode			1.89 GHz	2.45 GHz
Gc	Receive Conversion Gain[9]	dB	14	13.5
NF	Noise Figure[4]	dB	10	10
I_{IP3}	Input Third Order Intercept Point	dBm	-8	-9
I_{P1dB}	Input 1 dB Gain Compression Point	dBm	-18	-18
	LO Leakage (2 x f_{VCO}) at IF Port	dBm	-57	—
$VSWR_{in}$	Input VSWR[5]		1.3:1	1.3:1
Transmit Mode[6]				
PIM_3	Power Output Level for >35 dB IM_3 Suppression[10]	dBm	—	-5
O_{P1dB}	Output 1 dB Gain Compression Point	dBm	0	0
$VSWR_{out}$	Output VSWR		1.8:1	1.8:1
	LO Suppression (2 x f_{VCO})	dBc	25	30
$F_{3dB}IF$	IF 3 dB Bandwidth	MHz	500	500
	Transmitter C/N @ 2 x f_{VCO} + 4 MHz[11]	dBc/Hz	+137	+134
Synth Mode				
	1LO Frequency Range[7]	MHz	750-1200	

Notes:

1. All CMOS logic inputs are internally pulled up to logic high level.
2. See Figure 2 for detailed timing diagram.
3. Between any two different biasing modes. This switching time does not include PLL lock-up time.
4. Single sideband noise figure.
5. In modes other than receive, the VSWR may be as high as 10:1.
6. Single-ended 50 Ω RF load, 300 Ω series IF terminations (600 Ω differential), 100 MHz < IF < 300 MHz, 1.89 GHz RF.
7. The LO is followed by a frequency doubler which raises the LO range to 1500-2400 MHz.
8. DIV output AC coupled into a 2 kΩ || 10 pF load. See test diagram, Figure 28.
9. 50 Ω RF source, 110 MHz < IF < 300 MHz, 1.89 GHz or 2.45 GHz RF. There is a 750 Ω resistor on chip between RXIF and RXIFB (pins 3 and 4). A matching network from 750 Ω to 50 Ω is used for this measurement. Insertion loss of the matching network is included in the net conversion gain figure.
10. PIM_3 is the maximum SSB output power for at least 35 dB IM_3 spur suppression.
11. Measured at saturated output power for 1.89 GHz. Measured at -5 dBm SSB output power for 2.45 GHz.

Table 1 - HPMX-5001 Pin Description

No.	Mnemonic	I/O Type	Description
1	TXCTRL	CMOS I/P	Controls biasing of transmit mixer, amplifiers, and doubler
3	RXIFB	Analog O/P	Inverted single-ended downconverted receiver output, normally tied to V_{CC} (internal 750 Ω resistor connects to RXIF)
4	RXIF	Analog O/P	Single-ended downconverted receiver output, drives SAW filter (internal 750 Ω resistor connects to RXIFB)
5	TXIF	Analog I/P	Transmit non-inverting IF input
6	TXIFB	Analog I/P	Transmit inverting IF input
7	LNAREF	Analog DC I/P	Reference input for receive input amplifier
8	RXRF	Analog I/P	Receive RF input
10	TXRXVCC	DC Supply	Supply voltage for transmit path, receive front-end and mixer
11, 15	TXRXGND	Ground	Ground for transmit path, receive front-end and mixer
12	TXRFB	Analog O/P	Inverting output of transmit path (see test diagram for matching network)
14	TXRF	Analog O/P	Non-inverting output of transmit path (see test diagram for matching network)
16	DBLVCC	DC Supply	Supply voltage for LO frequency doubler
17	DBLGND	Ground	Ground for LO frequency doubler
20	VCOTNKS	Analog I/P	Sense line from external tank circuit to on-chip VCO amplifier
21	VCOTNKF	Analog O/P	Force line from on-chip VCO amplifier to external tank circuit
22	VCOVCC	DC Supply	Supply voltage for on-chip VCO amplifier
23	VCOGND	Ground	Ground for on-chip VCO amplifier
26	DIVVCC	DC Supply	Supply voltage for 32/33 dual-modulus prescaler
27	DIVGND	Ground	Ground for 32/33 dual-modulus prescaler
28	DIV	Analog O/P	Output from 32/33 dual-modulus prescaler
30	DIVMC	CMOS I/P	Modulus control signal for 32/33 dual-modulus prescaler
31	LOCTRL	CMOS I/P	Controls biasing for VCO and 32/33 dual modulus prescaler
32	RXCTRL	CMOS I/P	Controls biasing for receive mixer, amplifiers, and doubler
2, 9, 13, 18, 19, 24, 25, 29	VSUB	Ground	Substrate bias voltage

Table 2 - HPMX-5001 Mode Control

(CMOS Logic Levels - all pins internally pulled up to high level)

Mode	TXCTRL	RXCTRL	LOCTRL
Transmit	0	1	0
Receive	1	0	0
Synth	1	1	0
Standby	1	1	1

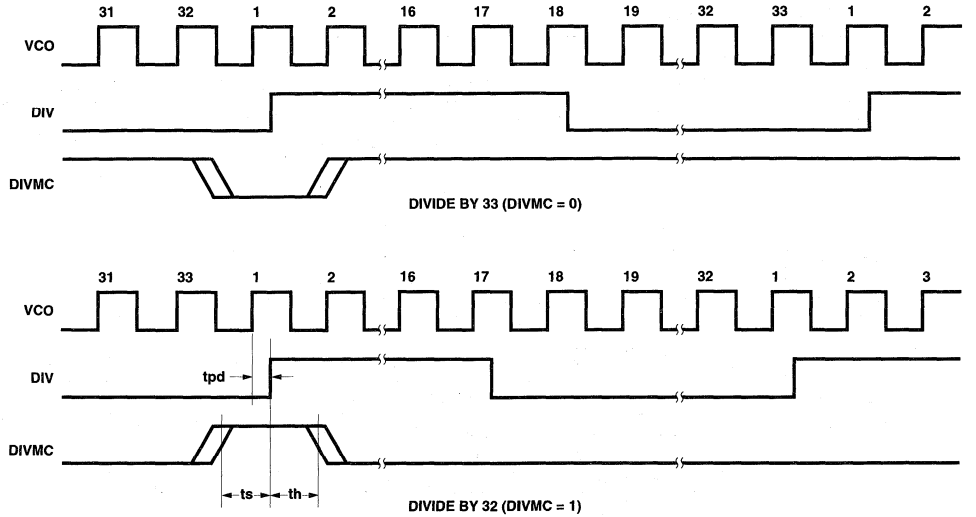


Figure 2. HPMX-5001 Prescaler Timing Diagram.

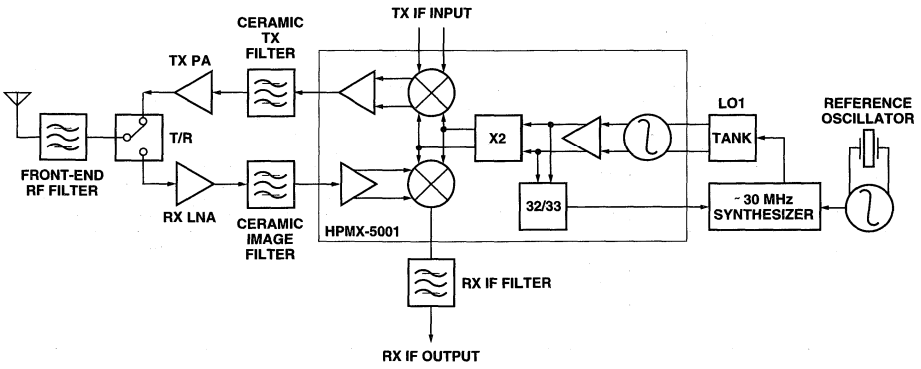


Figure 3. HPMX-5001 Block Diagram/Typical Application.

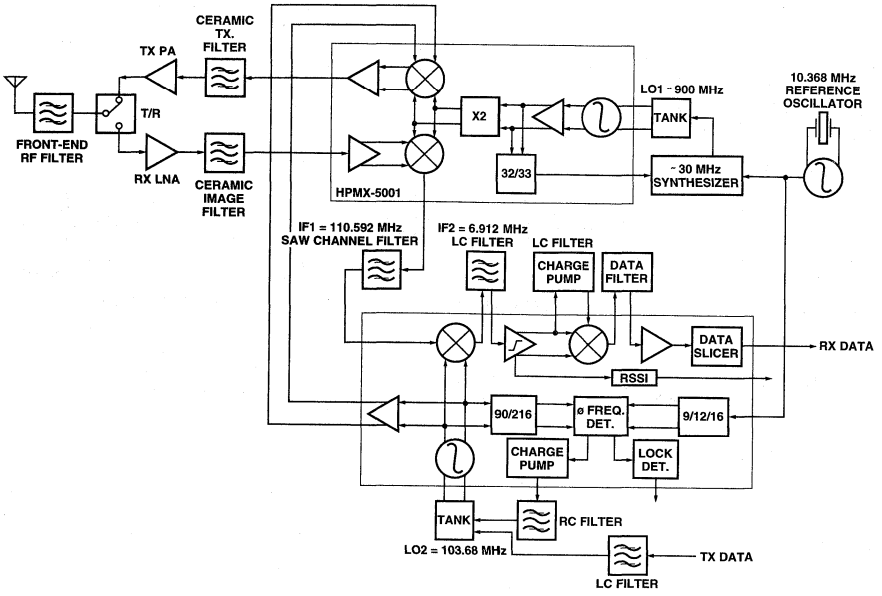


Figure 4. Typical HPMX-5001 Application with HPMX-5002 IF Chip. All Other Connections Go to Burst Mode Controller, Power Source, or Ground.

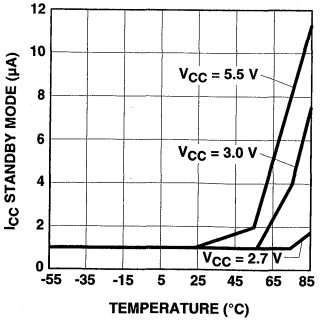


Figure 5. I_{CC} in Standby Mode vs. Temperature and V_{CC}.

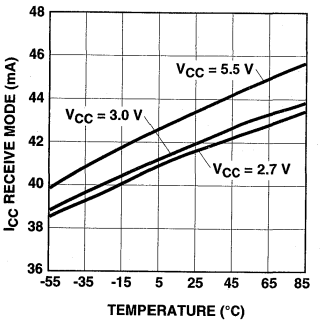


Figure 6. I_{CC} in Receive Mode vs. Temperature and V_{CC}.

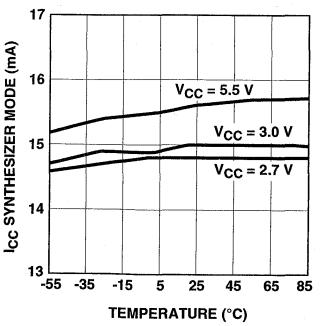


Figure 7. I_{CC} in Synthesizer Mode vs. Temperature and V_{CC}.

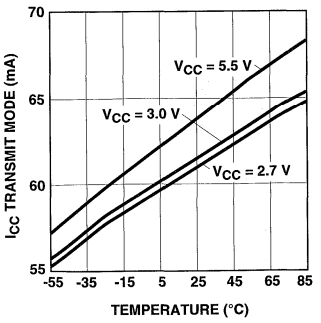


Figure 8. I_{CC} in Transmit Mode vs. Temperature and V_{CC}.

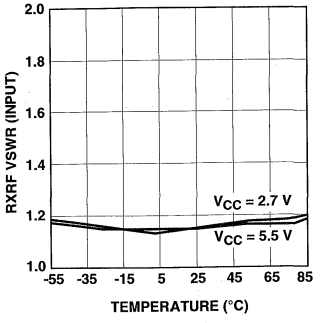


Figure 9. Receive Downconverter Input VSWR vs. Temperature and V_{CC}.

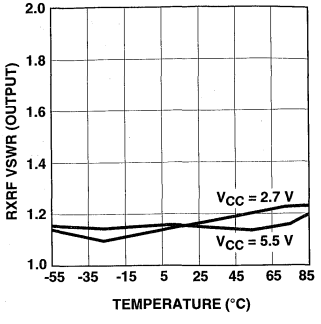


Figure 10. Receive Downconverter Output VSWR vs. Temperature and V_{CC}.

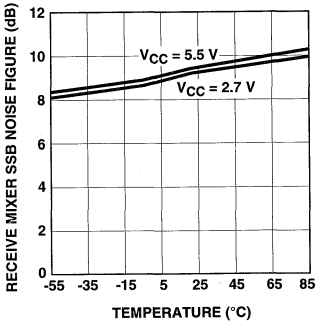


Figure 11. Receive Downconverter SSB Noise Figure vs. Temperature and V_{CC}.

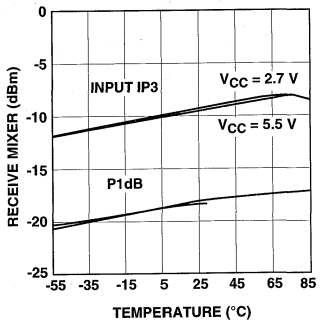


Figure 12. Receive Downconverter Input Third Order Intercept Point and Output 1 dB Compression Point vs. Temperature and V_{CC}.

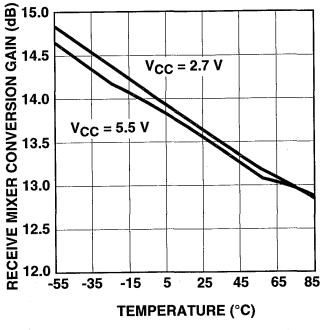


Figure 13. Receive Downconverter Conversion Gain vs. Temperature and V_{CC}.

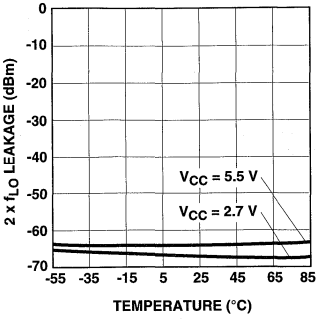


Figure 14. 2 x f_{LO} Leakage at Receive Downconverter Output vs. Temperature and V_{CC}.

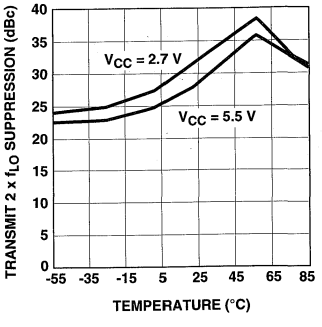


Figure 15. 2 x f_{LO} Suppression at Transmit Upconverter Output vs. Temperature and V_{CC}.

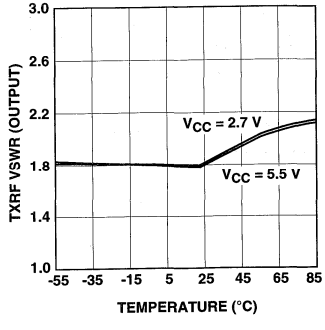


Figure 16. Transmit Upconverter Output VSWR vs. Temperature and V_{CC}.

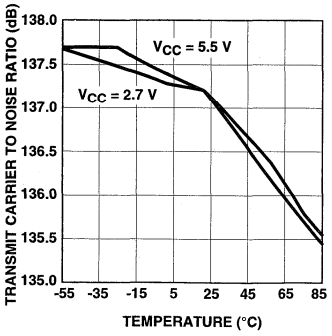


Figure 17. Carrier to Noise Ratio at Transmit Upconverter Output vs. Temperature and V_{CC}.

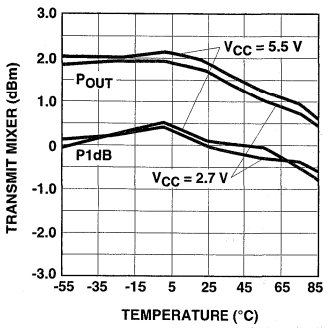


Figure 18. Transmit Upconverter Power Output and Output 1 dB Compression Point vs. Temperature and V_{CC}.

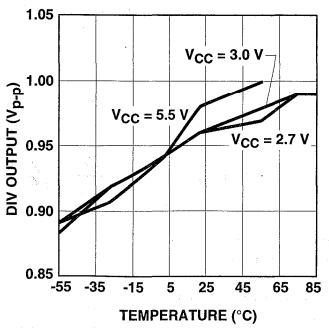


Figure 19. Prescaler Output Voltage vs. Temperature and V_{CC}.

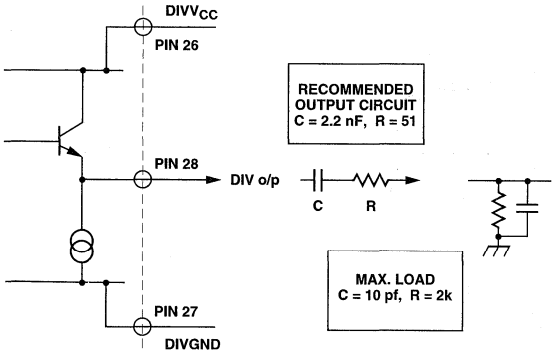


Figure 20. Equivalent Circuit and Recommended Output and Load Circuits for the HPMX-5001 Prescaler Output.

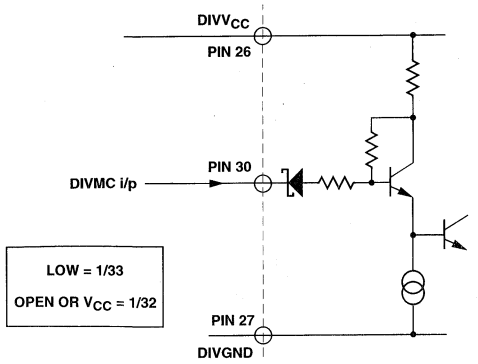


Figure 21. Equivalent Circuit for the Divider Modulus Control.

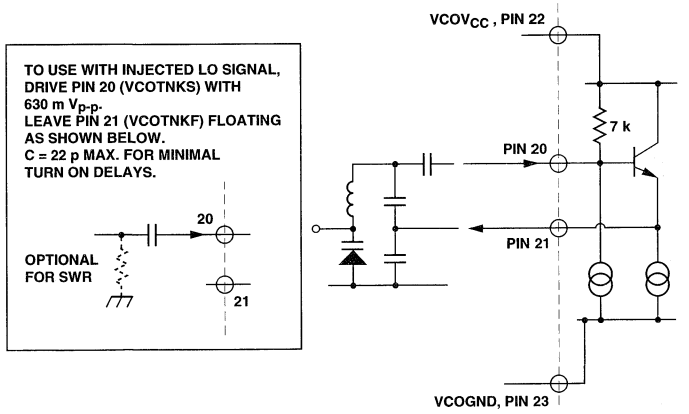


Figure 22. Equivalent Circuit for VCO Tank Connection and Recommended Tank Circuit.

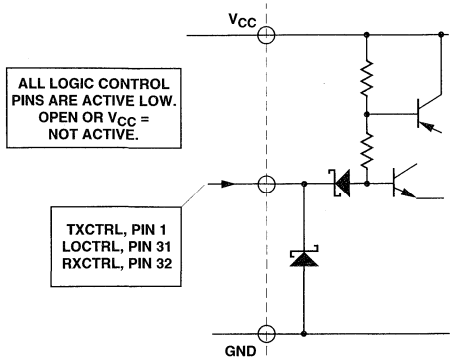


Figure 23. Equivalent Circuit for Logic Control Pin 1, 31, and 32.

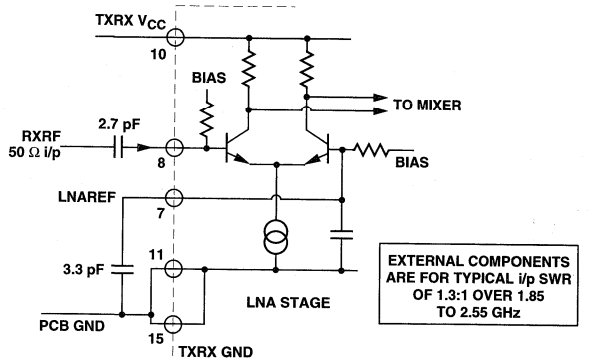


Figure 24. Equivalent Circuit for RXRF Input.

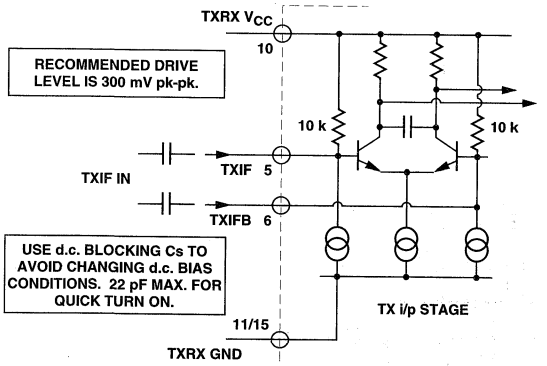


Figure 25. Equivalent Circuit for TXIF Input.

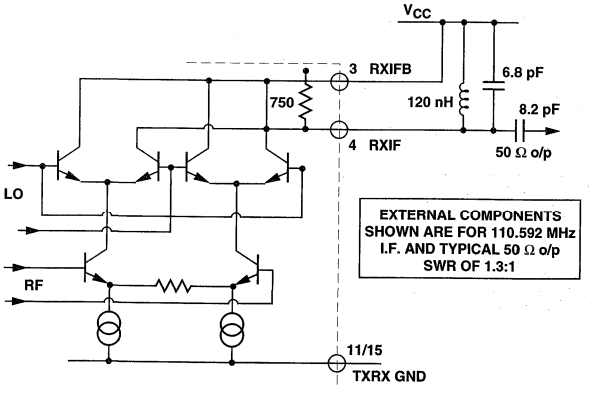


Figure 26. Equivalent Circuit for the RXIF Output and Recommended Matching Circuit for 110.592 MHz IF.

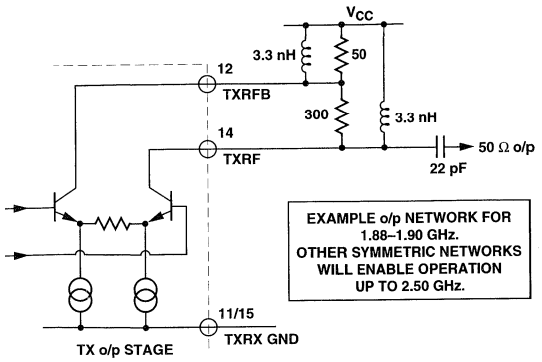


Figure 27. Equivalent Circuit for TXRF Output and Matching Network for DECT Phone Operation.

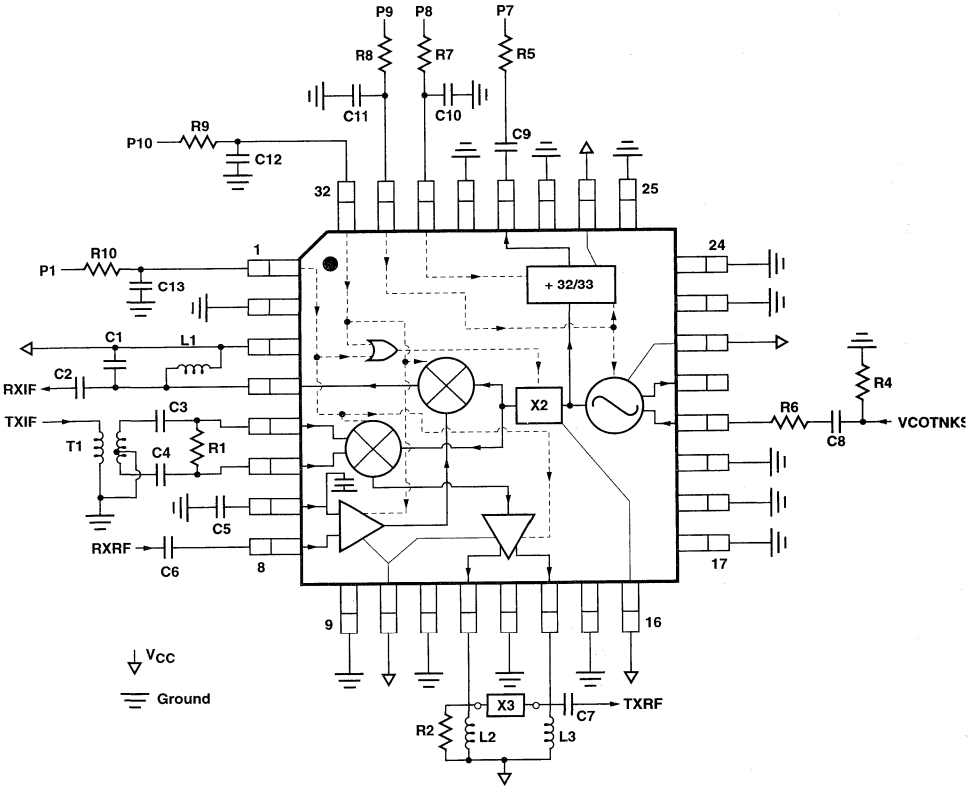


Figure 28. Test Board Schematic Diagram. All I/O Labels Correspond to Those on the Test board. See Table 3 for Component Values.

Table 3. Test Board Components Shown in Figure 28.
Note: Required V_{CC} decoupling capacitors are not shown on the schematic. Detailed schematic and board layout are available in Application Note 1081.

Component Label	Value (Size)
R1	270 (0805)
R2, R4, R5	51.1 (0805)
X3	R = 300 (0805) for 1.89 GHz, L = 3.3 nH for 2.45 GHz
R6	20 (0805)
R7, R8, R9, R10	1100 (0805)
C1	see Table 4
C2	see Table 4
C3, C4, C10, C11, C12, C13	1 nF (0805 or 0504)
C5	3.3 pF (0504 or 0603)
C6	2.7 pF (0805)
C7	22 pF (0805) for 1.89 GHz, 3.3 pF for 2.45 GHz
C8	12 pF (0805 or 0504)
C9	2.2 nF (0805)
L1	see Table 4
L2, L3	3.3 nH (0805)
T1	1:4 Balun T4-1-X65

Table 4. Component changes for dfferent IF frequencies.

IF Frequency	C1, pF	C2, pF	L1, nH	VSWR
110 MHz	6.8	8.2	120	1.3:1
200 MHz	1.0	3.9	100	1.3:1
250 MHz	1.2	3.9	56	1.3:1
300 MHz	1.2	3.9	39	1.3:1
350 MHz	2.7	2.7	27	1.3:1

Functional Description

A typical DECT application of the HPMX-5001 in a dual-conversion superheterodyne radio transceiver is shown in Figure 3. The HPMX-5001 is designed to provide four different modes of operation:

- Transmit, where the VCO, doubler, upconverting mixer, associated buffers, and prescaler are enabled
- Receive, where the VCO, doubler, downconverting mixer, associated buffers, and prescaler are enabled
- Synthesizer, where only the VCO and prescaler are active
- Standby, where all circuits are disabled

These four modes are controlled via a three wire interface, TXCTRL, RXCTRL, and LOCTRL. Figure 1 shows the programming logic states for all four modes. The detailed description of the three active modes is given below.

Transmit Mode

For transmit upconversion, a differential narrow-band modulated signal is AC-coupled into the TXIF and TXIFB inputs. The differential signal may be generated by the HPMX-5002 IF Demodulator/Modulator. Once on-chip, the signal is buffered and applied to a double-balanced Gilbert cell mixer. The upconverted RF signal is then amplified to generate a -0.6 dBm single-ended, single-sideband power signal at the 1 dB compression point. The RF outputs, TXRF and TXRFB, are open-collector outputs (see test diagram Figure 28 for recommended matching network). The TXRF output is AC-coupled into a 50 Ω transmit filter. This signal is then filtered and amplified off-chip by an external power amplifier before it is switched into the antenna. The HPMX-5001 may also be used in DECT systems which utilize direct modulation of the 1LO for data transmission. In this case, either the TXIF or TXIFB input, but not both, must be tied to V_{CC} to cause the upconverting mixer to act as a buffer stage.

Receive Mode

In receive mode, a preamplified RF signal is passed through an image filter and applied as a single-ended signal to the 50 Ω RXRF input. Use of a 2.7 pF blocking capacitor is recommended. RXRF is the non-inverting input of the RF input amplifier. The inverting input of this amplifier, LNAREF, is self-biased and requires only an external capacitor (recommended value of 3.3 pF) to ground. The receive downconversion mixer also employs a double-balanced Gilbert cell configuration. The production version of the HPMX-5001 will have two equivalent open collector outputs. The HPMX-5001 can operate at IF frequencies up to 300 MHz (see Figure 28 for recommended matching network).

Synthesizer Mode

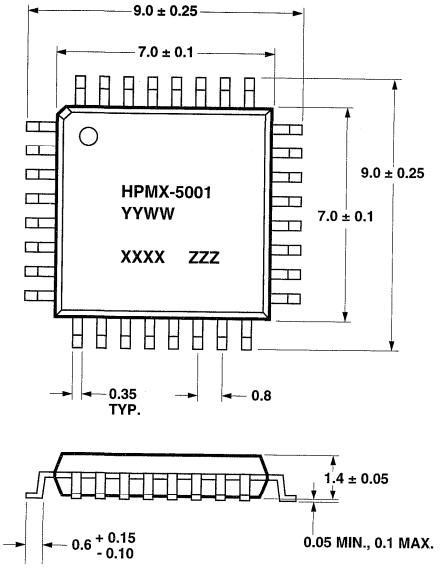
The on-chip 32/33 dual-modulus prescaler, in conjunction with the VCO, external tank circuit, and CMOS synthesizer, form a phase-locked loop (PLL). The prescaler divider output and modulus control input are designed to be compatible with positive-edge triggered CMOS synthesizers from a variety of vendors. The timing requirements for the prescaler are shown in Figure 2. It is important to note that the prescaler divides the VCO signal, and not the frequency doubler output. Local oscillator (LO) signal generation on the HPMX-5001 is accomplished through the combination of a VCO and frequency doubler. The VCO is a simple Clapp oscillator for the best possible noise performance. The VCO force and sense pins (VCOTNKF, VCOTNKS) are self-biased, so that the connections to the tank (minimum Q of 20) are through AC-coupling capacitors. VCOTNKS can also be used with an injected LO. VCOTNKF would then be left floating. The doubler circuit multiplies the VCO frequency by two. This enables the VCO to have lower sensitivity to both package parasitics and LO re-radiation. Separate bias pins and buffering are utilized to minimize pulling of the VCO when the chip is switched from synthesizer to transmit or receive mode.

Part Number Ordering Information

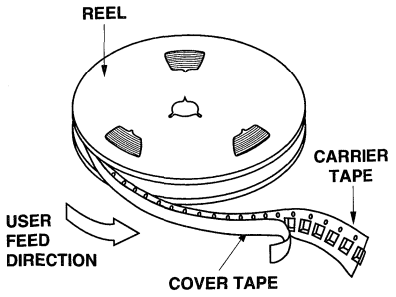
Part Number	No. of Devices	Container
HPMX-5001-STR	10	Strip
HPMX-5001-TR1	1000	Tape and Reel
HPMX-5001-TY1	250	Tray

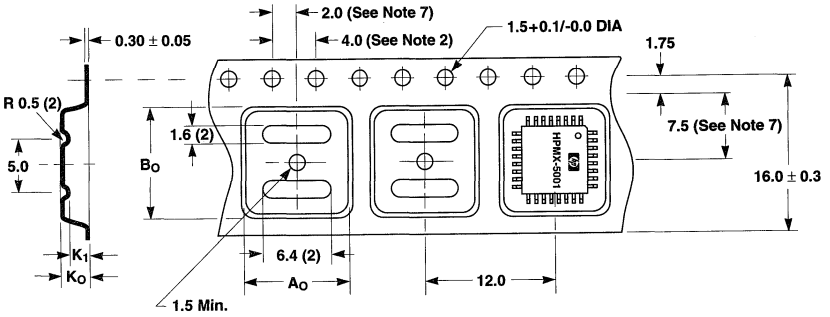
Package Dimensions 32 Pin Thin Quad Flat Package

All dimensions shown in mm.



Tape Dimensions and Product Orientation for Outline TQFP-32





Cover tape width = 13.3 ± 0.1 mm
Cover tape thickness = 0.051 mm (0.002 inch)

A_O = 9.3 mm
B_O = 9.3 mm
K_O = 2.2 mm
K_1 = 1.6 mm

NOTES:
1. Dimensions are in millimeters
2. 10 sprocket hole pitch cumulative tolerance ±0.2
3. Chamber not to exceed 1 mm in 100 mm
4. Material: black conductive Advantek™ polystyrene
5. A_O and B_O measured on a plane 0.3 mm above the bottom of the pocket.
6. K_O measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

HEWLETT® PACKARD

IF Modulator/Demodulator IC

Technical Data

HPMX-5002

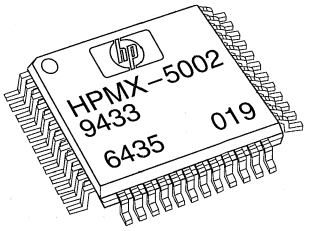
Features

- **Use with HPMX-5001 Up/Down Converter Chip for DECT Telephone Applications**
- **2.7–5.5 V Single Supply Voltage**
- **>75 dB RSSI Range**
- **Internal Data Slicer**
- **On-chip LO Generation, Including VCO, Prescalers and Phase/Frequency Detector**
- **Flexible Chip Biasing, Including Standby Mode**
- **Supports Reference Crystal Frequencies of 9, 12, and 16 Times the DECT Bit Rate (1.152 MHz)**
- **IF Input Frequency Range up to 250 MHz**
- **TQFP-48 Surface Mount Package**

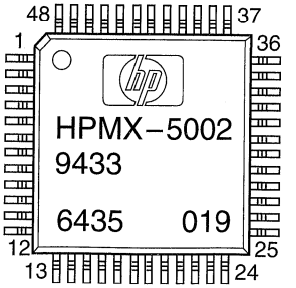
Applications

- **DECT, Unlicensed PCS and ISM Band Handsets, Basestations and Wireless LANs**

Plastic TQFP-48 Package



Pin Configuration



Description

The Hewlett-Packard HPMX-5002 IF Modulator/Demodulator provides all of the active components necessary for the demodulation of a downconverted DECT signal. Designed specifically for DECT, the HPMX-5002 contains a down-conversion mixer (to a 2nd IF), limiting amplifier chain, discriminator/data slicer, lock detector, and RSSI circuits. The LO2 generation is also included on-chip, via a VCO, dividers, and phase/frequency detector. The divide ratios are programmable to support reference frequencies of either 9, 12, or 16 times the DECT bit rate of 1.152 MHz allowing the use of common, low cost crystals.

The LO2 VCO can also be utilized in transmit mode by directly modulating the external VCO tank. An AGC loop in the buffered VCO output suppresses harmonics and reduces signal level variability.

The HPMX-5002 is designed to meet the size and power demands of portable applications. Battery cell count and cost are reduced due to the 2.7 V minimum supply voltage. The TQFP-48 package, combined with the high level of integration, means smaller footprints and fewer components. Flexible chip biasing takes full advantage of the power savings inherent in time-duplexed systems such as DECT.

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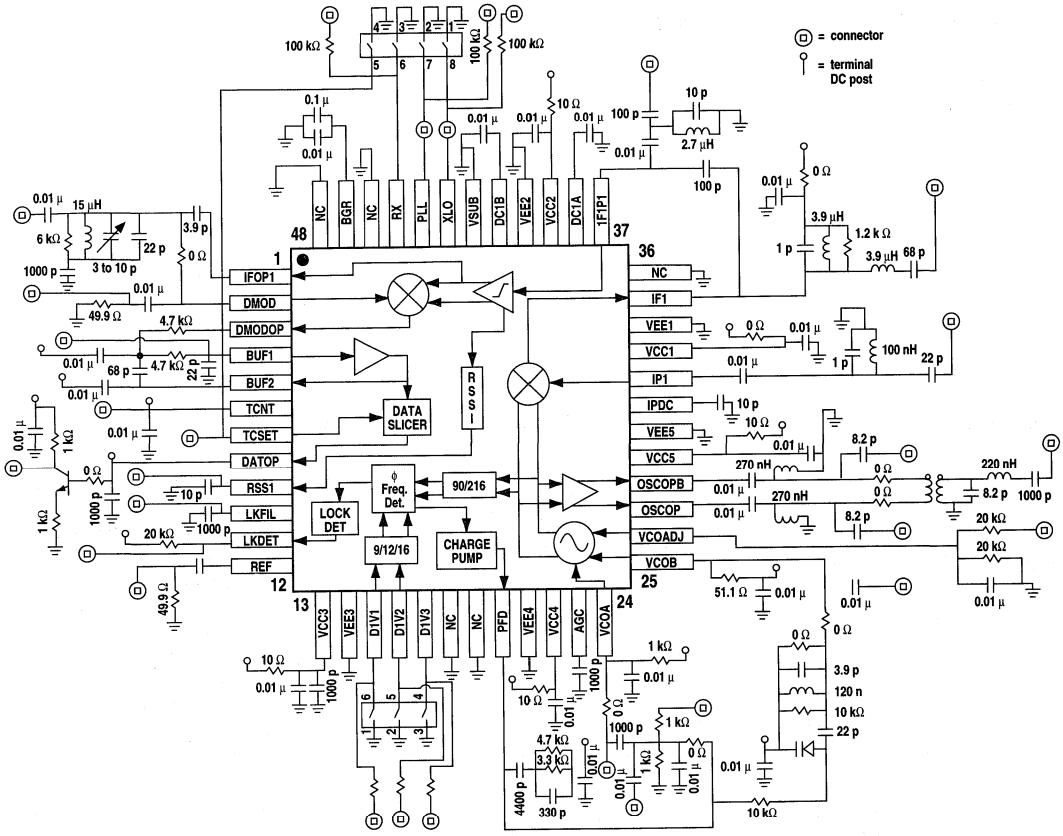
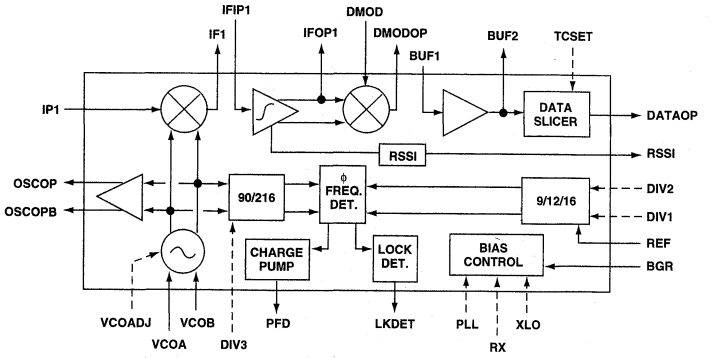


Figure 1. HPMX-5002 Test Board Schematic Diagram.

HPMX-5002 Functional Block Diagram



HPMX-5002 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Min.	Max.
	V_{CC} Supply Voltage	V	-0.2	7.5
	Voltage at any Pin[4]	V	-0.2	V_{CC} + 0.2
P_{diss}	Power Dissipation[2,3]	mW		200
	Junction Temperature	°C		+110
T_{STG}	Storage Temperature	°C	-55	+125

Thermal Resistance[2]:
θ_{jc} = 80°C/W

Notes:
1. Operation of this device in excess of any of these parameters may cause permanent damage.
2. T_{case} = 25°C
3. Derate at 10 mW/°C for T_{case} > 90°C
4. Except CMOS logic inputs, see Summary Characterization Information Table.

HPMX-5002 Guaranteed Electrical Specifications

Unless otherwise noted, all parameters are guaranteed under the following conditions: 2.7 V < V_{CC} < 5.5 V. Test results are based upon use of networks shown in test diagram (see Figure 1). f_{in} = 110.592 MHz. Typical values are for V_{CCX} = 3.0 V, T_A = 25°C.

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
I_{ccx}	Total V_{ccx} supply current (PLL locked)	RX mode	mA		21	27
	(PLL locked)	PLL mode	mA		16	20
		TX "flywheel" mode	mA		9	11.5
		Standby mode	µA			100
	Charge pump current	high current mode	µA	400	550	1000
	Charge pump current	low current mode	µA	30	50	100
GIF1	Mixer power gain from IP1 to IF1, external load impedance of 600 Ω	input matched to 50 Ω	dB	5	8	
VDATOP	Data slicer output level	Logic '0'	V			0.3
VDATOP	Data slicer output level	Logic '1'	V	V_{ccx}-0.3		

HPMX-5002 Summary Characterization Information

Typical values measured on test board shown in Figure 1 at V_{ccx} = 3.0 V, T_A = 25°C, f_{in} = 110.592 MHz, f_{LO2} = 103.68 MHz, unless otherwise noted.

Symbol	Parameters and Test Conditions		Units	Typ.
V_{IH}	CMOS input high voltage (can be pulled up as high as V_{cc}+7V)		V	≥ V_{cc}-0.8
V_{IL}	CMOS input low voltage		V	≤ 1.0
I_{IH}	CMOS input high current		µA	< 50
I_{IL}	CMOS input low current		µA	> - 50
	Mode switching time		µS	< 1
$P_{1\,dB}$	Mixer input 1 dB compression point	matched to 50 Ω source	dBm	-23
I_{IP3}	Mixer input IP3	matched to 50 Ω source	dBm	-17
NF_{IF1}	Mixer SSB noise figure (see test diagram Fig. 1)	input matched to 50 Ω source, 600 Ω load at output	dB	12
Z_{inIP1}	Mixer input impedance	50 MHz < f_{in} < 250 MHz	Ω	100
	RSSI dynamic range (for signal input at IFIP1; RSSI output measured with 6 bit ADC)	Note 1	dB	75
	RSSI voltage change	Note 1	mV/dB	17
	RSSI output voltage. V_{ccx} = 3 V, V_{RSSI} is monotonic	2 IF limiter input level: - 90 dBm -50 dBm -20 dBm	V	 0.88 1.48 2.04
$Z_{outRSSI}$	RSSI output impedance		kΩ	30
$IF2f_{3\,dB}$	IF2 limiter bandwidth		MHz	45
A_{VIF2}	IF2 limiter voltage gain	Prior to limiting, Note 2	dB	57
$Z_{inIFIP1}$	IF2 limiter input impedance at pin IFIP1	Note 2	Ω	600
V_{outLO2}	LO2 output buffer differential amplitude (between OSCOP and OSCOPB)	>1.5 kΩ differential load, f_{vco} = 103.68 MHz, V_{CC} = 3 V	mVp-p	335
	Bit slicer time constant ratio	TCSET = 0 vs. TCSET = 1		80:1
	LO2 VCO output buffer noise floor (@ 4 MHz offset)	tank circuit Q = 35	dBc/Hz	-142
	PLL charge pump leakage current		pA	<100
ILKDET	Lock detector current sink	Logic '0' (unlocked)	mA	1.1

Notes:

1: RSSI signal is monotonic over stated dynamic range, but not necessarily linear. Voltage change is defined in the linear region of the transfer curve.

2: IF2 frequency in the range 1 MHz < f < 45 MHz, with 10 nF capacitors from DC1A and DC1B to ground.

HPMX-5002 Pin Description

No.	Mnemonic	I/O Type	Description
1	IFOP1	Analog O/P	Output of IF amplifier, feeds quadrature network for discriminator
2	DMOD	Analog I/P	Input to discriminator mixer, driven by output of quadrature network
3	DMODOP	Analog O/P	Output of discriminator mixer, drives external low-pass data filter
4	BUF1	Analog I/P	Noninverting input of buffer amplifier that drives the data slicer
5	BUF2	Analog O/P	Output of buffer amplifer that drives the data slicer
6	TCNT	Analog DC	External capacitor connection which sets time constant for data slicer
7	TCSET	CMOS I/P	Data slicer time constant select
8	DATOP	CMOS O/P	Output bit stream from data slicer
9	RSSI	Analog O/P	Receive Signal Strength Indicator output
10	LKFIL	Analog DC	External capacitor connection which sets time constant for lock detector
11	LKDET	CMOS O/P	Indicates that LO2 PLL is in lock status
12	REF	Analog I/P	Reference signal for LO2 PLL
13	VCC3	DC Supply	PLL supply voltage
14	VEE3	Ground	PLL ground
15	DIV1	CMOS I/P	Controls divide ratio for reference frequency input to the LO2 PLL
16	DIV2	CMOS I/P	Controls divide ratio for reference frequency input to the LO2 PLL
17	DIV3	CMOS I/P	Controls divide ratio for VCO frequency input to the LO2 PLL
20	PFD	Analog O/P	LO2 PLL phase/frequency detector charge pump output
21	VEE4	Ground	LO2 VCO ground
22	VCC4	DC Supply	LO2 VCO supply voltage
23	AGC	Analog DC	External capacitor connection to compensate LO2 VCO AGC loop
24	VCOA	Analog I/P	VCO tank force line
25	VCOB	Analog O/P	VCO tank sense line
26	VCOADJ	Analog I/P	Controls amplitude of buffered LO2 VCO output
27	OSCOP	Analog O/P	Buffered LO2 output (+)
28	OSCOPB	Analog O/P	Buffered LO2 output (-)
29	VCC5	DC Supply	1st IF supply voltage
30	VEE5	Ground	1st IF ground
31	IPDC	Analog DC	External capacitor connection for decoupling 1st IF bias point
32	IP1	Analog I/P	1st IF input signal
33	VCC1	DC Supply	IF limiting amplifier supply voltage
34	VEE1	Ground	IF limiting amplifier ground
35	IF1	Analog O/P	Downconverted signal from front-end mixer, drives external filter (hi-Z output, open collector)
37	IFIP1	Analog I/P	Input to IF limiting amplifier, driven by external filter (600 Ω impedance, internally set)
38	DC1A	Analog DC	External capacitor connection for decoupling IF limiting amplifier
39	VCC2	DC Supply	IF limiting amplifier supply voltage
40	VEE2	Ground	IF limiting amplifier ground

HPMX-5002 Pin Description, continued

No.	Mnemonic	I/O Type	Description
41	DC1B	Analog DC	External capacitor connection for decoupling IF limiting amplifier
42	VSUB	Ground	Substrate connection
43	XLO	CMOS I/P	Controls bias to VCO and PLL components in conjunction with PLL pin
44	PLL	CMOS I/P	Controls bias to VCO and PLL components in conjunction with XLO pin
45	RX	CMOS I/P	Controls bias to receive signal path, RSSI, data slicer
47	BGR	Analog DC	External capacitor connection for decoupling bandgap reference voltage
18,19, 36, 46, 48	N/C	Not connected	All unconnected pins should be connected to a low-noise ground

Table 1: HPMX-5002 Mode Control
(CMOS Logic Levels)

Mode	PLL	XLO	RX
PLL	1	0	1
TX	0	0	1
RX	1	0	0
STBY	1	1	1
"flywheel"	see text		

Table 2: HPMX-5002 PLL Divider Programming
(CMOS Logic Levels)

REF divide by:	DIV1	DIV2	DIV3
9	1	0	X
12	0	0	X
16	0	1	X
Not defined	1	1	X
LO2 divide by:			
90	X	X	0
216	X	X	1

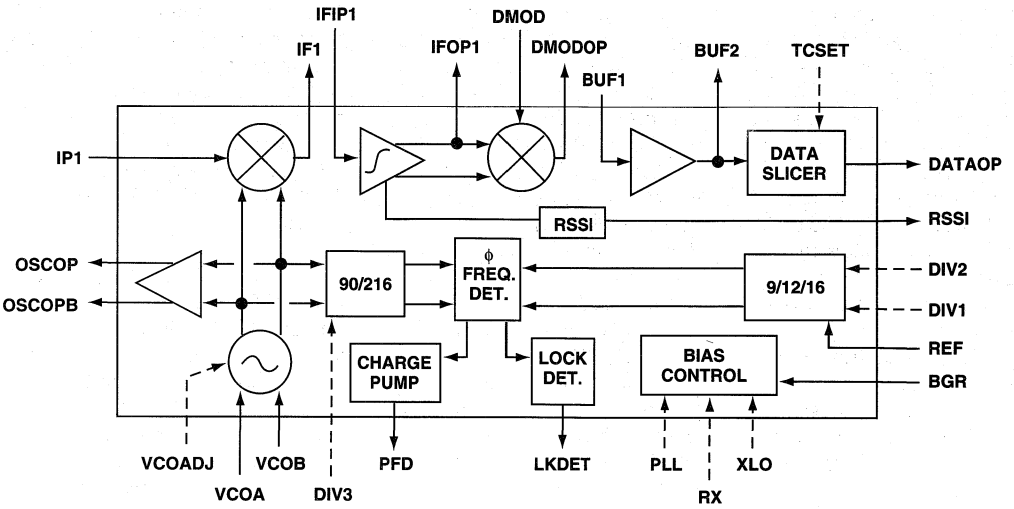


Figure 2. HPMX-5002 Detailed Block Diagram.

Functional Description

Please refer to Figure 2, Detailed Block Diagram, above. Figure 2 contains a graphical representation of all 32 active signal pins of the HPMX-5002. For clarity, the supply, ground, and substrate pins are deleted.

Modes of Operation

The HPMX-5002 supports four basic modes of operation. The logic states necessary to program each mode are listed in Table 1, Mode Programming. The modes are:

Receive mode (RX),
which is used during the receive time slot in DECT systems. All blocks are powered on in this mode.

LO2 synthesis mode (PLL),
which enables the IC to achieve phase lock without biasing the receive signal path, thus saving power. This is very useful for DECT blind-slot applications.

Transmit mode (TX),
designed for use when the LO2 VCO is directly modulated by the DECT data stream for subsequent up-conversion to the channel frequency (with the HPMX-5001 DECT Upconverter/Down-converter). In this mode, only the VCO and LO2 output buffer are biased and operational. In order to use the LO2 VCO as a modulation source, it is necessary to first program the HPMX-5002 in PLL mode. Once the loop has achieved lock, the PLL is then disabled by setting the PLL pin to a logic 0. This puts the VCO into "**flywheel**" operation, preventing the PLL from interfering with the modulation of the VCO. Leakage in the tank circuit shown in Figure 3 allows the VCO to drift at a rate of 2.5 kHz per mS, well within the DECT specs of 13 kHz per mS.

Standby mode,
where all blocks are powered down. This mode allows the system designer to effectively turn the IC off without having to use battery control, and also allows the IC to change quickly to an active mode.

Detailed Circuit Description

PLL Section

The PLL section of the HPMX-5002 contains three major sections: a set of reference and LO2 dividers, a phase/frequency detector with charge pump, and a lock detector.

The dividers for both the reference and LO2 signals in the PLL section are programmable to accomodate the most popular DECT reference frequencies and also to enable the use of higher 1st IF frequencies if desired.

Figure 3 illustrates the logic states necessary to program both the reference and LO2 dividers.

The reference divider ratios were selected to conform to the three most popular DECT reference frequencies of 10.368 MHz, 13.824 MHz, and 18.432 MHz. The LO2 divider values allow the use of either a 110.592 MHz or 112.32 MHz 1st IF with a divide value of 90 (which yields a LO2 of 103.68 MHz). In addition, the divide by 216 value permits the use of a much higher 1st IF (222.91 MHz, with a corresponding LO2 of 248.832 MHz), which enables the use of much smaller SAW filters and relaxes the image filtering requirements.

The phase/frequency detector also incorporates a lock detection feature. The user must supply a decoupling capacitor (recommended value of 1 nF) from the LKFIL pin to ground. If the loop is not in phase lock, the LKDET pin will sink up to 1 mA. This open collector output is utilized so that this signal can be wire-ORed with other lock detection circuits, such as from the 1LO portion of the system. The pullup resistor can also be tied to the CMOS positive supply, thus eliminating potential problems with CMOS logic high voltages when different positive supplies are used between the radio and the baseband processor. When the PLL loop phase error is less than approximately 0.3 radians, the LKDET current sink goes to zero.

VCO Section

The VCO section has two major components, a sustaining amplifier and a buffered external output. The sustaining amplifer is designed to be used with an external tank circuit, and incorporates a force (VCOA) and sense (VCOB) architecture to reduce the effects of package parasitics. As described earlier, the VCOB pin may be overdriven by an external LO, in which case the on-chip sustaining amplifier acts as a buffer stage before the downconverting mixer.

The buffered external output is a differential signal (OSCOP, OSCOPB). The buffer also incorporates an AGC loop in order to provide a sinusoidal output signal with constant amplitude which is insensitive to variations in tank Q and loading. This helps to suppress harmonics and eliminates therefore the need for an upconversion filter if the HPMX-5002 is used in a system together with the 2.5 GHz upconverter/downconverter HPMX-5001. The AGC requires an external compensation capacitor (recommended value 1 nF) from the AGC pin to ground.

Signal Path

The input to the HPMX-5002 is an AC-coupled IF signal (IP1). The input buffer before the downconverting mixer requires a decoupling capacitor from the IPDC pin to ground (recommended value 10 pF).

The buffered input is then mixed with the LO2, and the output of the mixer (IF1) drives an off-chip bandpass filter centered at the IF2 frequency (6.9 MHz for a 110.592 MHz 1IF). The filtered signal is then fed to the IFIP1 pin, which is the input to the limiting amplifier chain. The limiting amplifier requires two external decoupling capacitors from pins DC1A and DC1B to ground (recommended value 10 nF).

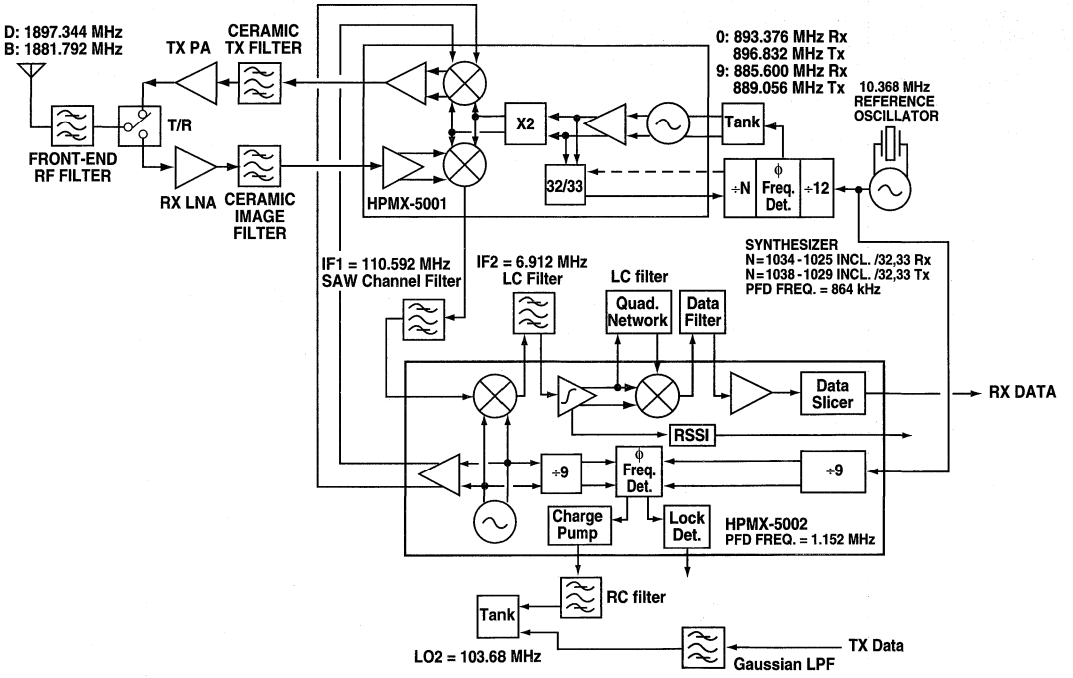
The limiting amplifier chain also feeds the Received Signal Strength Indicator (RSSI) block. The RSSI signal is monotonic over a 75 dB dynamic range, and in its linear range varies at 17 mV/dB. The RSSI signal is designed to be digitized by the CMOS burst mode controller.

The output of the limiting amplifier (IFOP1) drives the discriminator circuit. This signal is fed directly to one of the input ports of a Gilbert cell mixer, and it also drives an external quadrature network (with a recommended Q of 8 for optimum performance). The output of the external quadrature network is then fed into the other input port of the Gilbert cell (via the DMOD pin). The output of the Gilbert cell is taken at the DMODOP pin, which drives an external lowpass filter. To aid in the construction of the filter, a buffer stage is included on-chip. The BUF1 pin is the noninverting input of the buffer, and BUF2 is the output, which is also connected to the input of the data slicer.

The data slicer operates on a dual time constant architecture, controlled via the TCSET pin. During the preamble portion of a DECT timeslot (with TCSET set to 1), the data slicer quickly acquires the midpoint voltage of the incoming data stream, correcting any DC offsets that may have occurred due to frequency deviations within the DECT specification. The value of this initial time constant is determined by an external capacitor connected between TCNT and ground. A 10 nF capacitor allows the accurate acquisition of the midpoint voltage within half of the 16-bit DECT preamble.

Once the midpoint voltage has been acquired, TCSET is then forced to a 0, and the time constant of the midpoint voltage tracking circuit is increased by a factor of 80. This effectively freezes the midpoint voltage from any variations due to normal data transitions, but still allows for some correction of frequency drifts during the data burst.

The output of the data slicer (DATOP) is a CMOS-compatible bitstream. However, it is recommended that an external NPN amplifier stage be used to drive the CMOS baseband processor, in order to minimize the amount of ground and supply currents in the HPMX-5002 which might desensitize the chip.



All other connections go to Burst Mode Controller, power source, or ground.

Figure 3. Typical HPMX-5002 Application with HPMX-5001 T/R Chip.

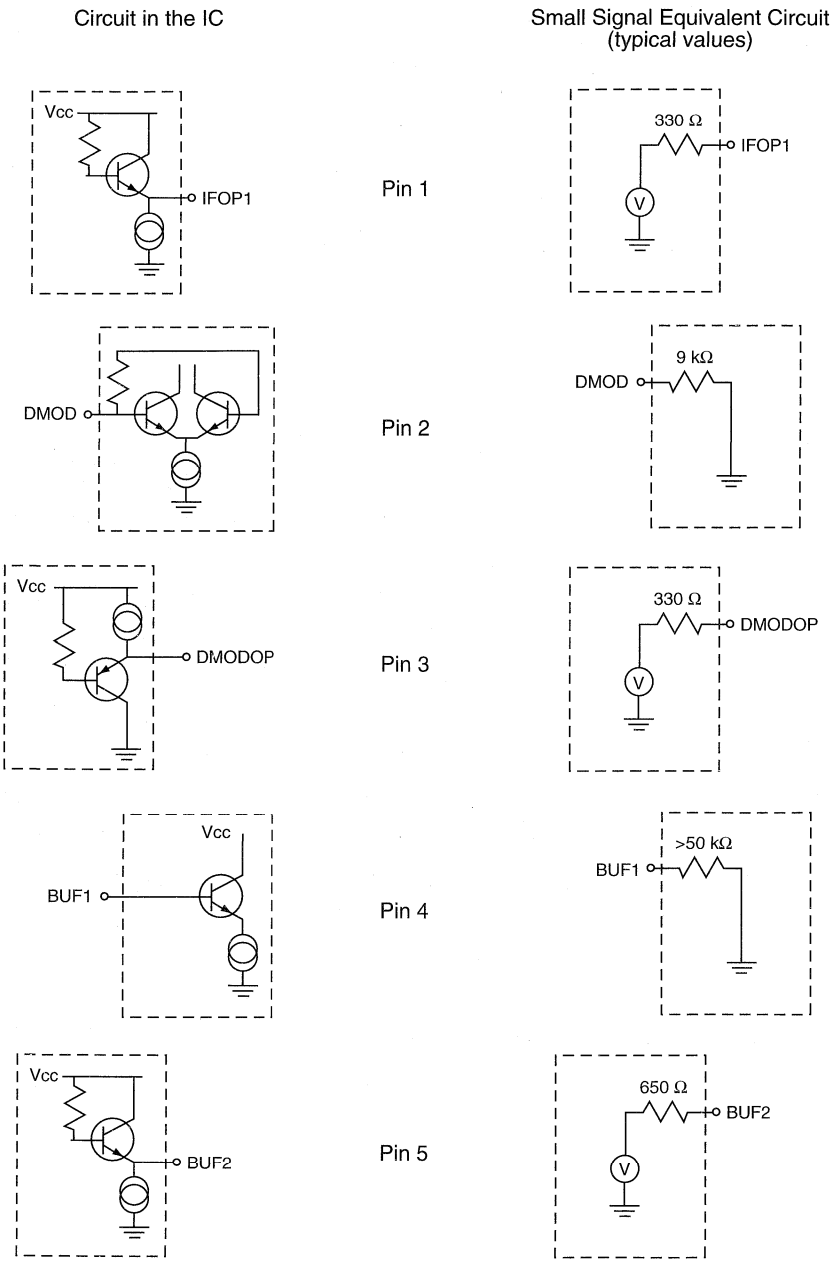


Figure 4. HPMX-5002 Internal and Equivalent Circuits, Pins 1-5.

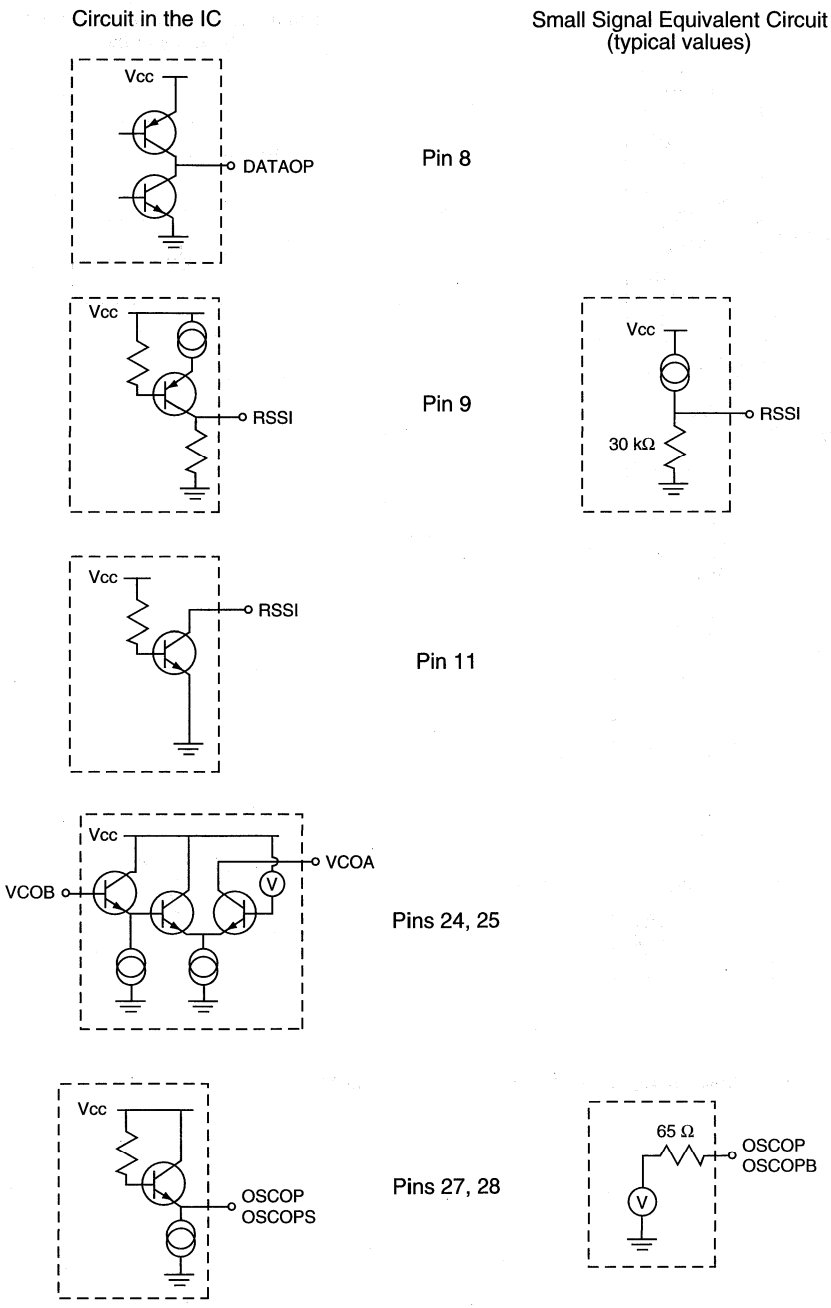


Figure 5. HPMX-5002 Internal and Equivalent Circuits, Pins 8, 9, 11, 24, 25, 27, and 28.

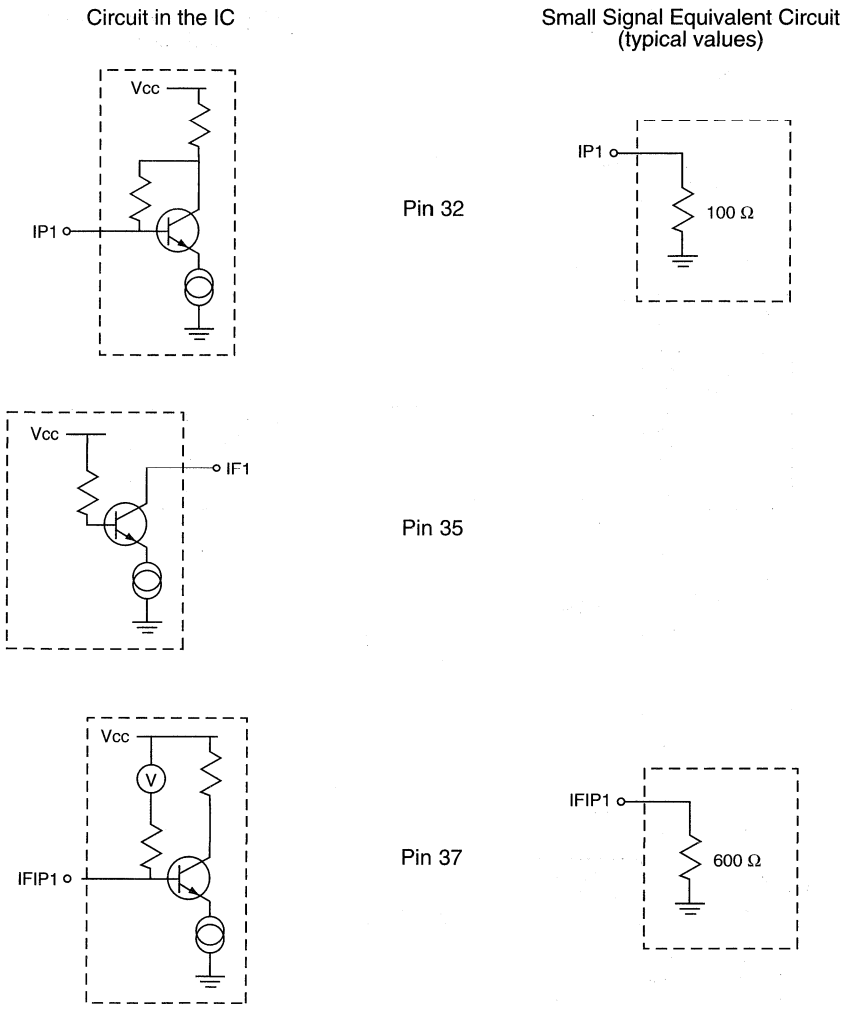
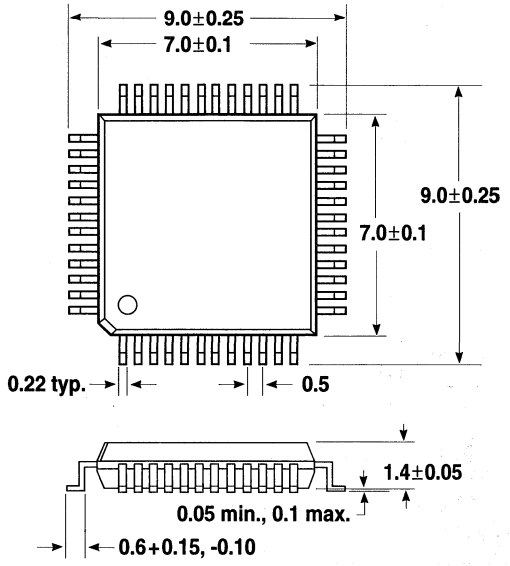


Figure 6. HPMX-5002 Internal and Equivalent Circuits, Pins 32, 35, and 37.

Package Dimensions 48 Pin Thin Quad Flat Package

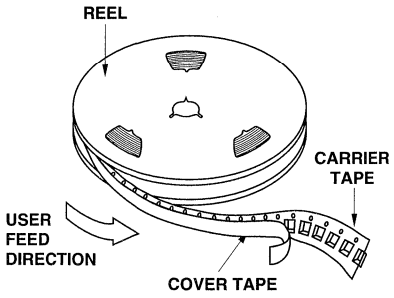
All dimensions shown in mm.

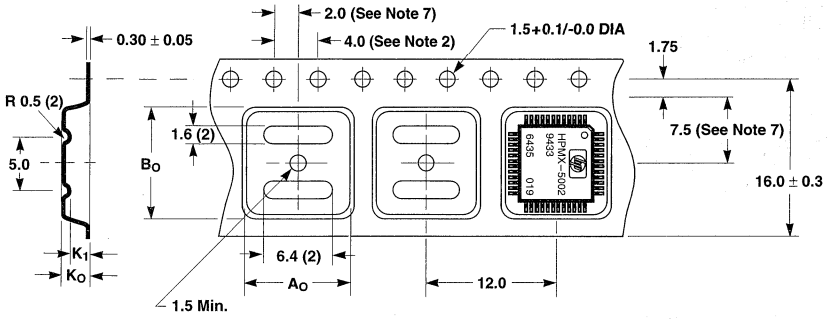


Part Number Ordering Information

Part Number	No. of Devices	Container
HPMX-5002-STR	10	Strip
HPMX-5002-TR1	1000	Tape and Reel
HPMX-5002-TY1	250	Tray

Tape Dimensions and Product Orientation for Outline TQFP-48





Cover tape width = 13.3 ± 0.1 mm
Cover tape thickness = 0.051 mm (0.002 inch)

A_O = 9.3 mm
B_O = 9.3 mm
K_O = 2.2 mm
K_1 = 1.6 mm

NOTES:
1. Dimensions are in millimeters
2. 10 sprocket hole pitch cumulative tolerance ±0.2
3. Chamber not to exceed 1 mm in 100 mm
4. Material: black conductive Advantek™ polystyrene
5. A_O and B_O measured on a plane 0.3 mm above the bottom of the pocket.
6. K_O measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

HEWLETT® PACKARD

Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/IF Amp

Technical Data

IAM-81008

Features

- **RF-IF Conversion Gain From 0.05–5 GHz**
- **IF Conversion Gain From DC to 1 GHz**
- **Low Power Dissipation:** 65 mW at V_{CC} = 5 V Typical
- **Single Polarity Bias Supply:** V_{CC} = 4 to 8 V
- **Load-insensitive Performance**
- **Conversion Gain Flat Over Temperature**
- **Low LO Power Requirements:** –5 dBm Typical
- **Low Cost Plastic Surface Mount Package**

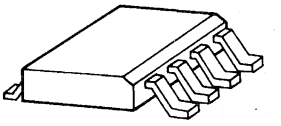
Description

The IAM-81008 is a complete low power consumption, double balanced active mixer housed in a miniature low cost plastic surface mount package. It is designed for narrow or wide bandwidth commercial and industrial applications having RF inputs up to 5 GHz. Operation at RF and LO frequencies less than 50 MHz can be achieved using optional external capacitors to ground. The IAM-81008 is particularly well suited for applications that require load-insensitive conversion and good spurious signal suppression with minimum LO and bias power consumption.

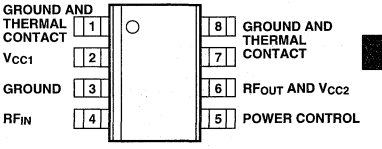
Typical applications include frequency down conversion, modulation, demodulation and phase detection. Markets include fiber-optics, GPS satelite navigation, mobile radio, and battery powered communications receivers.

The IAM series of Gilbert multiplier-based frequency converters is fabricated using HP's 10 GHz, f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process. This process uses nitride self alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

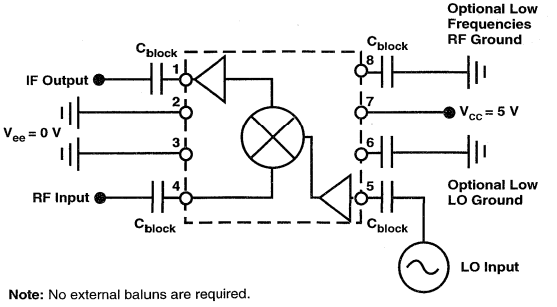
Plastic SO-8 Package



Pin Configuration



Typical Biasing Configuration and Functional Block Diagram



Note: No external baluns are required.

IAM-81008 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	10 V
Power Dissipation[2,3]	300 mW
RF Input Power	+14 dBm
LO Input Power	+14 dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance:
θ_{jc} = 80°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 4.4 mW/°C for T_C > 82°C.

IAM-81008 Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
IAM-81008-TR1	1000	7"

For more information, see "Tape and Reel Packaging for Semmiconductor Devices".

IAM-81008 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: V_{cc} = 5 V, Z_O = 50 Ω, LO =–5 dBm, RF = –20 dBm		Units	Min.	Typ.	Max.
G_C	Conversion Gain	RF = 2 GHz, LO = 1.75 GHz	dB	6.0	8.5	10
$F_{3\,dB}RF$	RF Bandwidth (G_C 3 dB Down)	IF = 250 MHz	GHz		3.5	
$F_{3\,dB}$ IF	IF Bandwidth (G_C 3 dB Down)	LO = 2 GHz	GHz		0.6	
$P_{1\,dB}$	IF Output Power at 1 dB Gain Compression	RF = 2 GHz, LO = 1.75 GHz	dBm		–6	
IP_3	IF Output Third Order Intercept Point	RF = 2 GHz, LO = 1.75 GHz	dBm		3	
NF	SSB Noise Figure	RF = 2 GHz, LO = 1.75 GHz	dB		17	
VSWR	RF Port VSWR	f = 0.05 to 3.5 GHz			1.5:1	
	LO Port VSWR	f = 0.05 to 3.5 GHz			2.0:1	
	IF Port VSWR	f < 1 GHz			1.5:1	
RF_{if}	RF Feedthrough at IF Port	RF = 2 GHz, LO = 1.75 GHz	dBc		–25	
LO_{if}	LO Leakage at IF Port	LO = 1.75 GHz	dBm		–25	
LO_{rf}	LO Leakage at RF Port	LO = 1.75 GHz	dBm		–30	
I_{CC}	Supply Current		mA	10	13	16

Note:
1. The recommended operating voltage range for this device is 4 to 8 V. Typical performance as a function of voltage is on the following page.

IAM-81008 Typical Performance, T_A = 25°C, V_{CC} = 5 V
RF: –20 dBm at 2 GHz, LO: –5 dBm at 1.75 GHz
(unless otherwise noted)

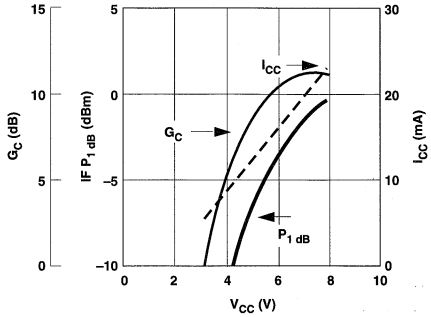


Figure 1. Conversion Gain, IF $P_{1\ dB}$ and I_{CC} Current vs. V_{CC} Bias Voltage.

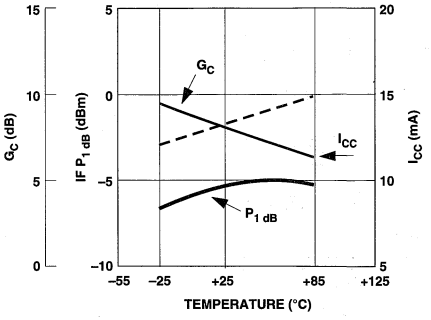


Figure 2. Conversion Gain, IF $P_{1\ dB}$ and I_{CC} Current vs. Case Temperature.

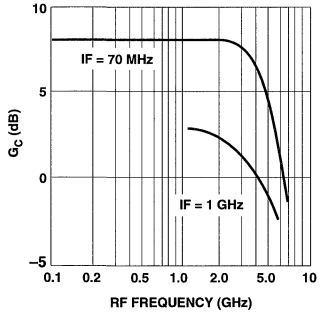


Figure 3. Typical RF to IF Conversion Gain vs. RF Frequency, T_A = 25°C (Low Side LO).

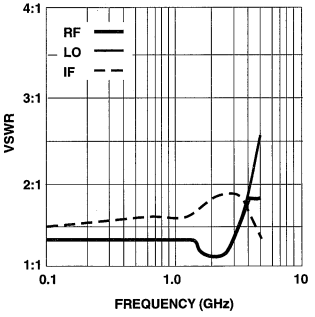


Figure 4. RF, LO and IF Port VSWR vs. Frequency.

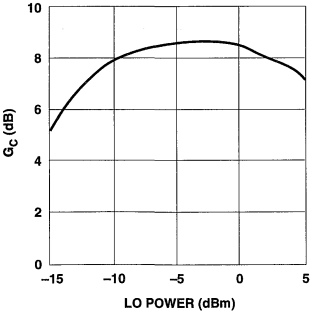


Figure 5. RF to IF Conversion Gain vs. LO Power.

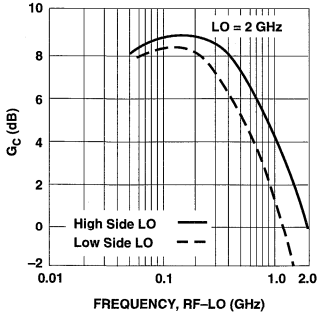


Figure 6. RF to IF Conversion Gain vs. IF Frequency.

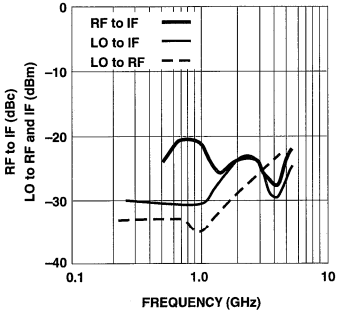


Figure 7. RF Feedthrough Relative to IF Carrier, dBm LO to RF and IF Leakage vs. Frequency.

HARMONIC LO ORDER	0	1	2	3	4	5
0	—	21	35	74	>75	>75
1	18	0	45	48	>75	>75
2	16	35	42	72	>75	>75
3	42	20	44	59	>75	>75
4	29	44	52	64	>75	>75
5	45	36	57	64	>75	>75

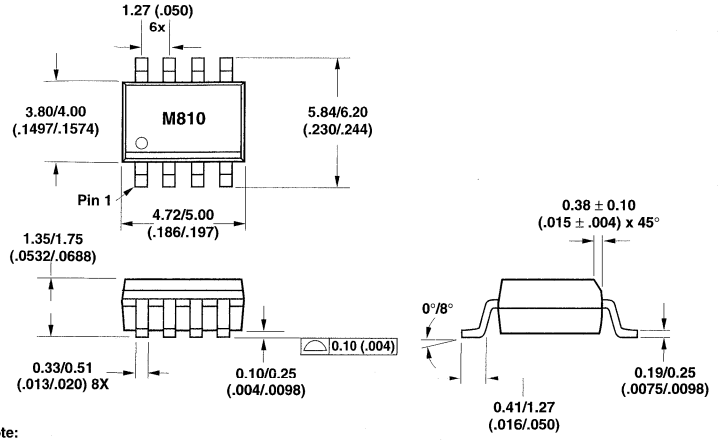
HARMONIC RF ORDER

Xmn = Pif – P(m*rf – n*lo)

Figure 8. Harmonic Intermodulation Suppression (dB Below Desired Output)
RF at 1 GHz, LO at 0.752 GHz, IF at 0.248 GHz.

Package Dimensions

SO-8 Plastic Package



Note:

1. Dimensions are shown in millimeters (inches).

HEWLETT® PACKARD

Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/IF Amp

Technical Data

IAM-81028

Features

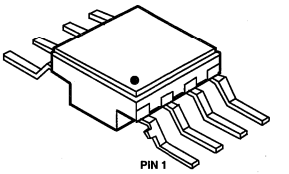
- **8 dB RF-IF Conversion Gain From 0.05 - 5 GHz**
- **IF Output from DC to 1 GHz**
- **Low Power Dissipation:** 60 mW at V_{CC} = 5 V Typ.
- **Single Polarity Bias Supply:** V_{CC} = 4 to 8 V
- **Load-Insensitive Performance**
- **Conversion Gain Flat Over Temperature**
- **Low LO Power Requirements:** -5 dBm Typical
- **Low RF to IF Feedthrough, Low LO Leakage**
- **Hermetic Ceramic Surface Mount Package**

Description

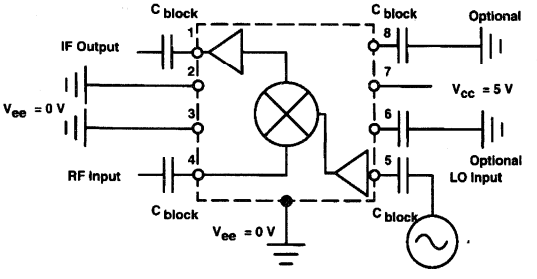
The IAM-81028 is a complete low-power-consumption double-balanced active mixer housed in a miniature ceramic hermetic surface mount package. It is designed for narrow or wide bandwidth commercial, industrial and military applications having RF inputs up to 5 GHz and IF outputs from DC to 1 GHz. Operation at RF and LO frequencies less than 50 MHz can be achieved using optional external capacitors to ground. The IAM-81028 is particularly well suited for applications that require load-insensitive conversion gain and good spurious signal suppression with minimum LO and bias power consumption. Typical applications include frequency down conversion, modulation, demodulation and phase detection for fiber-optic, GPS satellite navigation, mobile radio, and battery powered communications receivers.

The IAM series of Gilbert multiplier-based frequency converters is fabricated using HP's 10 GHz, f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process. This process uses nitride self alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

28 Package



Typical Biasing Configuration and Functional Block Diagram



Note: No external BALUNs are required.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	15 V
Power Dissipation[2,3]	300 mW
RF Input Power	+14 dBm
LO Input Power	+14 dBm
Junction Temperature	200°C
Storage Temperature	-65°C to 200°C

Thermal Resistance:[2,4]
$\theta_{jc} = 50°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 20 mW/°C for $T_C > 185°C$.
4. See MEASUREMENTS section "Thermal Resistance" in Communications Components Catalog, for more information.

Electrical Specifications[1]

$T_A = 25°C$

Symbol	Parameters and Test Conditions: V_{CC} = 5 V, Z_O = 50 Ω, LO = -5 dBm, RF = -20 dBm		Units	Min.	Typ.	Max.
G_C	Conversion Gain	RF = 2 GHz, LO = 1.75 GHz	dB	7.0	8.5	10
$f_{3dB}RF$	RF Bandwidth (G_C 3 dB Down)	IF = 250 MHz	GHz		4.5	
$f_{3dB}IF$	IF Bandwidth (G_C 3 dB Down)	LO = 2 GHz	GHz		0.6	
P_{1dB}	IF Output Power at 1 dB Gain Compression	RF = 2 GHz, LO = 1.75 GHz	dBm		-6	
IP_3	IF Output Third Order Intercept Point	RF = 2 GHz, LO = 1.75 GHz	dBm		3	
NF	SSB Noise Figure	RF = 2 GHz, LO = 1.75 GHz	dB		17	
VSWR	RF Port VSWR	f = 0.05 to 5 GHz			1.5:1	
	LO Port VSWR	f = 0.05 to 5 GHz			1.5:1	
	IF Port VSWR	f < 1 GHz			1.5:1	
RF_{if}	RF Feedthrough at IF Port	RF = 2 GHz, LO = 1.75 GHz	dBc		-25	
LO_{if}	LO Leakage at IF Port	LO = 1.75 GHz	dBm		-25	
LO_{rf}	LO Leakage at RF Port	LO = 1.75 GHz	dBm		-35	
I_{CC}	Supply Current		mA	10	12.5	16

Note:
1. The recommended operating voltage range for this device is 4 to 8 V. Typical performance as a function of voltage is on the following page.

Typical Performance, T_A = 25°C, V_{CC} = 5 V
RF: -20 dBm at 2 GHz, LO: -5 dBm at 1.75 GHz
(unless otherwise noted)

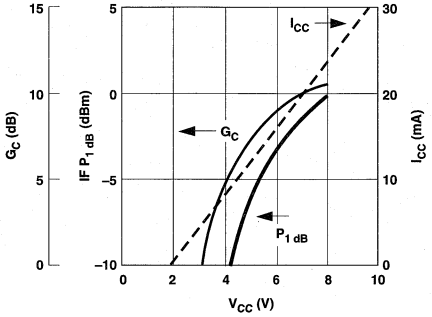


Figure 1. Conversion Gain, IF $P_{1\ dB}$ and I_{CC} Current vs. V_{CC} Bias Voltage.

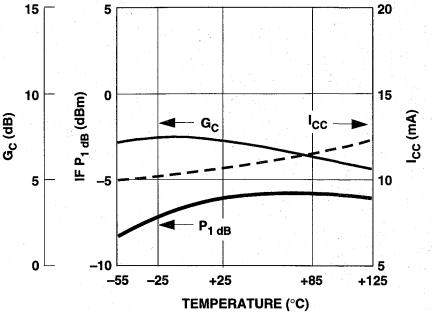


Figure 2. Conversion Gain, IF $P_{1\ dB}$ and I_{CC} Current vs. Case Temperature.

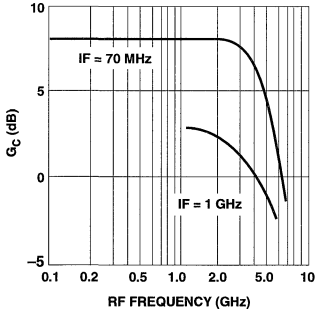


Figure 3. Typical RF to IF Conversion Gain vs. RF Frequency, T_A = 25°C (Low Side LO).

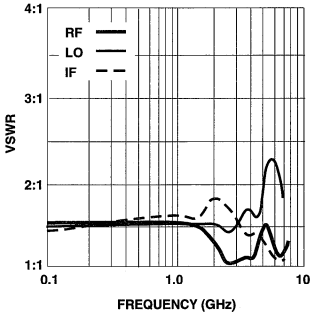


Figure 4. RF, LO and IF Port VSWR vs. Frequency.

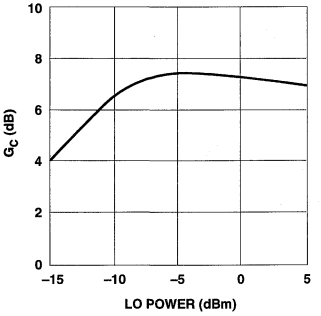


Figure 5. RF to IF Conversion Gain vs. LO Power.

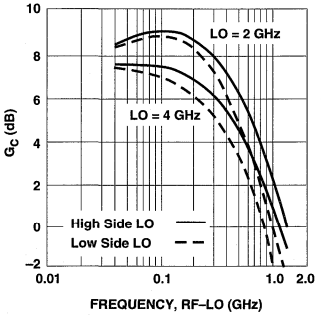


Figure 6. RF to IF Conversion Gain vs. IF Frequency.

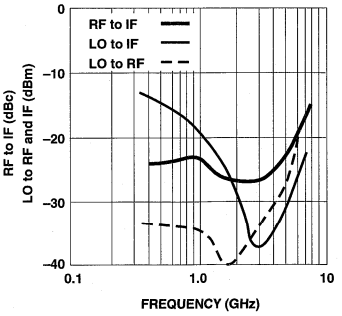


Figure 7. RF Feedthrough Relative to IF Carrier, dBm LO to RF and IF Leakage vs. Frequency.

HARMONIC LO ORDER

	0	1	2	3	4	5
0	—	21	35	>75	>75	>75
1	12	0	48	48	>75	>75
2	13	41	39	71	>75	>75
3	36	28	53	57	>75	>75
4	27	49	49	72	>75	>75
5	45	35	63	62	>75	>75

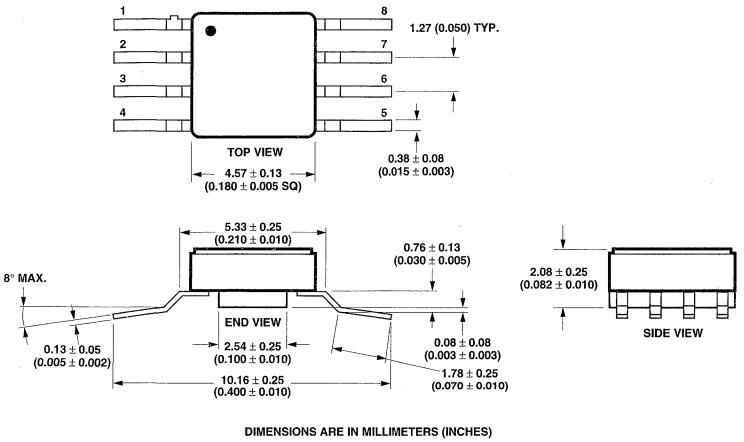
HARMONIC RF ORDER

Xmn = Pif – P(m•rf – n•lo)

Figure 8. Harmonic Intermodulation Suppression (dB Below Desired Output) RF at 1 GHz, LO at 0.752 GHz, IF at 0.248 GHz.

Package Dimensions

28 Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Package marking code is "M810"

HEWLETT® PACKARD

Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/ IF Amp

Technical Data

IAM-82008

Features

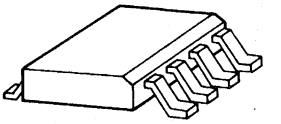
- **RF-IF Conversion Gain:** 15 dB from 0.05-5 GHz
- **IF Conversion Gain from DC to 2 GHz**
- **IF Output P_{1dB}:** +8 dBm Typical
- **Single Polarity Bias Supply:** V_{CC} = 7 to 13 V
- **Load Insensitive Performance**
- **Conversion Gain Flat over Temperature**

Description

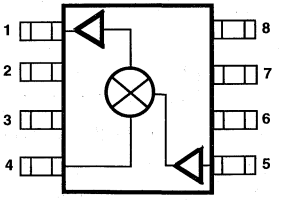
Hewlett-Packard's IAM-82008 is a complete moderate-power double-balanced active mixer housed in a miniature low cost surface mount package. It is designed for narrow or wide bandwidth commercial and industrial applications having RF inputs up to 5 GHz. Operation of RF and LO frequencies below 50 MHz can be achieved using optional external capacitors to ground. The IAM-82008 is particularly well suited for applications that require load-insensitive conversion gain and good spurious signal suppression and moderate dynamic range with low LO power. Typical applications include frequency down-conversion, up-conversion, modulation, demodulation, and phase detection. Markets include fiber-optics, GPS satellite navigation, mobile radio, and communications transmitters and receivers.

The IAM series of Gilbert multiplier-based frequency converters is fabricated using Hewlett Packard's 10 GHz f_T 25 GHz f_{MAX} ISOSAT™-1 silicon bipolar process. This process uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization, and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Plastic SO-8 Package



Functional Block Diagram and Pin Configuration



Pin Description	
1 IF Output	8 RF Ground (optional)
2 V_{ee}, AC Ground	7 V_{CC}
3 V_{ee}, AC Ground Thermal Contact	6 LO Ground (optional)
4 RF Input	5 LO Input

Absolute Maximum Ratings[1] (T_A = 25°C)

Symbol	Parameter	Units	Value
V_d	Device Voltage	V	15
P_t	Total Device Dissipation[2]	mW	1200
$P_{in\ RF}$	RF Input Power	dBm	+14
$P_{in\ LO}$	LO Input Power	dBm	+14
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to +150

θ_{jc}	Thermal Resistance Junction to Case[3]	°C/W	92

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Derate at 10.9 mW/°C for $T_{PIN\ 3}$ > 40°C.
3. T_j = 150°C.

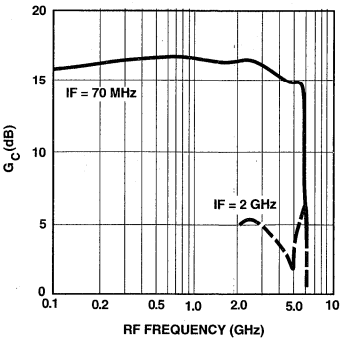


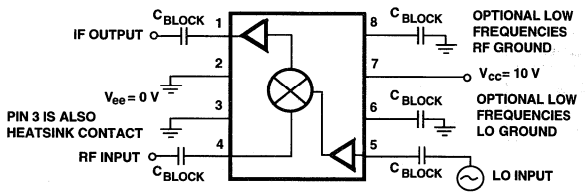
Figure 1. Typical RF to IF Conversion Gain vs. RF Frequency, T_A = 25°C, Low Side LO.

IAM-82008 Electrical Specifications

V_{CC} = 10 V, Z_O = 50 Ω, LO = 0 dBm, RF = -20 dBm, T_A = 25°C

Symbol	Parameter	Units	Minimum	Typical	Maximum
G_C	Conversion Gain, RF = 2 GHz, LO = 1.75 GHz	dB	13	15	17
$f_{3\ dB}$ RF	RF Bandwidth (G_C 3 dB down), IF = 250 MHz	GHz		5.5	
$f_{3\ dB}$ IF	IF Bandwidth (G_C 3 dB down), LO = 2 GHz	GHz		0.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression, RF = 2 GHz, LO = 1.75 GHz	dBm		8	
IP_3	Third Order Inpercept Point, RF = 2 GHz, LO = 1.75 GHz	dBm		18	
NF	SSB Noise Figure	dB		19	
VSWR	RF Port VSWR			1.5:1	
	LO Port VSWR			2.0:1	
	IF Port VSWR			2.5:1	
RF_{if}	RF Feedthrough at IF Port	dBc		-30	
LO_{if}	LO Leakage at IF Port	dBm		-15	
LO_{rf}	LO Leakage at RF Port	dBm		-22	
I_{CC}	Supply Current	mA	40	55	65

Note:
1. The recommended operating voltage range for this device is 7 to 13 V. Typical performance as a function of voltage is shown on the following page.



Notes:
1. No external baluns are required.
2. Good heatsinking required on Pin 3 for specified performance.

Figure 2. IAM-82008 Typical Biasing Configuration.

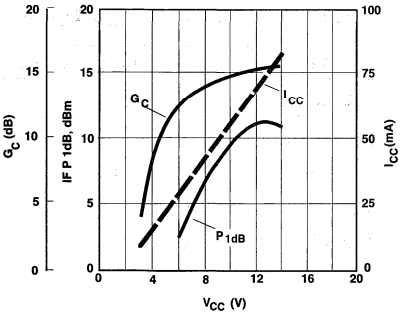


Figure 3. Typical Conversion Gain, IF $P_{1\,dB}$, and I_{CC} Current vs. V_{CC} Bias Voltage, T_A = 25°C, RF: -20 dBm at 2 GHz, LO: 0 dBm at 1.75 GHz.

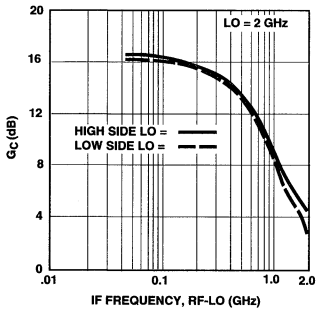


Figure 4. Typical RF to IF Conversion Gain vs. IF Frequency, T_A = 25°C, V_{CC} = 10 V, LO: 0 dBm at 2 GHz.

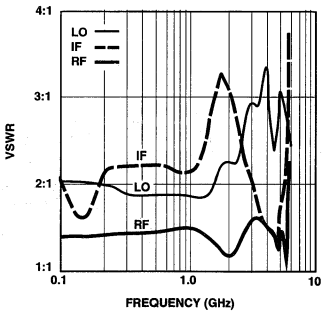


Figure 5. RF, LO, and IF Port VSWR vs. Frequency, T_A = 25°C, V_{CC} = 10 V.

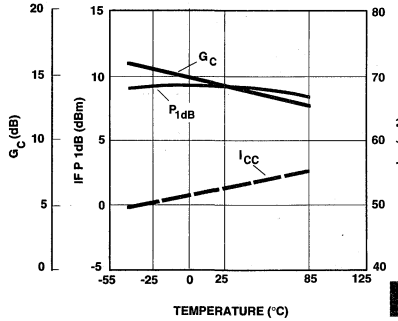


Figure 6. Typical Conversion Gain, IF $P_{1\,dB}$, and I_{CC} Current vs. Case Temperature, T_A = 25°C, V_{CC} = 10 V, RF: -20 dBm at 2 GHz, LO: 0 dBm at 1.75 GHz.

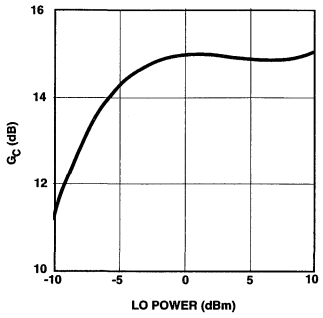


Figure 7. Typical RF to IF Conversion Gain vs. LO Power, T_A = 25°C, V_{CC} = 10 V, RF: -10 dBm at 2 GHz, LO: 0 dBm at 1.75 GHz.

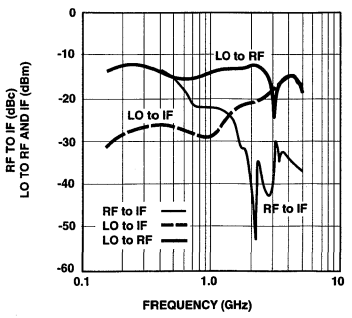


Figure 8. Typical RF Feedthrough Relative to IF Carrier, LO to RF and LO to IF Leakage vs. Frequency, T_A = 25°C, V_{CC} = 10 V, RF: -20 dBm at 2 GHz, LO: 0 dBm at 1.75 GHz.

HARMONIC LO ORDER						
0	–	21	40	73	>75	>75
1	12	0	51	60	>75	>75
2	6	22	41	>75	>75	>75
3	24	18	40	74	>75	>75
4	22	33	52	75	>75	>75
5	41	36	55	>75	>75	>75
	0	1	2	3	4	5

HARMONIC RF ORDER
Xmn = Pif – P(m*rf-n*lo)

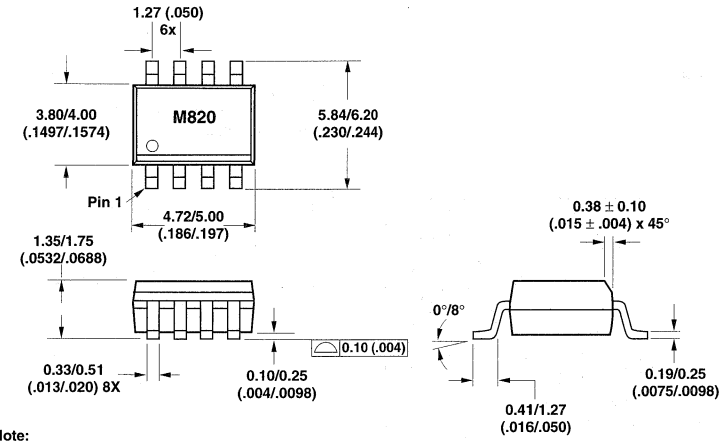
Figure 9. Harmonic Intermodulation Suppression (dB Below Desired Output) RF at 1 GHz, LO at 0.752 GHz, IF at 0.248 GHz.

Part Number Ordering Information

Part Number	No. of Devices	Container
IAM-82008-TR1	1000	7" Reel
IAM-82008-STR	10	Strip

Package Dimensions

SO-8 Plastic Package



Note:
1. Dimensions are shown in millimeters (inches).

HEWLETT® PACKARD

Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/ IF Amp

Technical Data

IAM-82028

Features

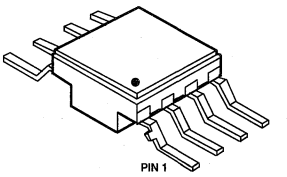
- **15 dB RF-IF Conversion Gain from 0.05 - 5 GHz**
- **IF Output from DC to 2 GHz**
- **IF Output P_{1dB} up to +12 dBm**
- **Single Polarity Bias Supply:** V_{CC} = 7 to 13 V
- **Load-Insensitive Performance**
- **Conversion Gain Flat Over Temperature**
- **Low LO Power Requirements:** 0 dBm Typical
- **Low RF to IF Feedthrough, Low LO Leakage**
- **Hermetic Ceramic Surface Mount Package**

Description

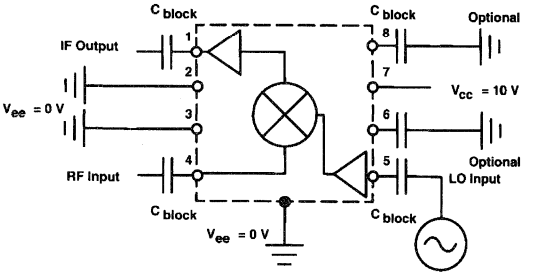
The IAM-82028 is a complete moderate-power double-balanced active mixer housed in a miniature ceramic hermetic surface mount package. It is designed for narrow or wide bandwidth commercial, industrial and military applications having RF inputs up to 5 GHz and IF outputs from DC to 2 GHz. Operation at RF and LO frequencies less than 50 MHz can be achieved using optional external capacitors to ground. The IAM-82028 is particularly well suited for applications that require load-insensitive conversion gain and good spurious signal suppression and moderate dynamic range with minimum LO power. Typical applications include frequency downconversion, modulation, demodulation and phase detection for fiber-optic, GPS satellite navigation, mobile radio, and communications receivers.

The IAM series of Gilbert multiplier-based frequency converters is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

28 Package



Typical Biasing Configuration and Functional Block Diagram



Note: No external BALUNs are required.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	15 V
Power Dissipation[2,3]	1200 mW
RF Input Power	+14 dBm
LO Input Power	+14 dBm
Junction Temperature	200°C
Storage Temperature	-65°C to 200°C

Thermal Resistance:[2,4]
θ_{jc} = 45°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 22.2 mW/°C for T_C >146°C.
4. See MEASUREMENTS section "Thermal Resistance" in Communications Components Catalog, for more information.

IAM-82028 Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: V_{CC} = 10 V, V_{ee} = 0 V, V_{gc} = 0 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_C	Conversion Gain	RF = 2 GHz, LO = 1.75 GHz	dB	13.5	15	16.5
$f_{3dB}RF$	RF Bandwidth (G_C 3 dB Down)	IF = 250 MHzz	GHz		5.5	
$f_{3dB}IF$	IF Bandwidth (G_C 3 dB Down)	LO = 2 GH	GHz		0.6	
P_{1dB}	IF Output Power at 1 dB Gain Compression	RF = 2 GHz, LO = 1.75 GHz	dBm		8	
IP_3	IF Output Third Order Intercept Point	RF = 2 GHz, LO = 1.75 GHz	dBm		18	
NF	SSB Noise Figure	RF = 2 GHz, LO = 1.75 GHz	dB		16	
VSWR	RF Port VSWR	f = 0.05 to 5 GHz			1.5:1	
	LO Port VSWR	f = 0.05 to 5 GHz			2:1	
	IF Port VSWR	f < 2 GHz			2.3:1	
RF_{if}	RF Feedthrough at IF Port	RF = 2 GHz, LO = 1.75 GHz	dBc		-30	
LO_{if}	LO Leakage at IF Port	LO = 1.75 GHz	dBm		-20	
LO_{rf}	LO Leakage at RF Port	LO = 1.75 GHz	dBm		-30	
I_{CC}	Supply Current		mA	40	55	65

Note:
1. The recommended operating voltage range for this device is 7 to 13 V. Typical performance as a function of voltage is on the following page.

Typical Performance, T_A = 25°C, V_{CC} = 10 V
RF: -20 dBm at 2 GHz, LO: 0 dBm at 1.75 GHz
(unless otherwise noted)

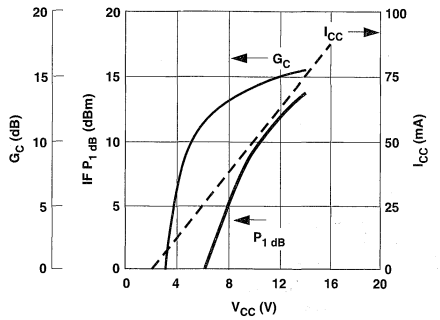


Figure 1. Conversion Gain, IF $P_{1\ dB}$ and I_{CC} Current vs. V_{CC} Bias Voltage.

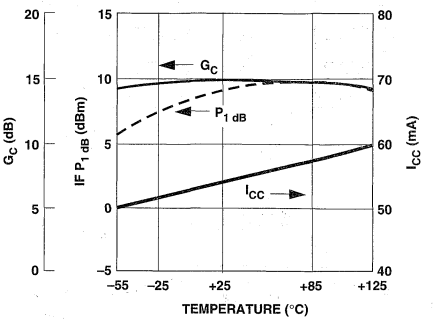


Figure 2. Conversion Gain, IF $P_{1\ dB}$ and I_{CC} Current vs. Case Temperature.

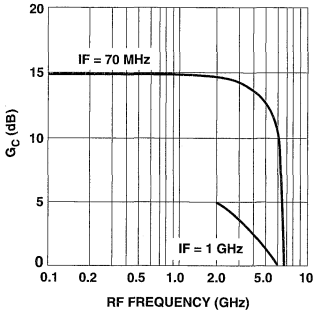


Figure 3. Typical RF to IF Conversion Gain vs. RF Frequency, T_A = 25°C (Low Side LO).

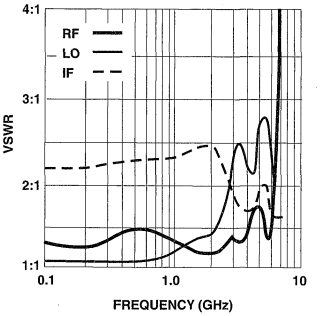


Figure 4. RF, LO and IF Port VSWR vs. Frequency.

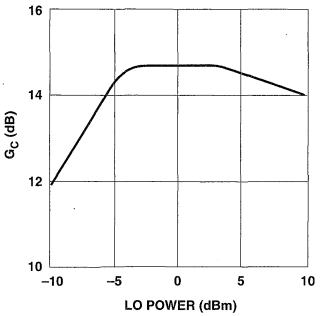


Figure 5. RF to IF Conversion Gain vs. LO Power.

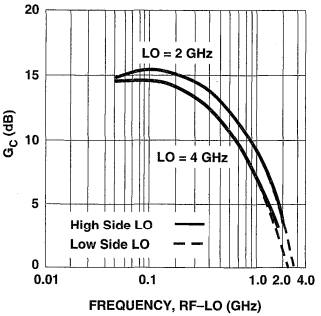


Figure 6. RF to IF Conversion Gain vs. IF Frequency.

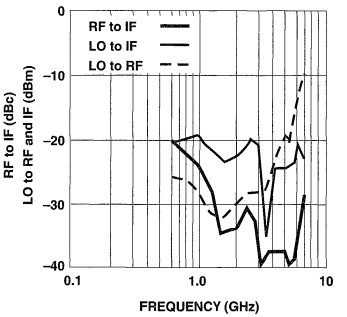


Figure 7. RF Feedthrough Relative to IF Carrier, dBm LO to RF and IF Leakage vs. Frequency.

HARMONIC LO ORDER

	0	1	2	3	4	5
0	—	23	40	>75	>75	>75
1	12	0	52	60	>75	>75
2	6	35	43	>75	>75	>75
3	27	18	59	74	>75	>75
4	22	38	52	>75	>75	>75
5	41	36	73	74	>75	>75

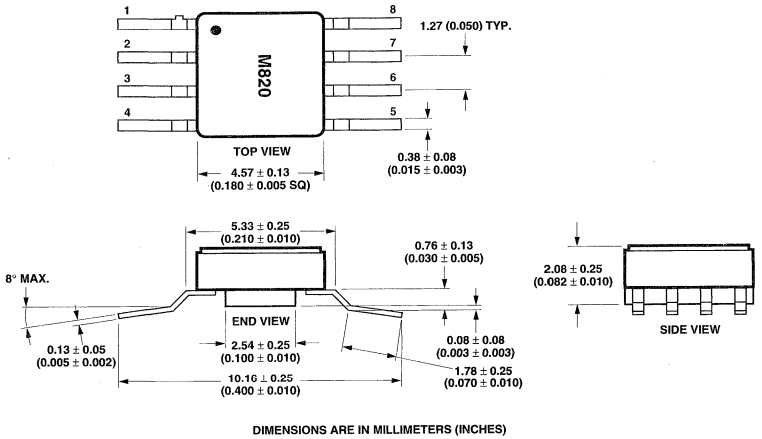
HARMONIC RF ORDER

Xmn = Pif – P(m•rf – n•lo)

Figure 8. Harmonic Intermodulation Suppression (dB Below Desired Output)
RF at 1 GHz, LO at 0.752 GHz, IF at 0.248 GHz.

Package Dimensions

28 Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

HEWLETT® PACKARD

0.8–6 GHz 3 V Downconverter

Technical Data

IAM-91563

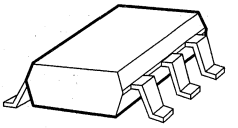
Features

- **+0 dBm Input IP_3 at 1.9 GHz**
- **Single +3V Supply**
- **8.5 dB SSB Noise Figure at 1.9 GHz**
- **9.0 dB Conversion Gain at 1.9 GHz**
- **Ultra-miniature Package**

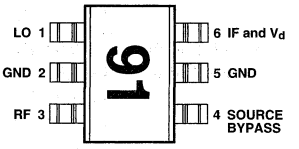
Applications

- **Downconverter for PCS, PHS, ISM, WLL, and other Wireless Applications**

Surface Mount Package SOT-363 (SC-70)

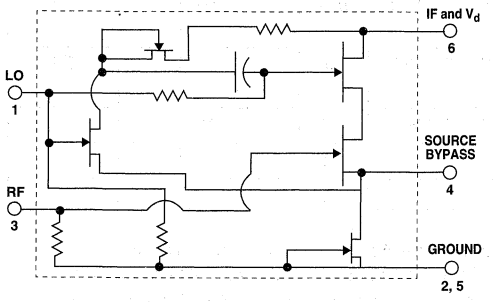


Pin Connections and Package Marking



Note:
1. Package marking provides orientation and identification.

Simplified Schematic



Description

Hewlett-Packard's IAM-91563 is an economical 3V GaAs MMIC mixer used for frequency down-conversion. RF frequency coverage is from 0.8 to 6 GHz and IF coverage is from 50 to 700 MHz. Packaged in the SOT-363 package, this 4.0 sq. mm. package requires half the board space of a SOT-143 and only 15% the board space of an SO-8 package.

At 1.9 GHz, the IAM-91563 provides 9 dB of conversion gain, thus eliminating an RF or IF gain stage normally needed with a lossy mixer. LO drive power is nominally only -5 dBm, eliminating an LO buffer amplifier. The 8.5 dB noise figure is low enough to allow the system to use a low cost LNA. The -6 dBm Input IP_3 provides adequate system linearity for most commercial applications, but is adjustable to 0 dBm.

The circuit uses GaAs PHEMT technology with proven reliability, and uniformity. The MMIC consists of a cascode FET structure that provides unbalanced gm modulation type mixing. An on-chip LO buffer amp drives the mixer while bias circuitry allows a single +3V supply (through a choked IF port). The LO port is internally matched to 50 Ω. The RF and IF ports are high impedance and require external matching networks.

5965-9973E

IAM-91563 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Device Voltage, RF output to ground	V	6.0
V_{RF}, V_{LO}	RF voltage or LO voltage to ground	V	+0.5, -1.0
P_{in}	CW RF Input Power	dBm	+13
T_{ch}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{ch-c} = 310°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

IAM-91563 Electrical Specifications, $T_C = 25°C$, $V_d = 3V$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.	Std Dev[2]
G_{test}	Gain in test circuit[1] RF=1890 GHz, IF=250 MHz		dB	4.0	9.0		
NF_{test}	Noise Figure in test circuit[1] RF=1890 GHz, IF=250 MHz		dB		8.5	11.0	
I_d	Device Current		mA	6.0	9.0	12.0	
NF	Noise Figure (RF & IF with external matching, IF=250 MHz, LO power=-5 dBm)	f = 0.9 GHz	dB		7.0		0.5
		f = 1.9 GHz			8.5		
		f = 2.4 GHz			11.0		
		f = 4.0 GHz			16.5		
		f = 6.0 GHz			18.0		
G_c	Conversion gain (RF and IF with external matching, IF=250 MHz, LO power=-5 dBm)	f = 0.9 GHz	dB		11.0		1.5
		f = 1.9 GHz			9.0		
		f = 2.4 GHz			7.7		
		f = 4.0 GHz			4.6		
		f = 6.0 GHz			1.7		
$P_{1\,dB}$	Output power @ 1 dB compression (RF and IF with external matching, IF=250 MHz, LO power =-5 dBm)	f = 0.9 GHz	dBm		-6.7		1.3
		f = 1.9 GHz			-8.0		
		f = 2.4 GHz			-8.7		
		f = 4.0 GHz			-15.0		
		f = 6.0 GHz			-17.8		
RL_{RF}	RF port return loss	f = 0.5 - 6.0 GHz	dB		-1.7		0.2
RL_{LO}	LO port return loss	f = 0.5 - 6.0 GHz	dB		-9.4		0.3
RL_{IF}	IF port return loss	f = 50 - 700 MHz	dB		-3.7		0.2
IP_3	Input Third Order Intercept Point I_d = 9.0 mA, LO power = -5 dBm	RF = 1.9 GHz, IF = 250 MHz	dBm		-6.0		1.3
IP_3	Input Third Order Intercept Point I_d = 15 mA, LO power = -2 dBm	RF = 1.9 GHz, IF = 250 MHz	dBm		0		1.1
$ISOL_{L-R}$	LO-RF Isolation	RF = 1.9 GHz	dB		18		
$ISOL_{R-I}$	RF-IF Isolation (No Match)		dB		2		
$ISOL_{L-I}$	LO-IF Isolation (No Match)		dB		4		

Notes:
1. Guaranteed specifications are 100% tested in the circuit in Figure 18 in the Applications Information section.
2. Standard deviation number is based on measurement of at least 500 parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.

IAM-91563 Typical Performance, $T_C = 25°C$, $V_d = 3.0$ V, RF = 1890 MHz, LO = -5 dBm, IF = 250 MHz, unless otherwise stated.

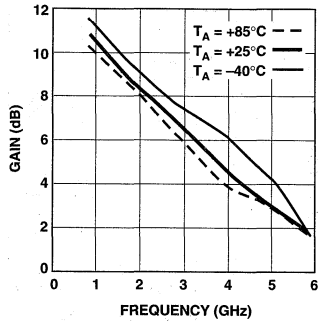


Figure 1. Available Conversion Gain vs. Frequency and Temperature.

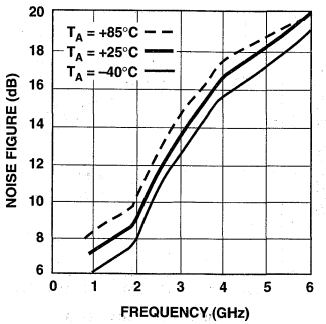


Figure 2. Noise Figure (into 50 Ω) vs. Frequency and Temperature.

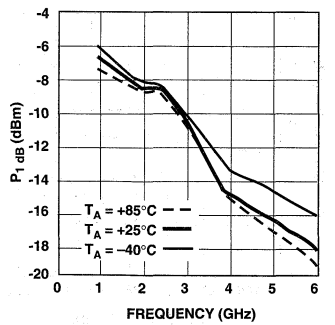


Figure 3. Output Power (@ 1 dB Compression) vs. Frequency and Temperature.

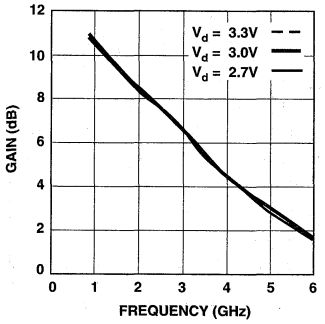


Figure 4. Available Conversion Gain vs. Frequency and Voltage.

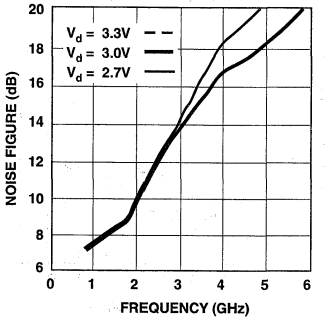


Figure 5. Noise Figure (into 50 Ω) vs. Frequency and Supply Voltage.

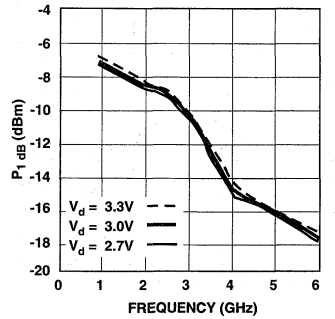


Figure 6. Output Power (@ 1 dB Compression) vs. Frequency and Voltage.

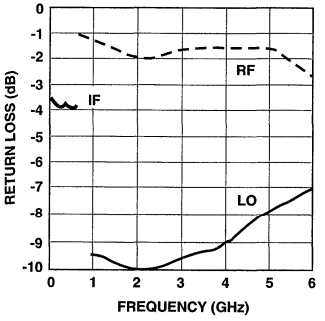


Figure 7. RF, LO, and IF Return Loss vs. Frequency.

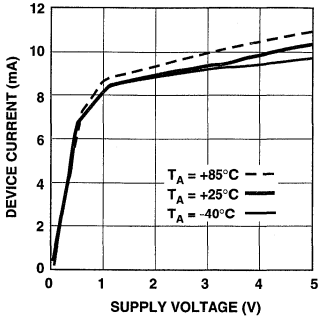


Figure 8. Device Current vs. Supply Voltage and Temperature.

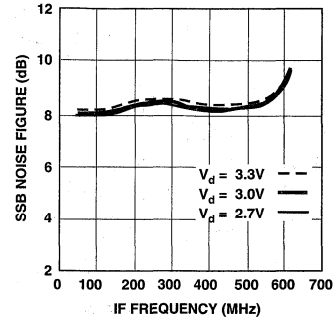


Figure 9. SSB Noise Figure vs. Frequency and Supply Voltage.

IAM-91563 Typical Performance, $T_C = 25°C$, $V_d = 3.0$ V, RF = 1890 MHz, LO = -5 dBm, IF = 250 MHz, unless otherwise stated.

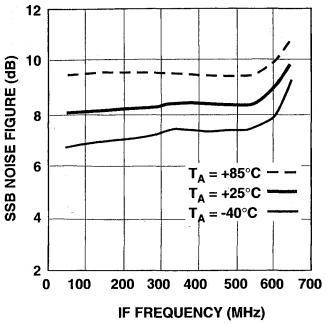


Figure 10. SSB Noise Figure vs. Frequency and Temperature.

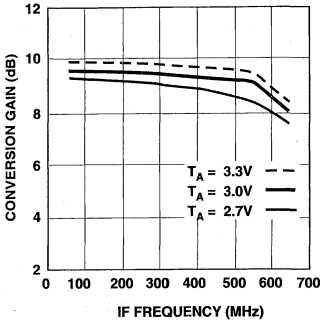


Figure 11. Conversion Gain vs. Frequency and Supply Voltage.

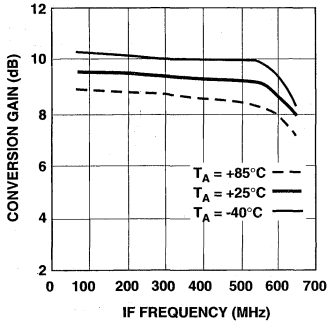


Figure 12. Conversion Gain vs. Frequency and Temperature.

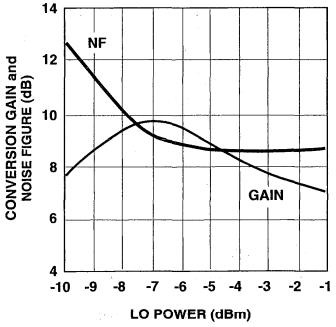


Figure 13. Available Conversion Gain and Noise Figure vs. LO Drive Power.

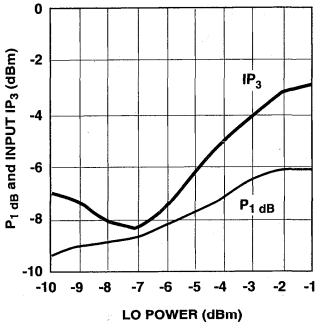


Figure 14. One dB Compression and Input Third Order Intercept vs. LO Drive Power.

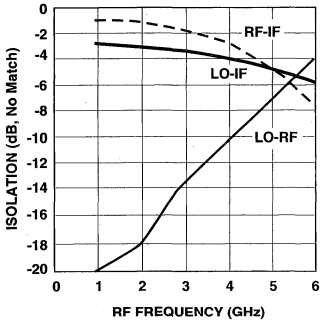


Figure 15. Isolation (LO-RF, RF-IF, LO-IF) vs. Frequency with no RF and IF Matching Networks.

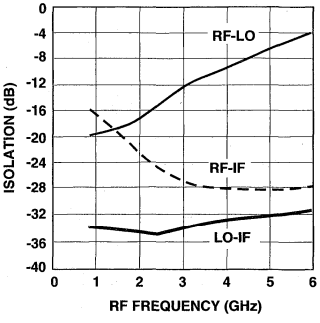


Figure 16. Isolation (RF-LO, RF-IF, LO-IF) vs. Frequency with RF and IF Matching Networks.

IAM-91563 Typical Reflection Coefficients, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_d = 3\ V$

Frequency (GHz)	RF (Mag)	RF (Ang)	LO (Mag)	LO (Ang)	IF (Mag)	IF (Ang)
0.1			0.43	-1	0.64	-8
0.2			0.39	-6	0.63	-9
0.3			0.39	-8	0.63	-10
0.4			0.39	-9	0.63	-10
0.5			0.39	-10	0.62	-11
0.6			0.39	-11	0.62	-12
0.7			0.40	-14	0.62	-13
0.8	0.91	-18	0.39	-14		
0.9	0.91	-21	0.39	-16		
1	0.91	-23	0.38	-17		
1.1	0.92	-25	0.39	-17		
1.2	0.91	-28	0.39	-19		
1.3	0.88	-29	0.40	-22		
1.4	0.87	-32	0.39	-22		
1.5	0.85	-33	0.39	-24		
1.6	0.84	-34	0.39	-25		
1.7	0.83	-35	0.39	-26		
1.8	0.82	-37	0.39	-27		
1.9	0.82	-37	0.38	-29		
2	0.81	-39	0.39	-29		
2.1	0.81	-40	0.38	-31		
2.2	0.81	-41	0.38	-31		
2.3	0.81	-42	0.37	-32		
2.4	0.81	-44	0.37	-33		
2.5	0.80	-45	0.36	-34		
2.6	0.80	-45	0.36	-35		
2.7	0.81	-46	0.35	-36		
2.8	0.81	-48	0.35	-36		
2.9	0.81	-50	0.34	-37		
3	0.82	-51	0.34	-37		
3.1	0.83	-53	0.33	-38		
3.2	0.83	-55	0.33	-39		
3.3	0.83	-56	0.32	-39		
3.4	0.85	-59	0.32	-40		
3.5	0.86	-61	0.31	-40		
3.6	0.87	-64	0.32	-42		
3.7	0.85	-67	0.31	-42		
3.8	0.83	-71	0.30	-45		
3.9	0.83	-71	0.30	-43		
4	0.82	-73	0.29	-46		
4.1	0.83	-76	0.29	-45		
4.2	0.83	-79	0.28	-47		
4.3	0.84	-82	0.29	-48		
4.4	0.84	-85	0.27	-49		
4.5	0.84	-87	0.28	-50		
4.6	0.85	-91	0.26	-51		
4.7	0.84	-95	0.28	-52		
4.8	0.85	-97	0.25	-52		
4.9	0.85	-100	0.27	-54		
5	0.85	-103	0.25	-54		
5.1	0.86	-106	0.27	-57		
5.2	0.85	-108	0.25	-56		
5.3	0.84	-113	0.27	-58		
5.4	0.84	-115	0.25	-58		
5.5	0.84	-117	0.27	-61		
5.6	0.83	-121	0.25	-61		
5.7	0.83	-123	0.27	-64		
5.8	0.81	-125	0.25	-65		
5.9	0.81	-128	0.26	-67		
6	0.80	-130	0.24	-65		

IAM-91563 Applications Information

Introduction

The IAM-91563 is a miniature downconverter developed for use in superheterodyne receivers for commercial wireless applications with RF bands from 800 MHz to 6 GHz. Operating from only 3 volts, the IAM-91563 is an excellent choice for use in low current applications such as: 1.9 GHz Personal Communication Systems (PCS) & Personal Handy System (PHS), 2 GHz Digital European Cordless Telephone (DECT), and 800 MHz cellular telephones (e.g., GSM, NADC, JDC). Combined with Hewlett-Packard's other RFICs and discrete components housed in the same ultra-miniature SOT-363 package, the IAM-91563 also provides flexible, building-block solutions for WLAN's and wireless datacomm such as PCMCIA RF modems as well as many Industrial, Scientific and Medical (ISM) systems operating at 900 MHz, 2.5 GHz, and 5.8 GHz.

The IAM-91563 is a 3-port, downconverting RFIC mixer of the cascode (common source - common gate) type that uses a low level (-5 dBm) local oscillator (LO) to convert an RF signal in the 800 MHz to 6 GHz range to an IF between 50 and 700 MHz. The basic mixing function takes place in a cascode connected pair of FETs as shown in Figure 17.

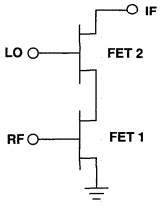


Figure 17. Cascode FET Mixer.

The received RF signal is connected to the gate of FET1 and the LO is applied to the gate of FET2. The purpose of FET2 is to vary the transconductance of FET1 over a highly nonlinear region at the rate of the LO frequency. This produces the nonlinearity required for frequency mixing to take place. This type of mixer is also known as a "transconductance mixer." The IF is taken from the drain of FET2.

An advantage of the cascode type of design is the inherent isolation between the gates of the two FETs which results in very good LO-to-RF isolation. An integrated buffer amplifier between the LO input and the gate of FET2 not only increases the LO-RF isolation but also reduces the amount of LO input power required by the mixer.

The IAM-91563 uses an innovative bias regulation circuit that realizes several benefits to the designer. First, the IAM-91563 operates with a single, positive device voltage from 1.5 to 5 volts with stable performance over a wide temperature range. Second, a unique feature of the IAM-91563 allows the device current to be easily increased by adding an external resistor to boost device current and increase linearity.

Using a minimum of external components with a standard bias of 3 volts/9 mA and LO power of -5 dBm, the IAM-91563 mixer achieves an RF to IF conversion gain of 9 dB at 1.9 GHz with a noise figure of 8.5 dB and an input third order intercept point of -6 dBm. LO-to-IF isolation is greater than 35 dB. Setting the bias for the higher linearity/higher current mode (approximately 16 mA) along with an LO drive level of -2 dBm will boost the input IP_3 to approximately 0 dBm.

Test Circuit

The circuit shown in Figure 18 is used for 100% RF and DC testing. The test circuit is impedance matched for an RF of 1890 MHz and an IF of 250 MHz. The LO is set at 1640 MHz and -5 dBm for low side conversion. (High side conversion with an LO of 2240 MHz would produce similar performance.) The RF choke at the IF port is used to provide DC bias. Tests in this circuit are used to guarantee the G_{test}, NF_{test}, and Device Current (I_d) parameters shown in the table of Electrical Specifications.

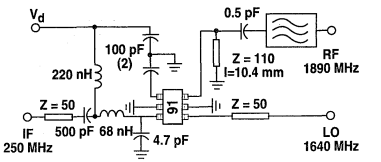


Figure 18. Test Circuit.

Specifications and Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either "minimum or maximum," "typical," or "standard deviations."

The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on of a minimum of 500 parts taken from 3 non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard "bell curve."

Parameters considered to be the most important to system performance are bounded by *minimum*

or *maximum* values. For the IAM-91563, these parameters are: Conversion Gain (G_{test}), Noise Figure (NF_{test}), and Device Current (I_d). Each of these guaranteed parameters is 100% tested.

Values for most of the parameters in the table of Electrical Specifications that are described by *typical* data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as the Typical Reflection Coefficients table or performance curves, the data represents a nominal part taken from the "center" of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate circuit using the IAM-91563, but to also optimize and evaluate trade-offs that affect a complete wireless system, the *standard deviation* (σ) is provided for many of the Electrical Specifications parameters (at 25°) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean. Referring to Figure 12 for example, the probability of a parameter being between $\pm 1\sigma$ is 68.3%; between $\pm 2\sigma$ is 95.4%; and between $\pm 3\sigma$ is 99.7%.

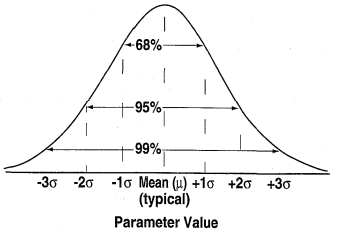


Figure 19. Normal Distribution.

Phase Reference Planes

The positions of the reference planes used to specify Reflection Coefficients for this device are shown in Figure 20. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

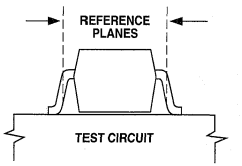


Figure 20. Phase Reference Planes.

RF Layout

An RF layout similar to the one in Figure 21 is suggested as a starting point for microstripline designs using the IAM-91563 mixer. This layout shows the capacitor for the Source Bypass pin and the optional resistor used to increase bias current. Adequate grounding is important to obtain maximum performance and to maintain stability. Both of the ground pins of the MMIC should be connected to the RF groundplane on the backside of the PCB by means of plated through holes (vias) that are placed near the package terminals. As a minimum, one via should be located next to each of the ground pins to ensure good RF grounding. It is a good practice to use multiple vias to further minimize ground path inductance.

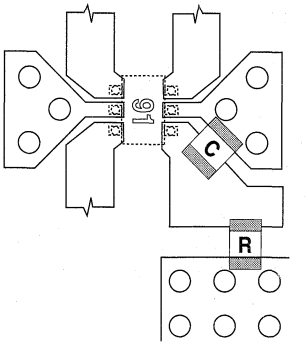


Figure 21. RF Layout.

It is recommended that the PCB pads for the ground pins *not* be connected together underneath the body of the package. PCB traces hidden under the package cannot be adequately inspected for SMT solder quality.

PCB Material

FR-4 or G-10 printed circuit board materials are a good choice for most low cost wireless applications. Typical board thickness is 0.020 to 0.031 inches. Thicknesses greater than 0.031 inch began to introduce excessive inductance in the ground vias. The width of the 50 Ω microstriplines on PC boards in this thickness range is also very convenient for mounting chip components such as the series inductor at the input or DC blocking and bypass capacitors.

For applications using higher frequencies such as the 5.8 GHz ISM band, the additional cost of PTFE/glass dielectric materials may be warranted to minimize transmission line loss at the mixer's RF input. An additional consideration of using lower cost

materials at higher frequencies is the degradation in the Q's of transmission lines used for impedance matching.

Biasing

The IAM-91563 is a voltage-biased device and is designed to operate in the "normal mode" from a single, +3 volt power supply with a typical current drain of only 9 mA. The internal current regulation circuit allows the mixer to be operated with voltages as high as +5 volts or as low as +1.5 volt.

The device current can be increased up to 20 mA by adding an external resistor from the Source Bypass pin to ground. This feature makes it possible to operate the IAM-91563 in the "high power mode" to achieve greater linearity. Refer to the section titled "High Linearity Mode" for information on applications and performance when using this feature.

Application Guidelines

Several design considerations should be taken into account to ensure that maximum performance is obtained from the IAM-91563 downconverter. The RF and IF ports must be impedance matched at their respective frequencies to the circuits to which they are connected. This is typically 50 ohms when the mixer is used as a building block component in a 50-ohm system. These ports have been left untuned on the MMIC to allow the mixer to be used over a wide range of RF and IF bands. The LO port is already sufficiently well matched (less than 1 dB of mismatch loss) for most applications.

As with most mixers, appropriate filters must be placed at the RF port and IF port such as in Figure 22. The filter in front of the RF port eliminates interference from the image frequency and the IF filter prevents RF and LO signal leakage into the IF signal processing circuitry.

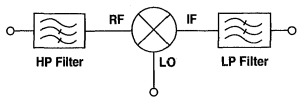


Figure 22. Image and IF Filters.

Additional design considerations relate to the use of higher bias current where greater linearity is required, bypassing of the Source Bypass pin, bias injection, and DC blocking and bypassing.

Each of these design factors will be discussed in greater detail in the following sections.

RF Port

A well matched RF port is especially important to maximize the conversion gain of the IAM-91563 mixer. Matching is also necessary to realize the specified noise figure and RF-to-LO isolation. The amount the conversion gain can be increased by impedance matching is equal to the mismatch loss at the RF port. The impedance of the RF port is characterized by the measured reflection coefficients shown in Typical Reflection Coefficients Table. The maximum "mismatch gain" that results from eliminating the mismatch loss is expressed in dB as a function of the reflection coefficient as:

$$G_{RF,\,mm} = 10 \log_{10}\left(\frac{1}{1-|\Gamma_{RF}|^2}\right) \qquad (1)$$

For wireless bands in the 800 MHz to 6 GHz range, the magnitude of the reflection coefficient of the RF port varies from 0.91 to 0.80, which corresponds to a mismatch gain of 7.6 to 4.4 dB.

The impedance of the RF port is capacitive, and for frequencies from 800 MHz to 2.4 GHz, falls very near the R=1 circle of a Smith chart. While these impedances could be easily matched to 50 ohms with a simple series inductor, it is advantageous to use a 2-element matching network of the series C, shunt L type as shown in Figure 23 instead. There are two main reasons for this choice. The first is to incorporate a high pass filter characteristic into the matching circuit. Second, the series C, shunt L combination will match the entire range of RF port impedances to 50 Ω. Most wireless communication bands are sufficiently narrow that a single (mid-band) frequency approach to impedance matching is adequate.

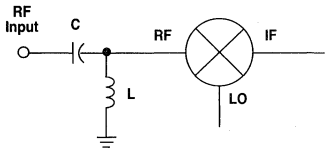


Figure 23. RF Input HPF Matching.

Impedance matching can be accomplished with lumped element components, transmission lines, or a combination of both. The use of surface mount inductors and capacitors is convenient for lower frequencies to minimize printed circuit board space. The use of high impedance transmission lines works well for higher frequencies where lumped element inductors may have excessive parasitics and/or self resonances.

If other types of matching networks are used, it should be noted that while the RF input terminal of the IAM-91563 is at ground potential, it should not be used as a current sink. If the input is

connected directly to a preceding stage that has a voltage present, a DC blocking capacitor should be used.

IF port

The IAM-91563 can be used for downconvesion to intermediate frequencies in the 50 to 700 MHz range. Similar to the RF port, the reflection coefficient at the IF is fairly high and Equation 1 can be used to predict a mismatch gain of up to 2.2 dB by impedance matching. A well matched IF port will also provide the optimum output power and LO-to-IF isolation. Reflection coefficients for the IF port are shown in the Typical Reflection Coefficients Table.

The IF port impedance matching network should be of the low pass filter type to reflect RF and LO power back into the mixer while allowing the IF to pass through. The shunt C, series L type of network in Figure 24 is a very practical choice that will meet the low pass filter requirement while matching any IF impedances over the 50 - 700 MHz range to 50 ohms.

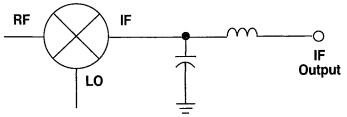


Figure 24. IF Output LPF Matching.

The DC bias is also applied to the mixer through the IF port. Figure 25 shows how an inductor (RFC) is used to isolate the IF from the DC supply. The bias line is bypassed to ground with a capacitor to keep RF off of the DC supply lines and to prevent dips or peaks in the response of the mixer.

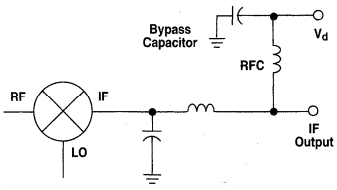


Figure 25. Bias Connection.

LO Port

The LO input port is internally matched to 50 Ω within a 2.2:1 VSWR over the entire operating frequency range. Additional matching will normally not be needed. However, if desired, a small series inductor can be used to provide some improvement in the LO match and thus reduce the LO drive level requirement by up to 0.7 dB. Reflection coefficients for the LO port are shown in the table of Typical Reflection Coefficients.

Source Bypass Pin

The Source Bypass pin should be RF bypassed to ground at both the RF and LO frequencies as well as the IF. Many capacitors with values large enough to adequately bypass lower intermediate frequencies contain parasitics that may have resonances in the RF band. It is often practical to use two capacitors in parallel for this purpose instead of one. A small value, high quality capacitor is used to bypass the RF/LO frequencies and a large value capacitor for the IF. When biased in the high linearity mode, a resistor is added from the Source Bypass pin to ground.

High Linearity Mode

The IAM-91563 has a feature that allows the user to place an external resistor from the Source Bypass pin to ground and increase the device current from a nominal 9 mA to as high as 20 mA. The additional current increases mixer linearity (IP_3) and output power(P_{1dB}). Mixer performance at higher device current is shown in Figures 26 and 27.

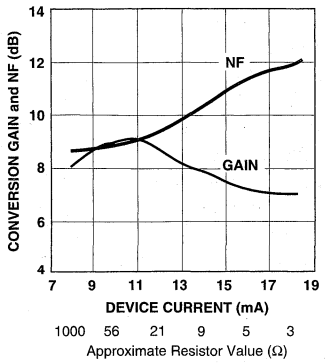


Figure 26. Available Conversion Gain and SSB Noise Figure vs. Device Current (Source Resistor).

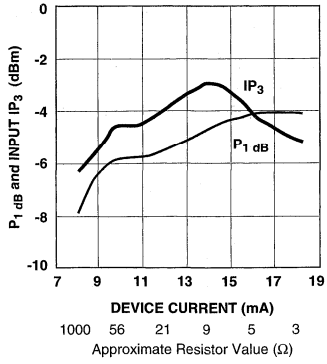


Figure 27. One dB Compression and Input Third Order Intercept Point vs. Device Current (Resistor).

As an example of improved linearity, the use of a 15 Ω resistor at the Source Bypass pin increases the device current to 14 mA. At 1.9 GHz, the input IP_3 is increased from -6.5 dBm to -3 dBm. Increasing the LO drive level from -5 dBm to -1 dBm further increases the input IP_3 to 0 dBm.

Application Example

The printed circuit layout in Figure 28 is a general purpose layout that will accommodate components for using the IAM-91563 for RF inputs from 800 MHz to 6 GHz. This layout is a microstripline design (solid groundplane on the backside of the circuit board) with 50 Ω interfaces for the RF input, IF output, and LO input. The circuit is fabricated on 0.031-inch thick FR-4 dielectric material. Plated through holes (vias) are used to bring the ground to the top side of the circuit where needed. Multiple vias are used to reduce the inductance of the paths to ground.

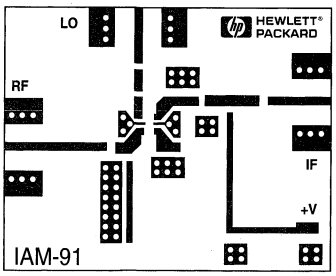


Figure 28. PCB Layout.

1.9 GHz Design Example

To illustrate a design approach for using the IAM-91563, a PCS band downconverter with an RF of 1.9 GHz and IF of 110 MHz is presented. The PCB layout above was used to assemble the mixer and verify performance.

A schematic diagram of the 1.9 GHz circuit is shown in Figure 29.

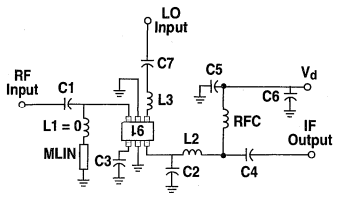


Figure 29. Schematic of Example Application Circuit.

At the RF input port, series capacitor C1 and transmission line MLIN form the input matching network and high pass filter. (Note: The PCB layout above has provision for an inductor, L1, in series with MLIN. Inductor L1 is not used in this design.)

Referring to the table of Reflection Coefficients, the RF input port $\Gamma_{RF} = 0.82 \angle -37°$ at 1.9 GHz. This point is plotted as Point A on the Smith chart in Figure 30. For reasons previously discussed in the "RF Port" section above, a series C - shunt L network (from the 50 Ω source to Γ_{RF}) will be used to match Γ_{RF} to 50 Ω. Addition of a 6.5 nH shunt inductance moves the impedance trajectory from Point A to Point B. The match to 50 Ω is completed with a 0.6 pF series capacitance, C1, that moves the match to Point C, the center of the Smith chart.

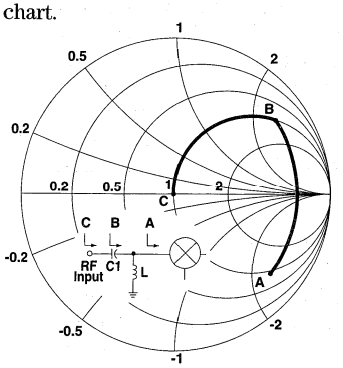


Figure 30. RF Input Impedance Match.

For this example, the shunt inductor was realized with the transmission line, MLIN in Figure 29 (Z_O = 90 Ω, length = 0.35 in.). A high quality capacitor should be selected for C1 to minimize the effects of the capacitor's parasitic inductance and resistance. Series capacitor C1 also serves to block any DC that may be present at the output of the stage preceding the mixer.

At the IF output, the low pass filter and impedance match is formed by shunt capacitor C2 and series inductor L2. Referring again to the table of Reflection Coefficients, the IF output port Γ_{IF} = $0.64 \angle -8°$ at 100 MHz, which is the frequency point closest to the desired IF of 110 MHz. Γ_{IF} is plotted as Point A in Figure 31.

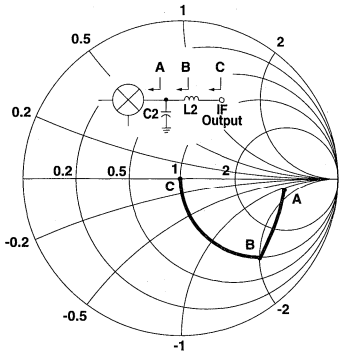


Figure 31. IF Input Impedance Match.

Adding a shunt capacitance (C2) of 11.3 pF brings the impedance to Point B. The match to Point C at the center of the chart is completed with a series inductance (L2) of 150 nH.

Although not necessary for many applications, the match at the LO port can be improved by the addition of series inductor L3 with a value of approximately 8 nH. Design information (Γ_{LO}) for matching the LO port is obtained

from the table of Reflection Coefficients. Capacitor C7 is a DC block for the LO port.

DC bias is applied to the IAM-91563 through the RFC at the IF Output pin. The power supply is bypassed to ground with capacitor C5 to keep RF, IF, and LO signals off of the DC bias lines and to prevent gain dips or peaks in the response of the mixer. C4 is a DC blocking capacitor for the output.

The values of the RF bypass capacitors and DC blocking capacitors that are not part of a impedance matching structure (i.e., C3 - C7) should be chosen to provide a small reactance (typically < 5 ohms) at the lowest frequency at the port for which they are used. The reactance of the RF choke (RFC) should be high (e.g., several hundred ohms) at the lowest IF.

The completed 1.9 GHz mixer from the design example above with all components and SMA connectors in place is shown in Figure 32. Again, L1 is not used and is replaced by a metal tab. The length of the shunt transmission line, MLIN, is adjustable by moving the position of the shorting tab between the line and the ground pad. Provision is made for an additional bypass capacitor, C6, to be added to the bias line near the V_d connection to eliminate unwanted RF feedback through bias lines.

When multiple bypass capacitors are used, consideration should be given to potential resonances. It is important to ensure that the capacitors, when combined with additional parasitic L's and C's on the circuit board, do not form resonant circuits. The addition of a small value resistor in the bias supply line between bypass capacitors will often "de-Q" the bias circuit and eliminate resonance effects.

Table 1 below summarizes the component values for the 1.9 GHz design.

Component	Value
C1	0.5 pF
C2	9 pF
C3, C5, C7	100 pF
C4	500 pF
L1	(not used)
L2	100 nH
L3	8.2 nH
MLIN	Z_o=90 Ω l = 0.41 in.
RFC	320 nH

Table 1. Component Values for 1.9 GHz Downconverter.

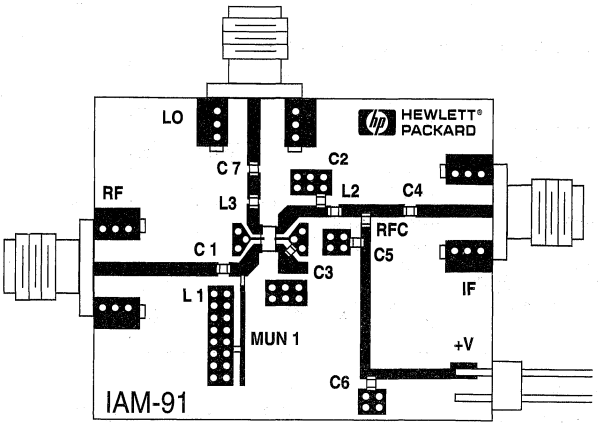


Figure 32. Complete 1.9 GHz Mixer.

The values shown in Table 1 may vary from those used above to describe the basic impedance matching approach. The final component values take into consideration additional effects such as, the various line lengths between components, parasitics in components (e.g., the series inductance in C1), as well as other circuit parasitics. A CAD program such as HP Touchstone® may be used to fully analyze and account for these circuit variables.

The following performance was measured for a 1.9 GHz circuit:

Measured results:

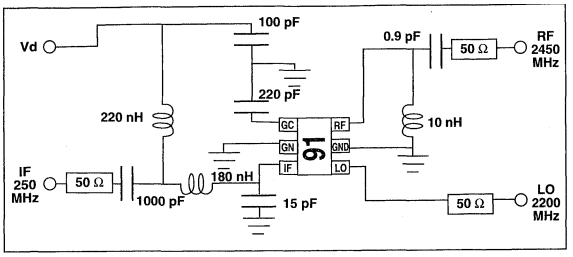
Conversion Gain = 9.0 dB
SSB Noise Figure = 8.5 dB
P_{1dB} (output) = -8.1 dB
IP_3 (Input) = -7 dBm
LO-RF Isolation = 17 dB
LO-IF Isolation = 34 dB
RF-IF Isolation = 23 dB

Operating conditions:

RF Frequency = 1.89 GHz
LO Frequency = 1.78 GHz
IF Frequency = 110 MHz
LO Drive Level = -5 dBm
DC Power = 3.0V @ 9 mA

Designs for Other Frequencies

The same design methodology described above can be applied to other wireless frequency bands. Design examples and measurement results for the 900 MHz and 2.4 GHz bands are shown in Figures 33 and 34.



Measured results:

Conversion Gain = 10.6 dB
SSB Noise Figure = 7.1 dB
1 dB Compression = -7.0 dB
P3 (Input) = -7 dBm

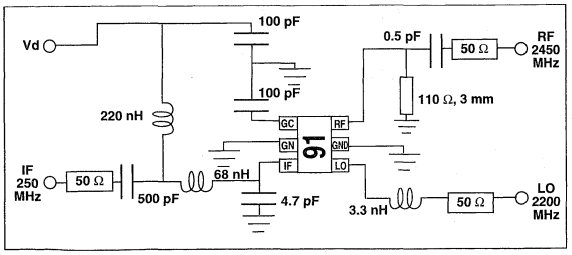
LO-RF Isolation = 21 dB
LO-IF Isolation = 33 dB
RF-IF Isolation = 17 dB

Operating conditions:

RF Frequency = 900 MHz
IF Frequency = 80 MHz
LO Frequency = 980 MHz

LO Drive Level = -5 dBm
DC Power = 3.0V @ 9 mA

Figure 33. 800-900 MHz Cellular and ISM Band Mixer.



Measured results:

Conversion Gain = 7.7 dB
SSB Noise Figure = 11 dB
1 dB Compression = -8.7 dB
IP3 (Input) = -7 dBm

LO-RF Isolation = 16 dB
LO-IF Isolation = 35 dB
RF-IF Isolation = 27 dB

Operating conditions:

RF Frequency = 2.45 GHz
IF Frequency = 250 MHz
LO Frequency = 2.2 GHz

LO Drive Level = -5 dBm
DC Power = 3.0V @ 9 mA

Figure 34. 2.4 GHz ISM Band Mixer.

SOT-363 PCB Footprint

A recommended PCB pad layout for the miniature SOT-363 (SC-70) package used by the IAM-91563 is shown in Figure 35 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the IAM-91563. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads.

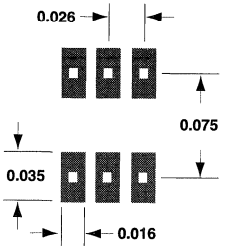


Figure 35. PCB Pad Layout (dimensions in inches).

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-363 package, will reach solder reflow temperatures faster than those with a greater mass.

The IAM-91563 is has been qualified to the time-temperature profile shown in Figure 36. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235 °C.

These parameters are typical for a surface mount assembly process for the IAM-91563. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

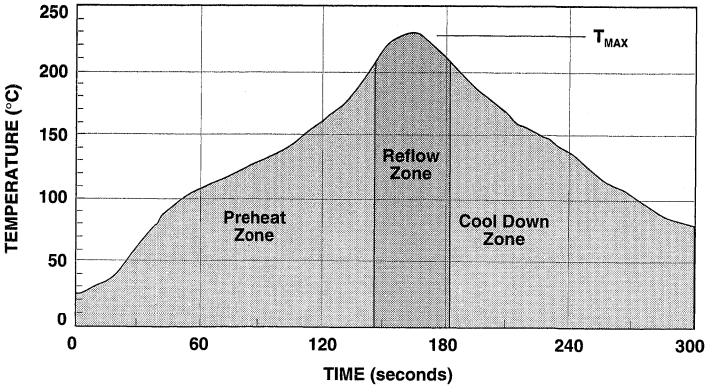


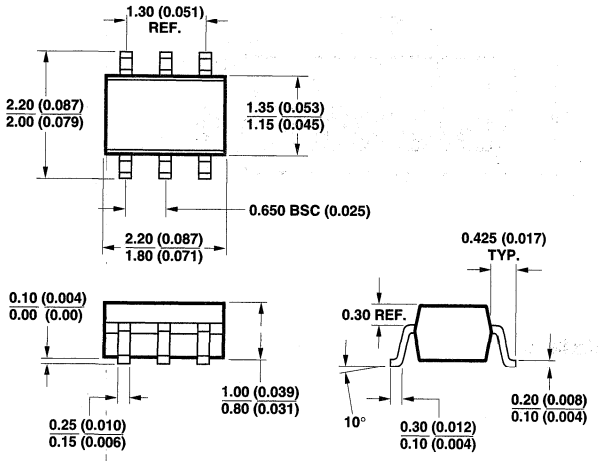
Figure 36. Surface Mount Assembly Profile.

Electrostatic Sensitivity

GaAs MMICs are electrostatic discharge (ESD) sensitive devices. Although the IAM-91563 is robust in design, permanent damage may occur to these devices if they are subjected to high energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without detection and may result in degradation in performance or failure. The IAM-91563 is a ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, and assembling these devices to avoid damage.

Package Dimensions

Outline 63 (SOT-363/SC-70)

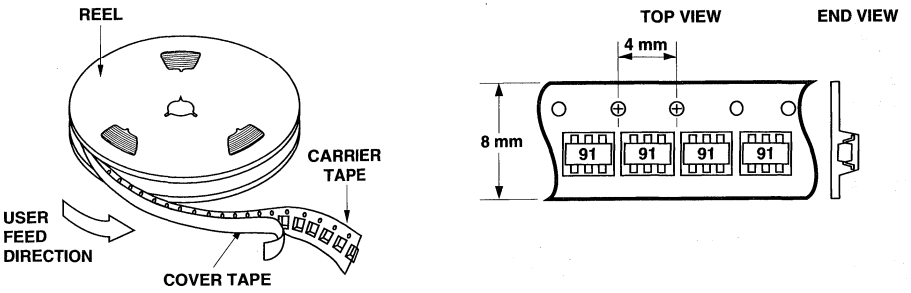


DIMENSIONS ARE IN MILLIMETERS (INCHES)

Part Number Ordering Information

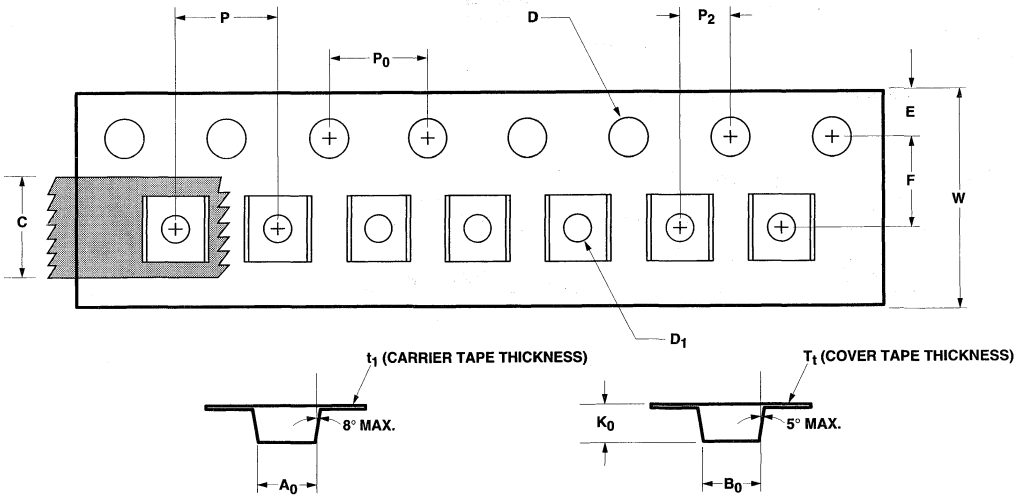
Part Number	No. of Devices	Container
IAM-91563-TR1	3000	7" Reel
IAM-91563-BLK	100	antistatic bag

Device Orientation



Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

HEWLETT® PACKARD

Silicon Bipolar MMIC 3.5 and 5.5 GHz Divide-by-4 Static Prescalers

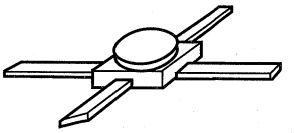
Technical Data

IFD-53010
IFD-53110

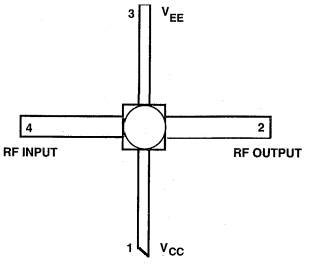
Features

- **Wide Operating Frequency Range:**
  IFD-53010: 0.15 to 5.5 GHz
  IFD-53110: 0.15 to 3.5 GHz
- **Low Phase Noise:**
  -143 dBc/Hz @ 1 kHz Offset
- **Output Power:** -5 dBm Typ.
- **Single Supply Voltage**
  V_{cc} = 5 V or V_{ee} = -5 V
- **On-Chip Terminations Provide Good Input and Output VSWRs**
- **Hermetic Gold-Ceramic Surface Mount Package**

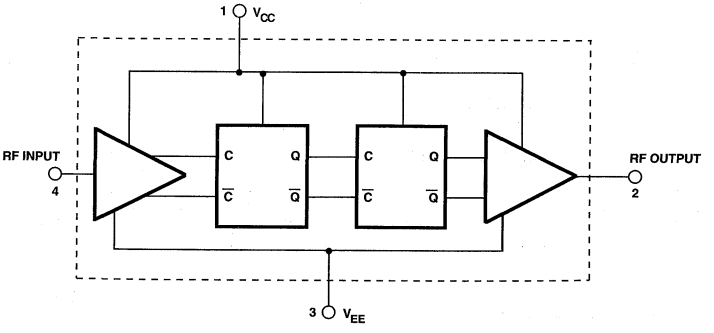
100 mil Stripline Package



Pin Configuration



Functional Block Diagram



Description

Hewlett-Packard's IFD-53010 and IFD-53110 are low phase noise silicon bipolar static digital frequency dividers using two scaled Emitter-Coupled-Logic (ECL) master-slave D flip-flops and buffer amplifiers. They are housed in hermetic high reliability surface mount packages suitable for commercial, industrial, and military applications. Typical applications include stabilized or digitally controlled local oscillators for GPS, SATCOM or military receivers, and frequency synthesizers and counters in instrumentation systems. The IFD-53110 is a lower cost selected version of the IFD-53010, and is distinguished by a reduced operating frequency range.

The IFD series of frequency dividers is fabricated using Hewlett-Packard's 18 GHz, f_t, ISOSAT™-2 silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion-implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent device uniformity, performance, and reliability.

5965-9115E

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{cc} - V_{ee}	Device Voltage	V	8
P_{diss}	Power Dissipation[2,3]	mW	650
P_{in}	RF Input Power	dBm	+15
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to +200

Thermal Resistance[2]: θ_{jc} = 107°C/W

Notes:
1, Operation of this device above any one of these parameters may cause permanent damage.
2. T_{case} = 25°C.
3. Derate at 9.3 mW/°C for $T_C \geq 130°C$.

Guaranteed Electrical Specifications, IFD-53010 and IFD-53110

T_A = 25°C, Z_O = 50 Ω, V_{cc} - V_{ee} = 5.0 V

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
F_{MAX}	IFD-53010: Maximum Clock Frequency P_{in} = -10 dBm (200 mVpp)	GHz	5.5	6.0	
F_{MAX}	IFD-53110: Maximum Clock Frequency P_{in} = -10 dBm (200 mVpp)	GHz	3.5	5.0	
I_{CC}	IFD-53010 and IFD-53110: Supply Current	mA	35	43	50

Typical Design Information, T_A = 25°C, Z_0 = 50 Ω, V_{cc} - V_{ee} = 5.0 V, P_{in} = -10 dBm.

All values apply to both IFD-53010 and IFD-53110. f_{test} is 5 GHz for IFD-53010 and 3 GHz for IFD-53110 (unless otherwise noted).

Symbol	Parameters and Test Conditions	Units	Value
F_{MIN}	Minimum Clock Frequency[1]	MHz	150
P_{in}	Input Sensitivity $f = f_{test}$	dBm mVpp	-22 50
P_{out}	Output Power $f = 0.15$ to f_{test}	dBm mVpp	-5 355
VSWR	Input VSWR $f = 0.15$ to f_{test} Output VSWR $f = 0.15$ to f_{test}		2.0:1 2.5:1
PN	SSB Phase Noise f = 3 GHz, 1 kHz offset f = 5 GHz, 1 kHz offset (IFD-53010 only)	dBc/Hz	-143 -138
T_r	Output Rise Time, 20% - 80% $f = f_{test}$	psec	145
T_f	Output Fall Time, 20% - 80% $f = f_{test}$	psec	85

Note:
1. Minimum clock frequency when driven from a sinusoidal input. Operation to lower frequencies is possible when using input signals with faster rise times, such as occurs in the case of a cascade of two or more IFDs.

Typical Performance, $T_A = 25°C$, $Z_O = 50\ \Omega$, $V_{cc} - V_{ee} = 5.0$ V

Graphs apply to both IFD-53010 and IFD-53110 (unless otherwise noted).

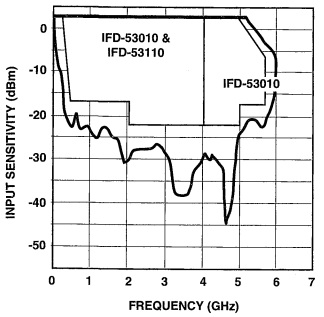


Figure 1. Input Sensitivity vs. Input Frequency and Recommended Operating Ranges for Nominal Operating Conditions (T = 25°C , $V_{cc} - V_{ee} = 5$ V).

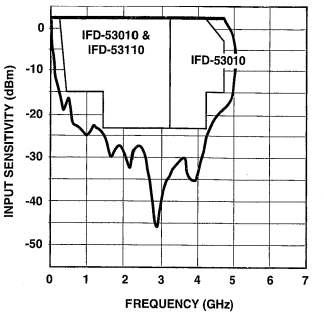


Figure 2. Input Sensitivity vs. Input Frequency and Recommended Operating Ranges for Worst Case Operating Conditions (-55°C < T < 125°C and 4.5 V < $V_{cc} - V_{ee}$ < 5.5 V.

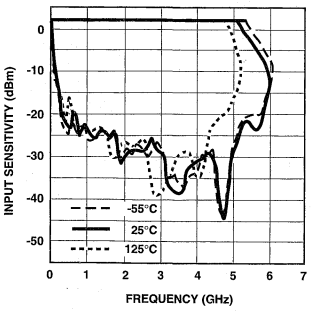


Figure 3. Input Sensitivity vs. Input Frequency and Temperature ($V_{cc} - V_{ee} = 5$ V).

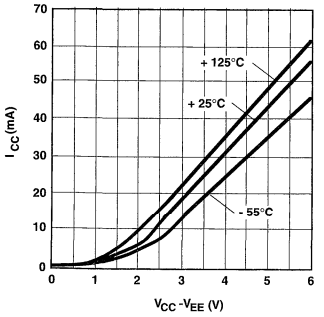


Figure 4. Device Current vs. Voltage and Temperature.

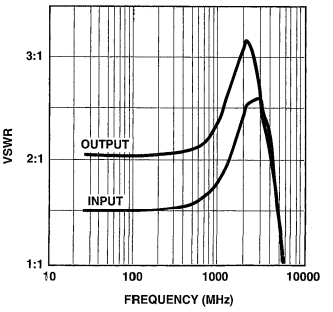


Figure 5. Input and Output VSWR vs. Frequency.

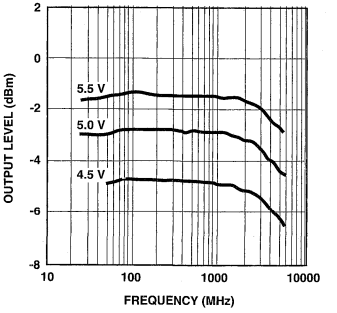


Figure 6. Output Power Level vs. Input Frequency and $V_{cc} - V_{ee}$.

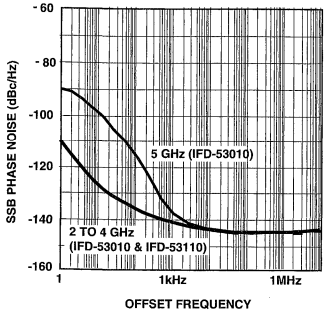


Figure 7. SSB Phase Noise vs. Offset Frequency, and Input Frequency.

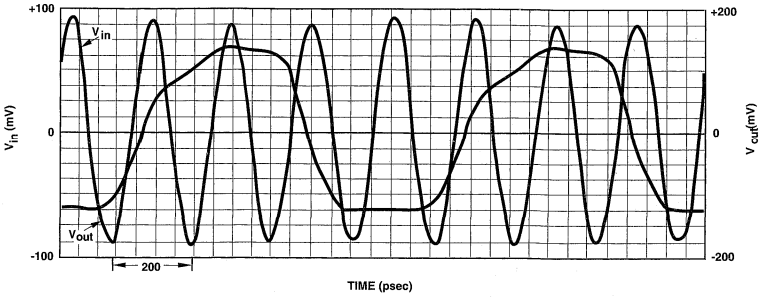


Figure 8. IFD-53010 Typical Output Response with 5 GHz Input.

BLOCKING CAPACITORS ARE 1000 pF TYP.
BYPASS CAPACITORS ARE 47 nF min.

BLOCKING CAPACITORS MAY BE OMITTED
IF GENERATOR AND LOAD ARE AT V_{CC} LEVEL.

TRANSMISSION LINES ARE 50 Ω.

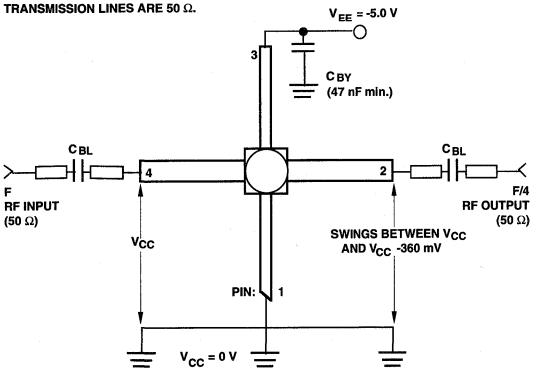


Figure 9. Typical ECL Biasing Configuration, IFD-53010 and IFD-53110.

BLOCKING CAPACITORS ARE 1000 pF TYP.

BYPASS CAPACITOR SHOULD BE 47 nF min.
TO ENSURE GOOD SENSITIVITY PERFORMANCE.

TRANSMISSION LINES ARE 50 Ω.

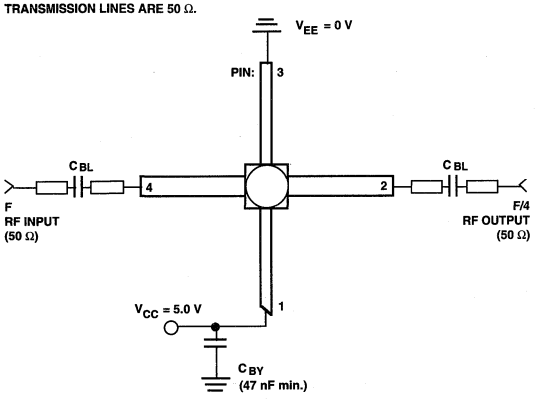


Figure 10. Typical RF Biasing Configuration, IFD-53010 and IFD-53110.

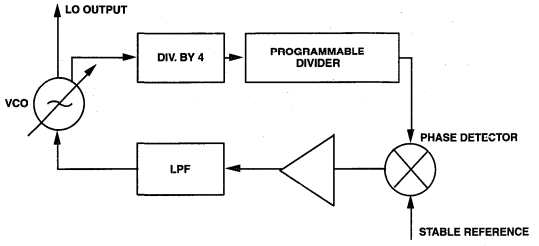


Figure 11. Typical Stabilized LO Configuration, IFD-53010 and IFD-53110.

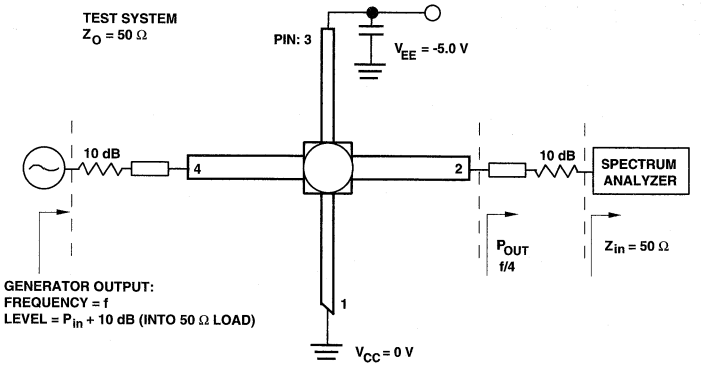
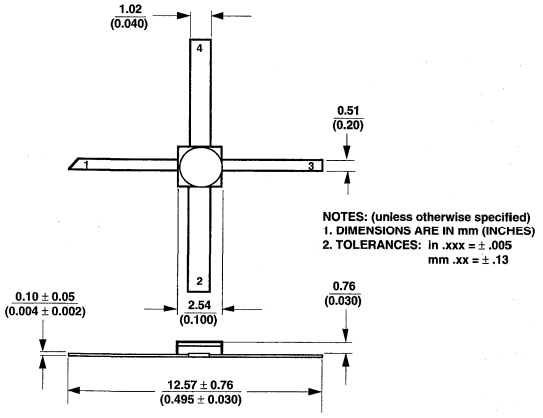


Figure 12. Sensitivity Test Configuration, IFD-53010 and IFD-53110.

Package Dimensions

100 mil Stripline Package



HEWLETT® PACKARD

Reflective SPDT GaAs MMIC Switch

Technical Data

MGS-70008

Features

- **Single-Pole, Double-Throw Output**
- **Broad Bandwidth:** DC to 3 GHz
- **Low Insertion Loss:** 0.8 dB Typical at 1 GHz
- **Fast Switching Time:** 3 ns Typical
- **Ultra Low DC Power Consumption**
- **Small Surface-Mount Plastic Package**

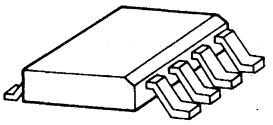
Description

The MGS-70008 is a single-pole, double-throw monolithic GaAs MMIC switch. The J2 and J3 of the MGS-70008 are terminated to ground when "off" (an absorptive version, the MGS-71008, which terminates the "off" port in an internal 50 Ω resistor, is also available). The switches are sealed in a small, plastic, surface-mount SO-8 package. Switching is actuated by a -5 V control voltage per the truth table shown on the next page. -3.3 V operation is also possible with some reduction in $P_{1\,dB}$ and IP_3.

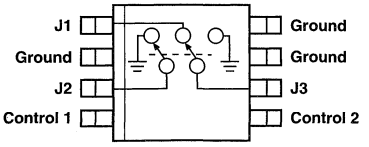
The MGS-70008 is designed for high volume commercial applications where low insertion loss, high isolation, and fast switching speed are required. Its low cost and high performance make it suitable for a wide variety of uses such as digital cellular, spread spectrum, GPS, and other RF switching applications. Refer to applications note AN-G007 for more application details.

The die is fabricated using HP's nominal 0.7 µm Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

SO-8 Package



AC Equivalent Circuit/Pinout



MGS-70008 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
	Maximum Input Power		
	below 500 MHz	dBm	+27
	above 500 MHz	dBm	+30
	Control Voltage	V	-8.0
T_{STG}	Storage Temperature	°C	-65 to 150

Note:

1. Operation of this device above any one of these limits may cause permanent damage.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
I_C	Control Input Current	DC	μA		12	110
BW	Bandwidth		GHz	DC-3		
IL	Insertion Loss	200 MHz	dB		0.6	
		1000 MHz	dB		0.8	1.1
		2000 MHz	dB		1.0	
		2500 MHz	dB		1.1	
		3000 MHz	dB		1.2	
ISO	Isolation	200 MHz	dB		51	
		1000 MHz	dB	29	33	
		2000 MHz	dB		23	
		2500 MHz	dB		19	
		3000 MHz	dB		16	
VSWR J1, J2 or J3	Voltage Standing Wave Ratio (on port)	DC-1000 MHz	—		1.2:1	1.4:1
		1000-3000 MHz	—		1.3:1	
VSWR J2 or J3	Voltage Standing Wave Ratio (off port)	DC-2000 MHz	—		≥10:1	
		2000-3000 MHz	—		≥10:1	
I_{SW}	Switching Speed	10% to 90%	ns		3	
$P_{1\,dB}$[2]	Output @ 1 dB Gain Compression	200 MHz	dBm		18.5	
		1000 MHz	dBm		26.0	
		2000 MHz	dBm		26.0	
IP_3[2]	3rd Order Intercept	200 MHz	dBm		41	
		1000 MHz	dBm		45	
		2000 MHz	dBm		45	

Notes:

1. Measured in a 50 Ω system at 1 GHz, unless otherwise specified, V_C = -5 V.
2. Measured in a 50 Ω system with V_C = -7 V.

MGS-70008 Typical Performance, T_A = 25°C

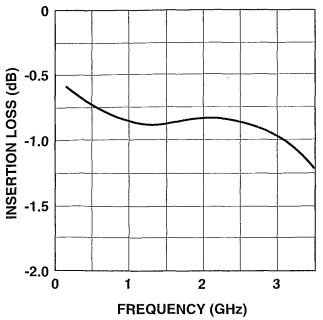


Figure 1. Insertion Loss vs. Frequency. $V_{Control}$ = -5 V.

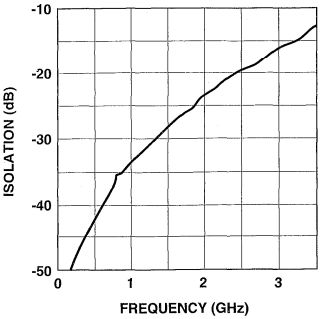


Figure 2. Isolation vs. Frequency. $V_{Control}$ = -5 V.

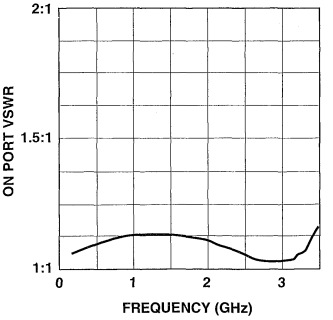


Figure 3. Input and Output Return Loss vs. Frequency. $V_{Control}$ = -7 V.

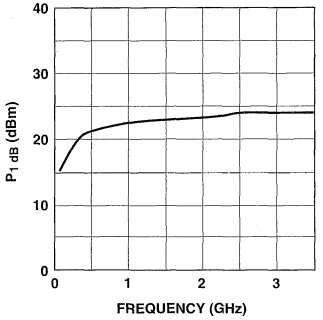


Figure 4. Output Power vs. Frequency. $V_{Control}$ = -7 V.

MGS-70008 Truth Table (Typical Performance at 1 GHz)

	Control Input		Insertion Loss		Return Loss		
	C1	C2	J1-J2	J1-J3	J1	J2	J3
	0 V	0 V	16 dB	16 dB	1 dB	1 dB	1 dB
For normal SPDT use	0 V	-5 V	33 dB	.8 dB	22 dB	1 dB	22 dB
For normal SPDT use	-5 V	0 V	.8 dB	33 dB	22 dB	22 dB	1 dB
	-5 V	-5 V	19 dB	19 dB	1 dB	1 dB	1 dB

MGS-70008 Typical Power Performance vs. Frequency and Control Voltage (V_C)

(All other typical specifications remain constant.)

	V_C = -7 V		V_C = -5 V		V_C = -3.3 V	
Frequency	$P_{1\ dB}$	IP_3	$P_{1\ dB}$	IP_3	$P_{1\ dB}$	IP_3
200 MHz	18.5 dBm	41 dBm	18.0 dBm	41 dBm	16.5 dBm	35 dBm
1000 MHz	26.0 dBm	45 dBm	23.7 dBm	44 dBm	17.5 dBm	38 dBm
2000 MHz	26.0 dBm	45 dBm	23.0 dBm	44 dBm	16.0 dBm	38 dBm

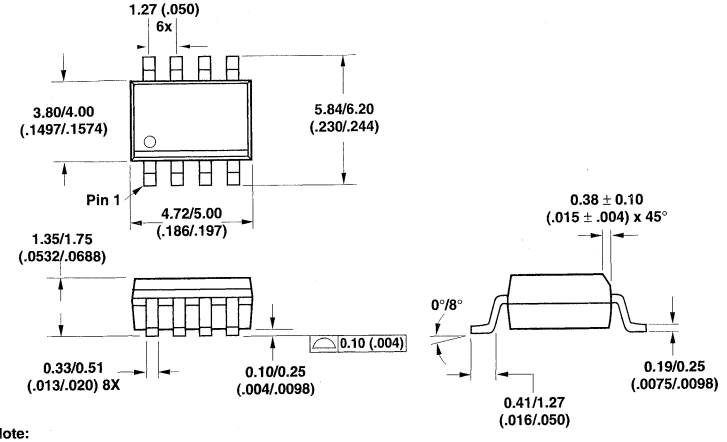
Typical Scattering Parameters, ON Switch Port, Z_O = 50 Ω, T_A = 25°C, V_C = -5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.2	.04	-6.2	-.6	.93	-4.5	-.6	.934	-4.4	.04	-2.5
0.4	.04	0.3	-.6	.93	-8.5	-.6	.934	-8.3	.03	10.6
0.6	.04	7.6	-.6	.93	-12.7	-.6	.930	-12.4	.03	30.7
0.8	.05	13.6	-.6	.93	-16.8	-.7	.927	-16.3	.04	52.8
1.0	.06	14.7	-.6	.93	-21.0	-.7	.927	-20.4	.05	63.0
1.2	.07	14.5	-.6	.93	-25.7	-.6	.931	-24.5	.07	67.1
1.4	.09	14.0	-.6	.93	-30.3	-.6	.930	-28.7	.08	69.1
1.6	.10	10.2	-.6	.93	-34.8	-.6	.930	-32.9	.10	69.2
1.8	.11	8.1	-.6	.93	-39.4	-.6	.928	-37.6	.10	66.6
2.0	.11	1.4	-.6	.93	-44.5	-.6	.928	-41.8	.11	65.2
2.2	.11	-3.2	-.7	.92	-49.9	-.7	.922	-46.8	.09	62.2
2.4	.10	-8.5	-.8	.91	-54.5	-.7	.927	-51.5	.09	60.8
2.6	.08	-13.1	-.7	.92	-58.9	-.7	.920	-56.2	.07	60.0
2.8	.05	-14.1	-.7	.92	-64.0	-.7	.922	-62.4	.04	70.8
3.0	.01	7.4	-.8	.91	-69.0	-1.0	.894	-68.7	.02	127.9
3.2	.04	141.4	-1.1	.88	-75.0	-1.3	.864	-74.4	.05	-178.2
3.4	.11	143.2	-1.2	.87	-79.2	-1.7	.823	-79.9	.10	-169.4
3.6	.17	129.5	-1.4	.85	-81.7	-1.6	.828	-85.7	.12	-178.5
3.8	.22	135.9	-1.3	.86	-85.4	-2.1	.788	-91.8	.19	-168.0
4.0	.32	133.2	1.6	.83	-94.4	-3.0	.708	-95.0	.22	165.6
4.2	.37	129.2	-2.2	.78	-96.8	-3.7	.652	-99.2	.24	166.9
4.4	.46	128.5	-2.0	.79	-96.4	-4.2	.619	-102.5	.30	163.4

Typical Scattering Parameters, OFF Switch Port, Z_O = 50 Ω, T_A = 25°C, V_C = -5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.2	.05	5.6	-50.0	0	92.1	-44.4	.006	92.4	.81	176.3
0.4	.05	20.6	-40.0	.01	94.2	-38.4	.012	95.2	.82	172.6
0.6	.06	36.0	-35.0	.02	98.1	-35.4	.017	100.3	.83	168.9
0.8	.09	39.3	-31.9	.03	100.9	-32.4	.024	104.4	.83	165.3
1.0	.11	35.8	-30.5	.03	103.9	-30.5	.030	108.5	.85	161.6
1.2	.13	30.9	-28.0	.04	103.6	-28.4	.038	110.4	.86	158.3
1.4	.14	25.0	-28.0	.05	107.5	-26.4	.048	116.2	.87	154.9
1.6	.15	18.9	-24.4	.06	107.0	-24.7	.058	116.8	.89	151.9
1.8	.16	14.5	-23.1	.07	108.5	-23.0	.071	119.6	.90	148.6
2.0	.16	10.6	-21.9	.08	105.9	-21.6	.083	118.0	.92	146.7
2.2	.17	7.8	-20.0	.10	105.3	-19.9	.101	118.6	.92	145.0
2.4	.17	3.0	-19.2	.11	105.4	-18.8	.115	119.8	.95	143.1
2.6	.18	-2.9	-17.7	.13	103.9	-16.9	.143	120.4	.95	141.7
2.8	.16	-9.2	-16.5	.15	102.1	-15.7	.165	119.3	.98	141.2
3.0	.14	-19.6	-14.9	.18	98.5	-13.9	.202	116.4	.99	140.6
3.2	.11	-33.2	-14.0	.20	97.6	-12.2	.246	115.5	1.01	139.6
3.4	.06	-78.5	-12.0	.25	88.8	-10.3	.307	105.1	1.00	139.0
3.6	.08	-156.7	-10.5	.30	79.5	-8.4	.379	89.9	.91	140.4
3.8	.13	-153.0	-11.1	.28	70.0	-10.3	.306	77.4	.94	146.5
4.0	.18	134.3	-11.7	.26	68.9	-8.6	.370	88.3	1.26	142.8
4.2	.22	129.6	-10.8	.29	72.1	-7.8	.407	85.3	1.33	133.7
4.4	.27	128.9	-9.9	.32	72.0	-6.8	.458	83.0	1.45	131.6

SO-8 Package Dimensions



Note:
1. Dimensions are shown in millimeters (inches).

HEWLETT® PACKARD

Absorptive SPDT GaAs MMIC Switch

Technical Data

MGS-71008

Features

- **Single-Pole, Double-Throw Output**
- **Broad Bandwidth:** DC to 3 GHz
- **High Isolation:** 37 dB Typical at 1 GHz
- **Fast Switching Time:** 3 ns Typical
- **Ultra Low DC Power Consumption**
- **Small Surface-Mount Plastic Package**

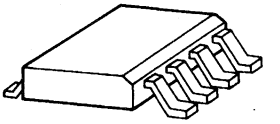
Description

The MGS-71008 is a single-pole, double-throw monolithic GaAs MMIC switch. The J2 and J3 of the MGS-71008 are terminated to ground by internal 50 Ω load resistors when "off" (a reflective version, the MGS-70008, which terminates the "off" port to ground, is also available). The switch is sealed in a small, plastic, surface-mount SO-8 package. Switching is actuated by a -5 V control voltage per the truth table shown on the next page. -3.3 V operation is also possible with some reduction in $P_{1\,dB}$ and IP_3.

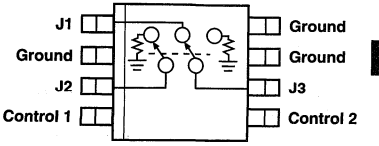
The MGS-71008 is designed for high volume commercial applications where low insertion loss, high isolation, and fast switching speed are required. Its low cost and high performance make it suitable for a wide variety of uses such as digital cellular, spread spectrum, GPS, and other RF switching applications. Refer to applications note AN-G007 for more application details.

The die is fabricated using HP's nominal 0.3 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

SO-8 Package



AC Equivalent Circuit/Pinout



5965-9118E

MGS-71008 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
	Maximum Input Power		
	below 500 MHz	dBm	+27
	above 500 MHz	dBm	+30
	Control Voltage	V	-8.0
T_{STG}	Storage Temperature	°C	-65 to 150

Note:
1. Operation of this device above any one of these limits may cause permanent damage.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
I_C	Control Input Current	DC	μA		12	110
BW	Bandwidth		GHz	DC-3		
IL	Insertion Loss	200 MHz	dB		0.9	
		1000 MHz	dB		1.2	1.5
		2000 MHz	dB		1.3	
		2500 MHz	dB		1.4	
		3000 MHz	dB		1.5	
ISO	Isolation	200 MHz	dB		52	
		1000 MHz	dB	30	37	
		2000 MHz	dB		26	
		2500 MHz	dB		22	
		3000 MHz	dB		16	
VSWR J1, J2 or J3	Voltage Standing Wave Ration (on port)	DC-1000 MHz	—		1.2:1	1.4:1
		1000-3000 MHz	—		1.3:1	
VSWR J2 or J3	Voltage Standing Wave Ration (off port)	DC-2000 MHz	—		1.2:1	
		2000-3000 MHz	—		1.3:1	
I_{SW}	Switching Speed	10% to 90%	ns		3	
$P_{1\,dB}$[2]	Output @ 1 dB Gain Compression	200 MHz	dBm		16.5	
		1000 MHz	dBm		25.2	
		2000 MHz	dBm		25.2	
IP_3[2]	3rd Order Intercept	200 MHz	dBm		41	
		1000 MHz	dBm		45	
		2000 MHz	dBm		45	

Notes:
1. Measured in a 50 Ω system at 1 GHz, unless otherwise specified, V_C = -5 V.
2. Measured in a 50 Ω system with V_C = -7 V.

MGS-70008 Typical Performance, T_A = 25°C

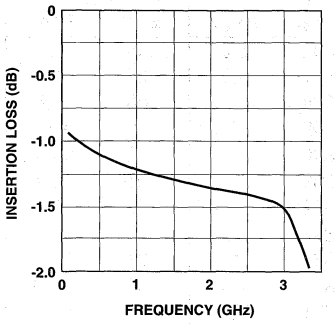


Figure 1. Insertion Loss vs. Frequency. $V_{Control}$ = -5 V.

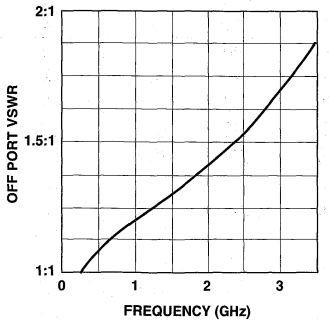


Figure 2. Off Port VSWR vs. Frequency. $V_{Control}$ = -5 V.

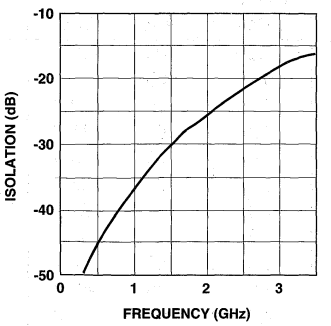


Figure 3. Isolation vs. Frequency. $V_{Control}$ = -5 V.

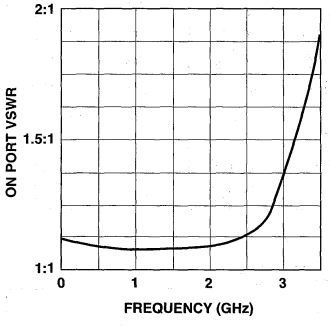


Figure 4. On Port VSWR vs. Frequency. $V_{Control}$ = -5 V.

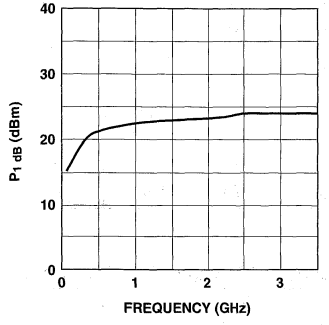


Figure 5. Output Power vs. Frequency. $V_{Control}$ = -7 V.

MGS-71008 Truth Table (Typical Performance at 1 GHz)

	Control Input		Insertion Loss		Return Loss		
	C1	C2	J1-J2	J1-J3	J1	J2	J3
	0 V	0 V	16 dB	16 dB	1 dB	1 dB	1 dB
For normal SPDT use	0 V	-5 V	37 dB	1.2 dB	22 dB	22 dB	22 dB
For normal SPDT use	-5 V	0 V	1.2 dB	37 dB	22 dB	22 dB	1 dB
	-5 V	-5 V	26 dB	26 dB	1 dB	1 dB	1 dB

MGS-71008 Typical Power Performance vs. Frequency and Control Voltage (V_C)

(All other typical specifications remain constant.)

	V_C = -7 V		V_C = -5 V		V_C = -3.3 V	
Frequency	$P_{1\ dB}$	IP_3	$P_{1\ dB}$	IP_3	$P_{1\ dB}$	IP_3
200 MHz	16.5 dBm	41 dBm	16.5 dBm	41 dBm	15.5 dBm	35 dBm
1000 MHz	25.2 dBm	45 dBm	23.7 dBm	44 dBm	19.0 dBm	38 dBm
2000 MHz	25.2 dBm	45 dBm	22.5 dBm	44 dBm	18.5 dBm	38 dBm

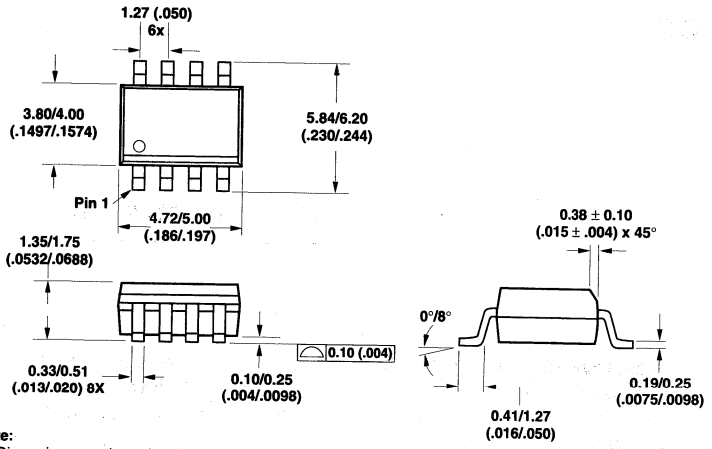
Typical Scattering Parameters, ON Switch Port, Z_O = 50 Ω, T_A = 25°C, V_C = -5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.2	.05	-18.2	-.9	.90	-5.1	-.9	.904	-5.0	.05	-14.1
0.4	.05	-18.3	-.9	.90	-9.4	-.9	.9.6	-9.2	.04	-10.1
0.6	.05	-20.6	-.9	.90	-13.9	-.9	.898	-13.6	.03	-8.2
0.8	.05	-18.7	-.9	.90	-18.2	-.9	.898	-17.8	.02	8.9
1.0	.05	-20.4	-1.0	.89	-22.8	-1.0	.890	-22.3	.02	30.5
1.2	.06	-26.3	-1.0	.89	-27.8	-1.0	.893	-26.9	.01	42.3
1.4	.06	-29.1	-1.0	.89	-32.7	-1.0	.891	-31.5	.02	55.2
1.6	.07	-38.1	-1.1	.88	-37.5	-1.0	.889	-36.3	.02	59.1
1.8	.06	-46.4	-1.1	.88	-42.4	-1.1	.884	-41.5	.01	19.1
2.0	.06	-63.8	-1.2	.87	-47.8	-1.1	.879	-46.6	.01	-75.6
2.2	.06	-82.3	-1.2	.87	-53.5	-1.2	.871	-52.2	.03	-103.5
2.4	.07	-109.8	-1.3	.86	-58.5	-1.2	.867	-57.8	.05	-115.3
2.6	.08	-128.7	-1.4	.85	-63.2	-1.4	.851	-62.9	.08	-126.2
2.8	.11	-153.4	-1.5	.84	-68.7	-1.5	.838	-70.0	.11	-134.4
3.0	.14	-169.6	-1.6	.83	-74.0	-2.0	.791	-76.5	.16	-144.1
3.2	.20	178.3	-2.0	.79	-80.3	-2.5	.746	-82.8	.20	-152.8
3.4	.26	167.7	-2.3	.77	-83.8	-3.1	.700	-87.2	.26	-163.4
3.6	.31	154.5	-2.4	.76	-87.3	-3.3	.686	-93.8	.29	-168.1
3.8	.40	152.0	-2.5	.75	-90.3	-4.0	.632	-99.3	.37	-169.7
4.0	.51	145.4	-3.0	.71	-100.2	-4.6	.588	-99.6	.37	167.2
4.2	.63	139.5	-3.3	.68	-101.6	-5.4	.534	-101.6	.43	168.5
4.4	.82	133.0	-3.1	.70	-103.8	-6.1	.498	-104.6	.46	162.7

Typical Scattering Parameters, OFF Switch Port, Z_O = 50 Ω, T_A = 25°C, V_C = -5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.2	.06	-9.8	-52.0	0	73.6	-46.0	.005	74.7	.01	146.5
0.4	.05	0	-42.4	.01	94.8	-41.9	.008	95.5	.03	130.7
0.6	.05	27.3	-36.4	.02	113.0	-36.5	.015	113.7	.05	125.1
0.8	.06	20.7	-35.2	.02	92.3	-35.4	.017	93.0	.07	116.9
1.0	.06	21.7	-33.7	.02	106.1	-33.6	.021	107.1	.08	115.7
1.2	.07	20.6	-31.4	.03	114.5	-32.0	.025	116.4	.10	114.8
1.4	.08	15.7	-30.5	.03	122.9	-29.1	.035	125.5	.12	114.6
1.6	.08	-5.6	-28.0	.04	112.0	-27.7	.041	114.2	.14	116.3
1.8	.08	-11.8	-26.0	.05	122.0	-26.2	.049	124.9	.16	115.2
2.0	.07	-17.0	-24.4	.06	121.9	-24.2	.062	125.4	.18	117.1
2.2	.08	-24.6	-21.9	.08	124.3	-22.3	.077	128.3	.21	118.5
2.4	.07	-40.0	-20.9	.09	119.5	-20.4	.095	123.5	.23	117.9
2.6	.06	-46.7	-20.0	.10	119.4	-19.6	.105	124.0	.25	117.8
2.8	.05	-66.2	-18.4	.12	119.0	-17.8	.129	122.9	.27	117.9
3.0	.05	-112.4	-16.5	.15	116.5	-16.1	.157	119.7	.30	118.0
3.2	.08	-158.0	-15.4	.17	111.0	-14.4	.191	113.1	.32	116.2
3.4	.16	170.2	-14.4	.19	100.7	-13.8	.204	100.3	.33	119.8
3.6	.23	158.7	-13.6	.21	100.8	-13.0	.223	96.7	.35	120.5
3.8	.34	146.0	-12.4	.24	97.3	-12.8	.229	90.9	.36	124.0
4.0	.45	138.0	-11.4	.27	83.0	-11.7	.260	78.3	.33	113.0
4.2	.54	129.9	-12.0	.25	82.7	-12.6	.234	78.8	.39	120.7
4.4	.65	125.4	-10.8	.29	81.1	-11.9	.253	74.5	.39	116.1

SO-8 Package Dimensions



Note:
1. Dimensions are shown in millimeters (inches).

HEWLETT® PACKARD

Silicon Bipolar Vector Modulator

Reliability Data

HPMX-2003/5 Series

Description

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-883. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

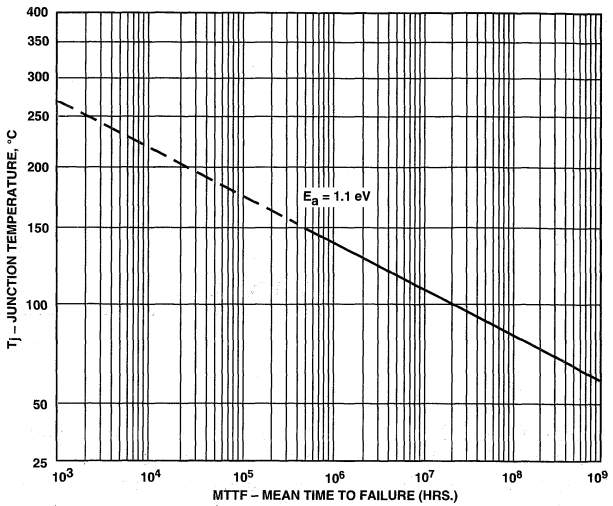
Test Name	Test Conditions	Units Tested	Total Device Hrs.	Total Failed
High Temperature Operating Life (O.L.)	T_J = 150°C V_{CC} = 5 V, I_{CC} = 36 mA	48	48,000	0
High Temperature Operating Life (O.L.) (INA Series)	T_J = 150°C	344	344,000	0
High Temperature Operating Life (O.L.) (IAM-82018)	T_J = 200°C V_{CC} = 10 V, I_{CC} = 50 mA	70	70,000	0
High Temperature Operating Life (O.L.) (IVA-05218)	T_J = 158°C V_{CC} = 5 V, I_{CC} = 35 mA	70	70,000	1

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1 eV, and is listed in the following table.

Junction Temp. T_J(°C)	Point(1) MTTF* (hours)	Point(1) MTTF FIT(3)	90% Confidence Level(2) MTTF (hours)	90% Confidence Level(2) FIT(3)
150	4×10^5	2500	1.7×10^5	5750
100	2×10^7	50	8.7×10^6	115
85	8×10^7	12	3.4×10^7	28
55	2×10^9	0.5	8.6×10^8	1.2

*MTTF data calculated from high temperature Operating Life tests.



Notes:
1. The point MTTF is simply the total device hours divided by the number of failures.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hours/day) x (5 days/week) ÷ 168 hours/week = 25%

Then the point failure rate per year is:

(50 x 10^{-9}/hr.) x (25%) x (8760 hours/year) = 0.011% per year

Likewise, the 90% confidence level failure rate per year is:

(115 x 10^{-9}/hr.) x (25%) x (8760 hours/year) = 0.025% per year

2. Environmental Tests

Test Name	MIL-STD-883 Method	Test Conditions	Units Tested	Units Failed
Temperature Cycle	M1010	-65°C to +150°C; 200 cycles	76	0
Thermal Shock	M1011	-65°C to +150°C; 200 cycles	76	1
Lead Integrity	M2004	—	22	0
Solderability	2003	Solder temp 260°C ±10°C; Dwell time 5 seconds; 8 hours steam age	22	0
Resistance to Solvents	2015	3 solvents	15	0
Physical Dimension and Visual Inspection	M2016	Outline Drawing	75	0

3. Flammability Test

(MIL-STD-202, Method 111):
Meets Needle Flame test per UL Category D (Flaming Time <3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD

Classification: Class I

HEWLETT® PACKARD

Silicon Bipolar Active Mixer

Reliability Data

IAM-8XXXX

Description

The following cumulative test results have been obtained from testing performed at Hewlett-Packard in accordance with the latest revision of MIL-STD-883. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in the Communications Components Designer's Catalog.

1. Life Test

A. Demonstrated Performance

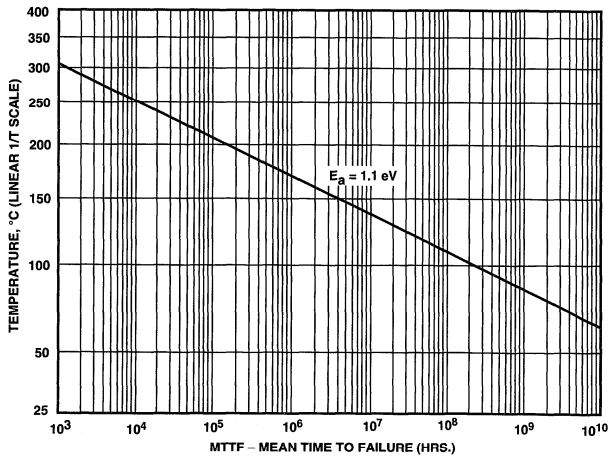
Test Name	Test Conditions	Units Tested	Total Device Hrs.	Total Failed
High Temperature Operating Life (O.L.)	T_J = 200°C	70	70,000	0
High Temperature Operating Life (O.L.)	T_J = 150°C	318	318,000	0
High Temperature Storage (HTS)*	T_J = 150°C	77	77,000	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1 eV, and is listed in the following table.

Junction Temp. T_J(°C)	Point(1)		90% Confidence Level(2)	
	MTTF* (hours)	MTTF FIT(3)	MTTF (hours)	FIT(3)
200	1.6×10^5	6319	1.2×10^5	8278
175	7.1×10^5	1402	5.4×10^5	1836
150	3.8×10^6	260	2.9×10^6	341
125	2.6×10^7	39	2.0×10^7	51
100	2.2×10^8	5	1.7×10^8	6
75	2.6×10^9	<1	2.0×10^9	<1
50	4.4×10^{10}	<<1	3.3×10^{10}	<<1

*MTTF data calculated from high temperature Operating Life tests.



Notes:
1. The point MTTF is simply the total device hours divided by the number of failures.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 100°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hours/day) x (5 days/week) ÷ 168 hours/week ≅ 25%

Then the point failure rate per year is:

$(4.55 \times 10^{-9}) \times (25\%) \times (8760 \text{ hours/year}) \cong 1.0 \times 10^{-3}$ % per year

Likewise, the 90% confidence level failure rate per year is:

$(5.88 \times 10^{-9}) \times (25\%) \times (8760 \text{ hours/year}) \cong 1.3 \times 10^{-3}$ % per year

2. Environmental Tests

Test Name	MIL-STD-883 Method	Test Conditions	Units Tested	Units Failed
Temperature Cycle	1010	-65°C to +150°C; 10 min. dwell; 200 cycles, min.	450	1
Thermal Shock	1011	-65°C to +150°C; 5 min. dwell; 200 cycles, min.	448	0
Autoclave, unbiased	HP GSS 12-109	121°C; 15 PSIG, 96 hrs., min.	327	1
Temperature Humidity, biased	HP GSS 12-107	85°C/85% RH; 1000 hrs., min.	131	0
Resistance to solvents	2015	3 solvent groups	15	0
Solderability	2003	260°C, 5 sec. dwell; Post 8 hours steam aging	82	0

3. Flammability Test

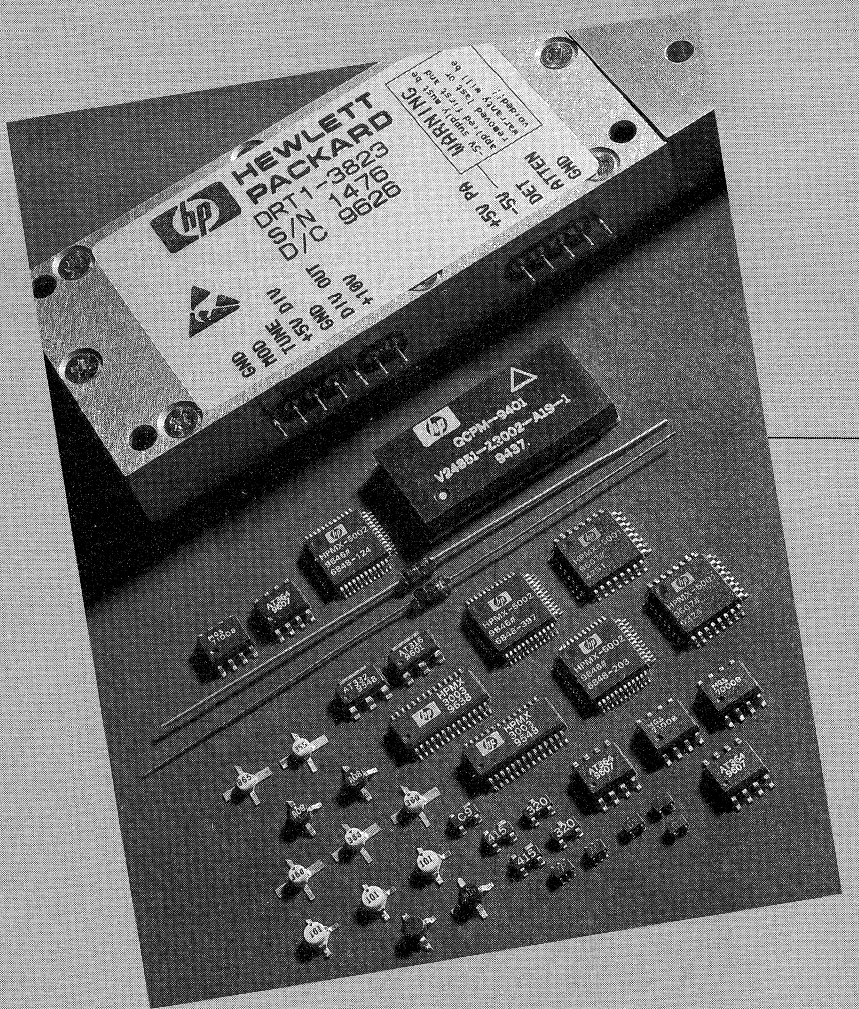
(MIL-STD-202, Method 111):
Meets Needle Flame test per UL Category D (Flaming Time <3 sec.) under Material Classification 94VO.

4. DOD-HDBK-1686 ESD

Classification: Class I

HEWLETT® PACKARD

Digital Radio Receiver and Transmitter Modules



Digital Radio Receiver and Transmitter Modules

Characteristics

The Digital Radio Transmitter Modules, (DRT1-23XX and DRT1-38XX) supply the transmit function for digital radios operating in the 23 and 38 GHz frequency bands. The Digital Radio Receiver Modules, (DRR1-23XX and DRR1-38XX) supply the receive functions in the same frequency bands.

These modules are used in short-haul radios that supply the back haul function between cellular and PCS base station sites as well as for private microwave links used in campus applications for voice and data transmission. They interconnect these sites with each other and with the switching networks. They are ideal for use in radios operating with 4 level FSK modulation and up to 34 mB/s data rates. They are capable of handling traffic levels from 1 T-1 line to 1 DS-3 line.

The modules feature an integrated ultra low noise silicon bipolar VCO operating in the S/C band as the local oscillator. A portion of the oscillator output is coupled off and is applied to a frequency divider network. This signal is divided down to a low frequency that allows the oscillator to be easily phase locked.

Both transmit and receive modules operate over a -30 to +70°C temperature range and are moisture sealed to provide protection against environmental conditions that the radio may have to operate in.

Receiver/Down Converter Modules

These modules incorporate a low noise MMIC amplifier coupled to an image reject mixer and an IF amplifier providing an output signal in the 630 or 1260 MHz range, other IF frequencies are available. The local oscillator function is provided by an integrated VCO, multiplier network providing the mmwave low phase noise signal to the mixer.

Transmitter Modules

This module uses the VCO described above coupled to a multiplier network to transform the signal to the mmwave region. Additional amplifiers are added to provide +18 to +20 dBm of output power in the specific mmwave band. A detector is provided at the output as a power indicator and an optional attenuator is also available providing 30 dB dynamic range adjustment and there is mute function providing 50 dB signal reduction for "hot standby" applications.

Other Frequency Bands

Additional models will be available for the 13, 15, 18 and 26 GHz bands by the end of 1997.

HEWLETT® PACKARD

Digital Radio Receiver and Transmitter Modules Selection Guides

Receiver Down Converter Modules

Part Number	RF Tuning Range (GHz)	IF Frequency (MHz)	Min. Gain (dB)	Gain Flatness (dB)	Noise Figure (dB)	Power Input at P_{1dB} (dBm)	Page No.
DRR1-23XX	21.2 to 23.6	630 or 1260	18	±1	4.5	-17	8-4
DRR1-38XX	37 to 40	630 or 1260	18	±1	7.5	-17	8-8

Transmitter Modules

Part Number	RF Tuning Range (GHz)	Phase Noise @ 100 KHz (dBc)	RF Output Power (dBm)	Main Tuning Sensitivity (MHz/V)	Attenuation (dB)	DC Circuit Power @ +5 V (mA)	Page No.
DRT1-2311 or -2312	21.2 to 23.6	-85	20	260	—	600	8-12
DRT1-2321 or -2322	21.2 to 23.6	-85	20	260	30	975	8-12
DRT1-3813	37 to 40	-82	19	200	—	600	8-16
DRT1-3823	37 to 40	-82	19	200	30	975	8-16

HEWLETT® PACKARD

Digital Radio Receiver Down Converter Modules for 21.2 to 23.6 GHz

Technical Data

DRR1-23XX

Features

- **Low Noise PHEMT MMIC Front End Amplifier**
- **Image Reject Mixer**
- **Integrated Silicon Bipolar VCO Local Oscillator**
- **Low Phase Noise**
- **Operated Over -30°C to +70°C**
- **Excellent Tuning Linearity**
- **Sample Output for Phase Locking**

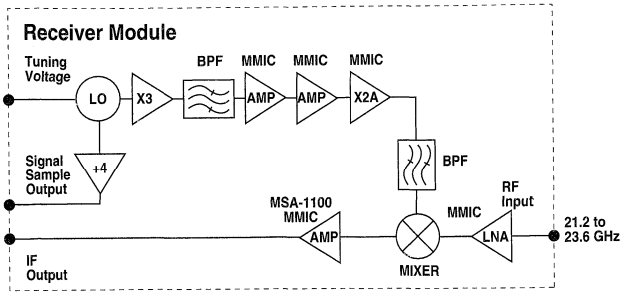
Description

This digital radio receiver module provides the RF receive and down conversion function for 23 GHz digital radios. These modules offer excellent phase noise performance and can be easily phase locked to a frequency reference. The receiver module provides an output power of 3 dBm at the IF frequency and is ideal for use in radios using 2 and 4 level FSK modulation. The excellent low noise figure is achieved by using the Hewlett-Packard PHEMT MMIC technology coupled with an image reject mixer. The receiver module features an integrated ultra low noise silicon bipolar VCO operating in the S/C band as the local oscillator. A portion of the oscillator output is coupled off and is applied to a frequency divider network. The low frequency output from the frequency divider can then be easily used to phase lock the source. The local oscillator output is applied to a frequency multiplier network to produce the desired LO frequency to the mixer.

Applications

This digital radio receiver module provides the total RF receive and down conversion function in radios operating in the 21.2 to 23.6 GHz band.

Block Diagram



DRR1-23XX Absolute Maximum Ratings (T_A = -30 to +70°C)

Parameters	Units	Ratings
DC Circuit Power +8.5	Volts	10
+5.0	Volts	+5.5
-5.0	Volts	-5.5
Tuning Voltage	Volts	14

Notes:

1. Operation in excess of any one of these parameters may result in permanent damage.
2. A thermal interface medium must be used between the bottom of the package and its mating surface to ensure optimum heat transfer.

DRR1-23XX Electrical Characteristics

Parameters	Units	Min.	Typ.	Max.
RF Tuning Range	GHz	21.2		23.6
IF Frequency	MHz		630 or 1260	
IF Bandwidth	MHz	±20		
LO Frequency	GHz	20.57 or 19.94		22.97 or 22.34
Gain	dB	18		26
Gain Flatness over 300 MHz	dB			±1
Noise Figure	dB		4.5	5.5
Operating Temperature Range	°C	-30		70
Storage Temperature Range	°C	-45		85
Power Input at P-1dB	dBm	-22	-17	
LO Leakage at I[1]	dBm			-15
LO Leakage at R[2]	dBm			-15
Return Loss RF Port	dB	12		
Return Loss IF Port	dB	14		
Image Rejection	dB	12	15	
Sample Out Frequency	MHz	857 or 831		957 or 931
Sample Out Power	dBm	-10		0
Spurious Output[3]	dBc			-60
Phase Noise @ 100 KHz	dBc/Hz		-85	-82
Tuning Voltage	V	1		12
Input Capacitance, Nom	pf		1,000	
LO Tuning Sensitivity	MHz/V		300	500
LO Tuning Sensitivity Variation			1.5 : 1	2.0:1
DC Circuit Power: 8.5 Volts	mA			300
5 Volts	mA			400
-5 Volts	mA			30
Case Dimensions	inches		3.5 x 1.25 x 0.40	
Max Power at Input/no damage	dBm			10
Humidity Non Condensing	%		85	
Condensing	%		95	
Connectors			WR 42 or SMA	

Notes:

1. LO and Harmonic/sub-harmonic leakage at I with RF terminated into a 50 Ω load.
2. LO and Harmonic/sub-harmonic leakage at R up to 50 GHz.
3. Measured at IF port within the IF bandwidth with single tone RF input of <-20 dBm.

DRR1-23XX Typical Performance

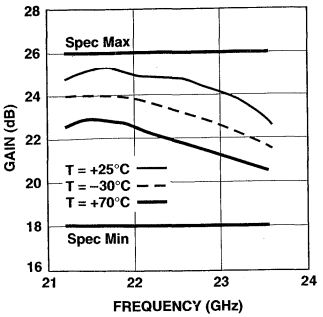


Figure 1. Conversion Gain vs. Frequency.

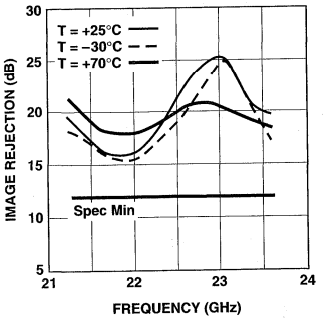


Figure 2. Image Rejection vs. Frequency.

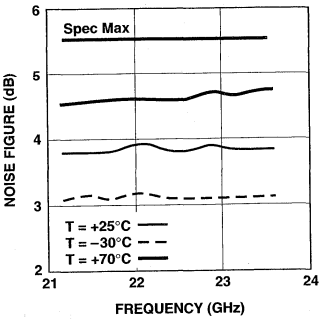


Figure 3. Noise Figure vs. Frequency.

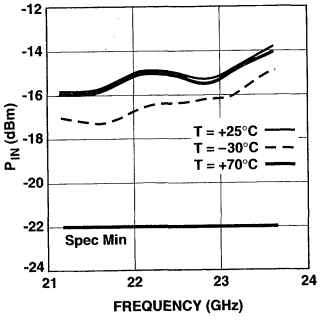


Figure 4. Power In at P_{1dB} Out vs. Frequency.

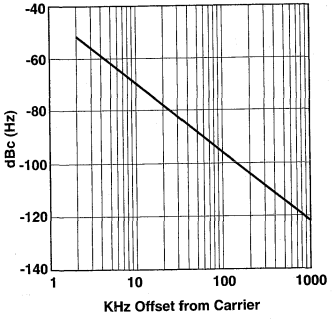


Figure 5. Phase Noise at 23 GHz vs. KHz Offset from Carrier.

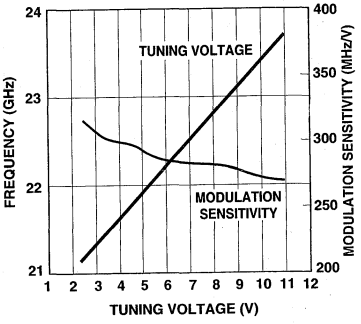


Figure 6. Tuning Voltage vs. Frequency and Modulation Sensitivity.

Powering Up Instructions

The -5 volts must be applied to the receiver module **before** applying the +5 volts. Likewise when shutting down the receiver module the +5 volts must be removed before the -5 volts is turned off. The +8.5 volts can be turned on in any sequence. Failure to follow this procedure could cause permanent damage to the module.

Mounting Instructions

Case must be mounted firmly, with screws, to an adequate metallic structure that has sufficient thermal properties to maintain the module case at a temperature not to exceed 70°C.

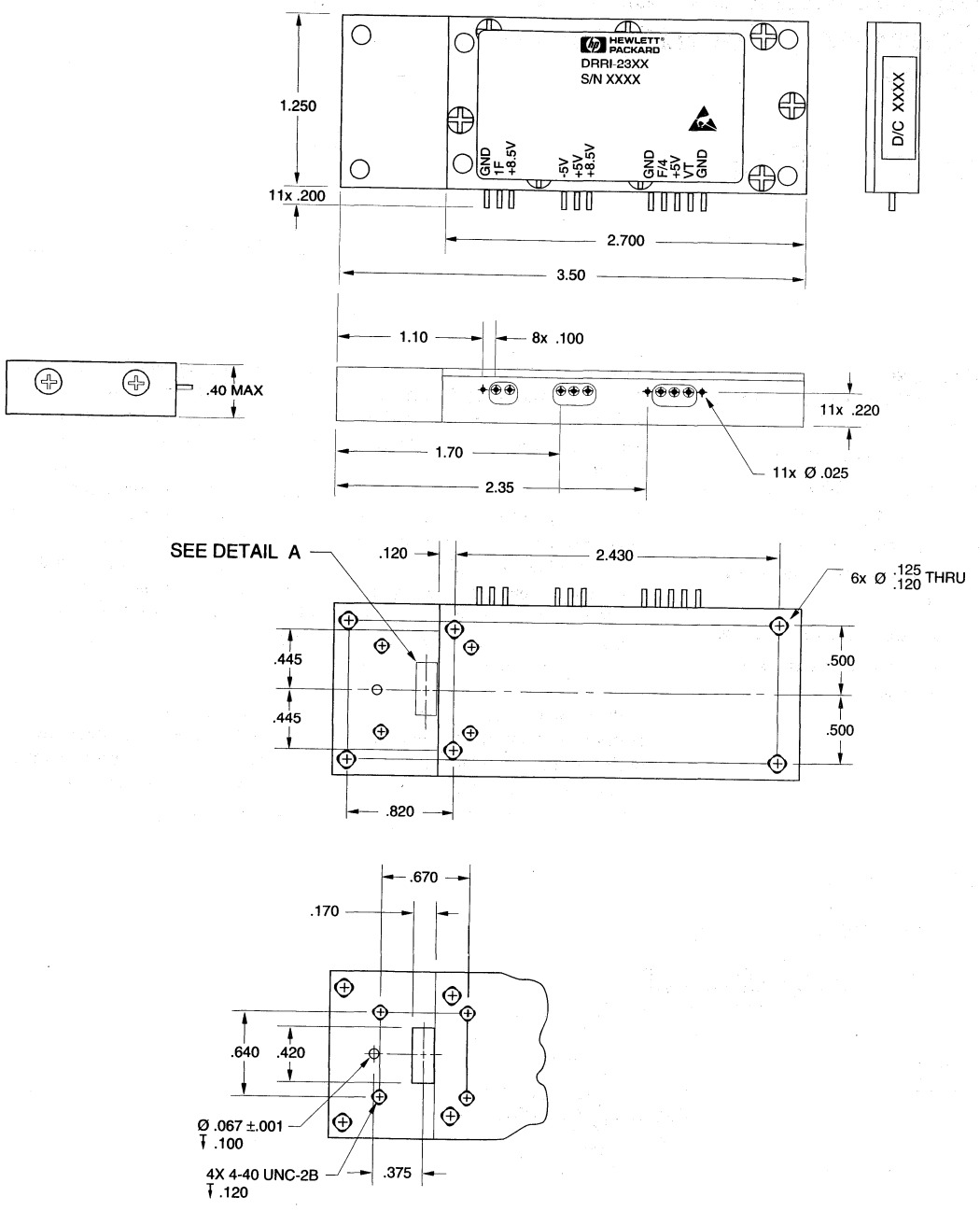
Product Options

Specify part number followed by option. For example:

DR R 1 – 23 X X

- Model Number Prefix = Digital Radio
- R = Receiver Module
- Internal Use
- 23 = 21.2 to 23.6 GHz Frequency Band
- 1 = 630 MHz IF Frequency
- 2 = 1260 MHz IF Frequency
- 1 = SMA Connector
- 2 = WR-42 Waveguide Connector

Case Dimensions (specified in inches)



HEWLETT® PACKARD

Digital Radio Receiver Down Converter Modules for 37 to 40 GHz

Technical Data

DRR1-38XX

Features

- **Low Noise PHEMT MMIC Front End Amplifier**
- **Image Reject Mixer**
- **Integrated Silicon Bipolar VCO Local Oscillator**
- **Low Phase Noise**
- **Operated Over -30°C to +70°C**
- **Excellent Tuning Linearity**
- **Sample Output for Phase Locking**

Description

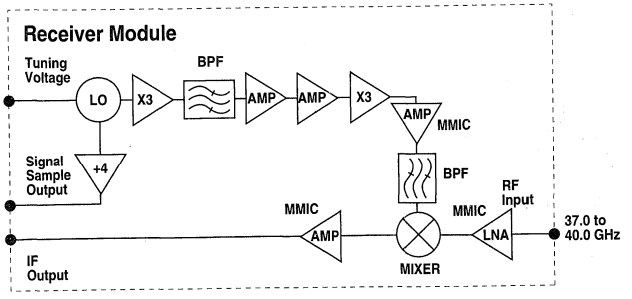
This digital radio receiver module provides the RF receive and down conversion function for 38 GHz digital radios.

This module offers excellent phase noise performance and can be easily phase locked to a frequency reference. The receiver module is ideal for use in radios using 2 and 4 FSK modulation. The low noise figure is achieved by using the Hewlett-Packard PHEMT MMIC technology coupled with an image reject mixer to minimize the noise figure. The receiver module features an integrated ultra low noise silicon bipolar VCO operating in the S/C band as the local oscillator. A portion of the oscillator output is coupled off and is applied to a frequency divider network. The low frequency output from the frequency divider can be used to phase lock the source. The local oscillator output is applied to a frequency multiplier network to produce the desired LO frequency to the mixer.

Applications

The digital radio receiver module provides the total RF receive and down conversion function in radios operating in the 37 to 40 GHz band.

Block Diagram



DRR1-38XX Absolute Maximum Ratings (T_A = -30 to +70°C)

Parameters	Units	Ratings
DC Circuit Power +8.5	Volts	10
+5.0	Volts	+5.5
-5.0	Volts	-5.5
Tuning Voltage	Volts	14

Notes:

1. Operation in excess of any one of these parameters may result in permanent damage.
2. A thermal interface medium must be used between the bottom of the package and its mating surface to ensure optimum heat transfer.

DRR1-38XX Electrical Characteristics

Parameters	Units	Min.	Typ.	Max.	Extended Range 39.5 – 40.0
RF Tuning Range	GHz	37		39.5	40
IF Frequency	MHz	630 or 1260			
IF Bandwidth	MHz	±20			
LO Frequency	GHz	RF – IF			
Gain[1]	dB	18		27	16 Min
Gain Flatness over 300 MHz	dB			±1	±1.5
Noise Figure	dB		7.5	9	9.5 Max
Operating Temperature Range	°C	-30		70	
Power Input at P-1dB	dBm	-20	-17		
LO Leakage at I[2]	dBm			-15	
LO Leakage at R[3]	dBm			-15	
Return Loss RF Port[4]	dB	8	10		5 Min
Return Loss IF Port	dB	14			
Image Rejection	dB	10	13		
Sample Out Frequency	MHz	1,010		1,080	1,094
Sample Out Power	dBm	-10		0	
Spurious Output[5]	dBc			-60	
Phase Noise @ 100 KHz	dBc/Hz		-83	-80	
Tuning Voltage	V	1		12	15 Max
Input Capacitance, Nom	pf		1,000		
LO Tuning Sensitivity	MHz/V		400	500	
LO Tuning Sensitivity Variation			1.5 : 1		
DC Circuit Power: 8.5 Volts	mA		270	350	
5 Volts	mA		470	650	
-5 Volts	mA		20	30	
Case Dimensions	inches	3.5 x 1.25 x 0.40			
Max Power at Input/no damage	dBm			7	
Humidity Non Condensing	%		85		
Condensing	%		95		
Connectors		WR 28			

Notes:

1. Gain degrades to 16 dB minimum from 39.5 to 40 GHz.
2. LO and Harmonic/sub-harmonic leakage at I with RF terminated into a waveguide.
3. LO and Harmonic/sub-harmonic leakage at R up to 50 GHz.
4. RF port return loss degrades to 5 dB minimum from 39.5 to 40 GHz.
5. Measured at IF port within the IF bandwidth with single tone RF input of <-20 dBm.

DRR1-38XX Typical Performance

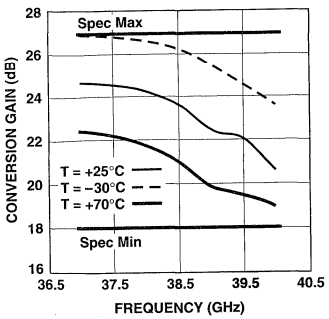


Figure 1. Conversion Gain vs. Frequency.

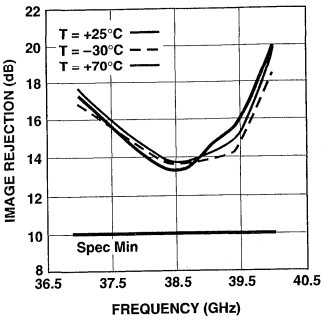


Figure 2. Image Rejection vs. Frequency.

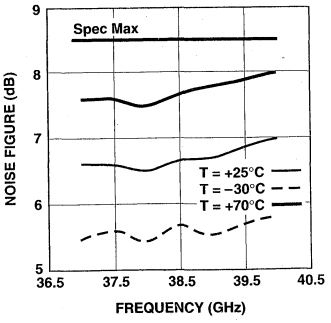


Figure 3. Noise Figure vs. Frequency.

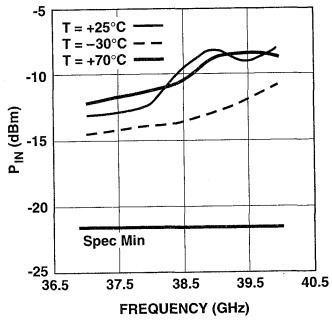


Figure 4. Power In at P_{1dB} Out vs. Frequency.

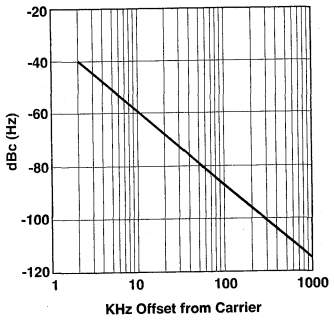


Figure 5. Phase Noise at 40 GHz vs. KHz Offset from Carrier.

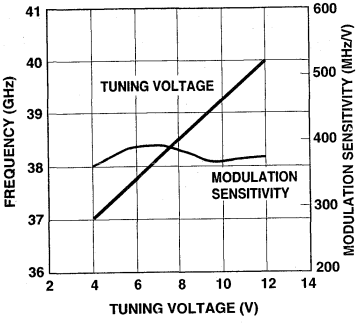


Figure 6. Tuning Voltage vs. Frequency and Modulation Sensitivity.

Powering Up Instructions

The -5 volts must be applied to the receiver module **before** applying the +5 volts. Likewise when shutting down the receiver module the +5 volts must be removed before the -5 volts is turned off. The +8.5 volts can be turned on in any sequence. Failure to follow this procedure could cause permanent damage to the module.

Mounting Instructions

Case must be mounted firmly, with screws, to an adequate metallic structure that has sufficient thermal properties to maintain the module case at a temperature not to exceed 70°C.

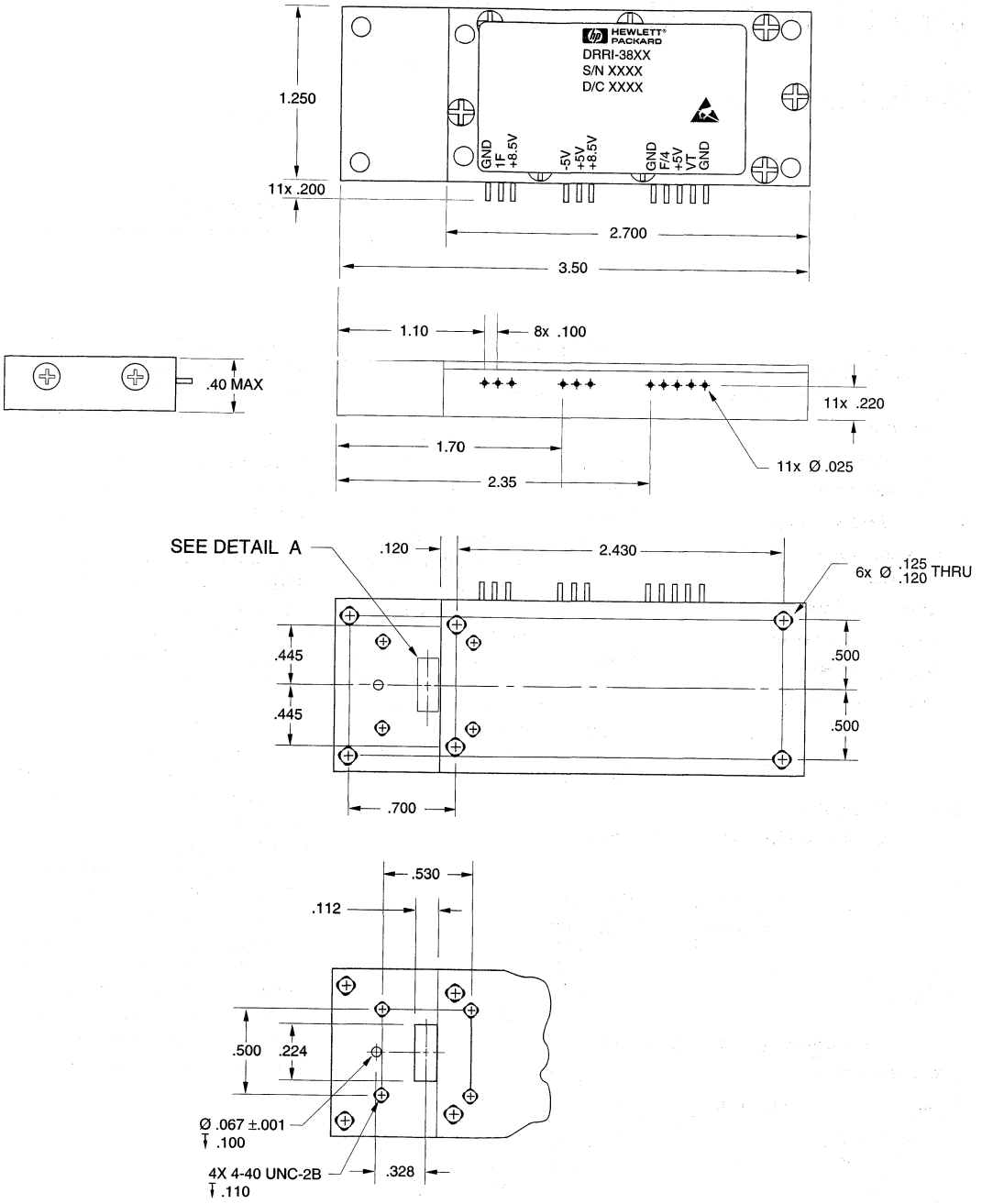
Product Options

Specify part number followed by option. For example:

DR R 1 – 38 X X

- Model Number Prefix = Digital Radio
- R = Receiver Module
- Internal Use
- 3 = WR-28 Waveguide Connector
- 1 = 630 MHz IF Frequency
- 2 = 1260 MHz IF Frequency
- 38 = 37 to 40 GHz Frequency Band

Case Dimensions (specified in inches)



DETAIL A

HEWLETT® PACKARD

Digital Radio Transmitter Modules for 21.2 to 23.6 GHz

Technical Data

DRT1-23XX

Features

- **Integrated Microwave/ Millimeter-Wave Modules**
- **Low Phase Noise**
- **Silicon Bipolar VCO**
- **Full Band Tuning**
- **GaAs MMIC Output Stage**
- **Sample Output for Phase Locking**
- **Excellent Tuning Linearity**
- **30 dB Attenuator**
- **Waveguide/SMA RF Output**
- **Detected Output**

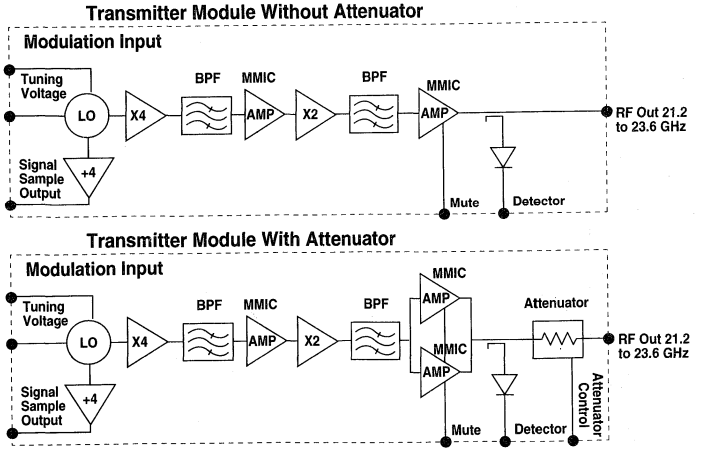
Description

This digital radio transmitter module is designed for medium data rate point to point communication systems operating at 23 GHz. This module offers excellent phase noise performance and can be easily phase locked to a frequency reference. The transmitter module provides +20 dBm of output power, ideal for use in radios using 2 and 4 level FSK modulation. The module features an ultra low noise silicon bipolar VCO operating in the S/C band. A portion of the oscillator output is coupled off and is applied to a frequency divider network. The low frequency output (less than 1 GHz) from the frequency divider can be easily used to phase lock the source. The main oscillator output is applied to a frequency multiplier network to produce the desired output frequency in the 23 GHz range. The output of this network is filtered then amplified by a GaAs MMIC device to produce the required output power. A detected sample of the output signal is provided to facilitate built in test of key radio components.

Applications

This digital radio module supplies the transmitter function in radios operating in the 21.2 to 23.6 GHz band. The source provides close to 100 mW output power over the temperature range of -30°C to +70°C. Included within the transmitter module is a muting function to reduce output power by 50 dB for "hot standby" applications. An internal voltage controlled attenuator function is optional allowing for 30 dB dynamic range adjustment.

Block Diagrams



DRT1-23XX Absolute Maximum Ratings (T_A = -30 to +70°C)

Parameters	Units	Ratings
DC Circuit Power +10	Volts	11
+5.0	Volts	+5.5
-5.0	Volts	-4.5
Power Control	Volts	5
Tuning Voltage	Volts	17

Notes:

1. Operation in excess of any one of these parameters may result in permanent damage.
2. A thermal interface medium must be used between the bottom of the package and its mating surface to ensure optimum heat transfer.

Electrical Characteristics

Part Number		DRT1-2321 or DRT1-2322			DRT1-2311 or DRT1-2312		
Parameters	**Units**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
RF Tuning Range	GHz	21.2		23.6	21.2		23.6
Operating Temperature Range	°C	-30		70	-30		70
Storage Temperature Range	°C	-45		85	-45		85
RF Power Output	dBm	19	20		19	20	
Sample Out Frequency	MHz	663		738	663		738
Sample Out Power	dBm	-10		0	-10		0
Detected Out	V	0.4		2	0.4		2
Harmonics and Sub-Harmonics from 2.65 to 55 GHz from carrier [1]	dBc			-30			-30
Spurious Output							
from 2.65 - 55 GHz [1]	dBc			-30			-30
@ fo ± 1.0 GHz	dBc			-50			-50
@ fo ± sample out frequency	dBc			-40			-40
Phase Noise @ 100 KHz	dBc		-85	-82		-85	-82
Tuning Voltage	V	1		16	1		16
Input Capacitance, Nom	pf		27			27	
Main Tuning Sensitivity	MHz/V		260	335		260	335
Main Tuning Sensitivity Variation			1.5:1	2.0:1		1.5:1	2.0:1
Modulation Bandwidth	MHz		20			20	
Modulation Sensitivity	MHz/V	7		25	7		25
Modulation Sensitivity Variation over any 300 MHz			1.15:1			1.15:1	
DC Circuit Power +10 Volts	mA			175			175
+5 Volts	mA			975			600
-5 Volts	mA			50			50
Frequency Pushing on +10V Line based on ±0.2V variation	MHz/V		40	50		40	50
Return Loss @ Full Power Output [2]	dB		10			10	
Mute Control	dBc		-50			-50	
Mute Control Range	V	0		5	0		5
RF Connector		WR 42 or Coax			WR 42 or Coax		
Attenuator Range	dB	30				NA	
Attenuator Control Voltage	V	0		5		NA	
RF Output Dynamic Range		30 Min.			NA		
Humidity Non Condensing	%		85			85	
Condensing	%		95			95	
Case Size	inches	3.50 x 1.25 x 0.40			3.50 x 1.25 x 0.40		

Notes:

1. Tested only to 50 GHz
2. Module is unconditionally stable with this load VSWR of 2.0:1

DRT1-23XX Typical Performance

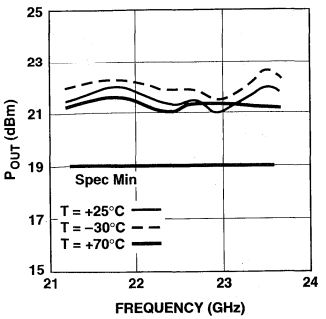


Figure 1. Power Out vs. Frequency.

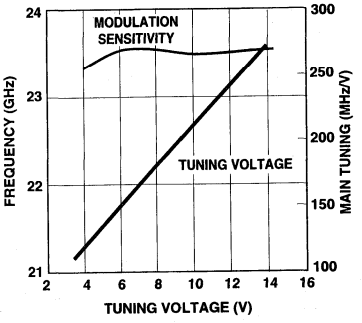


Figure 2. Tuning Voltage vs. Frequency and Modulation Sensitivity.

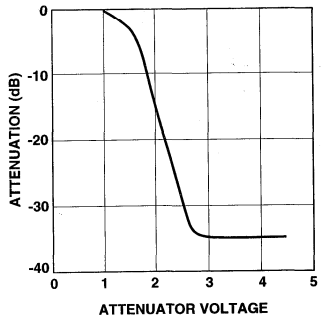


Figure 3. Dynamic Range Adjust.

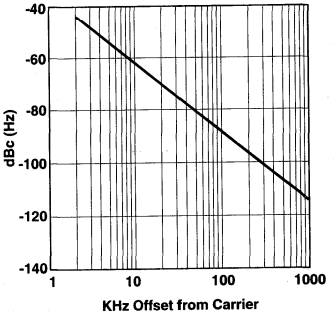


Figure 4. Phase Noise at 23 GHz vs. KHz Offset from Carrier.

Powering Up Instructions

The -5 volts must be applied to the receiver module **before** applying the +5 volts. Likewise when shutting down the receiver module the +5 volts must be removed before the -5 volts is turned off. The +10 volts can be turned on in any sequence. Failure to follow this procedure could cause permanent damage to the module.

Mounting Instructions

Case must be mounted firmly, with screws, to an adequate metallic structure that has sufficient thermal properties to maintain the module case at a temperature not to exceed 70°C.

Product Options

Specify part number followed by option. For example:

DR T 1 – 23 X X

Model Number Prefix = Digital Radio

T = Transmitter Module

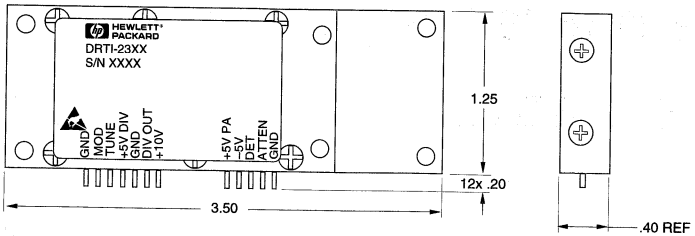
Internal Use

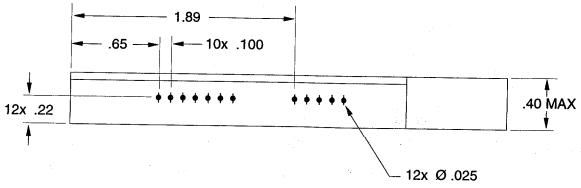
1 = SMA Connector
2 = WR-42 Waveguide Connector

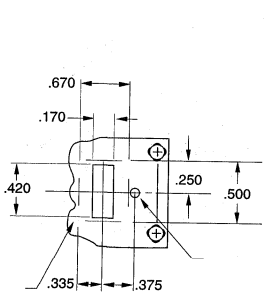
1 = No Attenuator
2 = Attenuator Option

23 = 21.2 to 23.6 GHz Frequency Band

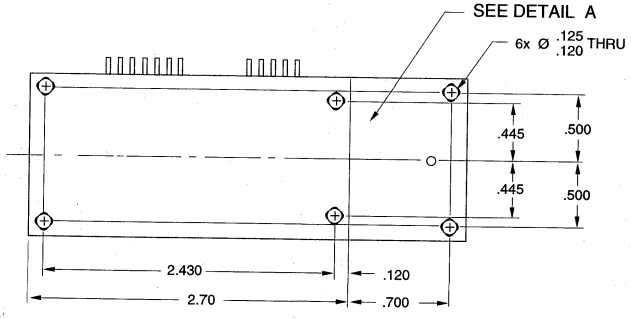
Case Dimensions







DETAIL A



HEWLETT® PACKARD

Digital Radio Transmitter Modules for 37 to 40 GHz

Technical Data

DRT1-38XX

Features

- **Integrated Microwave/ Millimeter-Wave Modules**
- **Low Phase Noise**
- **Silicon Bipolar VCO**
- **Full Band Tuning**
- **GaAs MMIC Output Stage**
- **Sample Output for Phase Locking**
- **Excellent Tuning Linearity**
- **30 dB Attenuator**
- **Waveguide/RF Output**
- **Detected Output**

Description

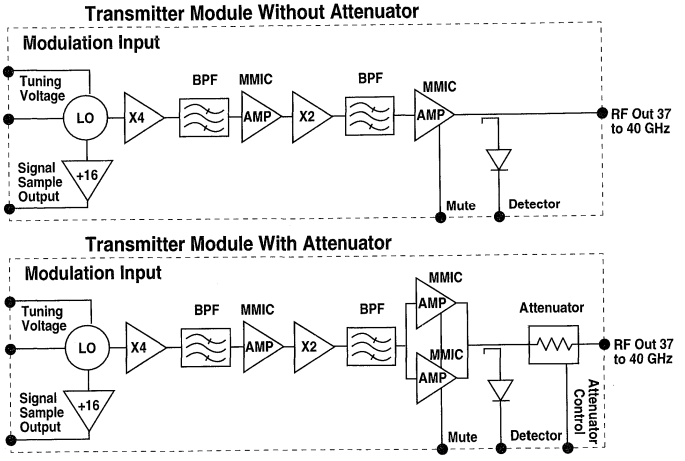
This digital radio transmitter module is designed for medium data rate point to point communication systems operating at 38 GHz. This module offers excellent phase noise performance and can be easily phase locked to a frequency reference. The transmitter module provides +19 dBm of output power, ideal for use in radios using 2 and 4 level FSK modulation. The module features an ultra low noise silicon bipolar VCO operating in the S/C band. A portion of the oscillator output is coupled off and is applied to a frequency divider network.

The low frequency output (less than 1 GHz) from the frequency divider can be easily used to phase lock the source. The main oscillator output is applied to a frequency multiplier network to produce the desired output frequency in the 37 to 40 GHz range. The output of this network is filtered then amplified by a GaAs MMIC device to produce the required output power. A detected sample of the output signal is provided to facilitate built in test of key radio components.

Applications

This digital radio module supplies the transmitter function in radios operating in the 37 to 40 GHz band. The source provides close to 100 mW output power over the temperature range of -30°C to +70°C. Included within the transmitter module is a muting function to reduce output power by 50 dB for "hot standby" applications. An internal voltage controlled attenuator function is optional allowing for 30 dB dynamic range adjustment.

Block Diagrams



DRT1-38XX Absolute Maximum Ratings (T_A = -30 to +70°C)

Parameters	Units	Ratings
DC Circuit Power +10	Volts	11
+5.0	Volts	+5.5
-5.0	Volts	-4.5
Power Control	Volts	5
Tuning Voltage	Volts	17

Notes:

1. Operation in excess of any one of these parameters may result in permanent damage.
2. A thermal interface medium must be used between the bottom of the package and its mating surface to ensure optimum heat transfer.

Electrical Characteristics

Part Number		DRT1-3823			DRT1-3813		
Parameters	**Units**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
RF Tuning Range	GHz	37		40	37		40
Operating Temperature Range	°C	-30		70	-30		70
Storage Temperature Range	°C	-45		85	-45		85
RF Power Output	dBm	18	19		18	19	
Sample Out Frequency	MHz	289		313	289		313
Sample Out Power	dBm	-10		0	-10		0
Detected Out	V	0.4		2	0.4		2
Harmonics and Sub-Harmonics from 2.65 to 55 GHz from carrier [1]	dBc			-30			-30
Spurious Output							
from 2.65 - 55 GHz [1]	dBc			-30			-30
@ fo ± 1.0 GHz	dBc			-50			-50
@ prescaler output frequency	dBc			-30			-30
Phase Noise @ 100 KHz	dBc		-82	-80		-82	-80
Tuning Voltage	V	1		16	1		16
Input Capacitance, Nom	pf		27			27	
Main Tuning Sensitivity	MHz/V	200		400	200		400
Main Tuning Sensitivity Variation			1.5:1	2.0:1		1.5:1	2.0:1
Modulation Bandwidth	MHz		20			20	
Modulation Sensitivity	MHz/V	10		35	10		35
Modulation Sensitivity Variation	%		20			20	
DC Circuit Power +10 Volts	mA			175			175
+5 Volts	mA			975			600
-5 Volts	mA			50			50
Frequency Pushing on +10V Line based on ±0.2V variation	MHz/V		40	50		40	50
VSWR @ Full Power Output [2]			2.5:1			2.5:1	
Mute Control	dBc		-50			-50	
Mute Control Range	V	0		5	0		5
RF Connector		WR-28			WR-28		
Attenuator Range	dB	30				NA	
Attenuator Control Voltage	V	0		5		NA	
RF Output Dynamic Range	dB	30 Min.			NA		
Humidity Non Condensing	%		85			85	
Condensing	%		95			95	
Case Size	inches	3.50 x 1.25 x 0.40			3.50 x 1.25 x 0.40		

Notes:

1. Tested only to 50 GHz
2. Module is unconditionally stable with this load VSWR of 2.0:1

DRT1-38XX Typical Performance

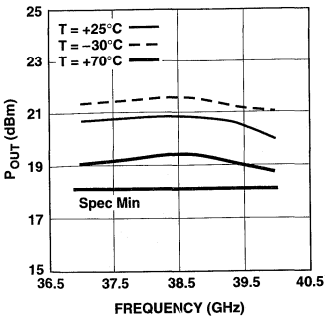


Figure 1. Power Out vs. Frequency.

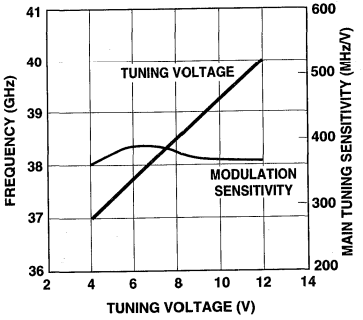


Figure 2. Tuning Voltage vs. Frequency and Modulation Sensitivity.

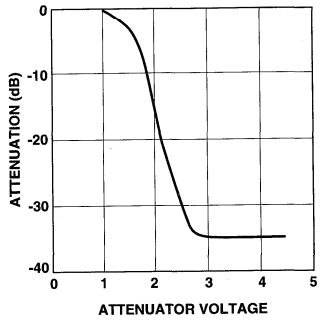


Figure 3. Dynamic Range Adjust.

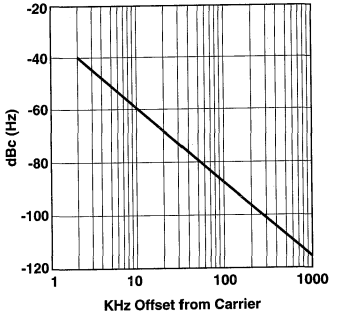


Figure 4. Phase Noise at 40 GHz vs. KHz Offset from Carrier.

Powering Up Instructions

The -5 volts must be applied to the transmitter module **before** applying the +5 volts. Likewise when shutting down the transmitter module the +5 volts must be removed before the -5 volts is turned off. The +10 volts can be turned on in any sequence. Failure to follow this procedure could cause permanent damage to the module.

Mounting Instructions

Case must be mounted firmly, with screws, to an adequate metallic structure that has sufficient thermal properties to maintain the module case at a temperature not to exceed 70°C.

Product Options

Specify part number followed by option. For example:

DR T 1 – 38 X X

Model Number Prefix = Digital Radio

T = Transmitter Module

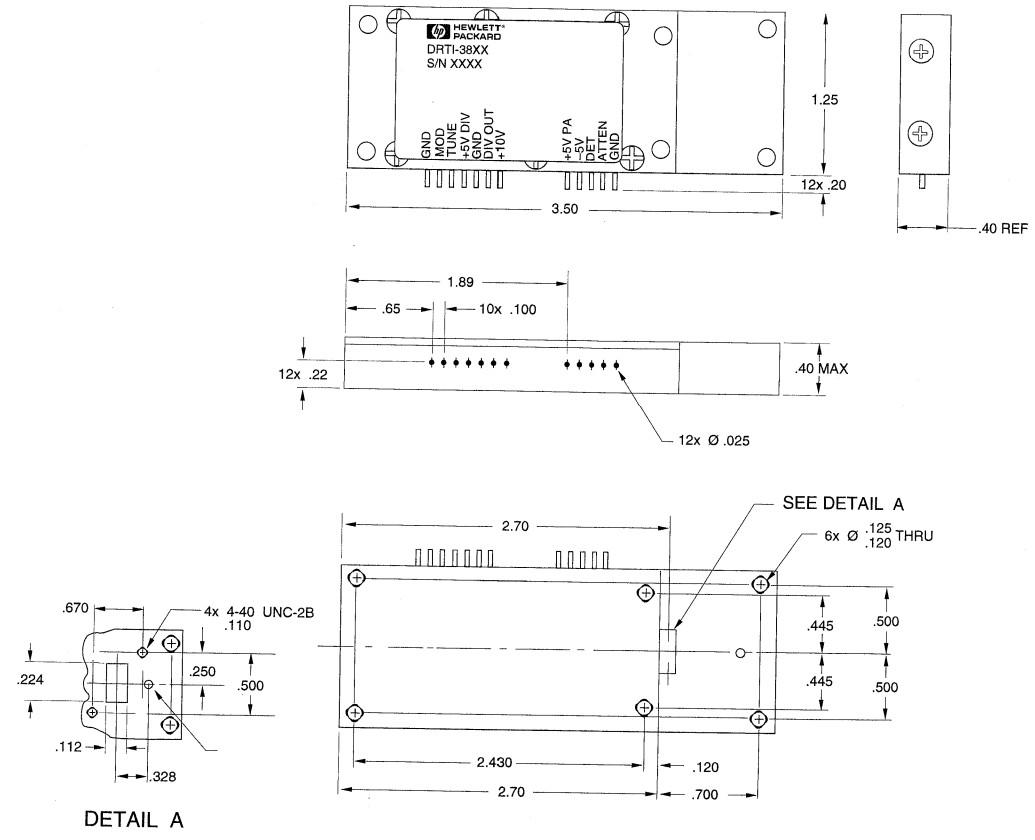
Internal Use

3 = WR-28 Waveguide Connector

1 = No Attenuator
2 = With Attenuator

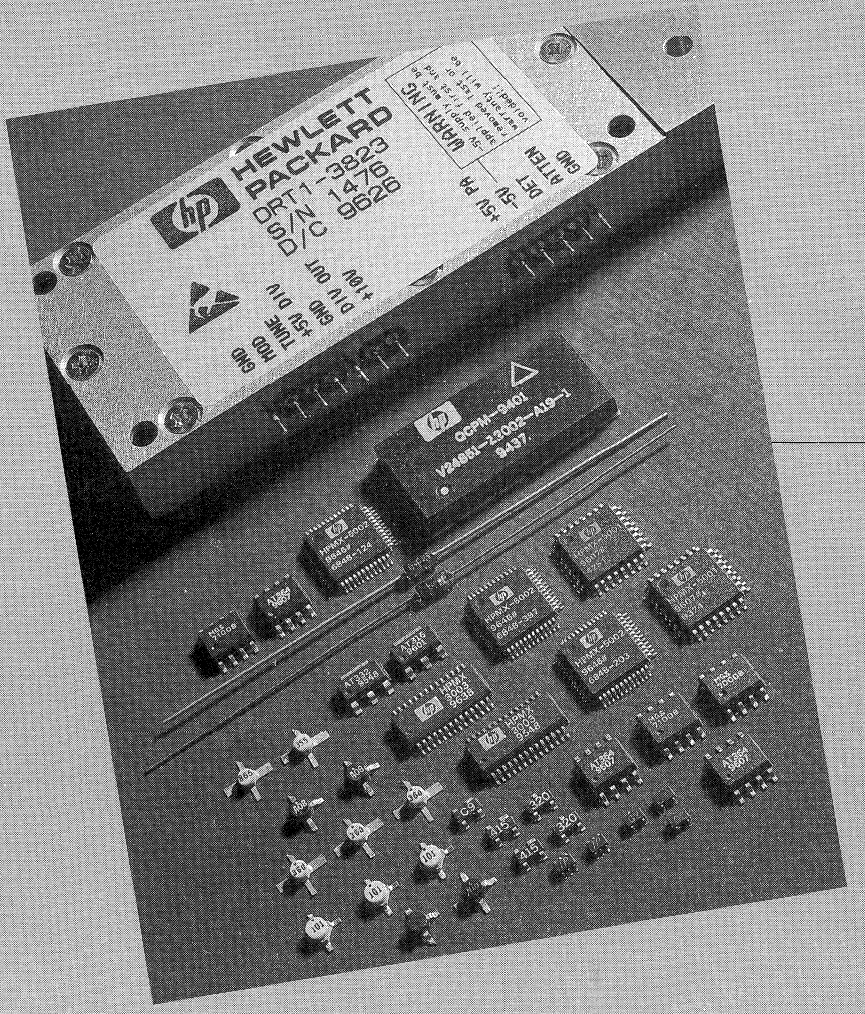
38 = 37 to 40 GHz Frequency Band

Case Dimensions



HEWLETT® PACKARD

Voltage Controlled Oscillators (VTOs)



Voltage Controlled Oscillators

The Hyperabrubt Varactor

A hyperabrupt varactor diode differs from the conventional (or abrupt) varactor used in microwave oscillators in that the concentration of the N-type material in the depletion region is made non-uniform through advanced computer-controlled profiling techniques. As a result, the hyperabrupt varactor produces a greater capacitance change in tuning voltage and a far more linear voltage-vs-frequency tuning curve.

In the HP HTO and VTO-9000 Series oscillator, the hyperabrupt varactor means improved tuning linearity (note the modulation sensitivity curves) and low tuning voltage.

Construction

HP fundamental varactor-tuned oscillators are constructed using ceramic substrates and thin-film construction techniques. Discrete transistors and capacitors are bonded directly to the ceramic substrate. All resistors are thin-film tantalum-nitride and are heat treated for stability. Exact resistor values are achieved using laser trimmers.

Hermeticity and reliability are assured by filling each completed oscillator package with an inert atmosphere, welding the lids in place and leak testing. HP MTO and HTO Series oscillators can be qualified to high reliability and MIL specifications appropriate to hybrid thin-film components.

Applications

VTOs are frequently used for commercial applications such as receiver oscillators and frequency synthesizers, the varactor-tuned oscillator is commonly used in a phase-locked loop. A VTO in a phase-locked loop has a frequency stability comparable to that of the reference oscillator (generally crystal controlled). Phase locked loops can be designed simply to stabilize a single output frequency or, with programmable frequency dividers, to allow the oscillator frequency to be varied in discrete steps as small as required .

Phase Locking the VTO

Where an oscillator of high stability is required, such as in communications equipment, HP VTOs can be readily phase-locked. A simplified block diagram of a practical circuit for use with the VT0-8060 (below 1000 MHz) is shown in Figure 1. At its RF output, this circuit duplicates the stability of the crystal input (frequently being multiplied by 16 times.)

Typical units built using this configuration display noise performance of better than—110 dBc/Hz at 20 kHz (sideband power to carrier power).

To fill requirements for highly stable oscillators above 1000 MHz, a possible circuit is offered in Figure 2.

Since phase locking is a rather complex subject requiring considerable tailoring to individual system requirements, several excellent sources of reference material have been prepared by manufacturers of op-amps and dividers. One of these books entitled, *Phase-Locked Loop Data Book*, is available from Motorola Semiconductor, Phoenix, Arizona. Another excellent reference on the subject is *Phase-Lock Techniques* by Floyd M. Gardner (John Wiley & Sons, publisher).

Typical PLL Circuits

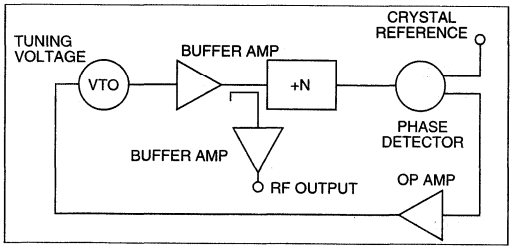


Figure 1. Programmable Divider

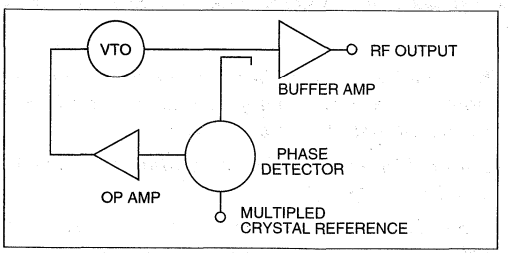


Figure 2. Multiplier

Application Information

The following application information is either published in this catalog or available from your local Hewlett-Packard sales office, authorized distributor, or representative.

Technical information is also available on the WWW at: ***www.hp.com/go/rf***

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455.

Application Notes

Installing TO-8 Oscillators

Application Note—M022

All TO-8 thin-film oscillators are designed to operate with unconditional stability and performance equal to or better than their guaranteed specifications when installed in a properly designed 50-ohm microstripline PC board. Problems encountered with systems using TO-8 oscillators can be directly traced to improper layout of the PC board, improper grounding of the devices to the board or the board to the case or chassis in which it is installed, or the lack of RF bypassing on DC leads when required.

In this section basic information on microstrip circuit design will be presented to allow designers to properly plan their custom microstrip board.

Microstripline Characteristics

A microstrip transmission line is fabricated with a single narrow conductor on one side of a relatively thin sheet of dielectric medium with a large area of ground plane on the other side. Generally the dielectric sheet is in the form of either a ceramic substrate for thin- and thick-film hybrid integrated circuits or PC board material for assemblies.

Electrically, a microstripline behaves like a two-wire transmission line with the second conductor formed by the image of the physical conductor appearing on the ground plane.

The characteristic impedance of a microstripline is determined by the width of the conductors and the dielectric constant and thickness of the substrate material on which it is fabricated. For the 0.062 in. thick, G-10 glass epoxy PC board material (1 oz. clad, both sides), a 50-ohm stripline is always 0.10 in. wide.

In a practical application, other conductors also appear on the microstrip board for DC bias and control voltages. The widths of these conductors are relatively unimportant so long as they are narrow compared to the large grounded areas which make up the bulk of the conductor side of the board to provide as much shielding and isolation as possible.

Figure 1 shows the standard mounting kit for TO-8 oscillators. Also shown is the correct installation for PC board mounting.

All connections to the pins on the modular devices are made via conductors on the bottom, or circuit, side of the board. The top, or ground plane, is left completely clad except for clearances milled around the holes drilled to pass device pins to prevent unintentional short circuits.

Since the ground plane side of the board is left completely clad, it assures both a good ground and effective heat sink when modules are clamped to it. Modules may also be secured with conductive epoxy or other means, so long as the cases are in intimate thermal and electrical contact with the ground plane.

On the conductor side of the board, all of the unused conductor areas are effectively interconnected to the ground plane, and the entire board is grounded to the case or chassis via mounting hardware.

Assembly Instructions For Customer-Designed Circuit Boards

The steps below apply to the assembly of HP modules into microstrips or stripline circuits. CAUTION: The HP modules are designed for use in a 50-ohm microstrip system and the package must be adequately grounded!

1. Cut all four pins to a length of approximately 3/16 inch.
2. After cutting the pins per Step 1, install the module directly on the circuit board ground plane with the Tune Voltage, RF output and DC Voltage pins (see Figure 1) passing through the board to the circuit on the other side. Be careful that these pins do not short out to the ground plane.
3. Using the clamp provided, secure the module firmly to the ground plane. Figure 1 shows the proper positioning and installation of the mounting clamp. This step ensures positive contact between the module package and the ground plane so that no problems with VSWR in a multistage system will be encountered.
4. Bend the Tune Voltage, RF Output, DC Voltage and GND pins flat against the proper portions of the printed circuit, then solder in place.

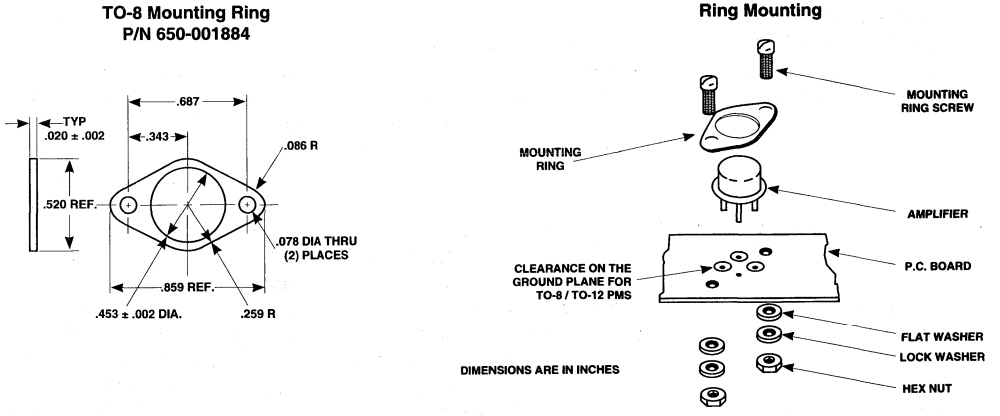


Figure 1. Mounting Kit for Standard TO-8 Packaged Oscillators

HEWLETT® PACKARD

Voltage-Controlled Oscillators Evaluated for System Design

Application Note—M024

High tuning speed, small size, and low power consumption make VCOs important components in a number of microwave applications. The designer must be able to evaluate these devices accurately in order to write proper VCO specifications for critical applications.

With its unique combination of very high tuning speed (typical full-band tuning in less than 30 ns.), small size, and low power consumption, the varactor-tuned, voltage-controlled oscillator (VCO) is a vital component in electronic defense systems, frequency-hopping radar, frequency synthesizers, and many other microwave applications. Unfortunately, high-performance microwave VCOs are difficult to design, build, and optimize.

Most microwave system designers find it far more practical to consider VCOs or integrated oscillator subsystems as components, and purchase them from one of the specialized manufacturers. Available production "raw" VCOs and VCO assemblies, which offer a wide selection of optimized performance features, are readily available in the 300 MHz to 18 GHz range. This article is intended primarily to help system designers evaluate available VCOs, and to assist them in writing VCO specifications for critical applications.

A Look at Oscillator Fundamentals

In its simplest form, a sinusoidal or quasi-sinusoidal oscillator (as opposed to such square-wave or pulse sources as the blocking or relaxation oscillator) can be modeled as the combination of an amplifier with a positive feedback loop and a frequency-determining network. Figure 1 illustrates this concept. The general feedback formula is

$$A_f = \frac{A}{1-\beta_f A} \quad \text{where} \qquad (1)$$

A = gain of the amplifier without feedback

A_f = gain of the amplifier with feedback

β_t = reverse transfer function of the feedback path

$$= \frac{V_f \text{ angle } \theta_1}{V_o \text{ angle } \theta_2} \qquad (2)$$

(the difference between $\theta 1$ and $\theta 2$ represents the phase shift through the path)

When feedback is positive, β_f is a positive quantity and, according to the Barkhausen criterion, when $\beta_f A=1$, A_f becomes infinite and the feedback amplifier becomes an oscillator. Since both the amplifier and the feedback circuit contain capacitive or inductive energy-storage elements (even if only due to parasitics), $\beta_f A$ is complex. To satisfy the Barkhausen criterion, the real part of $\beta_f A=1$ and the imaginary part is 0; thus the real part is unity and the phase is 0. Clearly, under these conditions, once oscillation begins due to any small amount of noise at the input of the amplifier, the signal would build up until the output of the amplifier reaches its saturated limit.

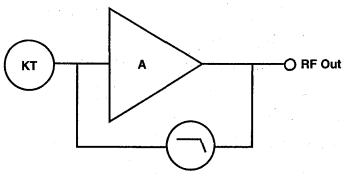


Figure 1. Block diagram of a microwave oscillator, modeled as a combination of an amplifier with a positive-feedback loop and a frequency-determining network. KT represents the noise input that starts oscillation.

The common-emitter amplifier circuit provides a nominal 180° phase shift, with the feedback network adding the additional 180° (or 540° . . . 360n + 180°). In the common-collector amplifier circuit, where the phase shift is nominally 0°, the feedback network must provide a full 360° phase shift.

The model in Figure 1 represents essentially a surface-acoustic-wave (SAW) oscillator in which the feedback path consists of a delay line and low-pass filter. Of course, if the transistor has a sufficiently high f_{max}, there is always a possibility that a simple delay will provide a total 360° phase shift at a fundamental frequency and at a number of harmonically related frequencies, or that other 360° feedback paths at non-harmonically related frequencies will exist since conductor lengths are a significant part of an electrical wavelength.

Actually, most microwave-oscillator designers use a different model, and analyze oscillators in terms of a negative-resistance generator and resonator. An example of a negative-resistance generator is shown in Figure 2. By first transforming it to its equivalent circuit (Figure 3), the input impedance of this circuit can be shown to generate a negative-resistance. It can be shown through nodal analysis that the input admittance of this circuit is:

$$Y_{in} = \frac{1}{R}\left\{\frac{1 - f_c^2}{f^2}\right\} + \frac{1}{j2\pi f1} \quad (3)$$

if $f_c > f$ Re $|Y_{in}| <$ Im $|Y_{in}|$ Inductive

where $f_c = \frac{1}{2\pi\sqrt{LC}}$ (4)

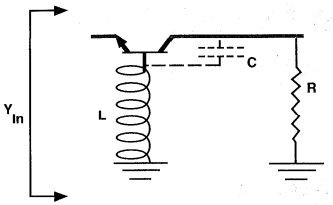


Figure 2. Example of a negative-resistance generator. Most designers model microwave oscillators as a negative-resistance generator and oscillator.

This equation demonstrates that a bipolar transistor with an inductor between base and ground becomes the equivalent of negative conductance in parallel with an inductive susceptance over a range of frequencies $f_c > f$. The inductor L is selected by design, whereas the value of C is provided by the collector-base capacitance of the transistor.

The common-base circuit is not the only topology that can be used to generate a negative resistance, and in practice a common-emitter configuration with the resonator in the base circuit is used as frequently as the former. The selection of an appropriate circuit topology is a complex task, dictated by such factors as the type of resonator being used, the characteristics of the transistor, and the frequency of the oscillator. The complete VCO is produced by adding a parallel or series resonant circuit (Figures 4 and 5).

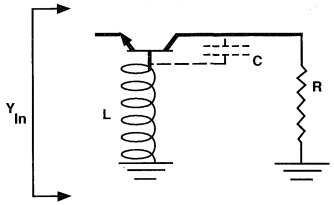


Figure 4. When the designer adds a parallel resonant circuit to the equivalent circuit shown in Figure 2, the result is a complete voltage-controlled oscillator.

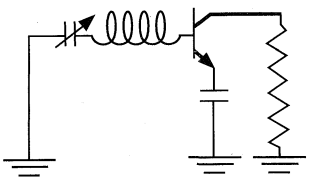


Figure 5. VCOs may also be constructed by adding a series resonant circuit to the negative-resistance generator. In this example, it is added to the base circuit in a common-emitter amplifier.

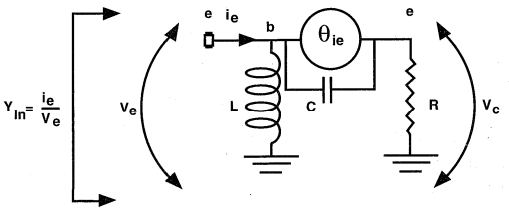


Figure 3. The equivalent circuit of the negative-resistance generator shown in Figure 2. Through nodal analysis, the input impedance of this circuit can be shown to generate a negative resistance.

Phase (FM) Noise — A Significant Criterion

The major concern of synthesizer designers is the phase stability (or phase noise). It is also critically important in EMC systems, frequency-agile radar systems, Doppler radar systems, radar warning receivers, and various communications applications. In such applications, an oscillator's phase-noise output may set the system's limits for dynamic range and reception sensitivity. The output of an ideal sine-wave oscillator can be described as:

$$V(t) = V_0 \sin 2\pi\mu_0 t$$

where V_0 is the nominal amplitude and μ_0 the nominal frequency. For an actual sine wave, the equation becomes:

$$V(t) = [V_0 + E(t)] \sin [2\pi\mu_0 t + \phi(t)], \quad (5)$$

where E(t) is the magnitude of random variation in amplitude, and $\phi(t)$ that of phase.

The phase noise of an oscillator is best seen in the frequency domain, where special purity is determined by measuring noise power in sidebands about the output-signal center frequency (carrier). Note, though, that on a spectrum analyzer it is impossible to tell whether the power at different Fourier frequencies is a result of implitude or of phase fluctuations. Fortunately, since most oscillators operate in saturation, AM noise is limited. It is usually 20 dB lower than phase noise and can often be disregarded.

In practice, phase spectral density is measured by passing the oscillator signal through a phase discriminator, substantially amplifying the resulting discriminator-output spectrum, then displaying it on a low-phase-noise spectrum analyzer. Single-sideband phase noise is usually specified in dBc/HZ at a given frequency from the carrier. Figure 6 is an FM noise nomograph that converts between single-sideband noise power ratio and frequency deviation at any distance from the carrier.

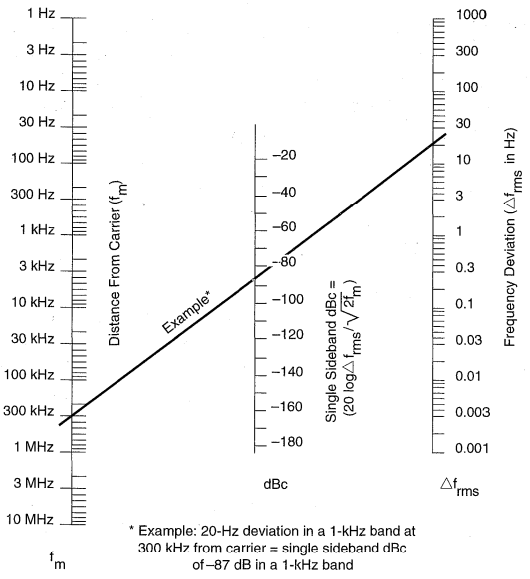


Figure 6. FM noise-conversion nomograph. By placing a straight edge on the frequency deviation in Hz (right column) and on the distance from the carrier at which that deviation occurs (left column), the single-sideband noise-power ratio in dBc is shown in the center column.

Total FM noise can be expressed as a sideband-to-carrier power ratio by the following relationship:

$$dB = 20 \log \sqrt{2} \left\{ \frac{f_m}{\Delta f_{RMS}} \right\} \quad (6)$$

where
Fm = frequency from the carrier
Δf_{RMS} = deviation

When frequency deviation is known in a given bandwidth, the following equation can be used to normalize the frequency deviation to any reference bandwidth:

$$\Delta f_{2RMS} = \Delta f_{1RMS} \frac{B_2}{B_1} \quad (7)$$

This relationship shows the importance of specifying the reference bandwidth when comparing the FM noise performance of various VCOs. The typical FM noise performance of four production VCOs is shown in Figure 7.

The phase noise generated by a VCO is determined primarily by the Q (quality factor–ratio of reactance to resistance) of the overall circuit and the Q of the varactor diode. The oscillator circuit itself is usually designed with a specific parameter in mind. In order to design a circuit with a very high Q, the tuning bandwidth must invariably suffer. Therefore, an oscillator circuit designed for optimum phase-noise performance will be ultimately a fairly narrow-band oscillator.

In most cases, choosing a varactor diode for low phase noise requires only that the highest available Q be selected for the operating frequency and tuning bandwidth required. The selection of transistors, however, is a more involved process. The transistor intended for use as a microwave oscillator must offer a high f_{max} to ensure reasonable efficiency, have a sufficiently large active area to provide adequate output power, and have a low-enough thermal resistance to ensure thermal stability.

The problem is that the f_{max} is higher for devices with smaller areas and, conversely, larger-area devices yield higher output power at lower frequencies. Thus, the transistor is selected by balancing output power vs. oscillator efficiency.

Once oscillation begins due to any small amount of noise at the amplifier's input, the signal will build up until the amplifier's output reaches its saturated limit.

The transistor with the largest device geometry or periphery that will operate at the design frequency is usually selected. For example, in designing a +10-dBm-power-output 10-GHz oscillator for low noise, a bipolar transistor with an F_t of 8 GHz and saturated output power of +20 dBm would be preferable to another device with an F_t of 12 GHz and the capability of only +13-dBm output power. As a general rule, silicon bipolar transistors are used rather than FETs in oscillators through Ku band when low noise is the most important consideration, since the phase-noise performance of silicon bipolar oscillators is typically 10 to 15 percent lower than that of FET oscillators operating under the same conditions.

The design of low-noise oscillators is complicated when frequency tuning is required. If only a narrow tuning range (< 2 percent) is needed, a cavity-stabilized or dielectric resonator oscillator with a frequency-pulling circuit — essentially an AFC with user access to the error voltage loop — is often the best choice. Thin-film VCOs can also be suitable with circuit optimization, and careful varactor and semiconductor selection.

When wider tuning bandwidths (10 to 15 percent) are required, VCO circuits using high-Q tuning diodes and low-noise silicon transistors, combined with special feedback techniques that reduce FM noise while retaining other critical VCO performance characteristics, are necessary. The best noise performance is obtained by tuning the VCO directly, without the use of a linearizer. A practical linearizer circuit will contribute AM noise to the control signal, which results in VCO phase noise at the oscillator output.

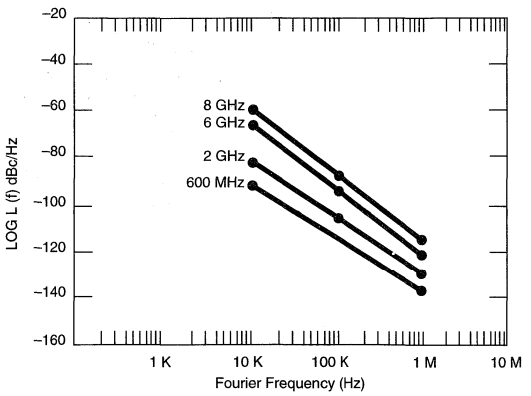


Figure 7. Single-sideband phase-noise comparison of four production VCOs.

The impedance of the tuning voltage source fed to a "raw" VCO should be very low and, in many cases, shielding may be required on interconnecting leads and wires to suppress stray pick-up. Noise specifications should include the required tuning video bandwidth, which should be as small as possible.

Power-supply voltage regulation is also a very important consideration when using low-noise VCOs. Fluctuations or noise on the bias voltage supplied to the oscillator will cause frequency pushing, which also appears as phase noise on the output-signal spectrum. Figure 8 shows the typical FM noise performance of a 600-MHz thin-film oscillator, and of an 8-GHz fundamental thin-film oscillator designed specifically for low-noise applications.

Settling Time and Post-Tuning Drift

For a VCO, settling time is defined as that interval between the time when the input-tuning-drive waveform reaches its final value and the time when the VCO frequency falls within a specified tolerance of a stated final value. In Figure 9, the input-drive waveform reaches its vinal value at time t_0. The VCO frequency reaches the lower edge of its specified tolerance band Df_{ST} at time t_{ST}. Settling time is the interval t_{ST} to t_0. The required final frequency is reached at time t_r.

Post-tuning drift is defined as the frequency drift that occurs between two arbitrarily defined times t_1 (which may be specified typically as 10 ms. to 1 sec. after the tuning step has been applied to the VCO) and t_2. For short-term PTD, time t_2 would generally be defined in the range of 10 ms. to 1 sec. after t_1; for long-term PTD, t_2 could range from 1 sec. to 1 hr. Drifting of bias voltages and thermal effects (i.e., changes in both the varactor and transistor junction temperatures) are the primary contributors to short-term PTD.

Bias circuit design is critical to PTD performance. The change in frequency due to a change in input bias is approximately 0.3 to 0.7 percent per Volt. This cannot be eliminated simply by using a well-regulated bias supply, since dramatic changes in PTD will occur due to changes in the transistor load present at the device end of the oscillator's internal bias circuitry. As the operating frequency of an oscillator is varied, the currents flowing in both the varactor and the transistor change (the reason why the frequency-vs.-output power curve is not perfectly flat), thus

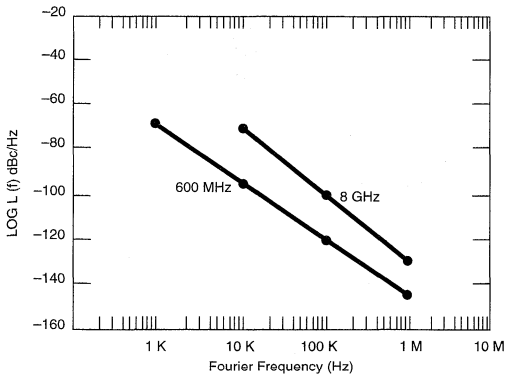


Figure 8. Low-noise VCOs typically have phase noise 10 to 15 dB lower than standard CVOs. These curves should be compared to those displayed in Figure 7.

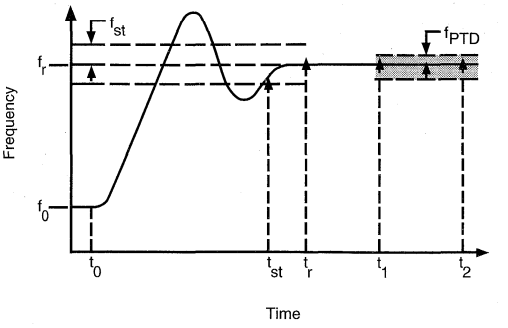


Figure 9. Frequency response of a VCO in response to a tuning-voltage step change. The input-drive waveform reaches its final value at time t_0. The VCO frequency reaches the lower edge of its specified tolerance band D_fST at time t_{ST}. Settling time is the interval t_{ST} to t_0. The required final frequency is reached at time t_r. The frequency drift that occurs between two arbitrarily defined times t_1 (which may be defined typically as 10 ms. to 1 sec. after the tuning step has been applied to the VCO) and t_2 (which is defined as "post-tuning drift").

varying the amoung of power dissipated (the efficiency of the oscillator). This means the load on the bias line varies with frequency, and the bias circuitry within the oscillator must compensate.

During the interval when a VCO is being tuned, the junction temperatures of both the transistor and varactor are also changing due to the changes in RF circuit efficiency and loading. This causes impedance changes, which result in frequency shift. The time interval during which this happens is dependent upon the thermal impedance of the devices.

Varactors used by Ku band are made typically from silicon. Above 12 GHz, GaAs varactors are used because of their higher Q. The GaAs devices have higher thermal resistance than silicon devices; this results in significantly higher short-term PTD factors.

Changes in the junction temperature of the transistor can be minimized through a reduction in input bias power. The trade-off is that reduced bias results in lower oscillator output power so that additional amplifier stages are required to bring the power output up to the required level.

Long-term PTD is affected mainly by the varactor-charging effect over a period of time. This reversible effect is caused by impurity ion buildup around the varactor junction over a long period of time. This causes a change in the capacitance of the varactor, resulting in a frequency change in the oscillator. Passivation of silicon varactors has been very successful in reducing this effect. Long-term PTD has been improved to yield less than 1 MHz frequency drift for one-hour periods. No such technique has yet been applied effectively to GaAs varactors, which display a significant charging effect.

Figure 10 is a comparison of fundamental transistor oscillators using a silicon varactor diode (Avantek VTO-8400) and a GaAs varactor diode (Avantek HTO-4000) at 4 GHz. Both settling time and post-tuning drift can also be affected by instability of the tuning signal.

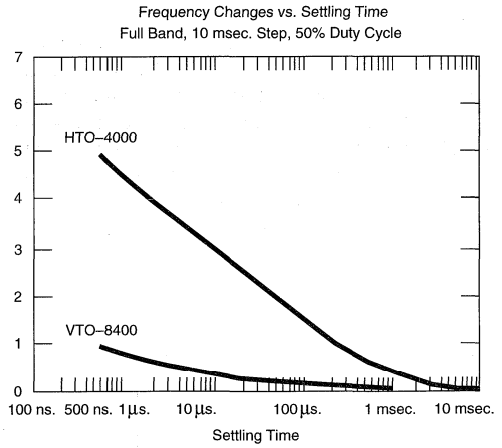


Figure 10. Comparison of the settling times of two standard VCOs at 4 GHz. Use of a silicon varactor results in substantially faster settling than does the use of a GaAs varactor.

Table I illustrates the various VCO parameters affected by the varactor. Care should be taken in selecting the correct type of VCO for a particular application, keeping in mind the trade-offs between tuning voltage limits, phase noise, settling time, and PTD. Figure 11 depicts a phase-noise comparison between a VCO using a silicon tuning diode versus one with a GaAs tuning diode, to highlight the phase-noise trade-offs.

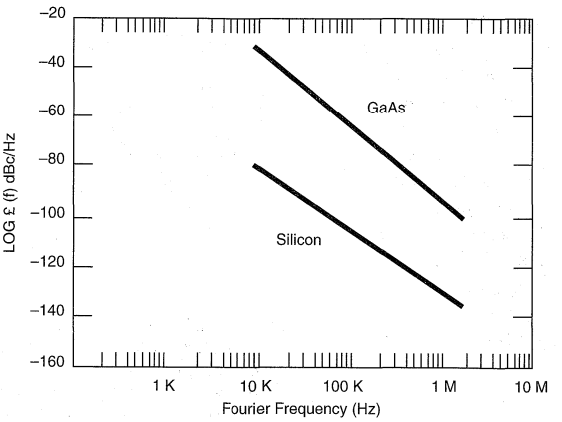


Figure 11. Single-sideband phase-noise comparison of a silicon and a GaAs varactor used in an 8-GHz VCO. The superiority of the silicon varactor in phase noise is readily apparent.

Tuning Linearity and Linearizers

Whether silicon or GaAs, there are two basic types of varactors: abrupt and hyperabrupt. The essential difference between the two is that the concentration of N-type dopant is nearly constant across the depletion region of an abrupt diode, but is nonlinear in a hyperabrupt diode. As the reverse bias is increased, the nonlinear doping profile causes a greater capacitance change in the hyperabrupt-junction diode than in the abrupt-junction diode. This results in a more nearly linear tuning curve, and a lower maximum tuning voltage.

The equation for junction capacitance vs. applied voltage for the abrupt varactor is approximated by:

$$C(V) = \frac{C(0)}{\left(1 + \frac{V}{\phi}\right)^{\gamma}} \qquad (8)$$

where
C(0) = junction capacitance at 0 V,
V = applied voltage
ϕ = contact potential
γ = a constant

γ is dependent on the doping of the device, but is usually equal to approximately 0.5 for an abrupt-junction diode. For $\gamma = 2$, which is approximately the case for a hyperabrupt-junction varactor, the tuning curve is nearly linear.

The abrupt-tuning diode will provide a very high Q with a continuous monotonic tuning curve, and will also operate over a very large range of tuning voltages (0 to 50 V). Because of its high Q, the abrupt diode offers the best available phase-noise performance. Both silicon and GaAs abrupt diodes are available, and both are used in VCOs.

Table I

Relative VCO Performance vs. Type of Varactor Diode

Diode	Linearity	Tuning Voltage	Harmonics	Residual FM	Phase Noise	Temperature Stability	Settling Time	PTD
Si-Abrupt	Fair	0 to 60	Good	Very Good	Very Good	Very Good	Excellent	Excellent
Si-Hyperabrupt	Good	0 to 20	Good	Good	Good	Good	Excellent	Excellent
GaAs-Abrupt	Fair	0 to 50	Good	Good	Good	Excellent	Good	Good
GaAs-Hyperabrupt	Good	0 to 20	Good	Fair	Fair	Fair	Fair	Fair

The hyperabrupt diode will provide a much more linear tuning response than the abrupt diode due to its linear tuning response than the abrupt diode due to its linear voltage-vs.-capacitance characteristics. This also enables it to cover a wider frequency range in a smaller tuning voltage (0 to 20 V). Its drawback is a much lower Q than the abrupt diode. This results in a phase noise typically about 3 dB higher than for an abrupt diode.

The trade-offs become obvious by examining the performance of two fundamental-output voltage-tuned oscillators covering 900 MHz to 1600 MHz (Figs. 12 to 14). The Avantek VTO-8090 employs an abrupt-tuning varactor while the VTO-9090 uses a hyperabrupt-tuning varactor.

The superior linearity of the VTO-9090 can be seen by comparing the two tuning-voltage characteristics (Fig. 12) and their modulation-sensitivity curves (Fig. 13). Note the power output difference of the two types of oscillators (Fig. 14). The abrupt-tuned VCO has higher power than its hyperabrupt-tuned counterpart. This is due to the higher Q of the abrupt varactor.

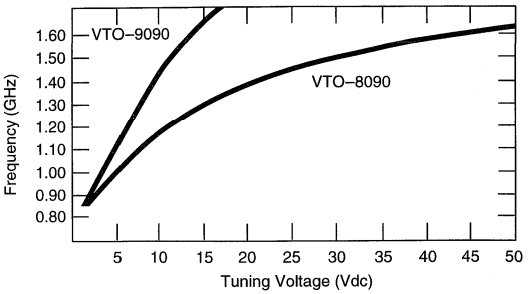


Figure 12. Tuning voltage vs. frequency for similar non-buffered VCO modules. One uses an abrupt-tuning varactor, the other a hyperabrupt-tuning varactor. The hyperabrupt varactor provides a significant improvement in tuning linearity with a significantly lower tuning-voltage range.

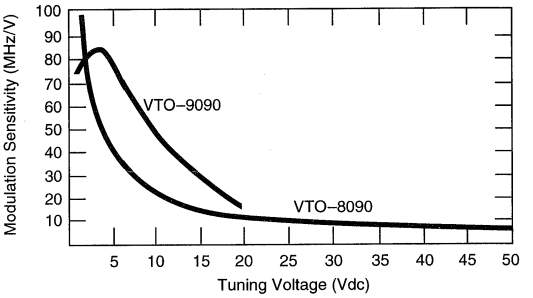


Figure 13. The superior linearity of the VTO-9090 can be seen by comparing the modulation-sensitivity curves displayed here, with the two tuning-voltage characteristics shown in Figure 12.

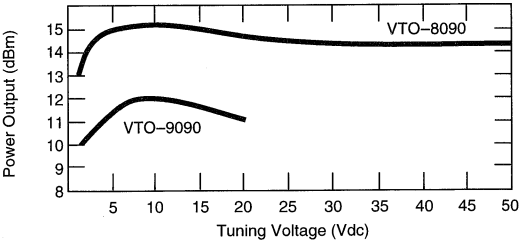


Figure 14. The disadvantage of the more-linear-tuning hyperabrupt varactor is that its lower Q tends to reduce the output power available from an oscillator.

A typical VCO tuning curve is shown in Figure 15. Where a straight voltage-vs.-frequency curve is necessary (e.g., in an open-loop system), a linearizer may also be needed.

Using a VCO linearizer can provide a very accurate tuning curve but creates its own set of problems. In addition to the tuning-curve correction, a linearizer can provide

1. a low tuning-voltage range, typically 0 to 10 Volts;
2. a constant tuning-port input impedance;
3. simple intervact to a digital-to-analog (D-A) converter.

On the negative side, a linearizer

1. requires additional input power;
2. may result in a higher MHz-per-Volt modulation sensitivity (which may not be desirable);
3. will almost invariably have a lower input impedance than the oscillator;
4. will reduce the modulation bandwidth.

Tuning curve of a linearized VCO will fall within a window about a straight line. Percent linearity is the termused to define the actual linearity achieved vs. the "best-fit straight line." This is graphically shown in Figure 16.

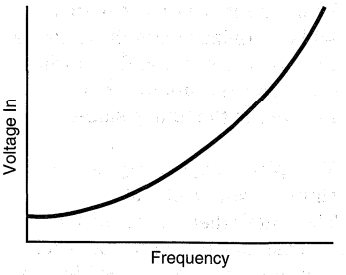


Figure 15. Typical varactor-tuned-oscillator voltage-vs.-frequency curve. Note that, although nonlinear, the curve is monotonic—an increase in tuning voltage always results in an increase in frequency. This curve can be linearized with additional circuitry at the expense of new problems.

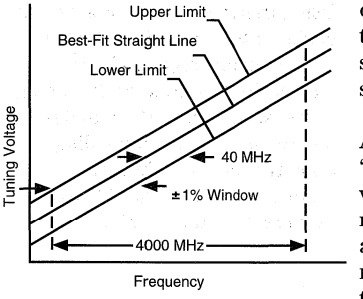


Figure 16. The tuning curve of a linearized VCO will fall within a window about a straight line. "Percent linearity" is the term used to define the actual linearity achieved vs. the "best-fit straight line." Within the window there will be typically some irregular variations in slope due to the breakpoints in the linearizer.

Calculating percent linearity is done by taking one-half the measured window, dividing this figure by the total tuning range, and expressing the result as a percentage. Using the values given in Figure 16, percent linearity is expressed as:

$$\text{Percent} = \pm \frac{80/2}{4000} \times 100 = 1\% \quad (9)$$

Within the percentage window specified there will be typically some irregular variations in slope due to the breakpoints in the linearizer. The result is that the amount of frequency change per tuning-voltage change will vary from point to point along the curve. If modulation is applied to the tuning input, varying FM deviation would result over the tuning range. A slope-ratio limit should be specified where constant FM deviation is required.

A properly designed and "tweaked" linearizer can provide virtually any degree of linearity required for a particular application. Linearizer circuits may also incorporate theadditional function of shifting the tuning voltage provided by the system to one more appropriate for the oscillator itself.

Typically two types of linearization schemes are employed today: analog and digital. The use of an analog linearizer is desirable when the oscillator interfaces with an analog tuning voltage or when a linear modulation spectrum is desired at any point in the frequency range. A simple analog-linearizer circuit is shown in Figure 17. The primary use for a digital linearizer is an applications where the oscillator is to be tuned by a digital computer.

Referring to the analog-linearizer circuit shown in Figure 17:

$$V_o = V_i + (I_2R_F) + (I_1R_F)$$

$$I_2 = \frac{V}{R_A}$$

$$I_B = \frac{V_B - V_D - V_{TH}}{R_{TH}} \quad (10)$$

$$I_1 = I_B + I_2$$

$$\text{Also } I_B = 0 \text{ if } (V_D + V_{TH}) \geq V_B \quad (11)$$

$$\text{Therefore, } V_0 = V_i\left(1 + \frac{2R_F}{R_A}\right) + I_BR_F$$

From this it is easily seen that V_{TH} will determine where the increase in slope will occur and R_{TH} will determine the amount of the increase in the tuning slope.

To replace R_{TH} and V_{TH} with a simple resistive divider, Thevenin's theorem is used. By this method, the circuit shown in Figure 18 may be replaced by the circuit shown in Figure 19 where

$$V = \frac{V_S}{V_{TH}}$$

$$R_1 = \frac{R_{TH}}{V} \quad (12)$$

$$R_2 = \frac{R_{TH}}{(V-1)}$$

Using this type of circuit gives the designer the capability of introducing almost any number of changes to the slope of the tuning curve, which may all be implemented in parallel, depending upon the degree of linearity required. This circuit will also provide good modulation response, which will only be restricted by the frequency response of the op amp itself.

One of the most efficient linearization techniques combines an analog-to-digital converter with a PROM and an op amp (Figure 20). Using this configuration and a small computer, the PROM may be programmed to provide linearity better than 0.5 percent across the full frequency spectrum of the VCO. The circuit will also provide extremely fast tuning-response time, primarily limited by the settling time of the op amp.

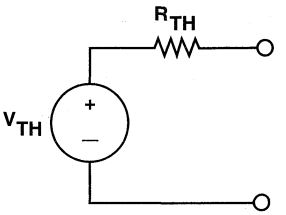


Figure 18. Simple analog-linearizer circuit. This equivalent model of V_{TH} and R_{TH} is derived from Figure 17.

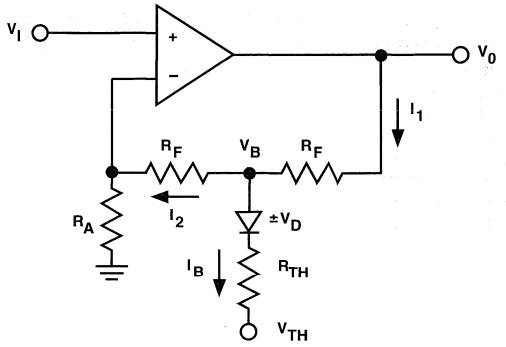


Figure 17. In this typical analog-linearizer circuit, V_{TH} will determine where an increase in the voltage-vs.-frequency slope will occur and R_{TH} will determine the amount of the increase in the slope that takes place.

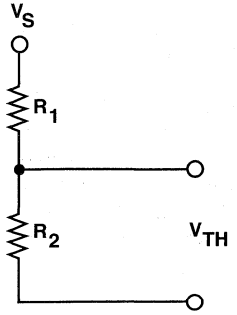


Figure 19. To replace R_{TH} and V_{TH} (Figs. 17 and 18) with a simple resistive divider, it is possible to calculate the required values using Thevenin's theorem. This provides the capability of introducing almost any number of changes to the slope of the tuning curve.

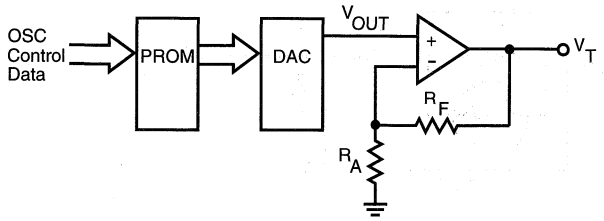


Figure 20. One of the most efficient linearization techniques combines an analog-to-digital converter with a PROM and an op amp. The PROM may be programmed to provide linearity better than 0.5% across the full frequency spectrum of the VCO and will also provide extremely fast tuning-response time, primarily limited by the settling time of the op amp.

Temperature Compensation and Stabilization

A reduction of VCO frequency variations with changes in temperature may be carried out using one or more of these three basic techniques: control of the oscillator temperature, tuning-voltage temperature compensation, or the use of a phase-locked loop.

The temperature of a small component such as a TO-packaged VCO is easily controlled either by a very small, low-power heater or by placing the component in a temperature-controlled chamber (oven). DC proportionally controlled heater assemblies specifically designed for use on TO-8-type cans are available commercially. It is also relatively simple to fabricate a heater by mounting the osciallator on a block (which provides thermal mass) that is temperature-controlled using a proportional heater (Figure 21).

A self-controlling heater that employs a material with a definitive temperature-vs.-resistance characteristic may be used. This material may be epoxied directly to the top of the TO-8 oscillator and then supplied with a bias voltage. The temperature-vs.-resistance characteristic of the material will make it act as a temperature-controlled heater that will provide very good temperature stability at a very low cost.

When any heater approach is used for temperature compensation, the temperature of the oscillator must be kept 5 to 10 degrees above the maximum expected system operating temperature. This will ensure that the oscillator will not be affected by the external temperature changes. The primary drawback to using the heater is the extra power required to keep the oscillator at a higher-than-ambient temperature.

The effect of temperature on the oscillator frequency may also be reduced indirectly by varying the tuning voltage in the proper direction to bring the oscillator back to the correct frequency. Temperature compensation of the tuning network requires using a negative-temperature-coefficient (NTC) or positive-

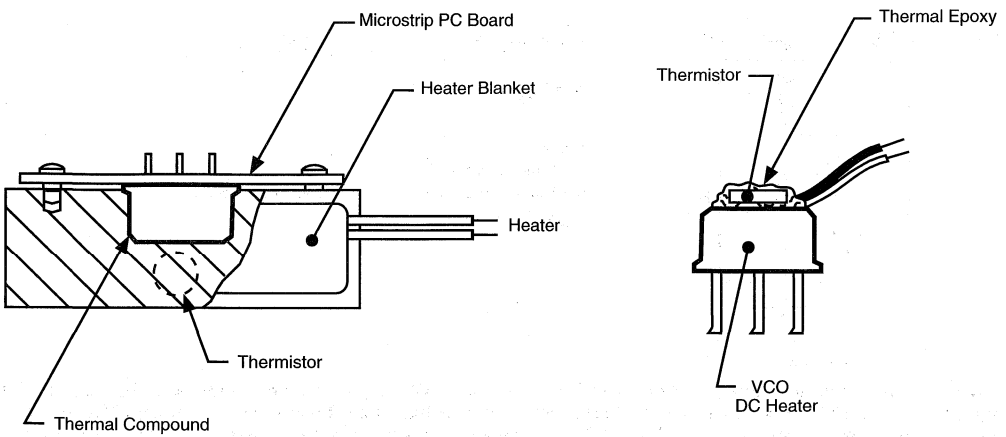


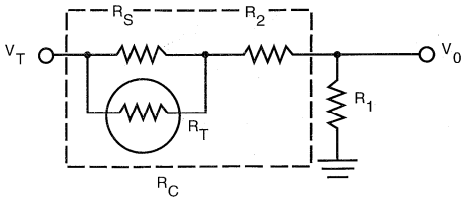
Figure 21. The temperature of a small VCO may be stabilized by mounting the oscillator on a block (which provides thermal mass) that is temperature-controlled by using a proportional heater, or with a small heater directly epoxied to the top of the TO-8 oscillator.

temperature-coefficient (PTC) thermistor or a network of thermistors, depending on the actual tuning circuitry used.

For example, Avantek VTO-8000 series oscillators will display typically a negative frequency-vs.-temperature drift coefficient. To compensate for this, a voltage-compensation network may be used. Two simple networks are shown in Figures 22 and 23.

Other types of resistance networks may be used in place of Rc. A suggestion for determining the resistor values for an effective compensation network is to hold the values of R1 fixed, and use a curve-fitting routine to determine the values of R_2 and R_S when the desired value of R_C is known for at least three different temperatures.

When temperature compensation of the tuning voltage is used, the temperature-sensing device should be mounted as close as possible to the oscillator itself. This will provide the shortest thermal time constant possible from the sensing device to the compensated oscillator.



PTC Network

$$V_0 = (V_T R_1) / [R_1 + R_2 + (R_S \,||\, R_T)]$$

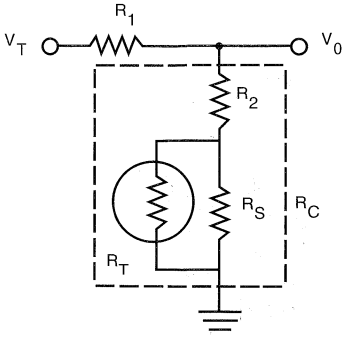
Figure 23. A VCO tuning-voltage-compensation network using a positive-temperature-coefficient (PTC) thermistor. Details of these terms are provided in Figure 22.

Phase-locked loops using VCOs are becoming much more common due to improvements in, and the greater availability of, divider techniques and SAW or crystal multiplied sources. Some of the more important requirements for an oscillator to be suitable for a phase-locked application are:

1. phase stability (spectral purity),
2. large electrical tuning range,
3. linearity of frequency vs. control voltage, and
4. (frequently) the capability of accepting wideband modulation.

From the information supplied so far it is clear that, if a very-low-noise oscillator is required, the best performance will be obtained when the bandwidth is kept as low as possible (<20%) and the tuning voltage as high as possible (>10 V).

The second network is that using an NTC thermistor.



NTC Network

$$V_0 = V_t \,(R_2 + R_s \,||\, R_T) / [R_1 + R_2 + (R_s \,||\, R_T)]$$

$$R_T = R_{25}\,(1 + A)\,(T - 25)$$

Where:
T = Temperature in °C
A = Temperature coefficient of thermistor % / °C @ 25°C
R_{25} = Thermistor resistance at 25°C

Figure 22. The effect of temperature on the frequency of a VCO may be reduced indirectly by varying the tuning voltage in the proper direction to bring the oscillator bakck to the correct frequency. This circuit, using a negative-temperature-coefficient (NTC) thermistor, is appropriate for use with oscillators that typically display a negative frequency-vs-temperature drift coefficient. Note that the current through the thermistor should be held to less than approximately 1 mA (depending on the thermistor's mass) to prevent self-heating. Figure 23 shows a similar circuit using a positive-temperature-coefficient (PTC) thermistor.

VCO Assemblies

Most VCO assemblies (such as the one shown in Figure 24) integrate the voltage-controlled oscillator with amplifiers, voltage regulators, linearizer, and heater circuitry. In some cases, multiple VCOs are used; this requires additional amplifiers and the incorporation of switch combiner networks. Typical specifications are shown in Table II.

To design a circuit with a very high Q, the tuning bandwidth must invariably suffer.

A complete VCO assembly is usually significantly smaller than an arrangement of separately packaged components. The thermal design is better, since it is done for the complete assembly. The integrated assembly minimizes the number of interfaces and connections; this helps improve reliability. It can also offer premium performance due to the complete control of all critical components, and of integrating and matching functions.

VCO assemblies tend to be custom designs for particular applications. The basis performance trade-offs for particular VCO types should also be considered when specifying VCO assemblies.

Table II

Typical Specifications for Integrated VCO Assemblies

Frequency range	1-2 GHz	8-12 GHz	12-18 GHz
Power output, min.	+15 dBm	+14 dBm	+14 dBm
Power flatness, max.	5 dB	3 dB	3 dB
Harmonics, min.	← 20 dBc →		
Spurious, min.	← 60 dBc →		
Residual FM (@ 3 dBc)	50 kHz	100 kHz	100 kHz
Load VSWR	← 1.5:1 →		
Linearity	← ±2% →		
Mod. sense ratio	1.8:1	2.0:1	2.0:1
Operating temperature	← −54° to +71°C →		
Tuning voltage	← 0 to +10 Vdc →		
Input power	← +20 Vdc @ 600 mA →		
	← 20 Vdc @ 250 mA →		
	← +28 Vdc @ 4.0 A (Heater) →		

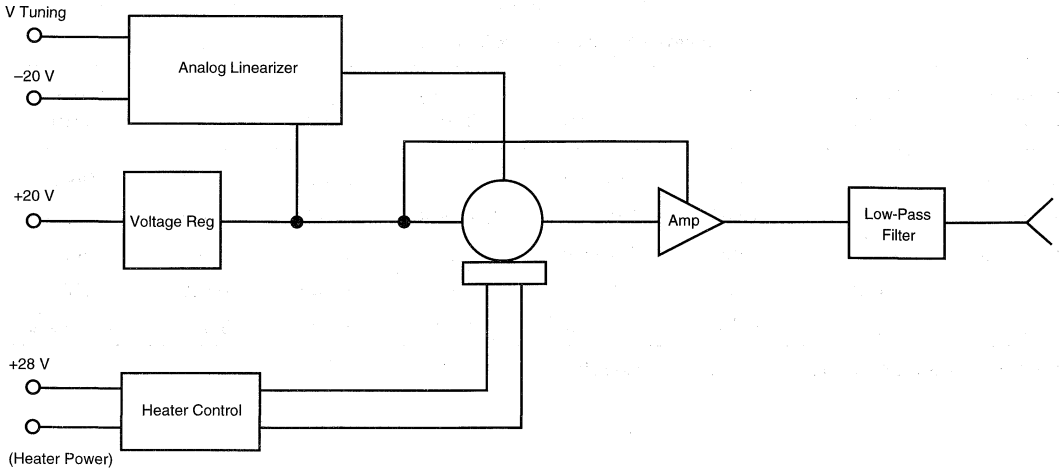


Figure 24. A typical VCO assembly integrates a voltage-controlled oscillator with amplifiers, voltage regulators, linearizer, and heater circuitry. Typical VCO assembly specifications are given in Table II.

One Family of "Raw" VCOs

To examine some of the characteristics of off-the-shelf VCOs, it is useful to look at the Avantek product line. The VTO-8000 series commercial VCOs combine a silicon transistor chip with a silicon abrupt varactor diode. Maximum tuning voltages are between 40 and 50 Volts, which typically is acceptable for most commercial applications. This series of VCOs, mated with a user-supplied low-impedance driver, exhibits tuning speeds on the order of less than 1 ms.across the full band. The operating temperature range for these products is 0° to +65°C, and they are packaged in compact, lightweight TO-8 cans.

The VTO-9000 series oscillators use a silicon transistor chip and silicon hyperabrupt varactor diode. This produces more linear tuning curves than their abrupt-tuned VTO-8000 counterparts. Tuning voltages required are less than 25 Volts, making them very compatible with digital systems. Nanosecond running speeds are achievable with a low-impedance driver due simply to the lower tuning-voltage sqing required. The operating temperature range for these products is also 0° to +65°C.

Militarized MTO-8000 products exhibit the same basic performance characteristics as the VTO-8000 series. The major difference is that they have been designed and tested to meet performance specifications over the military temperature range of –54°C to +85°C.

HTO series militarized hyperabrupt VCOs are designed specifically for octave band coverage. They use silicon transistors and silicon hyperabrupt diodes for frequencies from 900 MHz to 2 GHz and use GaAs transistors from 2 to 18 GHz. Tuning speeds are on the order of 3 ms. The VCOs have been designed and tested for specification compliance from -54°C to +85°C, and are packaged in either hermetically sealed TO-8 cans or the Avanpak miniature microwave flatpak with field-replaceable coaxial connectors.

VTO-series buffered VCOs are designed specifically for good phase-noise and frequency settling-time characteristics. They can be tuned full band typically in less than 3 ms. while settling to within 1 MHz. Internal buffer amplifiers provide very good isolation from variations in load impedance while also minimizing frequency pulling. A customer-supplied heater is required to maintain the oscillator temperature at 80° (±5°C) for specified performance.

Table III

Avantek Voltage-Controlled Oscillators

Product Series	Tuning Voltage	Phase Noise	Bandwidth	Linearity BSFL	Harmonics	Case	Post-Tuning Drift
VTO-8000	0 to +60	Good	75% max.	Fair	–15 dBc	TO-8V	Good
VTO-9000	0 to +20	Good	75% max.	Excellent	–14 dB	TO-8V	Very good
MTO-8000	0 to +60	Good	75% max.	Fair	–10 dBc	TO-8V	Good
HTO-	0 to +20	Fair	Octave	Excellent	–12 dBc	TO-8V*	Fair
LNO-	0 to –20	Excellent	30% max	Good	–12 dBc	TO-8V	Excellent

(*Select models available in Avanpak miniature flatpack)

HEWLETT® PACKARD

Voltage Controlled Oscillators Selection Guide

VTO Series

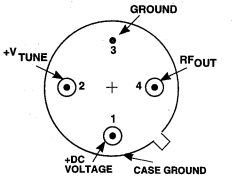
Description

In a varactor-tuned oscillator, a varactor diode serves as a voltage-variable capacitor in a tuned circuit to control the frequency of a negative resistance oscillator. The active device can be a Gunn or Impatt diode or a transistor with appropriate biasing and feedback circuitry. More specifically, the HP series oscillators use the varactor as part of a thin-film microstrip resonator and a transistor chip as the negative resistance device.

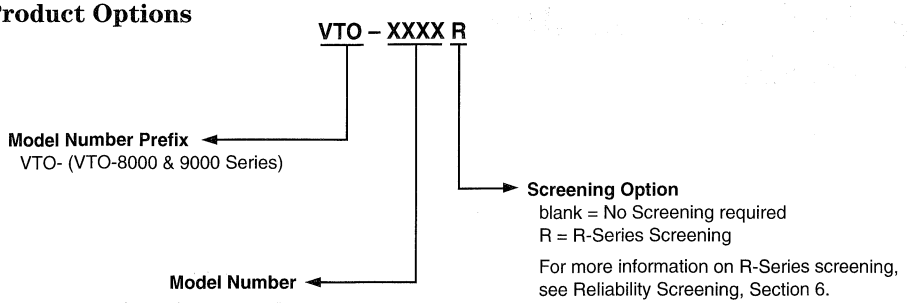
The major feature of a varactor-tuned oscillator is its extremely fast tuning speed. The limiting factor is the ability of the external voltage driver circuit to change the voltage across the varactor diode, which is primarily controlled by the driver impedance and the bypass capacitor in the tuning circuit.

Tuning curves for varactor-tuned oscillators are relatively nonlinear due both to the capacitance-voltage characteristic of the varactor itself and the varying RF impedance of the negative-resistance circuit. The curve, however, is quite smooth and monotonic.

Pin Configuration TO-8V



Product Options



VTO-8000 Series

Guaranteed Specifications at 25°C Case Temperature (0 to 65°C Operating Temperature)

Model #	Frequency Range F_{lo} (MHz) - F_{hi} (MHz)	Power Output (dBm)	Tuning Voltage @ F_{lo}	Tuning Voltage @ F_{hi}	Phase Noise 50kHz/100kHz Typical @ 25°C (dBc/Hz)	Case Style	Page Number
VTO-8060	600 - 1000	13	1 to 4	32 to 48	-110/-117	TO-8V	9-23
VTO-8080	800 - 1400	13	0.5 to 3.5	25 to 45	-100/-107	TO-8V	9-23
VTO-8090	900 - 1600	13	1 to 3	38 to 56	-100/-107	TO-8V	9-23
VTO-8150	1500 - 2500	10	1.5 to 3.5	41 to 55	-95/-102	TO-8V	9-23
VTO-8200	2000 - 3000	10	1 to 4	16 to 24	-95/-102	TO-8V	9-23
VTO-8240	2400 - 3700	10	1 to 4	22 to 38	-95/-102	TO-8V	9-23
VTO-8360	3600 - 4300	10	6 to 10	20 to 28	-100/-108	TO-8V	9-23
VTO-8430	4300 - 5800	10	>1	<20	-90/-97	TO-8V	9-23
VTO-8580	5800 - 6600	7	2.5 to 7.5	19 to 27	-85/-92	TO-8V	9-23
VTO-8650	6500 - 8600	10	1 to 3	15 to 25	-80/-88	TO-8V	9-23
VTO-8810	8100 - 9100	10	>2	<16	-80/-88	TO-8V	9-23
VTO-8850	8500 - 9600	10	3 to 7	8 to 18	-82/-90	TO-8V	9-23
VTO-8950	9500 - 10500	10	3 to 5	<10	-73/-80	TO-8V	9-23

VTO–9000 Series

Guaranteed Specifications at 25°C Case Temperature (0 to 65°C Operating Temperature)

Model #	Frequency Range F_{lo} (MHz) - F_{hi} (MHz)	Power Output (dBm)	Tuning Voltage @ F_{lo}	Tuning Voltage @ F_{hi}	Phase Noise 50kHz/100kHz Typical @ 25°C (dBc/Hz)	Case Style	Page Number
VTO-9032	320 - 640	10	>0	<20	-95/-103	TO-8V	9-30
VTO-9050	500 - 1000	10	>0	<20	-100/-108	TO-8V	9-30
VTO-9068	680 - 1360	10	>0	<20	-95/-103	TO-8V	9-30
VTO-9090	900 - 1600	10	>2	<18	-100/-108	TO-8V	9-30
VTO-9120	1200 - 2000	10	2 to 4	10 to 14	-97/-105	TO-8V	9-30
VTO-9130	1300 - 2300	10	>2	<20	-97/-105	TO-8V	9-30

HEWLETT® PACKARD

Varactor-Tuned Oscillators

Technical Data

VTO-8000 Series

Features

- **600 MIlz to 10.5 GHz Coverage**
- **Fast Tuning**
- **+7 to +13 dBm Output Power**
- **±1.5 dB Output Flatness**
- **Hermetic Thin-film Construction**

Description

HP VTO-8000 Series oscillators use a silicon transistor chip as a negative resistance oscillator. The oscillation frequency is determined by a silicon abrupt varactor diode acting as a voltage-variable capacitor in a thin-film microstripline resonator. This provides extremely fast tuning speed, limited primarily by the internal impedance of the user-supplied voltage driver. Fast settling is another feature of the HP VTO-8000 Series oscillators. Typical settling times for the VTO-8090 are <200 kHz within one microsecond while the VTO-8950 settles to <2 MHz within two microseconds referenced to ten milliseconds. The VTO-8850 combines a bipolar transistor oscillator with a GaAs FET buffer stage. This GaAs FET buffer isolates the oscillator from variations in load impedance for low frequency pulling, allows the oscillator to run lighty-loaded for low phase noise content and provides +10 dBm of minimum output power over the full tuning range. The VTO-8000 Series varactor-tuned oscillators are packaged in TO-8 transistor cans for simple installation in a conventional 50-ohm microstripline PC board. They are ideal for most compact, lightweight commercial and military equipment designs. Test fixturing is also available for lab bench test applications. See the "Test Fixtures for TO-8 Packages" section for additional information and outlines.

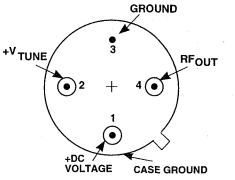
Applications

Frequency agile systems, such as digitally controlled receivers and active jamming transmitters often use externally linearized varactor-tuned oscillators. HP oscillators are monotonic making external linearization easy using analog (opamp) or digital (EPROM) linearizing techniques. The HP VTO Series has been designed with a tuning input bypass capacitance which is sufficient to provide the necessary RF filtering action yet as low as possible to maximize $\Delta V/\Delta T$ characteristics for excellent tuning speeds. Used in a phase locked loop PLL circuit, a VTO provides a receiver LO with stability equivalent to the reference oscillator (usually crystal controlled), yet variable in discrete steps or continuously depending on the PLL configuration.

Another important aspect of VTOs used in an LO application is their power vs. frequency flatness (±1.5 dB). This assures that once a receiver mixer is biased for best dynamic range the local oscillator drive will remain constant throughout the tuning range without complex leveling circuitry.

Pin Configuration

TO-8V



Electrical and Performance Specifications

Guaranteed Specifications @ 25°C Case Temperature (0° to +65°C Operating Temperature)

Part Number	VTO–8060	VTO–8080	VTO–8090	VTO–8150	VTO–8200
Frequency Range, Min.	600–1000 MHz	800–1400 MHz	900–1600 MHz	1500–2500 MHz	2000–3000 MHz
Power Output into 50–ohm Load,Min.	20 mW/+13 dBm	20 mW/+13 dBm	20 mW/+13 dBm	10 mW/+10 dBm	10 mW/+10 dBm
Power Output Variation @ 25°C, Max.	±1.5 dB	±1.5 dB	±1.5 dB	±1.5 dB	±1.5 dB
Operating Case Temperature Range	0° to +65°C	0° to +65°C	0° to +65°C	0° to +65°C	0° to +65°C
Frequency Drift Over Operating Temperature, Typ.	8 MHz	10 MHz	10 MHz	18 MHz	30 MHz
Pulling Figure (12 dB Return Loss), Typ.	25 MHz	25 MHz	25 MHz	35 MHz	35 MHz
Pushing Figure, +15 VDC Supply, Typ.	5 MHz/V	6 MHz/V	6 MHz/V	6 MHz/V	6 MHz/V
Harmonics, Below Carrier, Typ.	–15 dB	–15 dB	–15 dB	–15 dB	–18 dB
Spurious Output Below Carrier, Min.	–60 dB	–60 dB	–60 dB	–60 dB	–60 dB
Tuning Voltage					
Low Frequency	3±1 VDC	2±1.5 VDC	2±1 VDC	2.5±1 VDC	2+2/–1 VDC
High Frequency	40±8 VDC	35±10 VDC	48+8/–10 VDC	47±8 VDC	20±4 VDC
Maximum Tuning Voltage	+60 VDC	+60 VDC	+60 VDC	+60 VDC	+45 VDC
Tuning Port Capacitance, Nom.	180 pF	180 pF	180 pF	90 pF	45 pF
Phase Noise, Singie Sideband, 1 IIz Bandwidth, Typ.					
50 kHz From Carrier	–110 dBc/Hz	–100 dBc/Hz	–100 dBc/Hz	–95 dBc/Hz	–95 dBc/Hz
100 kHz From Carrier	–117 dBc/Hz	–107 dBc/Hz	–107 dBc/Hz	–102 dBc/Hz	–102 dBc/Hz
Input Power ±1% Regulation					
Voltage, Nom.	+15 VDC	+15 VDC	+15 VDC	+15 VDC	+15 VDC
Current, Max.	50 mA	50 mA	50 mA	50 mA	50 mA
Case Style	TO–8V	TO–8V	TO–8V	TO–8V	TO–8V

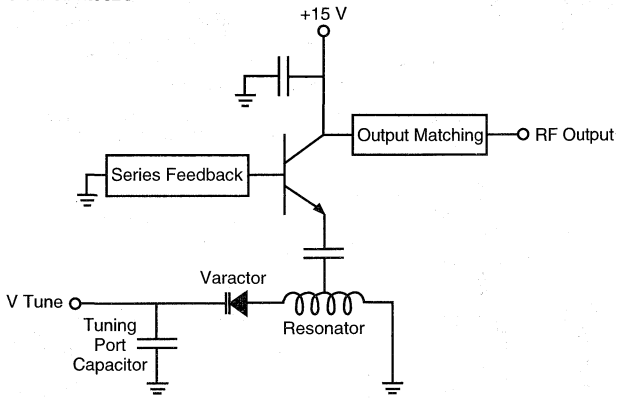
Part Number	VTO–8240	VTO–8360	VTO–8430	VTO–8580
Frequency Range, Min.	2400–3700 MHz	3600–4300 MHz	4300–5800 MHz	5800–6600 MHz
Power Output Into 50–ohm Load, Min.	10 mW/+10 dBm	10 mW/+10 dBm	10 mW/+10 dBm	5 mW/+7 dBm
Power Output Variation @25°C., Max.	±1.5 dB	±1.5 dB	±1.5 dB	±1.5 dB
Operating Case Temperature Range	0° to +65°C	0° to +65°C	0° to +65°C	0° to +65°C
Frequency Drift Over Operating Temperature, Typ.	30 MHz	35 MHz	60 MHz	70 MHz
Pulling Figure (12 dB Return Loss), Typ.	35 MHz	40 MHz	50 MHZ	70 MHz
Pushing Figure, +15 VDC Supply, Typ.	6 MHz/V	6 MHz/V	6 MHz/V	8 MHz/V
Harmonics, Below Carrier, Typ.	–18 dB	–25 dB	–25 dB	–25 dB
Spurious Output Below Carrier, Min.	–60 dB	–60 dB	–60 dB	–60 dB
Tuning Voltage				
Low Frequency	2+2/–1 VDC	8±2 VDC	1.0 VDC Min	5±2.5 VDC
High Frequency	30±8 VDC	24±4 VDC	20.0 VDC Max.	24+3/–5 VDC
Maximum Tuning Voltage	+45 VDC	+30 VDC	+30 VDC	+30 VDC
Tuning Port Capacitance, Nom.	45 pF	45 pF	45 pF	45 pF
Phase Noise, Single Sideband, 1 Hz Bandwidth, Typ.				
50 kHz From Carrier	–95 dBc/Hz	–100 dBc/Hz	–90 dBc/Hz	–85 dBc/Hz
100 kHz From Carrier	–102 dBc/Hz	–108 dBc/Hz	–97 dBc/Hz	–92 dBc/Hz
Input Power ±1% Regulation				
Voltage, Nom.	+15 VDC	+15 VDC	+15 VDC	+15 VDC
Current, Max.	50 mA	50 mA	50 mA	50 mA
Case Style	TO–8V	TO–8V	TO–8V	TO–8V

Electrical and Performance Specifications

Guaranteed Specifications @ 25°C Case Temperature (0° to +65°C Operating Temperature)

Part Number	VTO–8650	VTO–8810	VTO–8850	VTO–8950
Frequency Range, Min.	6500-8600 MHz	8100–9100 MHz	8500–9600 MHz	9500–10500 MHz
Power Output Into 50–ohm load, Min.	10 mW/+10 dBm	10 mW/+10 dBm	10 mW/+10 dBm	10 mW/+10 dBm
Power Output Variation @ 25°C., Max.	±1.5 dB	±1.5 dB	±1.5 dB	±1.5 dB
Operating Case Temperature Range	0° to +65°C	0° to +65°C	0° to +65°C	0° to +65°C
Frequency Drift Over Operating Temperature, Typ.	100 MHz	110 MHz	110 MHz	160 MHz
Pulling Figure (12 dB Return Loss), Typ.	15 MHz	8 MHz	10 MHz	20 MHz
Pushing Figure, +15 VDC Supply, Typ.	10 MHz/V	12 MHz/V	15 MHz/V	10 MHz/V
Harmonics, Below Carrier, Typ.	–20 dB	–15 dB	–25 dB	–20 dB
Spurious Output Below Carrier, Min.	–60 dB	–60 dB	–60 dB	–60 dB
Tuning Voltage				
Low Frequency	2±1 VDC	2 VDC Min.	5±2 VDC	4±1 VDC
High Frequency	20±5 VDC	16 VDC Max.	13±5 VDC	10 VDC Max.
Maximum Tuning Voltage	30 VDC	+30 VDC	+30 VDC	+15 VDC
Tuning Port Capacitance, Nom.	26 pF	26 pF	26 pF	26 pF
Phase Noise, Single Sideband, 1 Hz Bandwldth, Typ.				
50 kHz From Carrier	–80 dBc/Hz	–80 dBc/Hz	–82 dBc/Hz	–73 dBc/Hz
100 kHz From Carrier	–88 dBc/Hz	–88 dBc/Hz	–90 dBc/Hz	–80 dBc/Hz
Input Power ±1% Regulation				
Voltage, Nom.	+15 VDC	+15 VDC	+15 VDC	+15 VDC
Current, Max.	50 mA	100 mA	100 mA	100 mA
Case Style	TO–8V	TO–8V	TO–8V	TO–8V

Schematic



Typical Performance @ 25°C Case Temperature

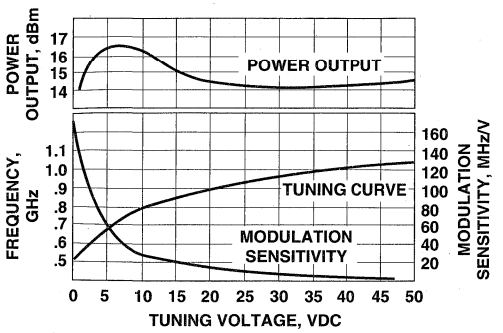


Figure 1. VTO–8060 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

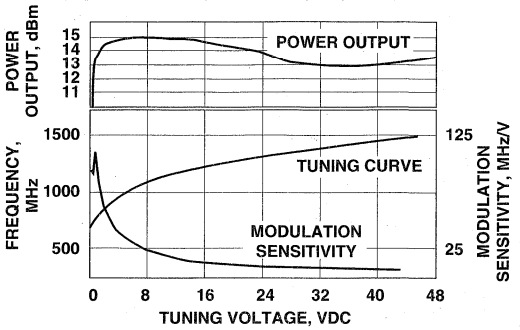


Figure 2. VTO–8080 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

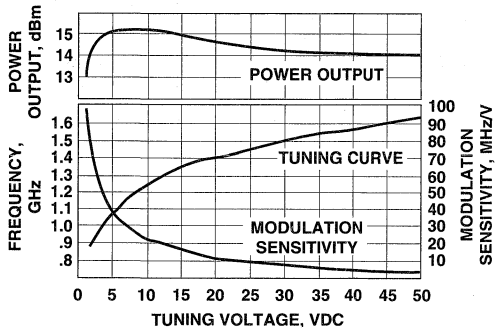


Figure 3. VTO–8090 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

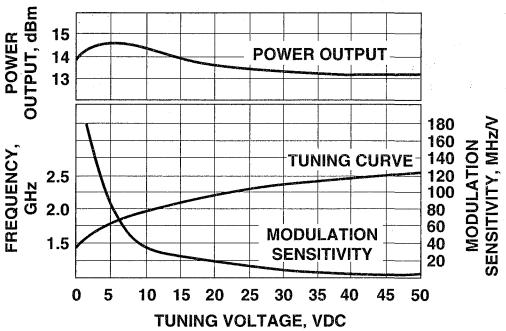


Figure 4. VTO–8150 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

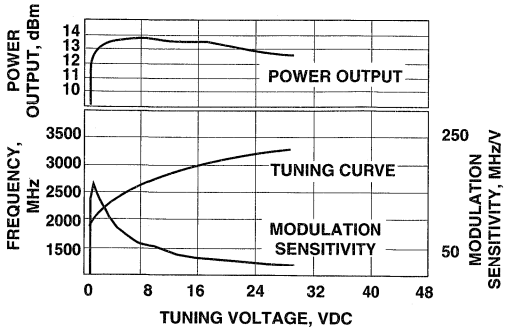


Figure 5. VTO–8200 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

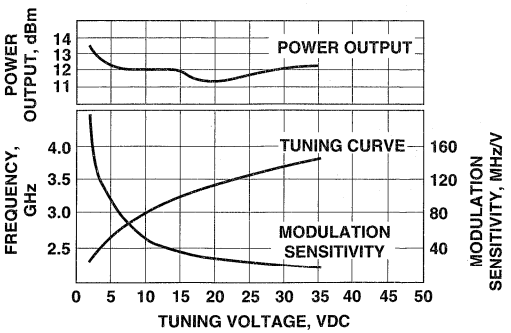


Figure 6. VTO–8240 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

Typical Performance (Continued)

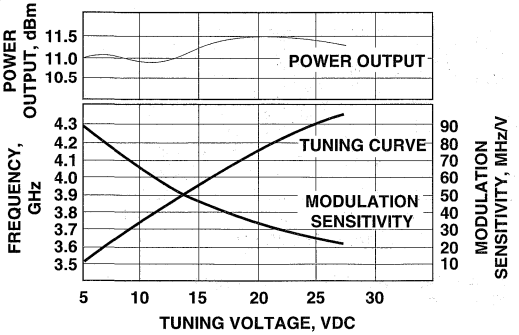


Figure 7. VTO–8360 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

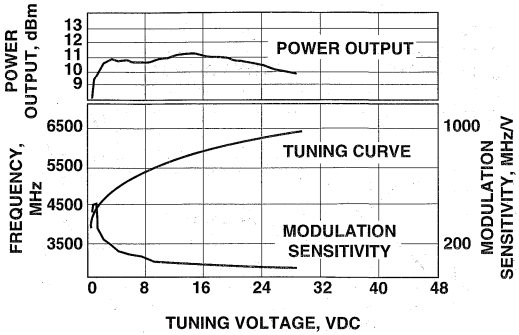


Figure 8. VTO–8430 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

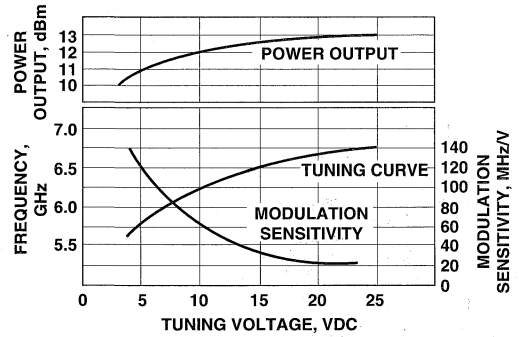


Figure 9. VTO–8580 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

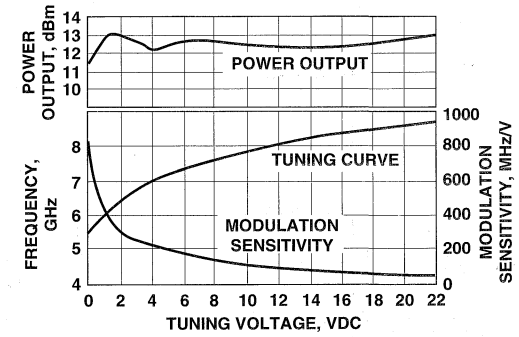


Figure 10. VTO–8650 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

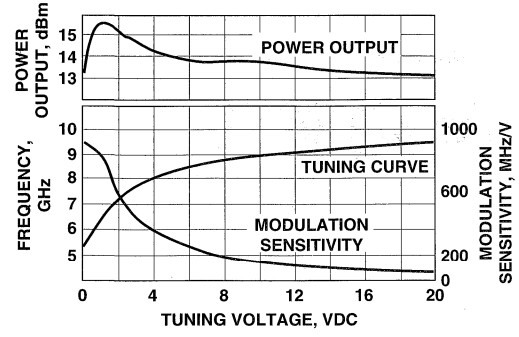


Figure 11. VTO–8810 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

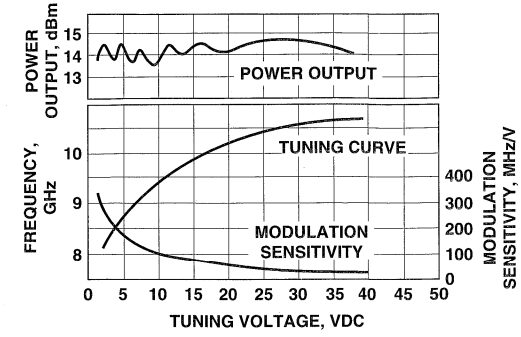


Figure 12. VTO–8850 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

Typical Performance (Continued)

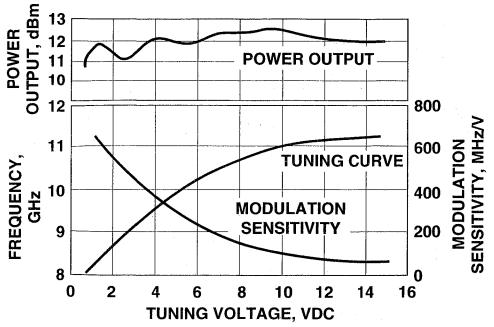


Figure 13. VTO–8950 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

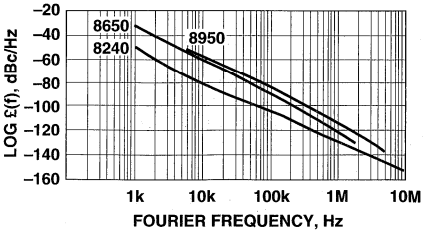
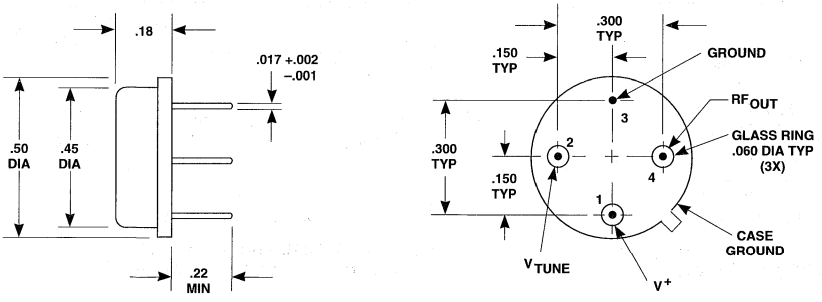


Figure 14. Noise Comparison Single Sideband Phase Noise.

TO-8V Case Drawing



APPROXIMATE WEIGHT 1.7 GRAMS

NOTES (UNLESS OTHERWISE SPECIFIED):
1. DIMENSIONS ARE SPECIFIED IN INCHES
2. TOLERANCES: xx ± .02
xxx ± .010

Test Fixtures for TO-8 Packages (TF 801/802) Oscillators (VTO)

Features

- **DC to 11 GHz Frequency Range**
- **Connectorized Tuning Port and RF Output**
- **Easy to Test Package**
- **Repeatable Performance**

Applications

- **Engineering Characterization**
- **Incoming Inspection**
- **System Prototype**
- **Demonstration of Device Performance**

Description

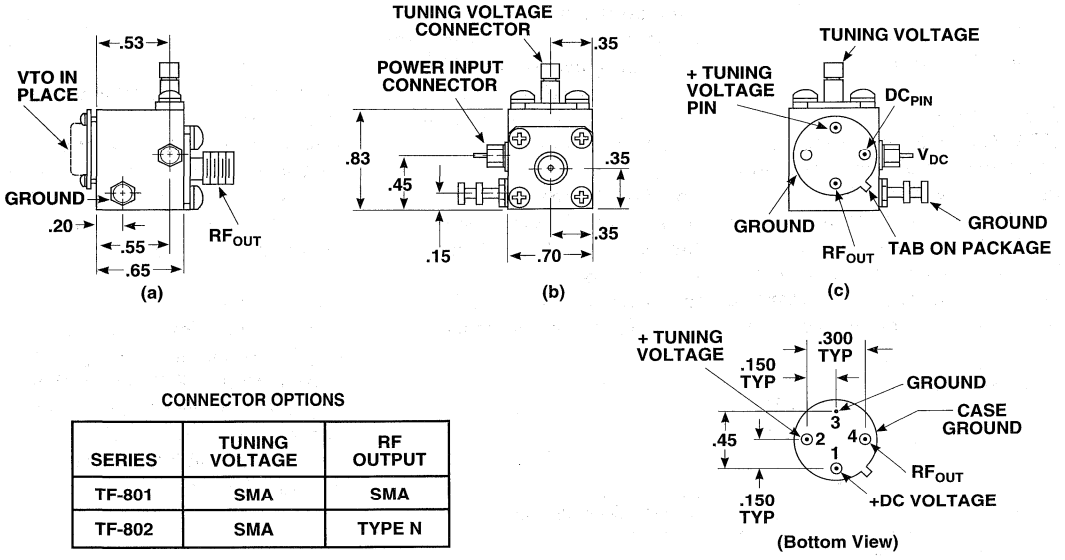
To facilitate testing and prototyping of products in the TO-8V package, a series of test fixtures is available. Designated the HP TF Series test fixtures, they feature rugged construction for precise, repeatable measurements.

The TF Series test fixtures come supplied with mounting hardware to ensure excellent ground contact between the oscillator package and test fixture. This assures excellent contact between package pins and test fixture connector pins for reliable testing.

The device under test is aligned according to Figure 15, and pushed fully down onto the fixture. The steel mounting ring clamp is placed over the device under test and secured by machine screws prior to testing. Orientation of pins can be verified by comparison with part (c) of Figure 15. It is recommended that both machine screws be used to fasten the ring clamp. Screws should be tightened down snugly with a jewelers type screwdriver.

For different connector options check the table in Figure 15 to identify the correct part numbers.

It should be noted that some output power variation may be seen, from unit data, at frequencies above 8 GHz. This is due to small differences in lengths of test fixture RF output connector pins.



CONNECTOR OPTIONS

SERIES	TUNING VOLTAGE	RF OUTPUT
TF-801	SMA	SMA
TF-802	SMA	TYPE N

Figure 15. TO-8 Test Fixture.

HEWLETT® PACKARD

Hyperabrupt Varactor-Tuned Oscillators

Technical Data

VTO-9000 Series

Features

- **25 MHz to 2.3 GHz Coverage**
- **Fast Tuning**
- **Fast Setting Time**
- **+20 VDC Max Tuning Voltage**
- **10 mW Output Power**
- **±2.0 dB Output Flatness**
- **Hermetic Thin-film Construction**

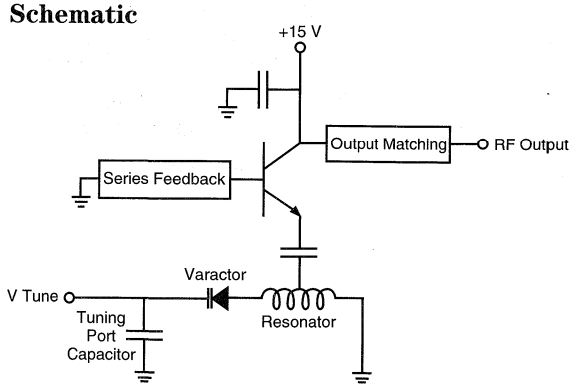
Description

HP VTO-9000 Hyperabrupt Series oscillators use a silicon transistor chip as a negative resistance oscillator. The oscillation frequency is determined by a silicon hyperabrupt varactor diode acting as a voltage-variable capacitor in a thin-film microstripline resonator. This provides extremely fast tuning speed limited primarily by the internal impedance of the user-supplied voltage driver.

This family of oscillators is similar to the standard commercial VTO-8000 Series except for the incorporation of a silicon hyperabrupt varactor tuning diode. This enables the oscillator to be tuned over the specified range in less than 20 volts rather than 40 to 50 volts in conventional oscillators.

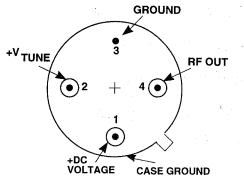
The VTO-9000 Series VTOs are packaged in TO-8 transistor cans for simple installation in a conventional 50-ohm microstripline PC board. They are ideal for most compact lightweight commercial and military equipment designs. Test fixturing is also available for lab bench test applications. See the "Test Fixtures for TO-8 Packages" section for additional information and outlines.

Schematic



Pin Configuration

TO-8V



Applications

The VTO-9000 Series oscillators may be used in the same applications as VTO-8000 Series oscillators. The VTO-9000 Series is the desired choice for superior linearity and modulation sensitivity requirements.

Electrical and Performance Specifications

Guaranteed Specifications @ 25°C Case Temperature (0° to +65°C Operating Temperature)

Model No.	VTO–9032	VTO–9050	VTO–9068	VTO–9090
Frequency Range, Min.	320–640 MHz	500–1000 MHz	680–1360 MHz,	900–1600 MHz
Power Output Into 50–ohm Load, Min .	10 mW/+10 dBm	10 mW/+ 10 dBm	10 mW/+10 d Bm	10 mW/+10 dBm
Power Output Variation @ 25°C, Max.	±2 dB	±2 dB	±2 dB	±2 dB
Operating Carrier Temperature Range	0° to +65°C	0° to +65°C	0° to +65°C	0° to +65°C
Frequency Drift Over Operating Temperature, Typ.	12 MHz	20 MHz	20 MHz	20 MHz
Pulling Figure (12 dB Return Loss), Typ.	20 MHz	20 MHz	25 MHz	25 MHz
Pushing Figure, +15 VDC Supply, Typ.	5 MHz/V	5 MHz/V	6 MHz/V	6 MHz/V
Harmonics, Below Carrier, Typ.	–14 dB	–10 dB	–14 dB	–14 dB
Spurious Output Below Carrier, Min.	–60 dB	–60 dB	–60 dB	–60 dB
Tuning Voltage				
Low Frequency, Min.	0 VDC	0 VDC	0 VDC	2 VDC
High Frequency, Max	20 VDC	20 VDC	20 VDC	18 VDC
Maximum Tuning Voltage	+20 VDC	+20 VDC	+20 VDC	+20 VDC
Tuning Port Capacitance, Nom.	200 pF	200 pF	190 pF	190 pF
Phase Noise, Single Sideband,				
1 Hz Bandwidth, Typ.				
50 kHz From Carrier	–95 dBc/Hz	–100 dBc/Hz	–95 dBc/Hz	–100 dBc/Hz
100 kHz From Carrier	–103 dBc/Hz	–108 dBc/Hz	–103 dBc/Hz	–108 dBc/Hz
Input Power, ±1% Regulaltion				
Voltage, Nom.	+15 VDC	+15 VDC	+15 VDC	+15 VDC
Current, Max.	50 mA	50 mA	50 mA	50 mA
Case Style	TO–8V	TO–8V	TO–8V	TO–8V

Electrical and Performance Specifications

Guaranteed Specifications @ 25°C Case Temperature (0° to +65°C Operating Temperature)

Model No.	VTO–9120	VTO–9130
Frequency Range, Min.	1200–2000 MHz	1300–2300 MHz
Power Output Into 50–ohm load, Min.	10 mW/+10 dBm	10 mW/+10 dBm
Power Output Variation @ 25°C, Max.	±2 dB	±1.5 dB
Operating Case Temperature Range	0° to +65°C	0° to +65°C
Frequency Drift Over Operating Temperature, Typ.	25 MHz	25 MHz
Pulling Figure (12 dB Return Loss), Typ.	25 MHz	50 MHz
Pushing Figure, +15 VDC Supply, Typ.	10 MHz/V	10 MHz/V
Harmonics, Below Carrier, Typ.	–14 dB	–15 dB
Spurious Output Below Carrier, Min.	–60 dB	–60 dB
Tuning Voltage		
Low Frequency	3±1 VDC	2 VDC Min.
High Frequency	12±2 VDC	20 VDC Max.
Maximum Tuning Voltage	+20 VDC	+ 20 VDC
Tuning Port Capacitance, Nom.	100 pF	100 pF
Phase Noise, Single Sideband,		
1 Hz, Bandwidth, Typ.		
50 kHz From Carrier	–97 dBc/Hz	–97 dBc/Hz
100 kHz From Carrier	–105 dBc/Hz	–105 dBc/Hz
Input Power, ±1% Regulation		
Voltage,Nom.	+15VDC	+15VDC
Current, Max.	50 mA	50 mA
Case Style	TO–8V	TO–8V

Typical Performance @ 25°C Case Temperature

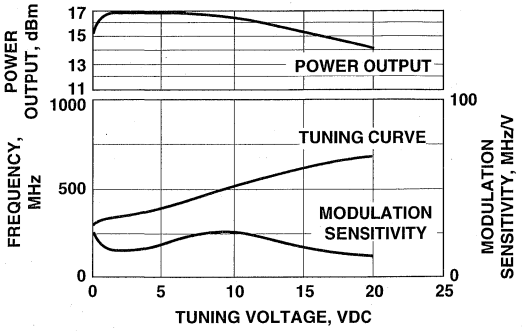


Figure 1. VTO-9032 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage

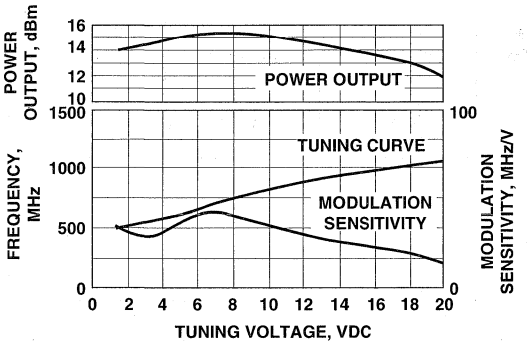


Figure 3. VTO-9050 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

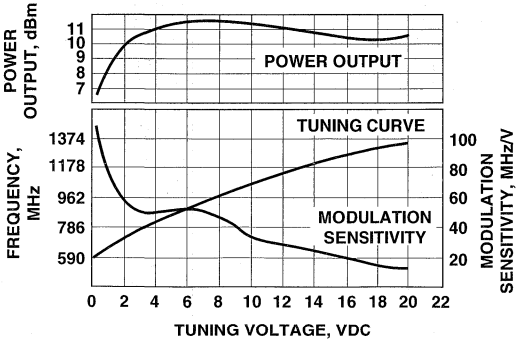


Figure 5. VTO-9068 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

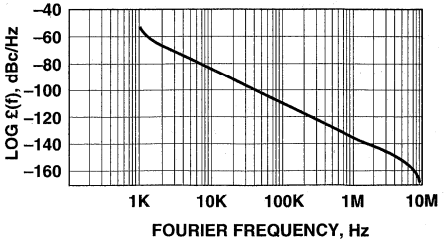


Figure 2. VTO-9032 Normalized Phase Noise @ 640 MHz S.S.B. Power Spectral Density.

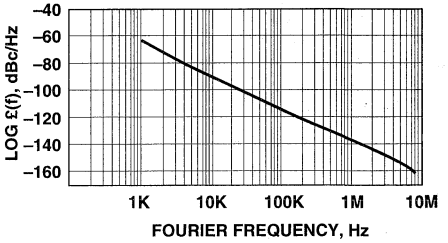


Figure 4. VTO-9050 Normalized Phase Noise @ 1000 MHz S.S.B. Power Spectral Density.

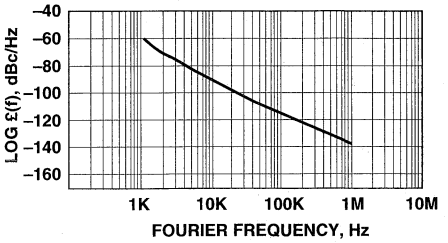


Figure 6. VTO-9068 Normalized Phase Noise @ 1360 MHz S.S.B. Power Spectral Density.

Typical Performance @ 25°C Case Temperature (continued)

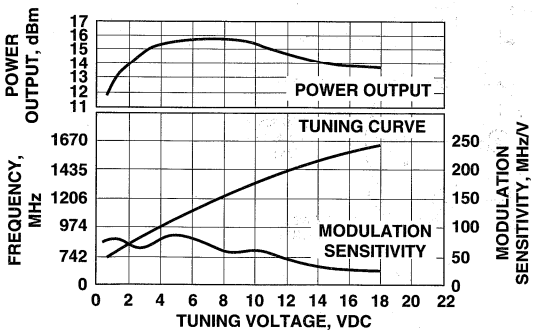


Figure 7. VTO-9090 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

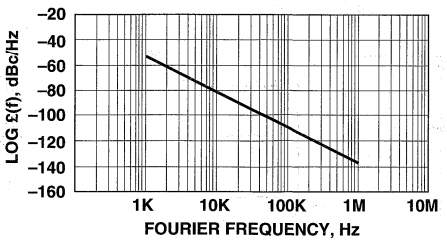


Figure 8. VTO-9090 Noise @ 1000 MHz Single Sideband Phase Noise.

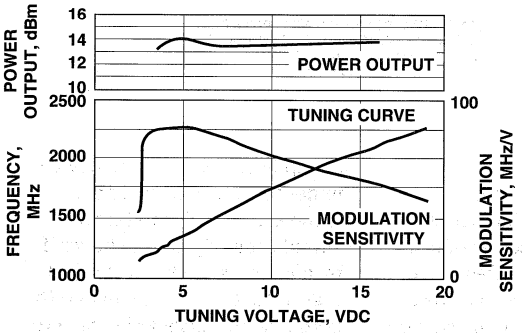


Figure 9. VTO-9120 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

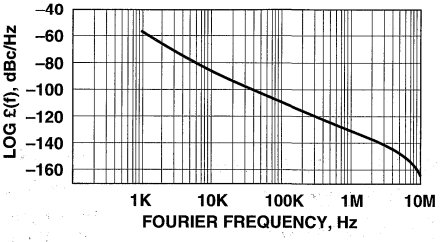


Figure 10. VTO-9120 Normalized Phase Noise @ 2000 MHz S.S.B. Power Spectral Density.

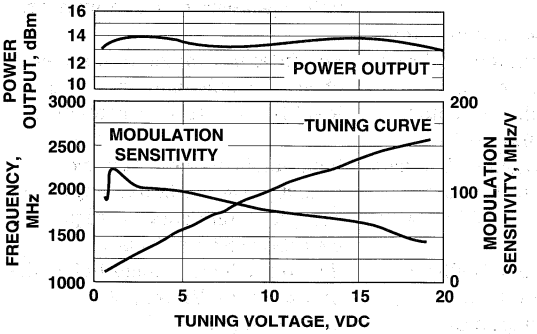


Figure 11. VTO-9130 Power Output, Frequency and Modulation Sensitivity vs. Tuning Voltage.

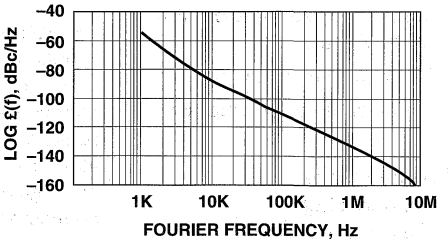
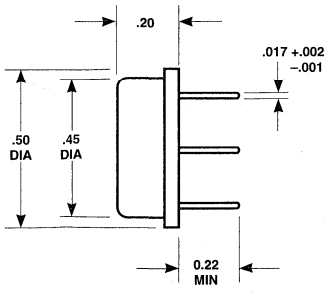
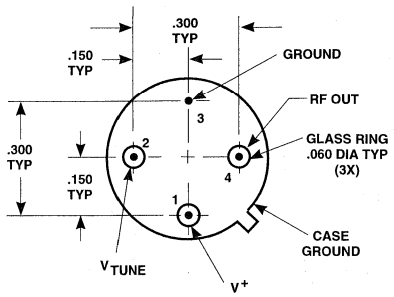


Figure 12. VTO-9130 Normalized Phase Noise @ 2300 MHz S.S.B. Power Spectral Density.

TO-8V Case Drawing





APPROXIMATE WEIGHT 1.7 GRAMS

NOTES (UNLESS OTHERWISE SPECIFIED):
1. DIMENSIONS ARE SPECIFIED IN INCHES
2. TOLERANCES: xx ± .02
xxx ± .010

Test Fixtures for TO-8 Packages (TF 801/802) Oscillators (VTO)

Features

- **DC to 11 GHz Frequency Range**
- **Connectorized Tuning Port and RF Output**
- **Easy to Test Package**
- **Repeatable Performance**

Applications

- **Engineering Characterization**
- **Incoming Inspection**
- **System Prototype**
- **Demonstration of Device Performance**

Description

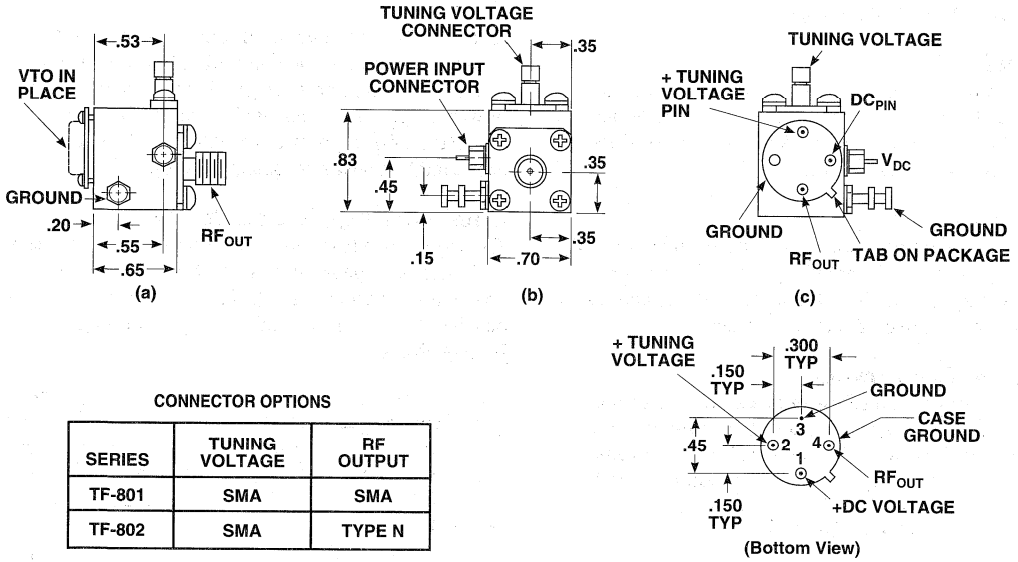
To facilitate testing and prototyping of products in the TO-8V package, a series of test fixtures is available. Designated the HP TF Series test fixtures, they feature rugged construction for precise, repeatable measurements.

The TF Series test fixtures come supplied with mounting hardware to ensure excellent ground contact between the oscillator package and test fixture. This assures excellent contact between package pins and test fixture connector pins for reliable testing.

The device under test is aligned according to Figure 13, and pushed fully down onto the fixture. The steel mounting ring clamp is placed over the device under test and secured by machine screws prior to testing. Orientation of pins can be verified by comparison with part (c) of Figure 13. It is recommended that both machine screws be used to fasten the ring clamp. Screws should be tightened down snugly with a jewelers type screwdriver.

For different connector options check the table in Figure 13 to identify the correct part numbers.

It should be noted that some output power variation may be seen, from unit data, at frequencies above 8 GHz. This is due to small differences in lengths of test fixture RF output connector pins.



CONNECTOR OPTIONS

SERIES	TUNING VOLTAGE	RF OUTPUT
TF-801	SMA	SMA
TF-802	SMA	TYPE N

Figure 13. TO-8 Test Fixture.

Glossary

Terms and Definitions

Alumina
(Aluminum Oxide, Al_2O_3) — Alumina ceramic is used as the substrate material on which is deposited thin conductive and resistive layers for thin-film microwave integrated circuits.

AM Noise
The random and/or systematic variations in output power amplitude. Usually expressed in terms of dBc in a specified video bandwidth at a specified frequency removed from the carrier.

AM-PM Conversion
AM-PM conversion represents a shift in the phase delay of a signal when a transistor changes from small-signal to large-signal operating conditions. This parameter is specified for HP communications amplifiers, since AM-PM conversion results in distortion of a signal waveform.

Analog Driver
An accessory circuit for an oscillator or filter which permits its frequency to be changed by a continuously varying signal.

Balanced Amplification
A transistor amplifier stage in which two identical single-ended amplifier circuits ("channels") are used, and the input signal and output power are equally divided between them. This technique produces approximately twice the output power of a single-ended amplifier stage with generally improved dynamic range and reduced VSWR.

Balanced Module
A gain module of an amplifier which utilizes a 3 dB input splitter and a 3 dB output coupler to combine the power of 2 or more paralleled FETs. Balanced modules have the characteristics of good input and output VSWR which lends to the cascadability of several modules in an amplifier. Balanced modules also have the benefit of indirect stability under adverse source and load conditions.

Cascadable
A device is cascadable if the output port of one such device can be connected to the input port of another such device without additional impedance matching being required.

Cascade
A series of microwave amplifier stages connected in sequence (sometimes including limiters, attenuators or other elements) to produce the desired gain, power output and other performance characteristics. HP modular products are designed to be cascaded in a 50Ω microstrip system.

Combined Ripple and Spurious
The worst case transmission loss (in dB) within the YIG filter 3 dB passband due to the presence of passband spurious (Item E, Figure 1) and/or passband ripple (Item F, Figure 1) responses. See Item G, Figure 1.

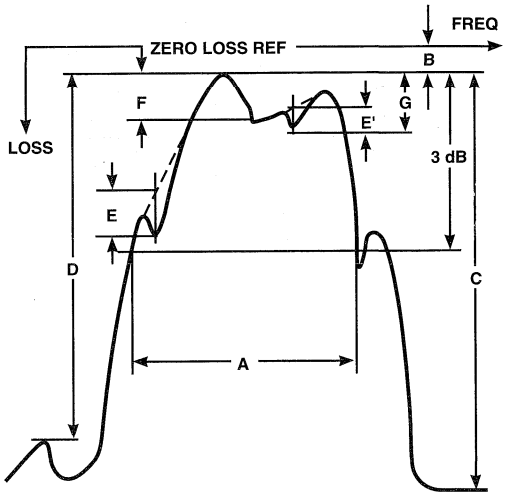


Figure 1

Conversion Compression Point (1 dB)
The specification which states the RF input power (in dBm) at which the IF output power will increase only 9 dB for a 10 dB increase in RF input power at a stated LO input power level.

Conversion compression point provides an indication of the mixer two-tone intermodulation performance and is usually of most concern in high level mixing applications.

dB
Decibel — A unit of gain equal to ten times the common logarithm of the ratio of two power levels or 20 times the common logarithm of the ratio of two voltage levels.

dBc
Decibels related to the signal carrier level.

dBm
Decibels related to 1 mW — The standard unit of power level used in microwave work. For example, 0 dBm = 1 mW, +10 dBm = 10 mW, +20 dBm = 100 mW, etc.

Drive Level
The power level of the local oscillator signal applied to the LO port of a mixer. Operating a mixer with the maximum recommended LO drive level will result in the best two-tone performance, lowest conversion loss and flattest conversion loss vs. frequency characteristics. A reduced LO drive level may help reduce mixer-generated intermodulation products and minimize 1/f noise in the output signal. A higher-than recommended LO power level will result in an increased noise figure and higher LO feedthrough at both the RF and IF ports of the mixer.

dV/dT
Device voltage temperature coefficient.

Dynamic Range
The range from the minimum, which is at a level at or below the amplifier's internally-generated noise, to a maximum input signal level that a component can accept and amplify without distortion.
In regard to mixers, the range of RF input power levels over which a mixer can operate within the specified range of performance. The upper limit of the mixer dynamic range is controlled by the conversion compression point (also a function of LO drive level), and the lower limit is set by the mixer noise figure.

EMI
Electromagnetic Interference — Unintentional interfering signals generated within or external to electronic equipment. Typical sources could be power-line transients, noise from switching-type power supplies and/or spurious radiation from oscillators. EMI is suppressed with power-line filtering, shielding, etc. EMI suppression requirements are frequently specified for military equipment.

EW
Electronic Warfare — Electronic warfare is military action involving the use of electromagnetic energy to determine, exploit, reduce or prevent hostile use of the electromagnetic spectrum and actions to retain friendly use of the electromagnetic spectrum.

fmax
Maximum Frequency of Oscillation — The frequency at which unilateral gain equals unity.

FM Noise/Phase Noise
The short-term frequency variations in the output frequency which appear as energy at frequencies other than the carrier. It is usually expressed in terms of dBc or as a RMS frequency deviation in a specified video bandwidth at a specified frequency removed from the carrier. **See Figure 2.**

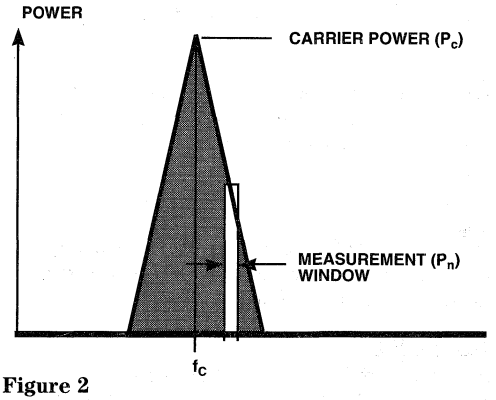


Figure 2

Frequency Accuracy
The maximum output frequency deviation from a specified tuning function under specified conditions. May be expressed in MHz, ppm, or ppm/°C.

Frequency Drift Over Operating Temperature, Max.
The maximum change in output frequency as a result of a specified change in operating temperature.

In regard to oscillators, a measure of the change in frequency over the specified operating temperature range. It is commonly expressed as parts-per-million per degree Celsius (ppm/°C) or as a percentage figure. From a system applications view, the total frequency drift with temperature is sometimes specified around the frequency set at room temperature in ± total parts per million.

Frequency Pulling
The difference between the maximum and minimum values of the oscillator frequency when the phase angle of the load impedance reflection coefficient varies through 360°. Typically this load impedance has a VSWR of 1.67:1.

Frequency Pushing
The incremental output frequency change produced by an incremental change in supply voltage (ΔMHz/ΔV). If supply voltage ripple, frequency range, and amplitude are not specified, measurements will be conducted at a DC rate.

Frequency Range
Usually presented as the minimum and maximum frequencies between which a particular component will meet all guaranteed specifications.

f_T
Gain-Bandwidth Product — (Also called transition frequency). It is the frequency at which the magnitude of the small-signal common-emitter current gain equals unity.

$f_{3\ dB}$
Frequency at 3 dB Gain Point — The frequency at which gain has been reduced 3 dB from the gain at a specified reference frequency.

GaAs FET
Gallium Arsenide Field Effect Transistor — (Also called GaAs MESFET for Metal Epitaxial Semiconductor Field Effect Transistor). A field effect transistor with a reverse-biased Schottky-barrier gate fabricated on a gallium arsenide substrate. Roughly equivalent to a silicon MOSFET, HP GaAs FETs are depletion mode devices. Because charge carriers reach approximately twice the velocity as in silicon, for a given geometry a given gain can be reached at about twice the frequency.

Gain Block
A single stage of gain or a cascaded series of gains stages.

GΔ
Gain Flatness — The variation of gain over a specified frequency range.

Gmax
Maximum Available Gain — The gain achieved when a transistor is unconditionally stable and the input and output ports are simultaneously conjugately matched. Also designated MAG.

$G_{1\ dB}$
1 dB Gain Compression Point — The level of gain from a device which is 1 dB less than the gain measured under small-signal conditions for a given input level. See also $P_{1\ dB}$.

Harmonic Intermodulation Distortion
The ratio (in dB) of distortion to the IF output waveform caused by mixer-generated harmonics of the RF and LO input signals. This characteristic is extremely dependent on input frequency, RF and LO signal levels and the precise impedance characteristics of all terminations at the operating frequency.

Harmonic Signals
Signals which are coherently related to the output frequency. In general these signals are integer multiples of the output frequency.

Hybrid Integrated Circuits
The combination of thin-film or thick-film circuitry deposited on substrates with chip transistors, capacitors and other components. Thin-film construction is used for HP microwave integrated circuits (MICs).

Incidental FM
The peak to peak variations of the carrier frequency due to external variations with the unit operating at a fixed frequency at any point in the tunable frequency range.

Insertion Loss
The transmission loss measured in dB at that point in the passband which exhibits the minimum value. **See Item B, Figure 1.**

Integrated Spurious Output Power
The total power of all spurious outputs in and out of the specified frequency range.

Intercept Point
A figure (expressed in dBm) that indicates the linearity and distortion characteristics of a microwave component. It represents the point where the fundamental power output and spurious responses (usually third-order) intersect, when plotted on a log-log scale with output power as ordinate and input power as abscissa. See "Intercept Point" in Application Notes Section 10 for more details.

Intercept Point 3rd Order

Third Order Intercept Point — The intersection point of the fundamental POUT vs. PIN extrapolated line and the third-order intermodulation products extrapolated line. Also referred to as IP_3. In regard to mixers, this parameter is highly dependent on the LO and RF frequency, the LO drive level, and the impedance characteristics of all terminations at the operating frequency.

IP_3

Third Order Intercept Point.

Isolation

The ratio (in dB) of the power level applied at one port of a mixer to the resulting power level at the same frequency appearing at another port. Commonly specified isolation parameters of mixers are:

1. LO to RF port: The degree of attenuation of the LO signal measured at the RF port with the IF port properly terminated.
2. LO to IF port: The degree of attenuation of the LO signal measured at the IF port with the RF port properly terminated.
3. RF to IF port: The degree of attenuation of the RF signal measured at the IF port with the LO port properly terminated.

Normally the inverse isolation characteristics (such as RF to LO, IF to LO, and IF to RF) are essentially equivalent in a double-balanced mixer.

Isolator

A device that permits microwave energy to pass in one direction while providing high isolation to reflected energy in the reverse direction. Used primarily at the input of communications-band microwave amplifiers to provide good reverse isolation and minimize VSWR. Consists of a microwave circulator with one port (port 3) terminated in the characteristic impedance.

Limiting Level

The input power level at which the input/output characteristics exhibit compression (i.e., the transfer function becomes nonlinear in that the output increases less than 1 dB for a 1 dB increase in the input).

Linearity

Any deviation from a best fit straight-line approximation under specified conditions. **See Figure 3.**

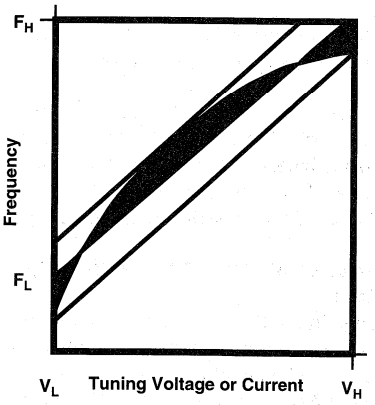


Figure 3

In regard to YIG-tuned and voltage-controlled oscillators, the maximum output frequency deviation from a best fit straight-line approximation of the tuning curve under specified load and constant temperature conditions.

In regard to YIG-tuned filters, the maximum deviation (in MHz) of the measured resonant frequency vs. coil current curve from the ideal linear tuning line over the YIG filter's operating frequency range.

Loss Bandwidth

The frequency span (in MHz) at a given insertion loss referenced to the passband minimum insertion loss.

MIC

Microwave Integrated Circuit — In microwave industry parlance, a hybrid circuit using thin- or thick-film conductors and passive components on a ceramic substrate combined with chip-form active and passive components. All HP MIC products use thin-film hybrid construction.

MICamp

Microwave Integrated Circuit Amplifier — HP's microwave integrated circuit amplifiers and related products.

Microstrip

(Microstripline) — A transmission line consisting of a metallized strip and a solid ground plane metallization separated by a thin, solid dielectric. This transmission line configuration is used in virtually all Avantek products since it permits accurate fabrication of 50Ω transmission line elements on a ceramic or PC board substrate.

MMIC
Monolithic Microwave Integrated Circuit designed using either Silicon or GaAs devices.

Modulation or Tuning Sensitivity
The slope or the first derivative of the tuning curve in ΔMHz/ΔV. Where necessary the fine grain or incremental slopes and the ratio of the slope should be specified over the frequency range.

Modulation or Tuning Sensitivity Variation
The change in the first derivative as a function of tuning voltage and/or frequency. Usually specified as percentage change of the first derivative over an incremental frequency range. Direction of tuning for measurement should be specified. Also may be specified as the ratio of the maximum to minimum value of the first derivative.

Modulation Response Bandwidth
The modulation frequency range where for a reference deviation bandwidth, all included modulation frequencies of equal amplitude will result in no less than a ratio of 1.414 (3 dB) of minimum to maximum deviation. The types of modulation should be specified as well as the internal impedance of the modulation source.

MTBF
Mean Time Between Failure — A calculated figure representing the estimated average lifetime of a device before it fails.

Noise Floor
The lowest input signal power level which will produce a detectable output signal from a microwave component, determined by the thermal noise generated within the microwave component itself. The noise floor limits the ultimate sensitivity to weak signals of a microwave system, since any signal below the noise floor will result in an output signal with a signal-to-noise ratio of less than one and will be more difficult to recover.

Non-Harmonic Signals
Signals which are not coherently related to the output frequency.

Octave
In microwave parlance, a band of frequencies, the limits of which have a 2:1 ratio. For example, 1-2 GHz, 4-8 GHz. Many components used in EW systems require an octave or greater than octave bandwidth.

1 dB Gain Compression
(1 dB GCP, Gain Compression Point, P_{1dB}) — The maximum output power of an amplifier at which amplification is nearly linear (higher power levels result in compression). As input power applied to an amplifier is increased, some point will be reached where a 10 dB increase in input signal results in only 9 dB of output signal increase — this is the 1 dB gain compression point. Other compression points such as 0.1 dB or 2 dB are sometimes specified.

Oscillator Load
The maximum VSWR seen by the oscillator at the output port, referenced to 50Ω.

Output Frequency
The frequency of the desired output of the component. The undesired frequency components may include harmonics, subharmonics, 3/2 harmonics or nonharmonic spurious signals.

Output Power
The minimum and/or maximum output power at the output frequency under all specified conditions. Usually the specified conditions are temperature, load, VSWR and supply voltage variations. It is typically expressed in dBm or milliwatts (mW).

Passband Ripple
The peak to peak value (in dB) of ripple occurring within the 3 dB passband referenced to the minimum insertion loss. **See Item F, Figure 1.**

Passband VSWR
The best VSWR as measured at any point within the 3 dB passband.

Passivation
The formation of an insulating layer directly over a circuit or circuit element to protect the surface from contaminants, moisture or particles.

Percent Bandwidth
$(2[f_2 - f_1]/[f_2 + f_1]) \times 100$ where f_1 and f_2 are the lower and upper endpoints, respectively, of the frequency range.

PIN diode
A diode made by diffusing the semiconductor so that a thin intrinsic layer exists between the P and N-doped regions (positive-intrinsic-negative). Such diodes do not rectify at microwave frequencies but behave as variable resistors controlled by the applied DC bias.

$P_{1\ dB}$
Output Power at 1 dB Gain Compression — Essentially the maximum output power available from the transistor while providing linear amplifications. Also designated: PO-1 dB, and in numerous other ways. See also $G_{1\ dB}$.

Post-Tuning Drift (PTD)
The maximum change in frequency (Δf_{PTD}) from the frequency measured at the beginning of the time interval (t_1). The time interval (t_1-t_2) shall be referenced to the application of a tuning command (t_0) The period of measurement ends at time (t_2). **See Figure 4.**

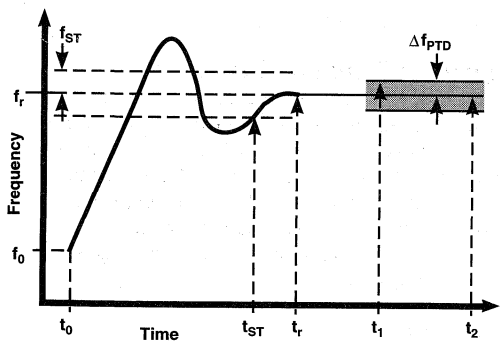


Figure 4

Power Output @ 1 dB Gain Compression
See: 1 dB Gain Compression.

Power Output Variation or Flatness
The maximum peak to peak power variation at all output frequencies in the tunable frequency range under all specified conditions.

P_T
Total power dissipated in a transistor. $P_T = V_C \times I_C + P_{IN(RF)} - P_{OUT(RF)}$.

Quadrature
Having a characteristic 90° phase shift. Used to describe a coupler in which the two output signals are 90° out of phase, and in telecommunications for modulation techniques such as QPR and QPSK.

Resonant Frequency or Passband Center Frequency
The arithmetic mean of the low and high normalized 3 dB frequencies.

Return Loss
When expressed in dB as the ratio of reflected power to incident power, it is a measure of the amount of reflected power on a transmission line when it is terminated or connected to any passive or active device. Once measured, it can be converted by equation to reflection coefficient which can then be converted to VSWR.

Saturated
With respect to microwave components, indicates the maximum output power available when the component is driven beyond its linear region.

Saturated Output Power
The maximum output power of a component. As input power is increased, some point will be reached to where the output power will maximize. This is known as the saturated output power (PSAT) and typically occurs at approximately 5 dB gain compression.

Sensitivity
The normalized change in a YIG component's center frequency resulting from a change in tuning coil current, specified in MHz/mA.

Settling Time
The time (t_{ST}) required for the output frequency to enter and stay within a specified error band ($\pm f_{ST}$) centered around a reference frequency (f_r) after application of a step input voltage (VCO) or current (YTO). The time (t_r) shall be specified for determining the reference frequency (f_r). The period of measurement ends at the reference time (t_r). **See Figure 4.**

Skirt (Bandpass)
The portions of the bandpass curve above the upper and below the lower 3 dB bandwidth points; and the upper and lower frequency points at which full off-resonance isolation is achieved. **See Figure 1.**

Skirt Spurious

The amount of additional transmission loss, referenced to the normalized filter skirt curve, outside the 3 dB passband, caused by the spurious resonance (absorption) modes. **See Item D, Figure 1.**

Slew Rates

The rate which the oscillator frequency can change in response to a step input on the tuning port. The step input waveform should be specified.

Small Signal Gain

The gain characteristics of an amplifier operating in the linear amplification region. HP typically measures small signal gain at least 10 dB below the input power level that creates 1 dB gain compression.

Small Signal Gain Flatness

Small signal gain deviation (stated as + and – and not P-P) from a flat reference line measured over the operating frequency of the amplifier at a fixed temperature.

S-Parameters

Scattering Parameter — Scattering parameters are a group of measurements taken at different frequencies which represent the forward and reverse gain, and the input and output reflection coefficients of a microwave component when the input and output ports of the component are terminated in specified impedances — usually 50Ω.

Magnitude	The length of the vector in the polar plane.
Angle	The direction of the vector in the polar plane.
dB	10 $\log_{10}$ (Power).
S_{11}	S-parameter input reflection coefficient — Expresses the magnitude and phase of the input reflection coefficient, measured with the input and output ports terminated in a pure resistance of 50Ω.
S_{21}	S-parameter forward transfer coefficient — Expresses the forward voltage gain magnitude and phase, measured with the input and output ports terminated in a pure resistance of 50Ω.
S_{12}	S-parameter reverse transfer coefficient — Expresses the reverse voltage gain (sometimes called isolation) magnitude and phase, measured with the input and output ports terminated in a pure resistance of 50Ω.
S_{22}	S-parameter output reflection coefficient — Expresses the magnitude and phase of the output reflection coefficient, measured with the input and output ports terminated in a pure resistance of 50Ω.

Specification Temperature Range

The range of temperatures as measured near the component or device mounting surface over which the operating component or device must meet all guaranteed specifications unless otherwise noted.

Spurious-Free Dynamic Range

The range of input signals lying between the tangential sensitivity level and an upper signal level at which generated in-band spurious outputs exceed the tangential level.

Spurious Signal and Outputs

Undesired signals produced by an active microwave component, usually at a frequency *unrelated* to the desired signal or its harmonics. Spurious outputs are both harmonically and non-harmonically related signals. Their tolerable amplitude should be specified within and out of the frequency range of the oscillator. Typical values range from -60 dBc to -80 dBc.

Stripline

A transmission line consisting of a conductor above or between extended conducting surfaces. Also see Microstrip.

Substrate

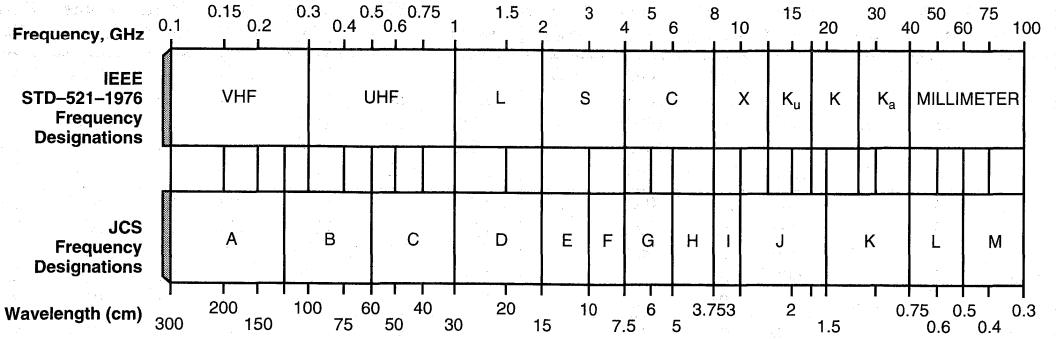
The wafer of ceramic (see alumina, beryllia) on which the thin-film circuit is deposited in hybrid microwave integrated circuit construction.

Suppression

The minimization of undesired side effects in circuit operations (e.g. two-tone intermodulation suppression, spurious output suppression, usually through a design compromise or the addition of specialized components).

Charts and Conversion Tables

Frequency Designation Chart



Charts and Conversion Tables, continued

The Effect of VSWR on Transmitted Power

VSWR	VSWR (dB)	Return Loss (dB)	Trans/ Loss (dB)	Volt. Refl. Coeff.	Power Trans (%)	Power Refl. (%)	VSWR	VSWR (dB)	Return Loss (dB)	Trans/ Loss (dB)	Volt. Refl. Coeff.	Power Trans (%)	Power Refl. (%)
1.00	.0	∞	.000	.00	100.0	.0	1.64	4.3	12.3	.263	.24	94.1	5.9
1.01	.1	46.1	.000	.00	100.0	.0	1.66	4.4	12.1	.276	.25	93.8	6.2
1.02	.2	40.1	.000	.01	100.0	.0	1.68	4.5	11.9	.289	.25	93.6	6.4
1.03	.3	36.6	.001	.01	100.0	.0	1.70	4.6	11.7	.302	.26	93.3	6.7
1.04	.3	34.2	.002	.02	100.0	.0	1.72	4.7	11.5	.315	.26	93.0	7.0
1.05	.4	32.3	.003	.02	99.9	.1	1.74	4.8	11.4	.329	.27	92.7	7.3
1.06	.5	30.7	.004	.03	99.9	.1	1.76	4.9	11.2	.342	.28	92.4	7.6
1.07	.6	29.4	.005	.03	99.9	.1	1.78	5.0	11.0	.356	.28	92.1	7.9
1.08	.7	28.3	.006	.04	99.9	.1	1.80	5.1	10.9	.370	.29	91.8	8.2
1.09	.7	27.3	.008	.04	99.8	.2	1.82	5.2	10.7	.384	.29	91.5	8.5
1.10	.8	26.4	.010	.05	99.8	.2	1.84	5.3	10.6	.398	.30	91.3	8.7
1.11	.9	25.7	.012	.05	99.7	.3	1.86	5.4	10.4	.412	.30	91.0	9.0
1.12	1.0	24.9	.014	.06	99.7	.3	1.88	5.5	10.3	.426	.31	90.7	9.3
1.13	1.1	24.3	.016	.06	99.6	.4	1.90	5.6	10.2	.440	.31	90.4	9.6
1.14	1.1	23.7	.019	.07	99.6	.4	1.92	5.7	10.0	.454	.32	90.1	9.9
1.15	1.2	23.1	.021	.07	99.5	.5	1.94	5.8	9.9	.468	.32	89.8	10.2
1.16	1.3	22.6	.024	.07	99.5	.5	1.96	5.8	9.8	.483	.32	89.5	10.5
1.17	1.4	22.1	.027	.08	99.4	.6	1.98	5.9	9.7	.497	.33	89.2	10.8
1.18	1.4	21.7	.030	.08	99.3	.7	2.00	6.0	9.5	.512	.33	88.9	11.1
1.19	1.5	21.2	.033	.09	99.2	.8	2.50	8.0	7.4	.881	.43	81.6	18.4
1.20	1.6	20.8	.036	.09	99.2	.8	3.00	9.5	6.0	1.249	.50	75.0	25.0
1.21	1.7	20.4	.039	.10	99.1	.9	3.50	10.9	5.1	1.603	.56	69.1	30.9
1.22	1.7	20.1	.043	.10	99.0	1.0	4.00	12.0	4.4	1.938	.60	64.0	36.0
1.23	1.8	19.7	.046	.10	98.9	1.1	4.50	13.1	3.9	2.255	.64	59.5	40.5
1.24	1.9	19.4	.050	.11	98.9	1.1	5.00	14.0	3.5	2.553	.67	55.6	44.4
1.25	1.9	19.1	.054	.11	98.8	1.2	5.50	14.8	3.2	2.834	.69	52.1	47.9
1.26	2.0	18.8	.058	.12	98.7	1.3	6.00	15.6	2.9	3.100	.71	49.0	51.0
1.27	2.1	18.5	.062	.12	98.6	1.4	6.50	16.3	2.7	3.351	.73	46.2	53.8
1.28	2.1	18.2	.066	.12	98.5	1.5	7.00	16.9	2.5	3.590	.75	43.7	56.2
1.29	2.2	17.9	.070	.13	98.4	1.6	7.50	17.5	2.3	3.817	.76	41.5	58.5
1.30	2.3	17.7	.075	.13	98.3	1.7	8.00	18.1	2.2	4.033	.78	39.5	60.5
1.32	2.4	17.2	.083	.14	98.1	1.9	8.50	18.6	2.1	4.240	.79	37.7	62.3
1.34	2.5	16.8	.093	.15	97.9	2.1	9.00	19.1	1.9	4.437	.80	36.0	64.0
1.36	2.7	16.3	.102	.15	97.7	2.3	9.50	19.6	1.8	4.626	.81	34.5	65.5
1.38	2.8	15.9	.112	.16	97.5	2.5	10.00	20.0	1.7	4.807	.82	33.1	66.9
1.40	2.9	15.6	.122	.17	97.2	2.8	11.00	20.8	1.6	5.149	.83	30.6	69.4
1.42	3.0	15.2	.133	.17	97.0	3.0	12.00	21.6	1.5	5.466	.85	28.4	71.6
1.44	3.2	14.9	.144	.18	96.7	3.3	13.00	22.3	1.3	5.762	.86	26.5	73.5
1.46	3.3	14.6	.155	.19	96.5	3.5	14.00	22.9	1.2	6.040	.87	24.9	75.1
1.48	3.4	14.3	.166	.19	96.3	3.7	15.00	23.5	1.2	6.301	.88	23.4	76.6
1.50	3.5	14.0	.177	.20	96.0	4.0	16.00	24.1	1.1	6.547	.88	22.1	77.9
1.52	3.6	13.7	.189	.21	95.7	4.3	17.00	24.6	1.0	6.780	.89	21.0	79.0
1.54	3.8	13.4	.201	.21	95.5	4.5	18.00	25.1	1.0	7.002	.89	19.9	80.1
1.56	3.9	13.2	.213	.22	95.2	4.8	19.00	25.6	.9	7.212	.90	19.0	81.0
1.58	4.0	13.0	.225	.22	94.9	5.1	20.00	26.0	.9	7.413	.90	18.1	81.9
1.60	4.1	12.7	.238	.23	94.7	5.3	25.00	28.0	.7	8.299	.92	14.8	85.2
1.62	4.2	12.5	.250	.24	94.4	5.6	30.00	29.5	.6	9.035	.94	12.5	87.5

Charts and Conversion Tables, continued

Decibels — Volts — Watts Conversion Table for a 50 ohm System

dBm	V	P_0	dBm	mV	P_0	dBm	μV	P_0	dBm	nV	P_0
+53	100.0	200 W	–17	31.5	.02 mW	–65	128		–107	1000	
+50	70.7	100 W	–18	28.5	.01 mW	–66	115		–108	900	
+49	64.0	80 W	–19	25.1	.01 mW	–67	100		–109	800	
+48	58.0	64 W	–20	22.5	.01 mW	–68	90		–110	710	.01 pW
+47	50.0	50 W	–21	20.0		–69	80		–111	640	
+46	44.5	40 W	–22	17.9		–70	71	.1 nW	–112	580	
+45	40.0	32 W	–23	15.9		–71	65		–113	500	
+44	32.5	25 W	–24	14.1		–72	58		–114	450	
+43	32.0	20 W	–25	12.8		–73	50		–115	400	
+42	28.0	16 W	–26	11.5		–74	45		–116	355	
+41	26.2	12.5 W	–27	10.0		–75	40		–117	825	
+40	22.5	10 W	–28	8.9		–76	35		–118	285	
+39	20.0	8 W	–29	8.0		–77	32		–119	251	
+38	18.0	6.4 W	–30	7.1	.001 mW	–78	29		–120	225	.001 pW
+37	16.0	5 W	–31	6.25		–79	25		–121	200	
+36	14.1	4 W	–32	5.8		–80	22.5	.01 nW	–122	180	
+35	12.5	3.2 W	–33	5.0		–81	20.0		–123	160	
+34	11.5	2.50 W	–34	4.5		–82	18.0		–124	141	
+33	10.0	2 W	–35	4.0		–83	16.0		–125	128	
+32	9.0	1.6 W	–36	3.5		–84	11.1		–126	117	
+31	8.0	1.25 W	–37	3.2		–85	12.9		–127	100	
+30	7.10	1.0 W	–38	2.85		–86	11.5		–128	90	
+29	6.40	800 mW	–39	2.5		–87	10.0		–129	80	
+28	5.80	640 mW	–40	2.25	.1 μW	–88	9.0		–130	71	.1 fW
+27	5.00	500 mW	–41	2.0		–89	8.0		–131	61	
+26	4.45	400 mW	–42	1.8		–90	7.1	.001 nW	–132	58	
+25	4.00	320 mW	–43	1.6		–91	6.1		–133	50	
+24	3.55	250 mW	–44	1.4		–92	5.75		–134	45	
+23	3.20	200 mW	–45	1.25		–93	5.0		–135	40	
+22	2.80	160 mW	–46	1.18		–94	4.5		–136	35	
+21	2.52	125 mW	–47	1.00		–95	4.0		–137	33	
+20	2.25	100 mW	–48	0.90		–96	3.51		–138	29	
+19	2.00	800 mW	–49	0.80		–97	3.2		–139	25	
+18	1.80	64 mW	–50	0.71	.01 μW	–98	2.9		–140	23	.01 fW
+17	1.60	50 mW	–51	0.64		–99	2.51				
+16	1.41	40 mW	–52	0.57		–100	2.25	.1 pW			
+15	1.25	32 mW	–53	0.50		–101	2.0				
+14	1.15	25 mW	–54	0.45		–102	1.8				
+13	1.00	20 mW	–55	0.40		–103	1.6				
+12	.90	16 mW	–56	0.351		–104	1.41				
+11	.80	12.5 mW	–57	0.32		–105	1.27				
+10	.71	10 mW	–58	0.28		–106	1.18				
+9	.64	8 mW	–59	0.251							
+8	.58	6.4mW	–60	0.225	.001 μW						
+7	.500	5 mW	–61	0.20							
+6	.445	4 mW	–62	0.18							
+5	.400	3.2 mW	–63	0.16							
+4	.355	2.5 mW	–64	0.141							
+3	.320	2.0 mW									
+2	.280	1.6 mW									
+1	.252	1.25 mW									
0	.225	1.0 mW									
–1	.200	.80 mW									
–2	.180	.64 mW									
–3	.160	.50 mW									
–4	.141	.400 mW									
–5	.125	.32 mW									
–6	.115	.25 mW									
–7	.100	.20 mW									
–8	.090	.16 mW									
–9	.080	.125 mW									
–10	.071	.10 mW									
–11	.064	.07 mW									
–12	.058	.06 mW									
–13	.050	.05 mW									
–14	.045	.04 mW									
–15	.040	.03 mW									
–16	.0355	.02 mW									

Product Specification Worksheets

How to use

A series of product specification worksheets are provided to help you document your system's requirements. Completed worksheets are useful when communicating with your HP sales representative or distributor and can be FAXed. To save time, use these worksheets throughout the design cycle for specifying components requirements and documenting changes.

To use these worksheets, fill-in your name and phone number plus your application and the priority column. (To communicate only the specifications you need, please draw a line through those that do not apply.) By knowing your application and prioritizing your specifications the sales representative can recommend the best solution.

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Voltage Controlled Oscillator Worksheet

DATE _____

NAME _____ COMPANY_____ PHONE _____

APPLICATION: Defense/Commercial Platform:

RANK	PARAMETER	SPEC	COMMENTS
_____	Freq Range, min	_____	MHz or GHz
_____	Temp Range, min/MAX	____/____°C	ref to CASE
_____	Min Pout, 50 Ohm _____dBm		
_____	Max Pout, 50 Ohm	_____dBm	
_____	Pout Var., MAX	+ _____dB	
_____	Frequency Drift, MAX	_____MHz	
_____	2nd Harmonics, MAX/typ (relative to carrier)	_____/_____dBc _____dBm	
_____	3rd Harmonics, MAX/typ (relative to carrier)	_____/_____dBc _____dBm	
_____	Spurs Output, min	_____dBc	REF TO _____
_____	Phase Noise @ _____ KHz offset	_____dBc/Hz	
_____	Phase Noise @ _____ KHz offset	_____dBc/Hz	
_____	Pulling Figure, MAX @ _____ dB return loss	_____MHz	
_____	Pushing Figure, MAX @ _____ Vdc	_____MHz / V	
_____	Tuning Voltage, VL	_____Vdc	
_____	Tuning Voltage, VH	_____Vdc	
_____	1dB G.C.P., min	_____/_____dBm	
_____	Input Capacitance	_____pf	
_____	Settling Time, MAX to within _____MHz	_____µsec	
_____	Post Tuning Drift, MAX from _____ to _____	_____ MHz	
_____	Primary Power	_____Vdc @ _____mA	typ/MAX

Mechanical Requirements: Connector in / out _____/_____ Case

Screening Requirements: _____

Voltage Controlled Oscillator Worksheet Definitions

Freq Range, min
Band of operation for guaranteed specifications

Temp Range, min/MAX
Measured at the case for guaranteed specifications

Pout, (50 Ohm) min/MAX
Output power range into 50 ohm load

Pout Var., MAX
Output power range variation over the specified freq range at a fixed temperature

Frequency Drift, MAX
Over operating temperature at fixed supply voltage

2nd Harmonic, MAX
Signal output at 2 times carrier signal

3rd Harmonic, MAX
Signal output at 3 times carrier signal

Spurs Output, MAX
Non-harmonicly related signal outputs.

Phase Noise, MAX
aka FM noise; rapid freq jitter measured at set distance from fundamental signal

Pulling figure, MAX
Freq change caused by VSWR or Return Loss change

Pushing Figure, MAX
Freq change caused by change in supply voltage

Tuning Voltage, VL
Tuning voltage to reach lowest specification frequency

Tuning Voltage, VH
Tuning voltage to reach highest specification frequency

Input Capacitance
Capacitance seen at the tuning input port of the VCO

Settling Time
Time required for output signal to enter and stay within a specified freq band, and is centered around a reference freq

Post Tuning Drift
aka PTD; The total frequency drift measured in a specific time window *after a change in frequency*. Note: this is NOT Settling time.

Input Bias
DC circuit power required to operate at guaranteed specification

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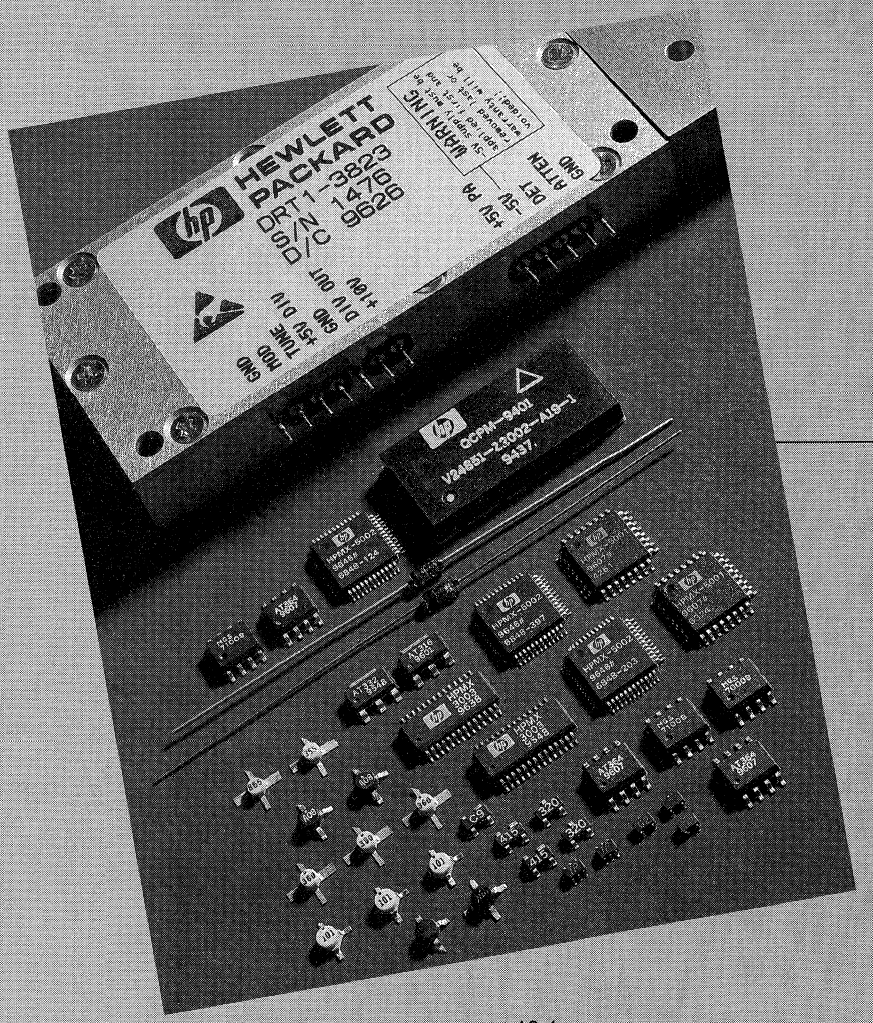
Application Design Tools



Application Design Tools

Services and Applications Literature

Hewlett-Packard customers are supported by an Applications Engineering Department. The applications engineering staff investigates circuit applications, design techniques, and device performance. The results of these investigations are published in Application Notes. These technical specialists are also available worldwide to assist customers in the use and selection of products contained in this catalog. For design assistance or to obtain more information about the services of the Applications Engineering Department, please call the HP office nearest you and ask for a Components sales engineer.

Electronic Selection Guide

HPRFhelp, an Electronic Selection Guide and information database for HP's RF and Microwave Semiconductor products, is available via ftp in the form of a collection of Microsoft Windows Help files in a self-installing archive. In addition to containing product information selectable by product family, electronic function, or market application, HPRFhelp also contains information about support literature and incorporates design information including s parameters and many SPICE models. HPRFhelp requires the use of a system running Microsoft Windows. This selection guide is available on the World Wide Web at **http://www.hp.com/go/rf**. Please contact your local HP sales representative for support information in printed form.

Electrostatic Discharge Damage and Control

This is an abstract from Application Note AN-A004R: Electrostatic Discharge Damage and Control.

Parametric or functional failure of silicon or GaAs semiconductors can occur as a result of electrostatic discharge. Failures in bipolar transistors are characterized by low breakdown voltage or high leakage current. FET failures are characterized by resistive shorts. In some cases, leakage current may increase with applied voltage and reduced reverse breakdown voltage.

Static discharge is almost always associated with people, the types of material or clothes that people wear, and the handling equipment that comes into contact with the semiconductor devices.

Recommendations for ESD Control

A partial listing of the most common generators of electrostatic charge is as follows:

1. Work stations and areas
   a. Work benches and surface coverings (non-conductive)
   b. Floors (vinyl and all waxed surfaces)
   c. Chairs (ungrounded)

2. Operator clothing
   a. Clean-room garments (synthetics)
   b. Personal clothing (synthetics, silk, and wool)

3. Part and assembly packaging materials
   a. Polyethylene bags and films
   b. Polyethylene bubble pack and foam
   c. Plastic boxes, trays, and cabinets

4. Cleaning and test areas
   a. High velocity gas flow temperature chambers for drying

A partial list of corrective measures for use in neutralizing these generators of electrostatic charge is as follows:

1. Work stations and areas
   a. Use grounded conductive mats and plates over non-conducting surfaces
   b. Ground conductive surfaces
   c. Use grounded floor mats
   d. Apply grounded conductive grids or nets to chairs
   e. Use electrostatic precipitators in the immediate work area

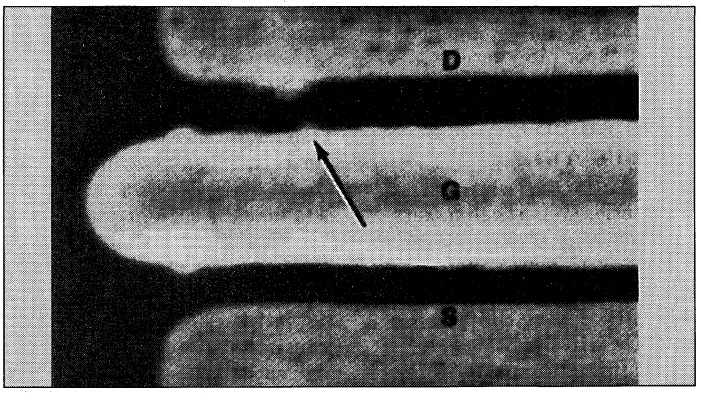
2. Operator clothing
   a. Use wrist grounding strap (10 megohm ground)
   b. Use static-free smocks
   c. Use foot-grounded straps on leather soles
   d. Control of personal clothing may be necessary

3. Part and assembly packaging material
   a. Use conductive bags and wrapping
   b. Eliminate the use of bubble pack
   c. Use shorting collars, rings, or wrappers on individual parts prior to installation

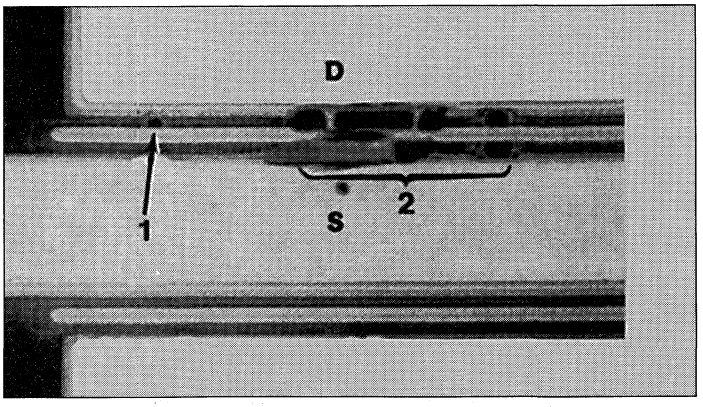
4. Cleaning and test areas
   a. Eliminate high velocity gas flow over assemblies and parts

Last, but definitely not least, are some common mistakes and problems associated with operator grounding. Some of these problems may be difficult to prevent if not carefully looked into.

1. Remember to place ground straps back on after breaks and lunch before handling any susceptible parts.
2. Be sure that the wrist strap is securely attached to the wrist touching the skin snugly for adequate connection. Wrist straps do not work when attached over clothing.
3. Do not wear smocks or clothing made of materials which tend to generate high electrostatic potentials such as synthetics, wool, or silk.
4. Do not use alligator clips or any other kind of quick-disconnect fasteners to ground the operator to the mat, as they tend to fall off easily.
5. Do not use tangled or knotted ground cords.
6. Do not allow wrist straps to become corroded or dirty from excessive use. They must be cleaned or replaced regularly.



T-Gate Channel with electrostatic damage (5.8KX).



An example of Hewlett-Packard Interdigitated metallization with electrostatic damage. (1) Initial static damage. (2) Side effect of discharge resulting from damage shown in (a).

Mounting Considerations for Packaged Microwave Semiconductors

This is an abstract from Application Note AN-A006: Mounting Considerations for Packaged Microwave Semiconductors.

This application note discusses how electrical, mechanical, and thermal connections should be made for packaged microwave devices. There are two primary package types: small signal and power.

Small Signal Device Packages

Soldering—Small signal microwave semiconductor packages can use the attachment of the leads to the electrical traces of the circuit board as the sole means of device mounting. Thus the lead attachment provides the mechanical, thermal, and electrical connections to the circuit. The most common way of attaching the leads of a package to a circuit board is by soldering.

The soldering process can subject devices to two different kinds of potentially dangerous stresses: electrical and thermal. A transistor or MMIC can suffer permanent electrical damage if any of its breakdown voltages are exceeded. This can happen when soldering equipment is not properly grounded, therefore MAKE SURE ALL SOLDERING EQUIPMENT IS AT GROUND POTENTIAL.

Thermal damage of various kinds can result if any of several critical temperatures are exceeded. Extremely high temperatures (above 425°C) will essentially cause new diffusions of the die, resulting in drastically changed electrical performance. Die attach temperatures establish a second critical temperature. Heating the package during soldering to above the die attach temperature (400°C for Si, 280°C for GaAs) can "float" the die, and seriously degrade the bond to the substrate. The third critical temperature is established by the maximum temperature the package can endure without damaging the integrity of the seal. Since there are a number of different types of seal (glass, epoxy, plastic, various solders) this temperature can vary from above 400°C to as low as 150°C.

In general the temperature at which the seal degrades is the lowest critical temperature in the die - package system, and establishes the maximum temperature ratings of the device. Each critical temperature is time dependent, and has associated with it a certain "dwell time" above which damage will occur.

Because of the relatively small volumes usually encountered in the microwave industry, hand soldering has been by far the most popular way of attaching a device to a circuit. Hewlett-Packard recommends the following guideline for this method: HAND SOLDERING SHOULD BE PERFORMED AT 250°C, IN LESS THAN 2 SECONDS PER LEAD. Hand soldering is the ONLY recommended method of soldering for any GaAs FET devices using low temperature solder seals.

Improved manufacturing technology and the advent of several consumer oriented microwave products has raised interest in more automated soldering techniques. These include wave soldering, vapor phase soldering, IR reflow soldering, and LASER reflow soldering, to name just a few. Rather than try to construct a recommended profile for each package type for each kind of soldering, Hewlett-Packard provides the information shown in Figures 1 through 3 to help the manufacturing engineer design a soldering profile. These curves show maximum recommended timed versus temperature for the

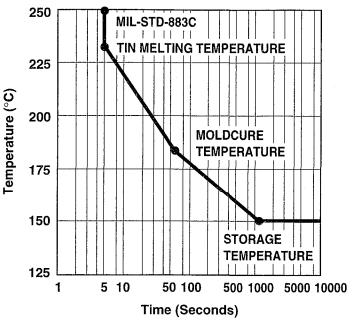


Figure 1. Temperature/Solder Graph for Plastic Packaged Devices.

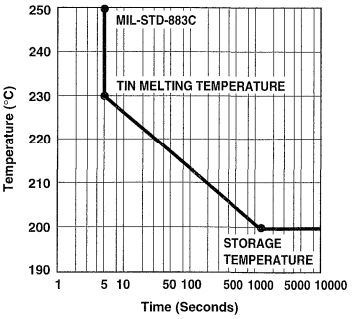


Figure 2. Temperature/Solder Graph for Micro-X Packaged Devices.

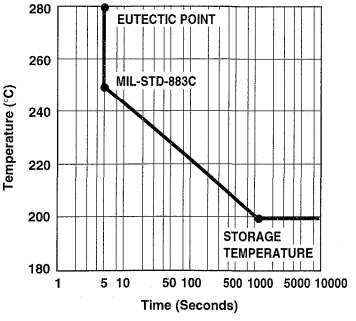


Figure 3. Temperature/Solder Graph for Gold Plated Packaged Devices.

plastic (04, 05, 11 (SOT-23), 33 (SOT-143), 84, 85, 86, SO-16, SOT-323, SOT-363, SOIC-8, MSOP-3, SSOP-16, SSOP-28, TQFP-32, and TQFP-48), micro-X ceramic (35, 36, 77) and gold (10, 20, 23, 70, 71) package families.

Electrical and Thermal Considerations—One extremely important electrical consideration should be kept in mind while mounting any microwave device. Any extra lead length becomes an additional undesired circuit element at microwave frequencies. This is especially important for ground lead length; seemingly small lengths of lead can result in deciBels of lost gain. In general all leads should mount flush with the pc board, with the smallest gap possible left between package body and circuit traces. For packages where the leads are not co-planar with the bottom of the package, it is better to make a hole in the pc board to allow for flush mounting than to bend the devices' leads.

Thermal considerations involved in the mounting of small signal devices are minimal. The device lead attachment provides sufficient heatsinking to these semiconductors. The output lead is the primary heat path for bipolar transistors and for these devices the bottom of the die is the collector (output) meaning these devices tend to be die attached directly to the output trace. The ground leads are the primary heat path in GaAs FETs, since these devices have electrically isolated backsides and are therefore usually die attached directly to ground. Note that this means additional lead length not only degrades electrical performance, it also increases the operating temperature of a small signal device by increasing the case-to-ambient thermal resistance. 100 mils of lead length in free air can raise the case-to-ambient thermal resistance of a small signal microwave package to between 150°C/W to 300°C/W. In contrast, properly mounted small signal devices should have case-to-ambient thermal resistances of less than 50°C/W.

Power Device Packages

Higher power devices come in specially designed packages that provide sufficient thermal conductivity to allow for reliable device operation at higher power dissipation levels. Packages for devices with bottom side electrical contacts (e.g. bipolar transistors) usually incorporate a Beryllium Oxide (BeO) ceramic substrate for superior thermal conductivity. Devices with electrically isolated backsides (e.g. GaAs FETs) do away with substrates under the die altogether, and mount directly to a rib of the heatsink brought up through the package for this purpose. Typically, power packages are much larger than are the small signal packages, due to the need for heat spreading. Thus such packages often incorporate some additional mechanical means of mounting beyond lead attachment.

Electrical and Thermal Considerations—Electrical attachment of power packages is done in the same manner as for small signal packages: through soldering of the leads. The same hand soldering guideline of 2 seconds per lead at 250°C applies. The graph of time vs. temperature for gold packages applies to the power packages as well. Mechanical and thermal attachment vary with the package style. The 20 style package has an electrically isolated area of metallization on the bottom of the package. It is intended that this area be attached to the circuit heatsink, either by soldering, or using a good thermal conductive epoxy. Soldering should follow the time-temperature guidelines of the "gold" packages (see Figure 3). Although the soldering of the leads to the circuit board is sufficient for mechanical attachment of this package, this bottom connection is necessary for proper thermal operation.

Most other power devices come in packages with flanges that can be bolted directly to the circuit heatsink. For best thermal conductivity, the bottom of the flange should be coated with a THIN layer (10 mils or so) of thermal conductive grease. This will result in the lowest possible case-to-ambient thermal resistance (θ_{ca})—usually giving a value less than 5°C/W. Note that a thick layer of thermal grease is almost as bad a thermal conductor as an air gap and would result in much higher values for θ_{ca}. Additionally, many flange packages use the flange as the ground connection to the device (see individual data sheets for terminal configuration) and excessive grease could degrade this important electrical contact.

Mechanical Considerations—Improper mounting techniques, can mechanically damage power device packages. Hewlett-Packard suggests that the following methods be used when a power device is installed in a circuit.

When bolting a flange device into the circuit, it is important to tighten both bolts only until they are finger tight, then ALTERNATELY tighten until the flange is

secured to the heat sink. Never tighten one bolt fully before inserting the second bolt; doing so can bow the package, resulting in miserable thermal contact or a cracked substrate.

It is also acceptable to solder the flange of a power device to the heatsink. The time vs. temperature guidelines for "gold" packages should also be used when soldering power devices in "gold" metalized packages (see Figure 3).

Leads of power devices should be soldered to the circuit traces only after the body of the device has been mechanically attached to the circuit. When a semiconductor already soldered to a pc board is bolted to a heatsink, extreme vertical shear forces can result at the package lead braze, fracturing the braze joint where the lead meets the package.

Following the above guidelines will help insure that your circuits built with Hewlett-Packard transistors and MMICs have the best possible longevity and reliability.

Transistor Chip Use

This is an abstract from Application Note AN-A005: Transistor Chip Use.

Packaging, Shipment, and Storage

Hewlett-Packard chips are supplied in two inch trays that use an elastomer as a carrier medium. The chips are held in place by the surface tension of the elastomer. One corner of the tray is beveled to provide orientation for chip selection. Each chip tray is enclosed in a plastic box to protect the die during shipping. Up to 300 chips can be contained in a tray.

Chip carriers should be opened only at a clean, well-lighted station without fast moving air. A white working surface is recommended for best visibility. The chips are kept in place by the surface tension of the elastomer on which they are placed. Once the clamps have been removed, the pack should be set down on the surface and the lid removed. Then, the paper can slowly (to avoid static electricity generation) be lifted off the lower half. Occasionally a chip may work loose from the surface of the elastomer and turn upside down. If this happens, the chip should be carefully picked up with tweezers, turned over, and placed back on the elastomer. At this point the die can be counted or visually inspected. The reverse of the procedure outlined above should be used to close the die carrier pack prior to storage or die attach operations.

Die can be stored in the trays in which they are shipped. Die that will be stored for long periods of time (greater than 1 to 2 weeks) should be kept in a dry nitrogen atmosphere for optimum reliability. Hewlett-Packard chips use a gold based metal system that is very resistant to deterioration; none the less, the best practice is to always store die in an inert atmosphere.

Die Handling

Normal die handling is with tweezers to prevent contamination of the die attach surface. The brittleness of both silicon and GaAs makes the sharp edges of the chip susceptible to damage if too much pressure is applied. A good precaution is to use only very sharp tweezers with excellent point alignment when handling die (e.g. EREM type 5 SA). Inexperienced operators should practice with bonding samples, which can be obtained from Hewlett-Packard.

The surface of the die is protected with a layer of silicon nitride passivation. This layer provides sufficient scratch protection to allow vacuum picks to also be used for moving die, as long as reasonable care is taken in die handling.

Die Attach

The die attach process serves three functions. First, it mechanically attaches the die to the circuit substrate. Second, it electrically connects the output of the circuit to the trace on which the die is mounted. Third, it establishes the thermal path by which excess heat leaves the die. All three factors must be considered when selecting a die attach process.

Different procedures are used for silicon chips and GaAs devices. To attach a silicon chip, the chip and mounting surface are heated sufficiently for the gold of the mounting surface to mix with the gold backside metal on the chip and melt into the silicon of the chip, forming a gold-silicon eutectic bond. This technique is suitable because devices built on silicon can tolerate the relatively high temperatures needed for eutectic formation without electrical degradation. Eutectic die attach yields the best thermal transfer and lowest contact resistance of available die attach methods. The temperature sensitivity of GaAs devices precludes the use of eutectic die attach; a low temperature gold alloy "solder-down" technique is used instead. In both cases the process should be carried out under an inert atmosphere blanket of

forming gas or nitrogen to prevent die attach contamination.

Recommended Eutectic Die Attach Procedure

1. Set the heater block temperature to 410°C ± 10°C. This temperature should be measured at the point on the die attach stage where the package is to be heated; often there is a significant difference between the dial reading and the actual stage temperature.

2. Place the circuit or package into which the chip will be attached on the heater block. Allow sufficient time for it to heat thoroughly—typically 5 to 15 seconds depending on thermal mass.

3. Using tweezers or a vacuum collet, pick up the chip and orient it properly for placement on the mounting surface.

4. Place the chip directly on the mounting surface (in general preforms are not needed for eutectic die attach). Scrub with a back-and-forth motion, being careful not to scratch the top surface of the chip. Continue scrubbing until wetting occurs; this should occur within three to four scrubs.

5. If wetting does not occur, check that the heater block is at the correct temperature, that the inert atmosphere is present, and that all gold surfaces are free of contamination. The inert atmosphere should be heated to around 250°C to prevent it from cooling the die to below the gold-silicon eutectic forming temperature of 387°C.

6. When wetting occurs, perform one circular scrub to insure wetting of the chip perimeter. 100% flow should be visible around the die. Carefully remove the tweezers or collet from the die.

7. Remove the circuit or package from the heater block and allow it to cool in air. The total time for die attach should be *less* than 10 seconds. Maintaining the die at the 410°C die attach temperature for longer than this can lead to reduced device reliability.

Recommended "Solder-down" Die Attach Procedure

1. Set the heater block temperature to 300°C ± 10°C. This temperature should be measured at the point on the die attach stage where the package is to be heated; often there is a significant difference between the dial reading and the actual stage temperature.

2. Place the circuit or package into which the die will be attached on the heater block. Allow sufficient time for it to heat thoroughly—typically 5 to 15 seconds depending on thermal mass.

3. Pick up a gold-tin (Au-Sn) preform and place it on the circuit or package in the die attach location. Use a sufficient quantity to insure good wetting and to produce a fillet around the die.

4. Using tweezers or a vacuum collet, pick up the chip that is to be die attached and orient it properly for placement on the mounting surface.

5. Place the chip on the mounting surface and scrub with a back-and-forth motion, being careful not to scratch the top surface of the chip. Continue scrubbing until wetting occurs; this should occur within three to four scrubs. If wetting does not occur, check that the heater block is at the correct temperature, that the inert atmosphere is present, and that all gold surfaces are free of contamination.

6. When wetting occurs, perform one circular scrub to insure wetting of the chip perimeter. 100% flow should be visible around the die. Carefully remove the tweezers or collet from the die.

7. Remove the circuit or package from the heater block and allow it to cool in air. The total time for die attach should be *less* than 10 seconds. Maintaining the die at the 300°C die attach temperature for longer than this can lead to reduced device reliability.

Wire Bonding

Electrical connections to the die are in general made by wire bonds. The output electrical connection to silicon products is most often made through the die attach, but can sometimes also be made through a topside wire bond (e.g. in the case of MSA chips). The bond pad size and metal adhesion strength of Hewlett-Packard chips are compatible with either gold-ball bonding or wedge bonding. Either technique may be used when building chip assemblies.

Recommended Ball Bonding Procedure

1. If thermocompression ball bonding, set the heater block temperature to 300° ± 10°C for silicon product, or to

260° ± 10°C for GaAs product. If thermosonic (ultrasonic) ball bonding, set the heater block to 150° ± 10°C for either silicon or GaAs product.

2. Use prestressed (annealed) gold wire between 0.0007 to 0.001 inches in diameter.

3. Calibrate the bond force as follows:

Wire Diameter (inches)	Bond Force (grams)	Machine Wedge Bond (grams)
0.0007	15–20	20±2
0.001	20–30	25±2

4. Proceed with bonding according to machine specifications. For common (emitter, source, or ground) wire bonds, start with the ball on the circuit bonding surface and bond to the common bond pad on the chip, then continue (stitch bond) to a second contact with the circuit bonding surface. Keep both loops of this common bond low and short.

Recommended Wedge Bonding Procedure

1. Set the heater block temperature to 300° ± 10°C for silicon product or to 260° ± 10°C for GaAs product. (Note: If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact temperature setting will need to be determined empirically, and will vary from machine to machine.)

2. Use prestressed (annealed) gold wire between 0.0005 to 0.001 inches in diameter.

3. Tip bonding pressure should be between 15 and 20 grams and should not exceed 20 grams. The footprint that the wedge leaves on the gold wire should be between 1.5 and 2.5 wire diameters across for a good bond.

4. Proceed with bonding according to machine specifications. Bonds should be made from the circuit element to the chip bonding pads to minimize pad damage. Also, bonds should be made to the source and drain pads of a FET prior to making the bond to the gate pad, to minimize the potential or electrostatic discharge damage.

MODAMP™ Silicon MMIC Chip Use

This is an abstract from Application Note AN-S009: MODAMP™ Silicon MMIC Chip Use.

Die Topography

MSA series RFICs share a common topology, shown in Figure 1. Two bipolar transistors (Q1 and Q2) are connected in Darlington configuration. Shunt (R_F) and series (R_E) resistive feedback are used to set both the gain and the impedance match of the structure. Resistors connecting the bases of Q1 (R_B) and Q2 (R_{bias}) to ground complete the DC bias network. Some geometries have additional resistors (R_{C1}, R_{C2}) connected to the collector of Q2 to allow for optional on-chip biasing. Figure 2 identifies these components on a typical MSA chip outline drawing.

The bond pad connected to the base of Q1 is the input to the circuit. The bond pad connected to R_E, R_B, and R_{bias} is the amplifier's common (or ground) terminal. Electrically, the output of the circuit is the collector of Q2. Since the MSA is built with conventional vertical bipolar technology, the entire bottom surface of the chip is a shared collector contact for the two transistors of the Darlington, and therefore serves as the output terminal of the MSA. For convenience, a topside collector contact is also provided for designers who would rather wire bond the output connection to the chip. The remaining bond pads are bias options that are not normally connected in typical chip use.

Use of Optional On-Chip Bias Resistors

The most common way of biasing MSAs is through a dropping resistor from a fixed voltage supply. The biasing resistor acts as a feedback element that stabilizes the DC operating point over temperature. The MSA-0100 MSA-0200, MSA-0300, MSA-0600,

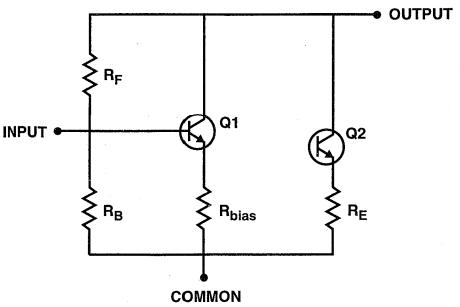
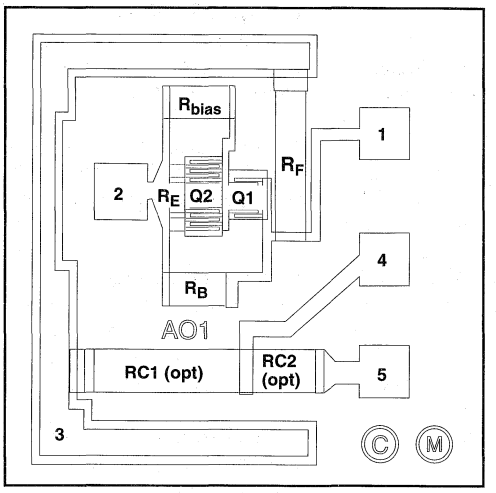


Figure 1. MSA Equivalent Circuit Schematic.



1 – INPUT
2 – COMMON
3 – OPTIONAL OUTPUT
4 – +12V ON-CHIP RC
5 – +15V ON-CHIP RC

Figure 2. Typical MSA Chip Outline Labeling Components and Bond Pads. (MSA-0100 shown as an example).

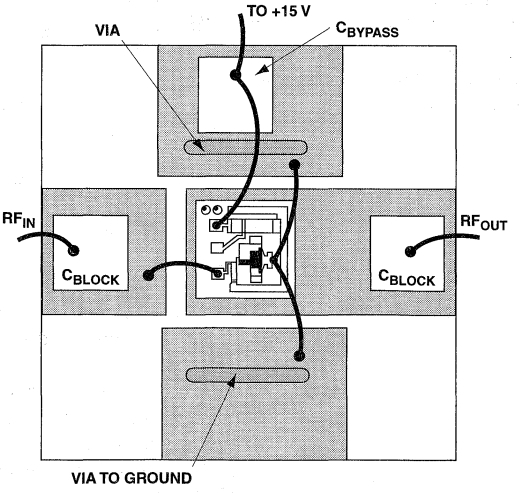


Figure 3. Representative Bond Scheme for Use of On-chip Bias Resistor. (+15 V option).

and MSA-0700 geometries include optional on-chip resistors that can be used to bias the device from a fixed voltage supply. For most designs, these on-chip resistors are left unconnected, and the bias is supplied through an external (off-chip) bias resistor. To make use of the on-chip bias option, wire bond the appropriate bond pad on the device to a circuit trace that will supply the appropriate voltage. The bond pad nearest to the RF input bond pad is for use with a nominal +12 volt supply; the remaining bond pad is for use with a nominal +15 volt supply (see Figure 3).

The MSA-0600 and MSA-0700 geometries have 3 bond pad options: a +5 volt pad which is nearest to the RF input bond pad, a +12 volt pad, and a +15 volt pad which is furthest from the RF input pad. The length of the bond wire is not critical. A long wire is, if anything, preferable as the added series inductance it provides improves the effectiveness of the bias feed as an RF choke. The circuit will no longer require external bias resistors or chokes or biasing the MSA, although an external inductor in series with the bias resistor usually improves P_{1dB} and gain performance. A bypass capacitor at the power supply rail is still recommended.

Several factors should be considered before using the on-chip bias resistors. First, the values of these resistors will vary from one wafer run to another; the nominal tolerance is ±15%. Hewlett-Packard does not guarantee either the values of these resistors or the performance that will be obtained if they are used. Next, these resistors are made of polysilicon, which has a temperature coefficient of -0.08%/°C. Since this coefficient is negative, the on-chip resistors provide less feedback at high temperatures (and hence less bias stability) than would an external carbon resistor possessing a positive temperature coefficient. Finally, using these resistors creates a significant new on-chip heat source that will raise the operating temperature of the

transistors in the MSA. This will decrease some aspects of RF performance (especially P_{sat}) and reduce the MTTF of the device.

Sample Circuits

Since MSAs are matched 50 Ω gain blocks, no special RF circuit design is required when using these chips. The MSA chip is die attached directly on the output trace, and the input connection is made by a wire bond. The ground connections are also made by wire bonds. Solid metallization should be brought up on either side of the die to allow for stitch bonding on the common bond. The bond attach points should be connected to the backside ground of the circuit through multiple vias.

Both input and output transmission lines need to be DC blocked; blocking capacitors should be of a high enough value to present a low series impedance across the frequency range over which the amplifier will operate. Remember to include the effect of parasitic inductance when calculating capacitor impedance. MOS capacitor die, ceramic chip capacitors, or gap capacitances in the transmission line traces can all be used as blocking capacitors.

MSA chips are DC biased in th same manner as packaged MSA products; refer to the next section on Biasing MSAs or to Applications Note AN-S003: Biasing MSA Series RF Integrated Circuits for more information.

A sample layout for a one stage MSA amplifier is shown in Figure 4. This layout uses MOS chips for blocking capacitors, ceramic chips for bypass capacitors, and thin film resistors for the bias feed. No additional choke inductance is used.

Conclusion

The simplicity and performance offered by MSA chips, combined with the reduced size and lower parasitics of chip-and-wire assembly technology, create microwave circuitry with superior performance.

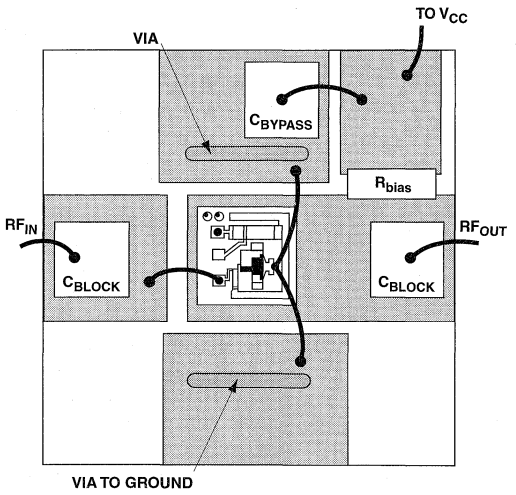


Figure 4. Typical One Stage MODAMP MMIC Circuit.

Biasing MODAMP MMICs

This is an abstract from Application Note AN-A003: Biasing MODAMP MMICs.

The bias point of the MSA-Series MMIC can best be described by specifying the total device current I_d.

Both power and gain can be adjusted by varying I_d. Curves of typical performance as a function of bias are shown on the individual MSA data sheets.

Bias Circuitry Options

Once an appropriate bias point has been chosen, circuitry must be provided to ensure that the MSA operates at that bias point. To be effective, this circuitry must establish an appropriate bias point across the entire operating temperature range the MSA will experience. The internal resistors on the MMIC have a temperature coefficient -0.08%/°C; the on-chip transistors increase in β at a rate of +0.07%/°C. If the bias current I_d is to remain constant over a broad temperature range, the bias circuitry must decrease the device voltage V_d at higher temperatures and increase V_d at lower temperatures.

Three possible biasing schemes are described in detail below.

Voltage Source On Collector

The simplest bias scheme available is to provide a fixed voltage to the collector or output terminal of the MSA. This voltage can be supplied either from a voltage regulator or from a power supply. It must be provided through an RFC (Radio Frequency "Choke," or high-value inductor) to keep the high frequency signal isolated from the DC circuitry. A large-value capacitor (e.g. 1 μF) should

be connected from the DC side of the RFC to Ground to provide a low impedance path to any signal that does get past the RFC. DC blocking capacitors (or alternatively transformers, if the MSA is to be operated at very low frequencies or at DC) must be used to isolate both the input of the MSA from the drive source and the output of the MSA from the load. The entire circuit is shown in Figure 1.

Because of its very narrow temperature operating range and sensitivity to V_d this bias scheme is not appropriate for most production circuits. It finds its major applications in laboratory testing of devices utilizing variable power supplies to provide the bias. With this bias scheme, temperature variations on the order of 25°C will cause significant alterations in performance; temperature variations on the order of 75°C can destroy devices by causing them to draw too much current. Device-to-device variations may also yield an MSA that draws an excessively high current if V_d is fixed, even at room temperature.

Collector Bias Stabilization Resistor

The fixed collector voltage bias circuit described above can be changed into a temperature-compensated bias circuit with the addition of a bias stabilization resistor in the collector feed. This resistor acts as a simple feedback element. As the temperature increases, the MSA tries to draw more and more current. Since this current is supplied through a resistor, the MSA bias voltage V_d decreases as I_d tries to increase: Vcc stays fixed; I_d increases with temperature causing the voltage drop I_dR_C across R_C to increase thus lowering V_d and "throttling back" on the bias current I_d. Note that the amount of feedback is proportional to the voltage drop across R_C and hence to the value of R_C. For effective compensation over normal operating temperature ranges (-25°C to +100°C), a voltage drop of at least 4 volts is recommended.

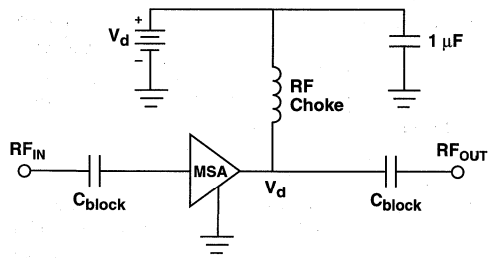


Figure 1. Fixed Collector Voltage Bias Circuit.

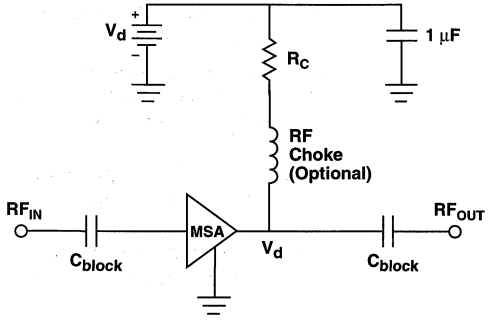


Figure 2. Collector Bias Stabilization Resistor Bias Circuit.

Remember that R_C itself will change in resistance as the temperature changes. By selecting a bias resistor with an appropriate temperature coefficient the temperature compensation of this circuit can be "fine tuned." Carbon composite resistors typically have a temperature coefficient of +0.0001%/°C, and work particularly well as bias stabilization resistors.

A side benefit of using a bias stabilization resistor is that it is often of high enough impedance that an RFC is no longer needed to keep the high frequency signal out of the DC bias. It is recommended that an RFC still be used if the MSA is being used near saturation; otherwise RC appears in parallel with the load resistance and can cause enough of a shift in load impedance to reduce both gain and saturated power by 1 to 2 dB.

The circuitry needed for a bias stabilization resistor scheme is shown in Figure 2.

Active Bias

Active bias circuitry can be used to provide temperature stability without requiring the large voltage drop or relatively high disputed power needed with a bias stabilization resistor. A simple realization using a resistively-biased PNP transistor as a current source is shown in Figure 3.

In this circuit R_1 and R_2 form a resistive divider that establishes the bias point of the PNP bias transistor. R_3 provides a "bleed path" for any excess bias current; it is a safety feature that can be omitted from minimum element realizations of this circuit. D_1 is also an optional element; its purpose is to provide temperature compensation by tracking the voltage variation with temperature of the emitter-to-base junction of the PNP bias transistor. For this reason, when it is included it is often realized using the E-B junction of a second PNP transistor identical to the bias transistor, connected with its collector-base junction shorted.

R_C is a feedback element that keeps I_d constant. If the device current starts to increase, the voltage drop across R_C also increases, turning off the E-B junction of the PNP transistor, and hence decreasing the bias voltage V_d applied to the MSA. For best circuit operation, there should be at least a 0.5 to 1 volt drop across R_C. The PNP transistor is acting in the saturated mode with both junctions forward biased. The voltage drop needed across the emitter to collector junction of this transistor will therefore be equal to its V_{CEsat} — typically only several tenths of a volt. Thus, the total voltage difference needed between V_{CC} and V_d is only about 1.3 volts for this circuit, as compared to the 4 volts or so needed by the bias stabilization resistor for good bias stability over temperature.

A side effect of the PNP bias transistor operating in the saturated mode is that this bias requires some extra "charge up" time at turn-on and "discharge" time at turn-off. How much extra time is required will depend on the time constants of the PNP transistor.

Systems requiring wide dynamic range operation or AGC (automatic gain control) often require that the MSAs operate at variable operating points. If R_2 is made variable this bias scheme will work well for such applications.

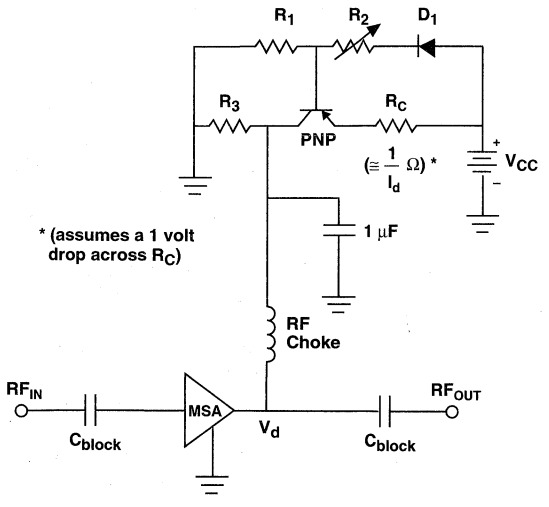


Figure 3. Active Bias.

Measurements

The data on the devices presented in this catalog were taken by measurements performed in 50 ohm test fixtures. These measurements may be divided into four basic groups: S-parameters, noise parameters, power parameters and thermal parameters. Except for power parameters, these subjects are covered in detail in the Hewlett-Packard Transistor Primer Series. The following are brief summaries of the topics.

S-Parameters

Scattering parameters are a group of measurements taken at different frequencies which represent the forward and reverse gain, and the input and output reflection coefficients of a microwave component when the input and output ports of the component nre terminated in equal impedances—usually 50 ohms. Some pertinent definitions are as follows:

Magnitude—The length of the vector in the polar plane.

Angle—The direction of the vector in the polar plane.

dB—10 $\log_{10}$ (Power Magnitude) or 20 $\log_{10}$ (Voltage Magnitude)

S_{11}—S-parameter input reflection coefficient—Expresses the

magnitude and phase of the input reflection coefficient with the input and output ports terminated in a pure resistance of 50 ohms.

S_{21}—S-parameter forward transfer coefficient—Expresses the forward voltage gain magnitude and phase measured with the input and output ports terminated in a pure resistance of 50 ohms.

S_{12}—S-parameter reverse transfer coefficient—Expresses the reverse voltage gain (sometimes called isolation) magnitude and phase, measured with the input and output ports terminated in a pure resistance of 50 ohms.

S_{22}—S-parameter output reflection coeffcient—Expresses the magnitude and phase of the output reflection coefficient with the input and output ports terminated in a pure resistance of 50 ohms.

Stability factor, given by

$$k = \frac{1 + |D|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{21}|\,|S_{12}|}$$

where $D = S_{11}\,S_{22} - S_{21}\,S_{12}$

If $k > 1$ and $|D| < 1$ then the two-port that k describes is unconditionally stable for all terminations with non-negative resistance. If $k < 1$ some terminations exist which will cause the two-port to oscillate.

The utility of S-parameters as a complete description of a device's small signal (linear) performance has been generally accepted by the microwave industry. S-parameters are preferred over other 2-port parameters (Z, Y, H, etc.) as a means of characterization because they are easier to measure: the terminations required usually result in stable device operation, and commercial equipment designed specifically for S-parameter measurement is readily available. None the less, accurate S-parameter device characterization is difficult to obtain for a number of reasons.

Since a device's performance characteristics are a function of both its bias point and its operating temperature, it follows that the S-parameter description used to describe the device's behavior should also vary with bias point and temperature. For this reason, both the bias and the temperature need to be specified. In general, Hewlett-Packard provides S-parameters measured at the recommended operating bias and at +25°C ambient temperature. In cases where operation at different bias levels might be appropriate, more than one description is generally given.

For a number of reasons, S-parameters will vary from device to device. The major reasons are process variations, material inconsistencies and assembly irregularities. A normal distribution of S-parameters is approximately ±10%. Hewlett-Packard publishes data which is representative of a "typical" unit. This data is based on the measurement of many devices taken from different wafers and several process lots.

The actual measurement of the device is made in a test fixture using an HP8510 Network Analyzer. The style of the fixture will greatly influence the measurement. To achieve the best results, the device should be measured in the medium in which it will be used. Since the majority of Hewlett-Packard's customers design in microstrip, this is the style of fixture that is currently being used to characterize the devices. Such a fixture is shown in Figure 2 where the device is mounted between two 50 ohm microstrip substrates which are sandwiched between two 50 ohm connector assemblies. Note that this fixture features excellent grounding and may have a shorter ground path than does a production circuit. The designer may wish to add some common lead inductance to the published S-parameters to compensate for this effect.

If the S-parameters that are published are to be repeated, the conditions under which they are taken must be duplicated as closely as possible. Measurements should be taken on the Intercontinental Microwave fixture (from the 1000 series or 2000 series) that Hewlett-Packard is currently using and measurements should be made on a HP8510 Network Analyzer. The device should be biased at the same bias as specified in the catalog, and the

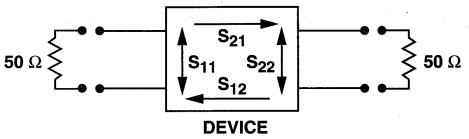


Figure 1. Two Port S-Parameters.

same method of correcting for the effects of the test fixture must be applied.

The simplest method for correcting is the reference plane extension (rpe) technique. Hewlett-Packard uses this method to characterize its silicon products up to 6 GHz. This method assumes a lossless, reflectionless, dispersionless fixture with the input and output having identical properties. The measured S-parameters are simply corrected mathematically by the software to account for the electrical length of the fixture. This electrical length can be determined by either measuring the distance to an open circuit or 1/2 the distance of a "through" line.

A more accurate method of correction is to de-embed the data. This is accomplished by characterizing the fixture and then subtracting its effects from the measured S-parameters.

Though generally more time consuming than the reference plane extension methods, this technique must be used to obtain accurate S-parameters above 8 GHz.

Hewlett-Packard uses the "through-delay" method of deembedding S-parameters for GaAs devices. The "through" is a 50 ohm microstrip transmission line with an electrical length equal to the sum of the input and output substrates used in the fixture. The "delay" is a transmission line similar to the "through" with a 50 mil longer physical length. Since this technique compares electrical lengths it is inaccurate at frequencies where the "through" and the "delay" are essentially the same length (below 1 GHz). For further explanation of this technique refer to the Hewlett-Packard Application Note *Measurement and Modeling of GaAs FET Chips*.

Since the unpackaged die are mounted on chip carriers (see Figure 3) in order to measure their S-parameters, it is impossible to 100% test this kind of device before shipping. Instead, S-parameters are measured on a sample of devices at the wafer qualification step. The chip S-parameters that Hewlett-Packard lists in this catalog are based on chip carrier measurements, and include the inductances associated with the bond wires (about 0.5 nH gate and drain bond and 0.15 nH source bond for a FET and about 0.5 nH base bond and 0.2 nH emitter bond for a bipolar device).

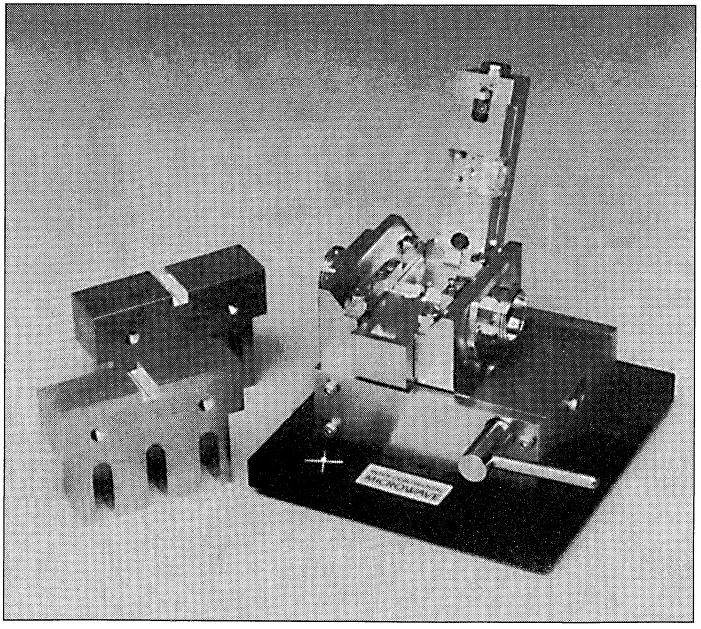


Figure 2. Typical 50 Ohm Test Fixture.

Noise Parameters

The noise performance of a transistor can be described by four noise-parameters in the noise figure equation:

$$F = F_{MIN} + \frac{R_N}{G_G} \mid V_G - Y_{OPT} \mid^2$$

where:

F_{MIN} is the minimum transistor noise figure.

R_{N1} is the noise resistance in ohms.

$Y_{OPT} = G_{OPT} + jB_{OPT}$ is the required generator admittance at the input port for minimum noise figure.

$Y_{GP} = G_{GP} + jB_{GP}$ is the generator admittance at the input port.

$\Gamma_{OPT} = \frac{Y_O - Y_{OPT}}{Y_O - Y_{OPT}}$ is the generator reflection coefficient corresponding to Y_{OPT}.

These parameters are measured in a 50 ohm system with a low loss tuner at the input and output ports. The transistor is biased for minimum noise, the output tuner set for maximum gain and the input tuner set for minimum noise figure. The measurement of F_{MIN} must include a correction for the tuner loss, as well as for second stage noise correction.[1] The input tuner is later measured for the G_{OPT} noise parameter, which is referred to the transistor input reference plane by translating the reflection coefficient by and equivalent circuit model of the test fixture.

The parameter R_{N1} is determined by measuring the 50 ohm noise figure:

$$F_{50} = F_{MIN} + 50R_N\,|0.02 - Y_{OPT}|^2$$

$$R_N = \frac{F_{50} - F_{MIN}}{50\,|0.02 - Y_{OPT}|^2}$$

This data is further verified by measuring F at several other tuner settings which are later measured for Γ_G or Y_G. As an additional check on the noise data, an internal device modeling program (AMCAP) is used to generate the theoretical noise parameters from the small-signal equivalent circuit. This simulation can also be used to generate noise parameters at other frequencies.

By plotting the noise figure circles in the Γ_G plane, the accuracy of both S-parameter and noise-parameter data can be verified. Figures 4 and 5 show these circles for three Hewlett-Packard low noise devices, AT-41435, ATF-10136 and ATF-13136 at appropriate frequencies when biased for best noise figure in a 50 ohm system.

Power Parameters

The power characteristics of devices in this catalog consist primarily of two parameters: P_{1dB} and G_{1dB}. P_{1dB} is the device output power at one dB gain compression. G_{1dB} is the one dB compressed gain.

Power measurements were made using Class A bias points. This kind of operation gives best linearity, and is typical of device use. In general P_{1dB} can be improved by increasing bias current though tradeoffs with MTTF, noise figure, IP_3, or other parameters may be involved. Improved efficiency can be obtained with the discrete devices by operating them Class C.

All silicon product power measurements were made in 50 ohm coaxial test fixtures. Bias was provided through HP bias tees. Separate collector and base supplies were used to bias the discrete devices; MSAs were biased from a power supply through an appropriate dropping resistor: in all cases the bias point was set to the catalog value of I_C or I_D under DC (no signal) conditions, and not subsequently adjusted during measurements. Note that some amount of current pulling can occur at P_{1dB} using these bias schemes.

Power measurements for small signal and unmatched power GaAs FETs and GaAs MMICs were made in 50 ohm coaxial test fixtures. Bias was provided through HP bias tees. Each device was biased to the catalog value of V_{Ds}, and I_D under DC (no signal) conditions. Small signal devices were tested using separate drain and gate supplies with a common ground point and active feedback via an operational amplifier to prevent current pulling. Discrete power devices used separate supplies with no feedback, allowing some amount of current pulling at P_{1dB}.

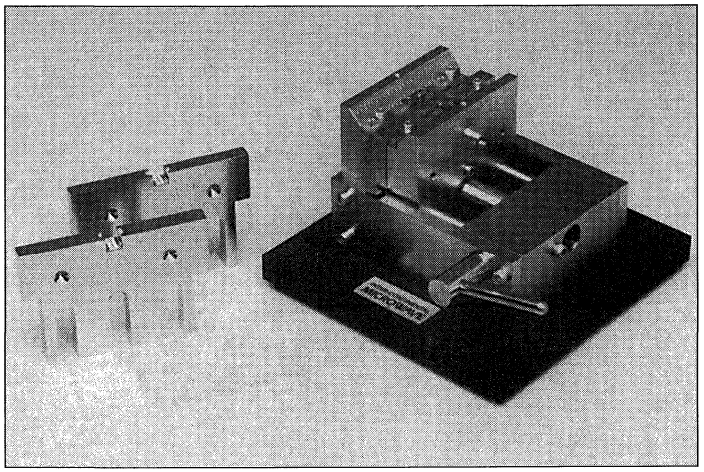


Figure 3. Test Carrier Used to Characterize Unpackaged GaAs FET Chips.

[1] Eric W. Strid, "Measurement of Losses in Noise-Matching Networks" *IEEE Transactions on MTT*, Vol. MTT-29, March 1981, pp 247-252.

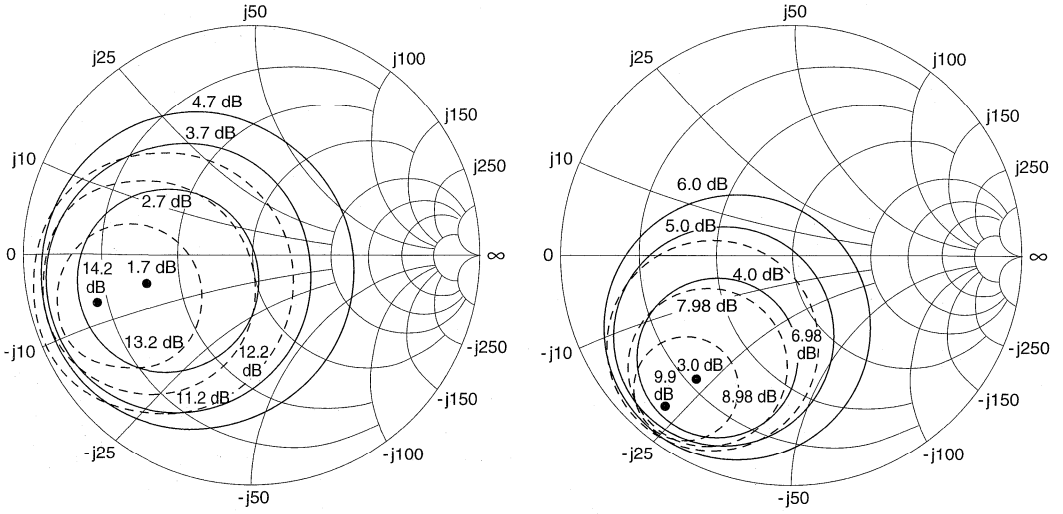
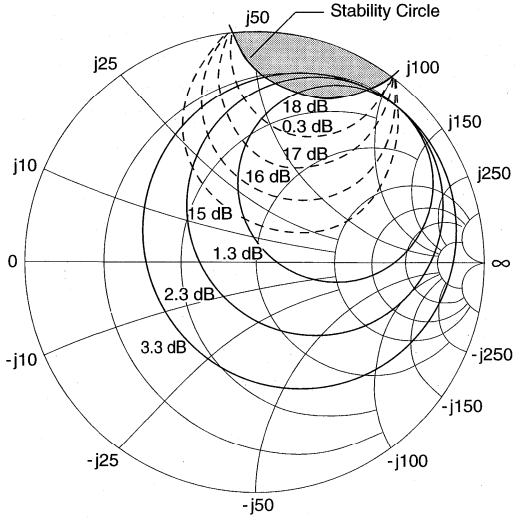
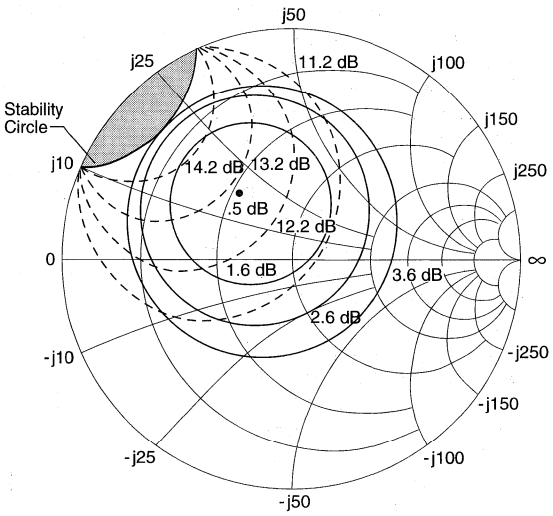


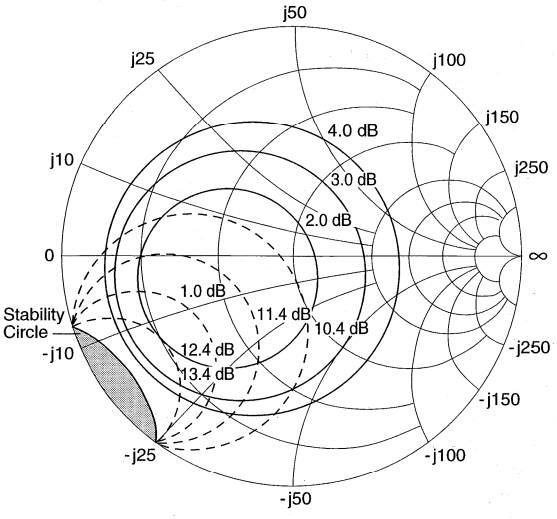
Figure 4. Noise Figure Circles and Available Gain Circles in the Γ_G Plane.



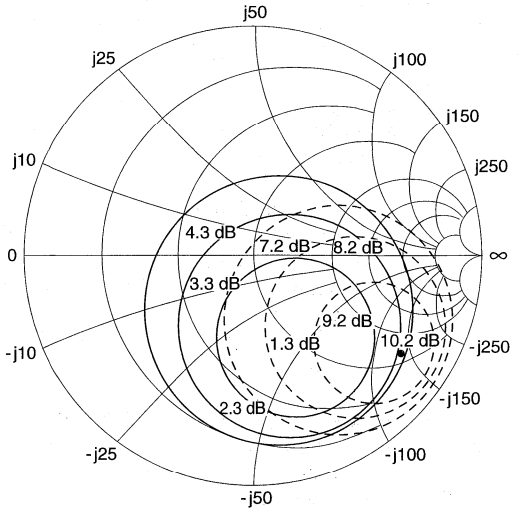
AT-10136: f = 2 GHz, V_{DS} = 2 V, I_{DS} = 20 mA



AT-10136: f = 4 GHz, V_{DS} = 2 V, I_{DS} = 20 mA



AT-13136: f = 8 GHz, V_{DS} = 3 V, I_{DS} = 20 mA



AT-13136: f = 12 GHz, V_{DS} = 3 V, I_{DS} = 20 mA

KEY: Noise Circles ———
Gain Circles - - - -

Figure 5. Noise Figure Circles and Available Gain Circles in the Γ_G Plane.

Tuners were used to present the correct large signal impedances to discrete and unmatched GaAs MMIC devices to obtain P_{1dB} and G_{1dB}. Both tuners were adjusted to obtain maximum output power with the device set at the catalog nominal value ($P_{1dB} - G_{1dB}$). The input drive level was then decreased by 10 dB, and the nominal small signal gain was measured. (Measurements for Silicon MSAs did not use tuners, as these devices are already matched for operation in a 50 ohm system.) The input drive level was then increased until the measured gain had decreased by one dB from the nominal small-signal value. This gain value was recorded as G_{1dB}. The power level at which this gain was measured was recorded as P_{1dB}.

For best power performance, discrete devices must be matched to the appropriate large signal impedances Γ_{GP} (at the input) and Γ_{LP} (at the load). These impedances are frequency, bias, and power level dependent. They are best obtained by direct measurement of the tuners used in the P_{1dB} setup described above, translating the measured tuner impedance back to the reference plane of the device. For bipolar devices, if measured large signal impedances are not available Γ_{GP} and Γ_{LP} may be estimated as follows.

Γ_{GP} is approximately equal to S_{11}*. Γ_{LP} can be obtained from the simple output model shown in Figure 6. This figure shows an equivalent circuit for the output of the transistor; this impedance should be matched to the system impedance (usually 50 Ω). For this model R is given by $(0.9\ V_{CE})\ 2/(8P_{OUT})$ for Class A operation where V_{CE} is the device collector to emitter voltage and P_{OUT} is the desired output power. C is approximately 1.5 C_{CB} (C_{CB} measured at $V_C/2$ is a slightly better determination). L depends on package style and is about 1 nH for microstripline packages and about 1.5 nH for larger power packages.[2]

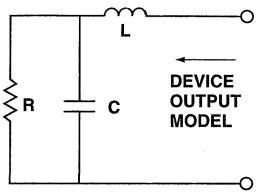


Figure 6. Large-Signal Load Model.

Thermal Resistance

Although a simple concept, the thermal resistance of a device is a complicated parameter that can be defined in several ways. It will vary with the operating temperature of the device being measured, the way in which the junction and case temperatures are specified, the bias point at which the device is operating, the presence or absence of an AC input signal to the device, and the environment.

Hewlett-Packard uses the following simple formula to define thermal resistance θ_{jc}:

$$\theta_{jc} = [T_J - T_C] / P_T$$

In this equation, T_J is the hottest junction or channel temperature on the device being measured. T_C is the case temperature if the device is a packaged component, or the temperature of the surface on which the device is mounted for an unpackaged die. P_T is the total power dissipated in the device, and is equal to the DC and RF power into the device minus the RF power out of the device.

There is also a thermal resistance θ_{ca} that characterizes the heat transfer between the case of the device and the ambient environment. Since this number depends at least as heavily on how the device is mounted, the surface (heatsink) it is mounted on, air flow and near-by heat sources as it does on the device itself, values for θ_{ca} are not included in this catalog.

A variety of measurement techniques exist for determining values for θ_{jc} Hewlett-Packard's preferred method is the liquid crystal technique[3], as it has the required 1 to 2 μm resolution needed for measuring the small device structures found in microwave devices. Although not used for any product in this catalog, infrared (IR) methods can be used in applications that do not require resolution below about 15 μm.

Several electrical methods also exist that rely on the measurement of a thermally sensitive parameter such as delta V_{BE} or delta V_{GS}, but have the drawback of providing an average as opposed to maximum junction temperature. Hewlett-Packard uses an electrical method[4] to

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[2] William Mueller, "Linear Amplifier Design — some General Considerations," *RF Design*, March 1980, pp. 37-41.

[3] K. J. Negus, R. W. Franklin, M. M. Yovanovich, "Thermal Modeling and Experimental Techniques for Microwave Bipolar Devices," IEEE Semiconductor Thermal and Temperature Measurement Symposium, Feb. 7-9, 1989, pp. 63-72.

[4] Ibid, pg 65.

determine the thermal resistance of plastic encapsulated transistors, which cannot be measured with methods requiring visual inspection of the die. The thermal resistance of plastic encapsulated MMICs is arrived at by combining separate determinations of die thermal resistance and package heat transfer characteristics.

In the liquid crystal method, the package lid is removed and the die surface is coated with a nematic liquid crystal layer. The active junction area is observed through a microscope having crossed linear polarizers in the incident and reflected light paths. Because of the change in optical properties at its melting point T_{NI} (nematic to isotropic transition), the liquid crystal regions of the die that are above and below the melting point can be visually identified. The device is biased and heated until the specified area exceeds the transition temperature and the thermal resistance is calculated from the measured T_{NI}, T_C, and P_T. Gallium Arsenide products are measured at a channel temperature of 150°C. Silicon products are measured at a junction temperature of +100°C. The θ_{jc} values in this data book for silicon products are specified at a case temperature of +25°C; a mathematical conversion is performed using model[5] based on the temperature dependent thermal resistance of the silicon die.

The case temperature T_C is determined by direct measurement with a small thermocouple. For devices in small signal packages with straight leads, the thermocouple is mounted as near as possible to the body of the case on the lead with the highest thermal conductivity path to the die. For plastic surface mount package with gull wing leads, the thermocouple is mounted to the bottom of the lead. This is the collector lead for silicon bipolar transistors, the output lead for MSA-series silicon MMICs and the ground lead for all other silicon MMICs and GaAs devices.

For hermetic surface mount packages with gull wing leads, the thermocouple is mounted to the bottom of the package. In power packages, the thermocouple is mounted on the flange (230 mil flange package) or on the bottom (200 mil BeO package) of the BeO disc. To determine the thermal resistance of an unpackaged die, the device is either mounted in a package with excellent thermal transfer properties (e.g. the 230 mil flange package), or on a ceramic die carrier.

For additional information on thermal resistance theory and measurements, contact Hewlett-Packard for available applications notes.[6, 7]

Device Modeling

Hewlett-Packard makes use of computer models to design high frequency transistors and to predict their performance in various applications. Both linear and non-linear models are used. Linear models apply at one specific set of (non-changing) bias and temperature conditions, and simulate small signal performance in the frequency domain. Non-linear models add the capability of predicting performance changes as a function of temperature or bias, and also allow for analysis of transient behavior. These models work in the time domain, and require much more data and computational time than do linear models.

Diode Models

Diode models are included on the individual data sheets.

Bipolar Transistor Models

Hewlett-Packard makes use of computer models to design high frequency transistors and to predict their performance in various applications. In general these models are non-linear time domain models based on the SPICE calculation engine. These models have the ability to predict small signal performance, distortion and noise perfromance, performance changes as a function of temperature or bias, and allow for analysis of transient behavior. In general these models can be relied on to predict trends in performance, but are not sufficiently accurate to predict limits of performance. For predictions of limits it is recommended that the designer defer to measured data. For predictions of linear performance, s parameter characterizations in general provide more accurate results than do SPICE models.

Most of Hewlett-Packard's bipolar transistors have been modeled using a "distributed base" description. The SPICE program's transistor model (represented by Q in the accompanying schematics) is used to describe the intrinsic transistor function, and a transmission line structure of resistors (RB1, RB2, RB3) and

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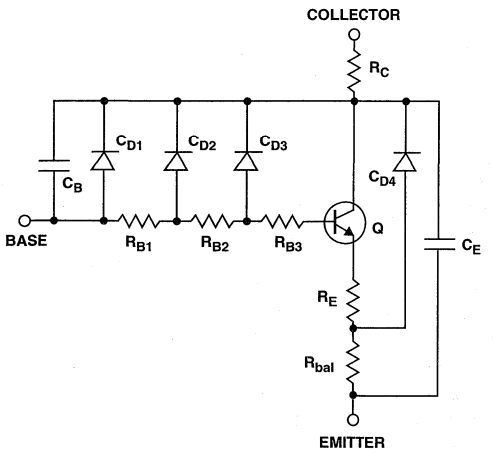
[5] Ibid, pg 67.

[6] Hewlett-Packard Transistor Primer III (Thermal Properties), publication ATP-1040.

[7] Hewlett-Packard Transistor Primer III-A (Thermal Resistance), publication ATP-1072.

capacitors (CD1, CD2, CD3) is added to simulate the significant electrical length of the base region at microwave frequencies. Since base capacitance varies with bias voltage, a diode model (similar to a varactor model) is used to describe CD1, CD2, and CD3. Collector and emitter contact resistances are described by the parameters RC and RE. The power device model has an additional emitter ballast resistor Rbal, and a voltage variable output capacitance CD4. The model is completed by adding fixed bond pad capacitances (CE and CB). A schematic showing the equivalent circuit corresponding to this "distributed base" model appears in Figure 1. Table 1 lists the values of the circuit elements corresponding to this model by die type.

HP CMCD uses one basic fabrication process to manufacture the bipolar transistors described here. This allows a basic set of SPICE parameters to be used in all the "distributed base" models, requiring only scaling to describe variations in device size. Changes in epi material between the small signal transistors and the power devices do, however, result in changes in values for the parameters BF, VAF, TF, and PTF. To facilitate the use of a "process description" set of parameters, a "unit transistor" is defined for each kind of device. QDIS describes a "unit" small signal transistor, QPWR describes a "unit" power device. The nonlinear base capacitances are built up from a "unit diode" (really a "unit voltage variable capacitor") model DMOD in a similar fashion.



C_{D1}, C_{D2}, C_{D3} use a diode model to represent voltage variable capacitance in the base.

Both diode and transistor models are scaled per unit area; the number of such unit areas needed is given (in # units) in Table 1.

R_{bal} (ballast resistance) and C_{D4} (voltage variable output capacitance) appear only in the model for power devices.

Figure 1. Discrete Transistor SPICE Equivalent Circuit.

Product chip level models are constructed from an appropriate number of these unit blocks by using the scaling capability available in most versions of SPICE. The value given in # units for Q, CD1, CD2, CD3, and CD4 in Table 1 is the number of "unit transistors" or "unit diodes" (i.e. the scaling factor) needed in the completed SPICE model. The values for the SPICE parameters describing these "unit transistors" and "unit diodes" are listed in Table 2. Table 3 is an example PSPICE netlist for the AT-41511 transistor based on this "distributed base" model.

The "distributed base" model was not used to describe the AT-305, AT-310, and AT-320 transistors. Conventional "collapsed" models are provided for these devices in SPICE netlist format. These listings appear in Table 4. A "collapsed" model for the AT-415 transistor also appears in Table 4.

The above models are chip level models. To complete the device simulation, the appropriate package model must be added. The bond wires that connect the device chip to the package (or substrate in the case of chip use) must also be simulated, as they are NOT included in the above chip models.

The standard Hewlett-Packard package model treats the leads and internal metallization as transmission lines (T1, T2, and T3). Optionally, these transmission lines can be replaced by simple pi networks of shunt C, series L, shunt C (Cpi1, Cpi2, Cpi3, Lpi1, Lpi2, Lpi3). Coupling capacitances between the device terminals are included (CEB, CBC, CEC), as are the emitter and

Table 1. Bipolar SPICE Model Equivalent Circuit Element Values (Distributed Base Form).

Element	Name	Geometry:	41400	41500	42000	64000	Units
Resistors:	RB1	value	1.0	1.0	0.7	0.4	Ω
		temp coeff	0.8E-3	0.8E-3	0.8E-3	0.8E-3	pp°C
	RB2	value	3.1	3.1	2.2	1.2	Ω
		temp coeff	1.2E-3	1.2E-3	1.2E-3	1.2E-3	pp°C
	RB3	value	2.7	2.7	1.9	0.98	Ω
		temp coeff	1.8E-3	1.8E-3	1.8E-3	1.8E-3	pp°C
	RC	value	5	5	5	1.3	Ω
		temp coeff	0.6E-3	0.6E-3	0.6E-3	0.6E-3	pp°C
	RE	value	0.24	0.24	0.17	0.06	Ω
		temp coeff	0.6E-3	0.6E-3	0.6E-3	0.6E-3	pp°C
	Rbal	value	-	-	-	1.65	Ω
		temp coeff	-	-	-	0.8E-3	pp°C
Capacitors:	C_B	fixed	0.032	0.064	0.034	0.082	pF
	CD1	scaling	782	782	1051	2287	#
		model	DMOD	DMOD	DMOD	DMOD	
	CD2	scaling	629	629	899	4692	#
		model	DMOD	DMOD	DMOD	DMOD	
	CD3	scaling	365	365	522	1360	#
		model	DMOD	DMOD	DMOD	DMOD	
	C_E	fixed	0.032	0.064	0.034	0.108	pF
	CD4	scaling	-	-	-	1717	#
		model	-	-	-	DMOD	
Active Device:	Q	scaling	420	420	600	1560	#
		model	QDIS	QDIS	QDIS	QPWR	

Table 2. Bipolar Transistor SPICE Parameter Values.

Model Name:	**QDIS**	**QPWR**	Model Name:	**DMOD**
Model Type:	NPN	NPN	Model Type:	D
BF	100	75	IS	1 E-25
BR	5	5	CJO	2.45E-16
IS	1.65E-18	1.65E-1 8	VJ	.76
VAF (VA)	20	30	M	.53
TF	12PS	14PS	BV	45
CJE	1.8E- 15	1.8E- 15	IBV	1E-9
VJE (PE)	1.01	1.01		
MJE (ME)	.60	.60		
PTF	35	50		
XTB	1.818	1.818		
VTF	6	6		
ITF	.3MA	.3MA		
IKF (IK)	.100MA	.100MA		
XTF	4	4		
NF	1.03	1.03		
ISE	5E-15	5E-15		
NE	2.5	2.5		

Table 3. PSPICE AT-41511 Simulation Using the Distributed Base Model.

```
* PSPICE AT41511 MODEL
.options acct node abstol=10n nopage
.width out=80
*temp calculated from VccxIcx(Rjc)+Ta : [5Vx10mAx(550 C/W)+27C = 55C]
.temp 55
.probe
.ac     lin     6       .5ghz   3ghz
.dc     vbb     0.0     3       0.2
.dc     vcc     2.0     10.0    1.0
*sources, blocking capacitors, chokes, and terminations
vin     52      0       sin(0   100mv   1ghz)   ac      1
vbb     53      0       0.814
vcc     56      0       8
rrs     52      51      50
c_cs    51      50      1000pf
lli     50      53      1e4nh
xr      50      54      xr_41511
c_cout  54      55      1000pf
rrl     55      0       50
llo     54      56      1e4nh
*model for AT-41511
.subcktxr_41511         50      54
x_xr    50      54      at
.ends
*define package : SOT-143 (style 11) Cpi -Lpi description
.subcktat       40      49
l_l1    40      41      0.05nh
l_t1l   41      42      0.40nh
c_t1c1  41      0       0.11pf
c_t1c2  42      0       0.11pf
l_lb    42      43      0.5nh
c_cbe   42      44      0.04pf
x_q1    47      43      45      sub415
l_t2l   44      46      0.10nh
c_t2c1  44      0       0.06pf
c_t2c2  46      0       0.06pf
c_cec   44      47      0.01pf
l_le    45      44      0.25nh
l_l2    46      0       0.01nh
l_t3l   47      48      0.47nh
c_t3c1  47      0       0.13pf
c_t3c2  48      0       0.13pf
c_cbc   42      47      0.04pf
l_l3    48      49      0.05nh
.ends
*define AT-415 transistor chip subcircuit
.subcktsub415   10      14      17
r_rb1   10      11      r1      1
r_rb2   11      12      r2      1
r_rb3   12      13      r3      1
d_cd1   10      15      dmod    782
d_cd2   11      15      dmod    629
d_cd3   12      15      dmod    365
r_rc    14      15      rc      1
r_re    16      17      re      1
c_ce    15      17      0.064pf
c_cb    10      15      0.064pf
q_1     15      13      16      qdis    420
.ends
```

Table 3, continued. **PSPICE AT-41511 Simulation Using the Distributed Base Model.**

```
* include resistor and semiconductor model files
.inc res1.mod
.inc Qdis.mod
.end
* <Qdis.mod>
* include file for the semiconductor used in 41511_S.CIR
.MODEL DMOD D(IS=1E-25 CJO=2.45E-16 VJ=.76 M=.53 BV=45 IBV=1E-9)
.MODEL QDIS NPN(BF=100 BR=5 IS=1.65E-18 VA=20 TF=12PS CJE=1.8E-15
+ PE=1.01 ME=0.60 PTF=35 XTB=1.818MA VTF=6 ITF=.3MA IK=.100MA
+ XTF=4 NF=1.03 ISE=5E-15 NE=2.5)
* <res1.mod>
* include file for the resistors used in 41511_S.CIR
.model  rb1 res  (r=1.0  tc1=0.8e-3  tc2=0.0)
.model  rb2 res  (r=3.1  tc1=1.2e-3  tc2=0.0)
.model  rb3 res  (r=2.7  tc1=1.8e-3  tc2=0.0)
.model  rc res  (r=5  tc1=0.6e-3 tc2=0.0)
.model  re res  (r=0.24  tc1=0.6e-3  tc2=0.0)
```

Table 4. PSPICE Netlist for the AT-305, AT-310, AT-320 and AT-415 Transistors.

```
* AT-305
.SUBCKT AT305  1  2  3
Q1 1 2 3  X305
C_CE 1 3   0.03pf
C_CB 2 1   0.03pf
.MODEL X305 NPN      BF=100          IS=7.8E-17      VAF=20
+       BR=2.5       MJE=0.6         NF=1.03         PTF=25
+       TF=1.2E-11   CJE=1.1E-13     XTF=4           IKF=6.3E-03
+       VJE=1.01     ISE=2.4E-13     NE=2.5          VTF=6
+       XTB=1.818    ITF=1.4E-02     RB=38.49        RE=2.44
+       RC=61.57     CJC=5.1E-14     CJS=7.0E-14     XCJC=0.19
+       PS=0.80      MS=0.5          PC=0.76         MC=0.53
.ENDS AT305

* AT-310
.SUBCKT AT310  1  2  3
Q1 1 2 3  X310
C_CE 1 3   0.03pf
C_CB 2 1   0.03pf
.MODEL X310 NPN      BF=100          IS=1.6E-16      VAF=20
+       BR=2.5       MJE=0.6         NF=1.03         PTF=25
+       TF=1.2E-11   CJE=2.3E-13     XTF=4           IKF=1.3E-02
+       VJE=1.01     ISE=4.8E-13     NE=2.5          VTF=6
+       XTB=1.818    ITF=2.9E-02     RB=19.44        RE=1.22
+       RC=40.68     CJC=9.5E-14     CJS=1.0E-13     XCJC=0.20
+       PS=0.80      MS=0.5          PC=0.76         MC=0.53
.ENDS AT310
```

Table 4, continued. **PSPICE Netlist for the AT-305, AT-310, AT-320 and AT-415 Transistors.**

```
* AT-320
.SUBCKT AT320  1  2  3
Q1 1 2 3  X320
C_CE 1 3  0.03pf
C_CB 2 1  0.03pf
.MODEL X320 NPN      BF=100          IS=3.1E-16      VAF=20
+       BR=2.5       MJE=0.6         NF=1.03         PTF=25
+       TF=1.2E-11   CJE=4.6E-13    XTF=4           IKF=2.5E-02
+       VJE=1.01     ISE=9.5E-13     NE=2.5          VTF=6
+       XTB=1.818    ITF=5.7E-02     RB=9.78         RE=0.61
+       RC=35.97     CJC=1.8E-13     CJS=1.7E-13     XCJC=0.20
+       PS=0.80      MS=0.5          PC=0.76         MC=0.53
.ENDS AT320

* AT-415
.SUBCKT         AT41500 1 2 3
C_CE    1 3     .064pf
C_CB    2 1     .064pf
Q1 1 2 3        X41500
.MODEL  X41500  NPN  BF=100          IS= 4.2E-16     VAF=20
+       BR=2.5       MJE=0.6         NF=1.03         PTF=25
+       TF=1.2E-11   CJE=6.0E-13    XTF=4           IKF=3.4E-02
+       VJE=1.01     ISE=1.3E-12     NE=2.5          VTF=6
+       XTB=1.818    ITF=7.6E-02     RB=11.57        RE=0.40
+       RC=18.03     CJC=2.5E-13     CJS=2.3E-13     XCJC=0.20
+       PS=0.80      MS=0.5          PC=0.76         MC=0.53
.ENDS   AT41500
```

Table 5. Circuit Elements for Bipolar Package Models.

element	units	**00**	**10**	**11**	**20**	**33**	**35**	**70**	**85**	**86**
LB	nH	0.5	0.65	0.5	0.55	0.5	0.6	0.5	0.55	0.55
LE	nH	0.2	0.1	0.25	0.2	0.5	0.3	0.14	0.1	0.1
L1	nH	-	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.55
L2	nH	-	0.01	0.01	0.01	0.05	0.01	0.01	0.01	0.06
L3	nH	-	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.25
T1: Z	Ω	-	45	45	50	45	65	40	65	65
T1: l	mils	-	40	50	80	50	35	25	30	30
T1: k	-	-	7	5	4.8	5	7	7	9	9
alt T1: Cpi1	-		.100	0.11	.150	0.11	0.06	.070	0.06	0.06
alt T1: Lpi1	-		0.38	0.40	.730	0.40	0.49	0.22	0.48	0.48
T2: Z	Ω	-	35	30	25	45	30	20	30	30
T2: l	mils	-	10	20	25	40	15	5	10	10
T2: k	-	-	7	5	5.3	5	7	7	9	9
alt T2: Cpi2	-		0.03	0.06	0.10	0.09	0.05	0.03	0.04	0.04
alt T2: Lpi2	-		0.08	0.10	0.12	0.33	0.09	0.02	0.08	0.08
T3: Z	Ω	-	45	45	50	45	65	40	60	60
T3: l	mils	-	45	60	155	60	50	35	20	20
T3: k	-	-	7	5	4.8	5	7	7	9	9
alt T3: Cpi3	-		0.12	0.13	0.30	0.13	0.09	0.10	0.04	0.04
alt T3: Lpi3	-		0.42	0.47	1.35	0.47	0.67	0.30	0.03	0.03
CEB	pF	-	.03	.04	.04	.04	.01	.02	.02	.02
CEC	pF	-	.03	.01	.02	.01	.03	.01	.03	.03
CBC	pF	-	.05	.04	.02	.04	.02	.02	.03	.03

base bond wires (LE and LB). As the bottom (collector) of the transistor chip is typically die attached directly to the output lead metallization, there is usually no collector bond wire in the simulation. The package model is completed by adding small amounts of series inductance (L1, L2, L3) to each device terminal, to simulate the short lengths of lead that occur between circuit and device package. The completed package model is shown schematically in Figure 2. Values for model elements are given in Table 5.

The style 23 package used for power devices has a different topology from the other packages. It can also incorporate an input matching capacitor (CIN). The equivalent circuit for this package is shown in Figure 3. The associated values shown are for the AT-64023 device. The style 63 package is used for the AT-32063 dual transistor. The model for this device is given in Table 6.

For models of HP's power transistors, please refer to the individual data sheets.

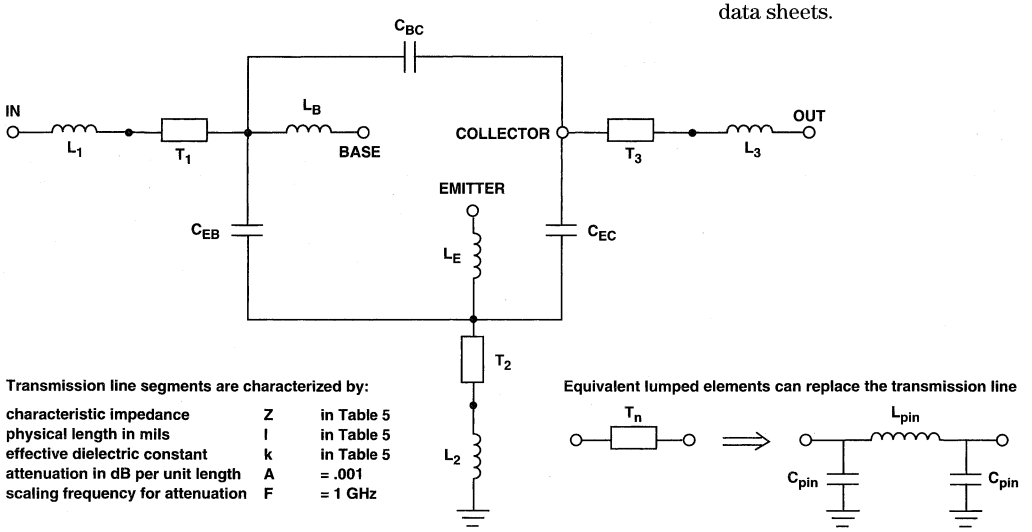
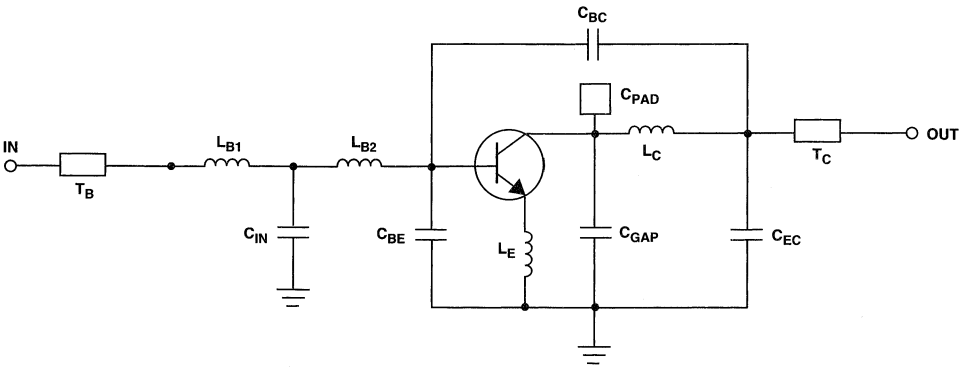


Figure 2. Bipolar Transistor Package Model Equivalent Circuit.



T_B: Z0 = 40 Ω L = 100 mils k = 10 A = .001 F = 1
L_{B1}: L = 35 nH
C_{IN}: C = 3.0 pF
L_{B2}: L = .2 nH
L_E: L = .1 nH
C_{PAD}: Z0 = 25 Ω L = 100 mils k = 6.8 A = .001 F = 1
L_C: L = .4 nH
T_C: Z0 = 40 Ω L = 80 mils k = 10 A = .001 F = 1
C_{BC}: C = .03 pF
C_{EC}: C = .03 pF
C_{EB}: C = .03 pF
C_{GAP}: C = .1 pF

Figure 3. Package Equivalent Circuit for AT-64023.

Table 6. AT Package Style 63 (SOT-363 or SC-70) Model.

SPICE model for AT320 dual in style 63 package

```
*Terminal connections: C1 B1 E1 C2 B2 E2
.SUBCKT AT32063  40  10 20  30  60  50
* "63" PACKAGE MODEL
* Lead inductances
L1    10    12    .70NH
L2    20    22    .70NH
L3    30    32    .70NH
L4    40    42    .70NH
L5    50    52    .70NH
L6    60    62    .70NH
*Parasitic capacitances
C1    12    0     .03PF
C2    22    0     .03PF
C3    32    0     .03PF
C4    42    0     .03PF
C5    52    0     .03PF
C6    62    0     .03PF
* Bond wire / internal lead frame inductances
LB1   12    13    .5NH
LB2   22    23    .5NH
LB3   32    33    .05NH
LB4   42    43    .05NH
LB5   52    53    .5NH
LB6   62    63    .5NH
*Coupling capacitances
C12   12    22    .14PF
C23   22    32    .14PF
C45   42    52    .14PF
C56   52    62    .14PF
* INSERT DIE MODELS
XAT320 43  13  23  AT320
XAT320 33  63  53  AT320

.ENDS

* DIE MODEL
.SUBCKT AT320  100    101     102
CBBP   101    100    .03PF   ; BASE BOND PAD CAPACITANCE
CEBP   102    100    .03PF   ; EMITTER BOND PAD CAPACITANCE
QINT   100    101    102     Q320
.ENDS
.MODEL  Q320    NPN (BF=100, BR=2.5, IS=3.1E-16, VA=20, TF=12PS,
+           CJE=4.6E-13, VJE=1.01, MJE=0.6, PTF=25, XTB=1.818,
+           VTF=6, ITF=5.7E-2, IKF=2.5E-2, XTF=4, NF=1.03, ISE=9.5E-13,
+           NE=2.5, RB=9.78, RE=0.61, RC=35.97, CJC=1.8E-13, CJS=1.7E-13,
+           XCJC=0.20, PS=0.8, MS=0.5, PC=0.76, MC=0.53)
```

FET Models

In general only linear models are available for the small signal GaAs FETs included in this catalog. These models are simplified hybrid pi models. In this model, the intrinsic FET consists of a voltage controlled current source (gm Vc), a capacitance (Cgs) across which the controlling voltage appears, and an input resistance (Rc). Terminal contact resistances (Rg, Lg, Rs) and parasitic inductances (Ls, Ld) are added to this structure. Included in the values for Lg, Ls, and Ld are both the inductance of the on-chip traces and the bond wire inductances used for carrier measurements. The drain resistance (Rd) is sufficiently low in value that it does not influence the S-parameters or noise performance in the frequency range where the model is applicable (up to approximately 20 GHz), consequently it does not appear in the model. The gate-to-drain coupling capacitance (Cgd), which is the predominant determiner of S12, and the output capacitance (Cds) complete the model. The schematic of the FET model equivalent circuit is shown in Figure 1. Component values for both low noise and gain bias are given in Table 1.

The topology derived for the bipolar package model can also be applied to GaAs FET packages, with one additional element being required. Since the bottom of the bipolar die is also the output terminal, bipolars in general do not require output (collector) bond wires. In contrast, the bottom of a GaAs FET is either electrically isolated or connected to the common terminal, so an output (drain) bond wire (Ld) is required. The consequent differences in metallization patterns means that although the model topology stays the same, the values of the model elements change. Thus, even though a FET package may have the same external appearance and numeric designation as bipolar package, it will have different values for its equivalent circuit elements - a FET style 70 package model will not be the same as a bipolar style 70 package model. For convenience, the package model is repeated in Figure 2 with the appropriate labels for a GaA FET. Values for this model are listed in Table 2 for the various FET package styles. Modified values of Ld, Lg, and Ls are included for each package type. When modeling a packaged die, use the values for Ld, Lg, and Ls from Table 2 and omit the parameters Ld, Lg, and Ls from Table 1.

A non-linear model is available for the ATF-36 series PHEMT die in the form of Statz model parameters. This model is only valid for small signal operation. The parameter values are given in Table 3.

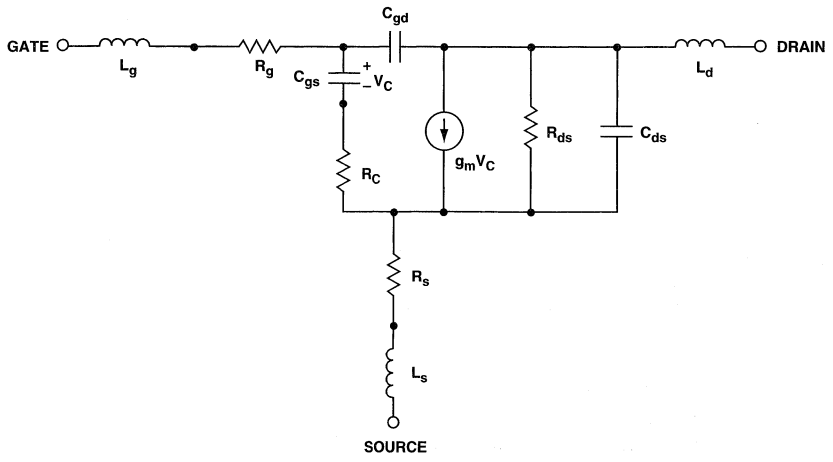


Figure 1. Equivalent Circuit for Linear GaAs FET Models.

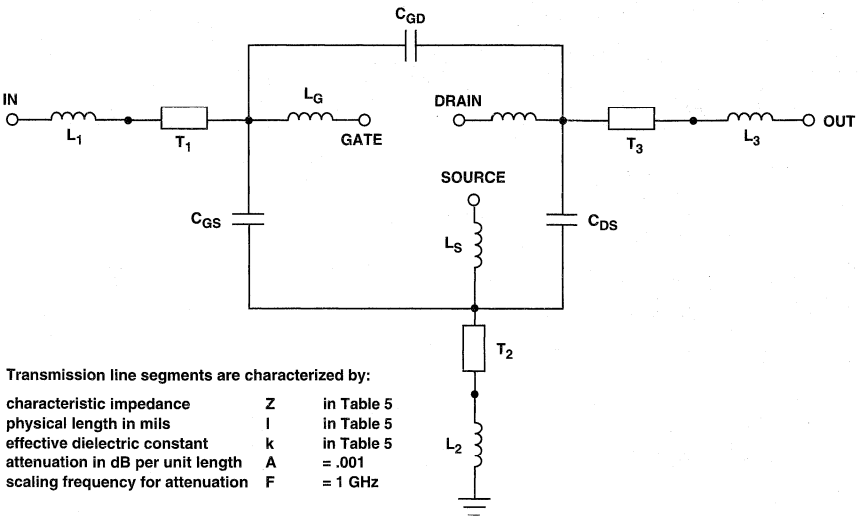


Figure 2. FET Transistor Package Equivalent Circuit.

Table 1. Circuit Element Values for Linear GaAs FET Models.

	Components											
Part No., Bias	**Lg nH**	**Ld nH**	**Ls nH**	**Rd Ω**	**Rg Ω**	**Rs Ω**	**Cgs pF**	**Cgd pF**	**Cde pF**	**gm mS**	**TF ps**	**Rds Ω**
ATF-101XX												
2 V, 20 mA	0.9	0.6	0.15	2.0	2.5	2.0	0.25	0.1	0.1	70	0.001	200
ATF-102XX												
2 V, 20 mA	0.9	0.6	0.15	2.0	2.5	2.0	0.40	0.1	0.1	60	0.001	200
ATF-107XX												
2 V, 20 mA	0.9	0.6	0.15	2.0	3.0	2.0	0.40	0.15	0.1	60	0.001	200
4 V, 70 mA	0.9	0.6	0.15	4.0	6.0	2.0	0.80	0.1	0.2	130	0.001	200
ATF-131/132XX												
3 V, 20 mA	0.9	0.6	0.15	2.0	3.0	0.5	0.14	0.05	0.03	60	0.001	250
ATF-133/134XX												
3 V, 20 mA	0.9	0.6	0.15	2.0	3.0	0.5	0.20	0.05	0.03	40	0.001	250
ATF-137XX												
3 V, 20 mA	0.9	0.6	0.15	2.0	3.0	2.0	0.20	0.05	0.03	40	0.001	250
4 V, 20 mA	0.9	0.6	0.15	4.0	3.0	2.0	0.24	0.05	0.03	50	0.001	250
ATF-211XX												
3 V, 30 mA	0.4	0.5	0.15	1.5	1.5	1.0	0.70	0.10	0.14	68	0.001	180
6 V, 80 mA	0.4	0.5	0.15	1.0	1.0	0.5	1.2	0.08	0.15	115	0.001	180
ATF-251XX												
3 V, 20 mA	0.4	0.7	0.15	2.0	2.5	1.0	0.36	0.07	0.16	48	0.001	150
5 V, 50 mA	0.4	0.7	0.15	1.0	2.0	0.5	0.60	0.06	0.08	75	0.001	180
ATF-261XX												
3 V, 10 mA	0.6	0.7	0.15	2.0	5.0	5.0	0.16	0.03	0.06	27	0.001	275
5 V, 30 mA	0.6	0.7	0.15	2.0	5.0	5.0	0.26	0.015	0.06	42	0.001	275
ATF-35XXX												
1.5 V, 10 mA	29.4 pH	26.6 pH	5 pH	5.0	1.0	0.5	0.088	0.0459	0.0527	53.7	0.47	105.1
ATF-441XX												
9 V, 500 mA	0.20	0.20	0.03	0.15	0.02	0.16	3.0	0.3	1.35	350	5	15
ATF-451XX												
9 V, 250 mA	0.20	0.20	0.06	0.30	0.75	0.32	1.5	0.2	0.70	175	5	.0
ATF-461XX												
9 V, 125 mA	0.20	0.20	0.1	0.60	1.60	0.60	0.8	0.1	0.35	80	5	55

Table 2. Circuit Element Values for FET Package Models.

element	units	35/36	70	77	84	86
LG	nH	0.9	0.5	0.9	0.5	0.5
LD	nII	0.6	0.5	0.6	0.5	0.5
LS	nH	0.15	0.15	0.15	0.15	0.15
L1	nH	.01	.01	.01	.01	.5
L2	nH	.005	.005	.005	.005	.05
L3	nH	.01	.01	.01	.01	.2
T1: Z	W	65	40	65	65	65
T1: l	mils	35	25	35	25	25
T1: k	-	7	7	7	9	9
T2: Z	W	30	20	30	30	30
T2: l	mils	15	5	15	7	7
T2: k	-	7	7	7	9	9
T3: Z	W	65	40	65	65	65
T3: l	mils	35	25	35	25	25
T3: k	-	7	7	7	9	9
CGS	pF	.05	.05	.05	.03	.03
CDS	pF	.05	.05	.05	.05	.05
CGD	pF	.005	.005	.005	.01	.01

Note: Both the die and package models include inductance values for the gate, drain, and source bond wires (Ld, Lg, Ls). When placing the die model in a package model, use the bond wire value given in the package description and omit the values given in the die model.

Table 3. ATF-36 FET Statz Model Parameters for Small Signal Operation.

MODEL=FET

IDS model	Gate model	Parasitics	Breakdown	Noise
NFET=yes	DELTA=0.2	RG=1	GSFWD=1	FNC=01e+6
PFET=	GSCAP=3	RD=0.5	GSREV=0	R=0.17
IDSMOD=3	CGS=0.13 pF	RS=0.5	GDFWD=1	P=0.55
VTO=-0.55	GDCAP=3	LG=0.03 nH	GDREV=0	C=0.2
BETA=0.10	CGD=0.04 pF	LD=0.04 nH	VJR=1	
LAMBDA=0.25		LS=0.01 nH	IS=1 nA	
ALPHA=5.0		CDS=0.05 pF	IR=1 nA	
B=1.5		CRF=0.1	IMAX=0.1	
TNOM=27		RC=350	XTI=	
IDSTC=			N=	
VBI=0.7			EG=	

Integrated Circuit Device Modeling

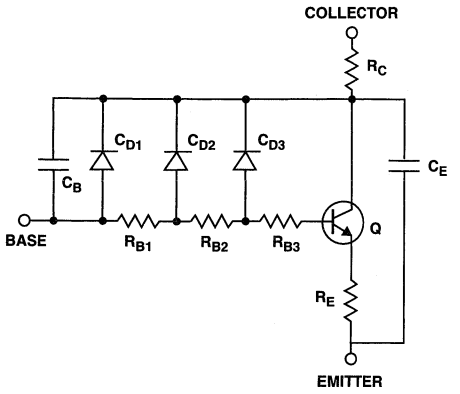
Hewlett-Packard makes use of computer models when designing our high frequency integrated circuits. In general these models are non-linear, time domain models based on SPICE. For linear designs, the small signal s and noise parameters provided on individual product data sheets (also available from Hewlett Packard on diskette - request our DesignPak, publication number 5963-2301E) are the most accurate and easiest to use device description. However, for indications of changes in performance as a function of bias or temperature, or for investigation of distortion, transient response, or other non-linear parameters, the non-linear design models can be useful.

MSA RFIC Models

The MSA series are some of the simplest RFICs built by Hewlett Packard. They consist of two bipolar transistors in a Darlington connection, embedded in a network of resistors to provide both feedback and DC bias. Since all active devices are collector-connected, these devices can be fabricated using HP's standard SAT "discrete transistor" process—isolation of the collectors is not required. Models for these consist of two active device models (Q1 and Q2), values for the feedback resistors (RE and RF), values for the bias resistors (RB and Rbias), and the parasitic capacitors (Cp1, Cp2, Cp3, and CF) associated with the structure.

The transistor model used takes the form described in detail in the Transistor Models section. The corresponding schematic is given in Figure 1. Note that no CB or CE elements exist in the device simulations incorporated in the MODAMP device models as the bond pad capacitances are included at the RFIC level. The interconnection for these elements is shown schematically in Figure 3. Some MSA RFICs (the MSA-05, MSA-09, MSA-10, and MSA-11 series) require DC blocking capacitors in series with the shunt feedback resistor to prevent excess power dissipation on the chip. A schematic for this kind of MSA RFIC is shown in Figure 1. Tables 1 and 2 give the value of the model elements of both kinds of MSA RFICs. SPICE parameters for the "unit transistor" description (QMSA) corresponding to the MSA RFIC fabrication process are included in Table 3. Individual device models are constructed using an appropriate number of these unit blocks: The non-linear base capacitances are built up from a "unit diode" model (DMOD) in a similar fashion. The number in parenthesis in the columns labeled Q, CD1, CD2, GD3, and CD4 in Tables 1 and 2 are the number of unit transistors or unit diodes needed in the completed SPICE model.

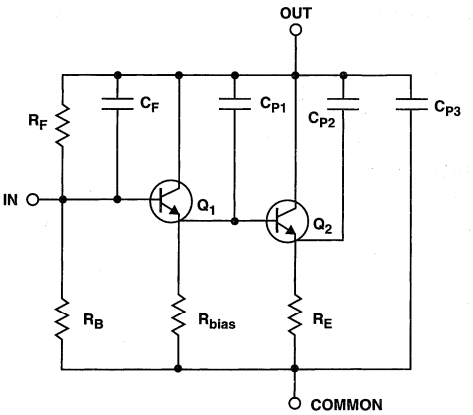
The above models are chip level models. To complete device simulations, appropriate package models must be added. The bond



C_{D1}, C_{D2}, C_{D3} use a diode model to represent voltage variable capacitance in the base.

Both diode and transistor models are scaled per unit area; the number of such unit areas needed is given (in # units) in Table 1.

Figure 1. Discrete Transistor SPICE Equivalent Circuit.



Note that Q_1 and Q_2 are active devices, and each represents a discrete transistor simulation of the kind described above.

Figure 2. MODAMP RFIC Equivalent Circuit.

wires that connect the device chip to the package (or substrate in the case of chip use) must also be simulated, as they are NOT included in the above chip models.

The standard Hewlett-Packard package model treats the leads and internal metallization as transmission lines (T1, T2, and T3). Coupling capacitances between the device terminals is included (CEB, CBC, CEC), as are the emitter and base bond wires (LE. and LB). As the bottom (collector) of the transistor chip is typically die attached directly to the output lead metallization, there is usually no collector bond wire in the simulation. The package model is completed by adding small amounts of series inductance (L1, L2, L3) to each device terminal, to simulate the short lengths of lead that occur between circuit and device package. The completed package model is shown schematically in Figure 4. Values for model elements are given in Table 4.

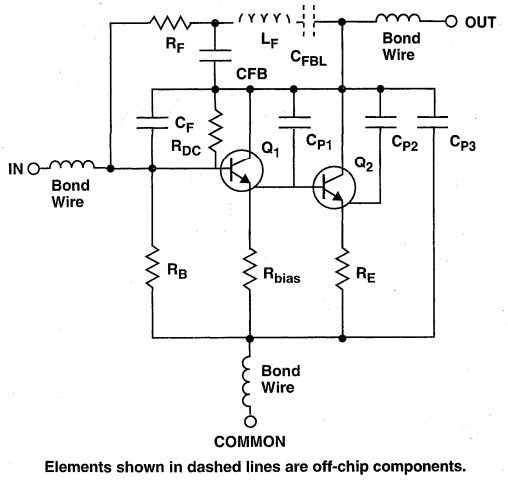


Figure 3. Equivalent Circuit for MSA RFICs with DC Blocking Capacitor in Feedback Path.

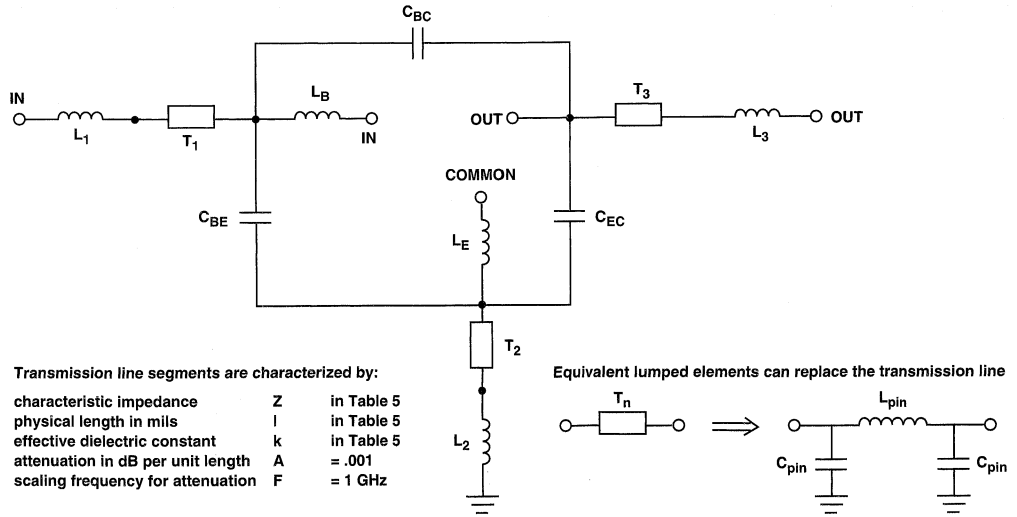


Figure 4. MSA RFIC Package Equivalent Circuit.

Table 1 MSA RFIC SPICE Models.

		Geometry:	**A01**		**A02**		**A03**		**A04**		
Element	Name		**Q1**	**Q2**	**Q1**	**Q2**	**Q1**	**Q2**	**Q1**	**Q2**	Units
Resistors:	RB1	value	5.0	3.1	5.0	2.5	3.1	1.7	1.7	1.0	Ω
		temp coeff	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	pp°C
	RB2	value	13.2	8.2	13.2	6.6	8.2	4.4	4.4	2.6	Ω
		temp coeff	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	pp°C
	RB3	value	9.9	6.2	9.9	5.0	6.2	3.3	3.3	2.0	Ω
		temp coeff	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	pp°C
	RC	value	5	5	5	5	5	5	5	5	Ω
		temp coeff	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	pp°C
	RE	value	0.78	0.49	0.78	0.39	0.449	0.26	0.26	0.16	Ω
		temp coeff	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	pp°C
Capacitors:	CD1	scaling	348	478	348	564	478	780	780	1204	#
		model	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	
	CD2	scaling	390	624	390	780	624	1170	1131	1885	#
		model	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	
	CD3	scaling	114	182	114	228	182	342	331	551	#
		model	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	
Active Device:	Q	scaling	125	200	125	250	200	375	375	625	#
		model	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA	
Resistors:	RF	value	550		330		330		11		Ω
	RE	value	0		5		6.86		11		Ω
	RB	value	245		156		170		122		Ω
	RBIAS	value	250		167		190		134		Ω
		temp coeff	-0.8E-3		-0.8E-3		-0.8E-3		-0.8E-3		pp°C
Capacitors:	CF	value	.12		.12		.12		.12		pF
	CP1	value	.033		.033		.033		.033		pF
	CP2	value	-		-		-		-		pF
	CP3	value	.103		.103		.103		.103		pF

Table 1, continued. **MSA RFIC SPICE Models.**

		Geometry:	**A06**		**A07**		**A08**		**A20**		**A31**		
Element	Name		**Q1**	**Q2**	**Q1**	**Q2**	**Q1**	**Q1**	**Q1**	**Q2**	**Q1**	**Q2**	Units
Resistors:	RB1	value	0.95	0.95	1.5	1.2	2.6	1.0	2.42	1.48	2.42	1.48	Ω
		temp coeff	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	pp°C
	RB2	value	3.26	3.26	4.4	3.1	9.1	3.3	7.45	4.47	7.45	4.47	Ω
		temp coeff	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	pp°C
	RB3	value	2.83	2.83	3.8	2.7	7.9	2.8	6.25	3.75	6.25	3.75	Ω
		temp coeff	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	pp°C
	RC	value	10	10	10	10	5	5	5	5	5	5	Ω
		temp coeff	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	pp°C
	RE	value	0.22	0.22	0.33	0.24	0.63	0.22	0.55	0.33	0.55	0.33	Ω
		temp coeff	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	pp°C
Capacitors:	CD1	scaling	782	782	602	782	377	782	292	432	292	432	#
		model	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	
	CD2	scaling	609	609	450	629	218	609	292	486	292	486	#
		model	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	
	CD3	scaling	386	386	261	365	138	385	146	243	146	243	#
		model	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	
Active Device:	Q	scaling	438	438	300	420	156	438	180	300	180	300	#
		model	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA	
Resistors:	RF	value	600		360		6000		670		1115		Ω
	RE	value	0		6		0		2.9		0		Ω
	RB	value	480		244		1600		75		75		Ω
	RBIAS	value	157		215		85		350		570		Ω
		temp coeff	-0.8E-3		-0.8E-3		-0.8E-3		-0.8E-3		-0.8E-3		pp°C
Capacitors:	CF	value	.083		.067		-		0.04		0.06		pF
	CP1	value	.019		.020		.086		0.05		0.05		pF
	CP2	value	.010		.045		.021		0.15		0.25		pF
	CP3	value	.085		.104		.134		0.25		-		pF

Table 2. MSA RFICs with DC Blocked Shunt Feedback SPICE Models.

		Geometry:	**A05**		**A09**		**A10**		**A11**		
Element	Name		**Q1**	**Q2**	**Q1**	**Q2**	**Q1**	**Q2**	**Q1**	**Q2**	Units
Resistors:	RB1	value	1.26	0.91	2.6	1.0	0.9	0.7	0.42	0.67	Ω
		temp coeff	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	pp°C
	RB2	value	2.15	1.07	9.1	3.3	1.1	0.6	1.42	2.3	Ω
		temp coeff	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	pp°C
	RB3	value	1.56	0.78	7.9	2.8	0.8	0.4	1.24	2.0	Ω
		temp coeff	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	pp°C
	RC	value	5.87	3.00	5	5	2.7	1.24	5	5	Ω
		temp coeff	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	pp°C
	RE	value	0.14	0.07	0.63	0.22	0.7	0.3	0.10	0.16	Ω
		temp coeff	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	pp°C
	Rbal	value	2.75	1.38	-	-	1.38	0.69	-	-	Ω
		temp coeff	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	pp°C
Capacitors:	CD1	scaling	1267	2354	377	782	2354	4530	1591	1051	#
		model	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	
	CD2	scaling	2380	4760	218	609	4750	9520	1392	870	#
		model	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	
	CD3	scaling	612	1224	138	385	1224	2448	882	551	#
		model	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	
	CD4	scaling	1717	1717	-	-	1717	1717	-	-	#
		model	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	DMOD	
Active Device:	Q	scaling	720	1440	156	438	1440	2880	1000	625	#
		model	QPWR	QPWR	QMSA	QMSA	QPWR	QPWR	QMSA	QMSA	
Resistors:	RF	value	210		150		120		300		Ω
	RE	value	15		12		8.73		10		Ω
	RB	value	800		2000		270		2400		Ω
	RBIAS	value	50		115		25		80		Ω
	RDC	value	2000		6000		900		4000		Ω
	for above	temp coeff	-0.8E-3		-0.8E-3		-0.8E-3		-0.8E-3		pp°C
Capacitors:	CF	value	.26		.114		.33		.10		pF
	CPFB	value	-		.058		-		.058		pF
	CP1	value	.274		.020		.52		.050		pF
	CP2	value	.150		.023		.230		.080		pF
	CP3	value	.496		.168		.790		.120		pF
	CFBL	value	45		45		80		200		pF
Inductors:	LF	value	0.35		0.35		1.00		0.35		nH

Table 3. MSA RFIC SPICE Parameter Values.

Model Name:	**QMSA**	**QPWR**	Model Name:	**DMOD**
Model Type:	NPN	NPN	Model Type:	D
BF	90	75	IS	1 E-25
BR	5	5	CJO	2.45E-16
IS	1.65E-18	1.65E-1 8	VJ	.76
VAF (VA)	20	30	M	.53
TF	12PS	14PS	BV	45
CJE	1.8E- 15	1.8E- 15	IBV	1E-9
VJE (PE)	1.01	1.01		
MJE (ME)	.60	.60		
PTF	25	50		
XTB	1.818	1.818		
VTF	6	6		
ITF	.3MA	.3MA		
IKF (IK)	.133MA	.100MA		
XTF	4	4		
NF	1.03	1.03		
ISE	5E-15	5E-15		
NE	2.5	2,5		

Table 4. Circuit Elements for MSA RFIC Package Models.

element	units	**00**	**04**	**05**	**10**	**11**	**20**	**35/36**	**70**	**85**	**86**
LB	nH	0.5	0.6	0.6	0.65	0.5	0.55	0.6	0.5	0.55	0.55
LE	nH	0.2	0.2	0.2	0.1	0.25	0.2	0.3	0.14	0.1	0.1
L1	nH	-	0.05	0.15	0.05	0.05	0.05	0.05	0.05	0.05	0.55
L2	nH	-	0.01	0.06	0.01	0.01	0.01	0.01	0.01	0.01	0.06
L3	nH	-	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.25
T1: Z	Ω	-	55	55	45	45	50	65	40	65	65
T1: l	mils	-	80	80	40	50	80	35	25	30	30
T1: k	-	-	9	9	7	5	4.8	7	7	9	9
alt T1: Cpi1	-		.189	.189	.100	0.11	.150	.061	.070	.059	.059
alt T1: Lpi1	-		1.083	1.083	.401	0.40	.730	.507	.224	.493	.493
T2: Z	Ω	-	25	25	35	30	25	30	20	30	30
T2: l	mils	-	30	30	10	20	25	15	5	10	10
T2: k	-	-	9	9	7	5	5.3	7	7	9	9
alt T2: Cpi2	-		.153	.153	.032	0.06	.098	.055	.019	.042	.042
alt T2: Lpi2	-		.190	.190	.078	0.10	.122	.098	.034	.076	.076
T3: Z	Ω	-	55	55	45	45	50	65	40	60	60
T3: l	mils	-	60	60	45	60	155	50	35	20	20
T3: k	-	-	9	9	7	5	4.8	7	7	9	9
alt T3: Cpi3	-		.140	.140	.113	0.13	.297	.087	.098	.039	.039
alt T3: Lpi3	-		.824	.824	.450	0.47	1.346	.721	.312	.330	.330
CEB	pF	-	.03	.03	.03	.04	.04	.01	.02	.02	.02
CEC	pF	-	.04	.04	.03	.01	.02	.03	.01	.03	.03
CBC	pF	-	.04	.04	.05	.04	.02	.02	.02	.03	.03

Table 5 Typical PSPICE MSA-0311 Simulation.

```
* MSA-0311 MODEL
* "11" PACKAGE MODEL
.SUBCKT MSA0311 OUT    IN     GND
LL1    IN     25     .05NH
C1T1   25     0      .11PF
LT1    25     30     .40NH
C2T1   30     0      .11PF
LLB    30     DIEIN  .5NH
CCEB   30     50     .04PF
LL2    GND    45     .01NH
C1T2   45     0      .06PF
LT2    45     50     .10NH
C2T2   50     0      .06PF
LLE    50     DIEGND .25NH
CCEC   50     DIEOUT .01PF
LL3    OUT    65     .05NH
C1T3   65     0      .13PF
LT3    65     DIEOUT .47NH
C2T3   DIEOUT 0      .13PF
CCBC   30     DIEOUT .04PF
* CALL DIE MODEL
XA03DIE DIEOUT  DIEIN   DIEGND  MSA03
.ENDS
.SUBCKT MSA03  DIEOUT DIEIN  DIEGND
RF     DIEIN  DIEOUT 330   (TC1=-0.8E-3)
RB     DIEIN  DIEGND 170   (TC1=-0.8E-3)
RBIAS  Q1E    DIEGND 190   (TC1=-0.8E-3)
RE     Q2E    DIEGND 6.86  (TC1=-0.8E-3)
CF     DIEIN  DIEOUT 0.12PF
CP1    Q1E    DIEOUT 0.033PF
CP3    DIEGND DIEOUT 0.103PF
XA03Q1 DIEOUT DIEIN  Q1E    A03Q1
XA03Q2 DIEOUT Q1E    Q2E    A03Q2
.ENDS
.SUBCKT A03Q1  Q1C    Q1B    Q1E
RB1    Q1B    20     3.1    (TC1=0.8E-3)
RB2    20     30     8.2    (TC1=1.2E-3)
RB3    30     40     6.2    (TC1=1.8E-3)
RE     50     Q1E    0.49   (TC1=0.6E-3)
RC     60     Q1C    5      (TC1=0.6E-3)
Q1     60     40     50     QMSA   200
DCD1   Q1B    60     DMOD   478
DCD2   20     60     DMOD   624
DCD3   30     60     DMOD   182
.ENDS
.SUBCKT A03Q2  Q1C    Q1B    Q1E
RB1    Q2B    20     1.7    (TC1=0.8E-3)
RB2    20     30     4.4    (TC1=1.2E-3)
RB3    30     40     3.3    (TC1=1.8E-3)
RE     50     Q1E    0.26   (TC1=0.6E-3)
RC     60     Q1C    5      (TC1=0.6E-3)
Q1     60     40     50     QMSA   375
DCD1   Q2B    60     DMOD   780
DCD2   20     60     DMOD   1170
DCD3   30     60     DMOD   342
.ENDS
```

INA Series RFIC Models

INA series RFICs are more complex than MSA series devices, and require the use of an isolated collector fabrication process (ISOSAT). The design models for some of the devices from the INA series of amplifiers follow.

At the heart of the model are the SPICE parameters listed in Table 3. The equations built into the SPICE program use these values to describe how the intrinsic semiconductors function. The SPICE intrinsic transistor description is then used with the equivalent circuit shown in Figure 1 to accurately portray a semiconductor device with electrically significant base length operating at microwave frequencies. Values for the other components in this equivaent circuit are listed in Table 2. Note that in this equivalent circuit, non-linear capacitance versus voltage characteristics are modeled using a diode model, which also has a set of SPICE parameters. Finally, the "spread base" models for the semiconductor devices are used in an equivalent circuit that describes the interconnections and circuit elements of the RFIC being modeled. This circuit is shown in Figure 2. Significant parasitics, such as the capacitance associated with the metalization areas, are also included, as are the bond wires. The component values are listed in Table 3.

The INA10 geometry is different from the INA01, INA02, and INA03 geometries. An equivalent circuit for the INA-10 is given in Figure 3. Values for the components appear in Table 2. SPICE parameter listings for the component transistors appear in Table 4. Note that the resistors on the INA-10 IC have a temperature coefficient of -0.8E-3 (model R1).

The user of these models should be aware that as device complexity increases, model accuracy decreases. HP recommends that these models be used to predict device trends in performance, and that actual performance values be determined through the testing of physical devices.

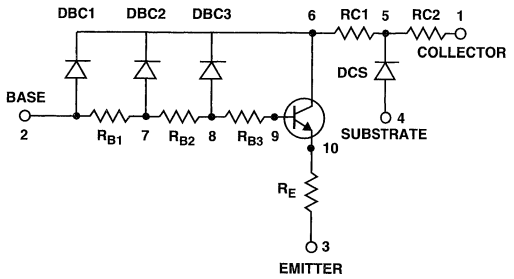


Figure 1. Discrete Transistor SPICE Equivalent Circuit.

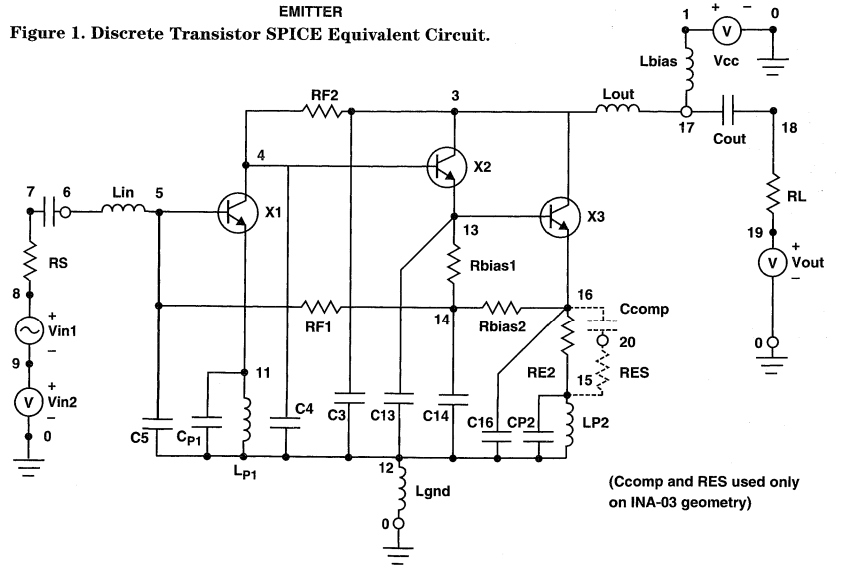


Figure 2. INA Series RFIC Equivalent Circuit.

The topology derived for the bipolar package model can also be applied to INA RFIC packages, with one additional element being required. Since the bottom of the bipolar die is also the output terminal, bipolars in general do not require output (collector) bond wires. In contrast, the bottom of INA RFICs is electrically isolated, so an output bond wire (Lout) is required. The consequent differences in metallization patterns means that although the model topology stays the same, the values of the model elements change. Thus, even though an INA RFIC package may have the same external appearance and numeric designation as a bipolar package, it will have different values for its equivalent circuit elements - an INA RFIC style 70 package model will not be the same as a bipolar style 70 package model. For convenience, the package model is repeated in Figure 4 with the appropriate labels for an INA RFIC. Values for this model are listed in Table 5 for the various INA RFIC package styles.

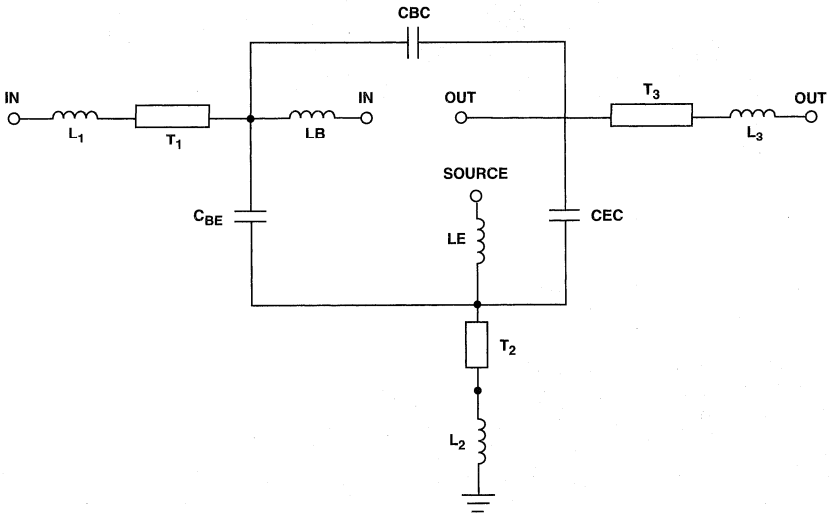


Figure 3. INA Series RFIC Package Equivalent Circuit.

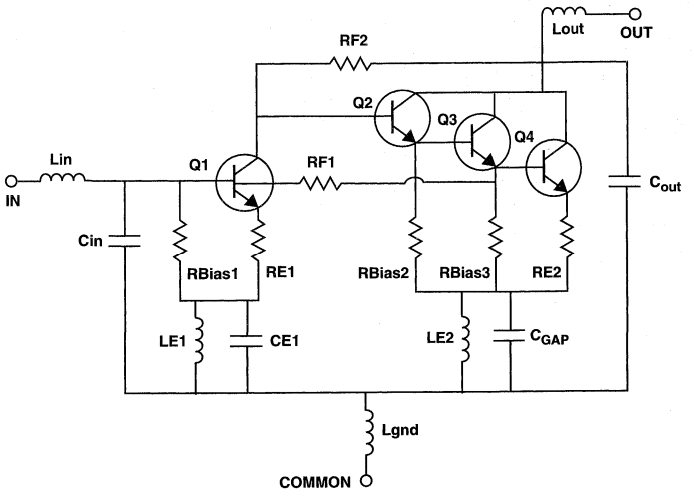


Figure 4. INA-10 Die Equivalent Circuit.

Table 1. INA Transistor Equivalent Circuit Values.

		INA-01			INA-02			INA-03		
element	model	X1	X2	X3	X1	X2	X3	X1	X2	X3
RC1	R2	10	10	9	8	10	9	6.5	5.5	7
RC2	R2	10	10	8	17	10	7	22.5	80	27
RB1	R3	1.1	1.1	1.2	1.8	1.1	1.2	2.4	8.4	3.6
RB2	R4	3.2	3.2	3.7	5.6	3.2	3.7	7.5	28	11.2
RB3	R5	2.7	2.7	3.1	4.7	2.7	3.1	6.3	23.5	9.4
RE	R2	0.24	0.28	0.28	0.42	0.24	0.28	0.55	2.1	0.83
Q1	Q	420	420	360	240	420	360	180	48	120
DBC1	D1	572	570	502	362	572	502	292	123	209
DBC2	D1	680	680	583	389	680	583	292	79	198
DBC3	D1	340	340	292	195	340	292	146	40	99
DCS	D2	2475	2475	2409	1683	2475	2409	1419	756	1092

Table 2. MODEL Statements for Active Devices used in the INA-10 Geometry.

```
.MODEL q1  NPN BF=   100   IS= 2.0E-16   VA=    20
+  BR=  2.5   ME=   0.6   NF=  1.03   PTF=    25
+  TF=1.2E-11   CJE= 2.9E-13   XTF=    4   IK= 1.6E-02
+  PE=  1.01   ISE= 6.0E-13   NE=   2.5   VTF=    6
+ XTB=  1.818   ITF= 3.6E-02   RB=  24.15   RE=   0.83
+  RC=  25.22   CJC= 1.2E-13   CJS= 1.5E-13   XCJC=   0.20
+  PS=  0.80   MS=   0.5   PC=  0.76   MC=   0.53

.MODEL q2  NPN BF=   100   IS= 2.4E-16   VA=    20
+  BR=  2.5   ME=   0.6   NF=  1.03   PTF=    25
+  TF=1.2E-11   CJE= 3.5E-13   XTF=    4   IK= 1.9E-02
+  PE=  1.01   ISE= 7.2E-13   NE=   2.5   VTF=    6
+ XTB=  1.818   ITF= 4.3E-02   RB=  20.15   RE=   0.69
+  RC=  22.80   CJC= 1.5E-13   CJS= 1.6E-13   XCJC=   0.20
+  PS=  0.80   MS=   0.5   PC=  0.76   MC=   0.53

.MODEL q3  NPN BF=   100   IS= 4.0E-16   VA=    20
+  BR=  2.5   ME=   0.6   NF=  1.03   PTF=    25
+  TF=1.2E-11   CJE= 5.8E-13   XTF=    4   IK= 3.2E-02
+  PE=  1.01   ISE= 1.2E-12   NE=   2.5   VTF=    6
+ XTB=  1.818   ITF= 7.2E-02   RB=  12.13   RE=   0.42
+  RC=  10.10   CJC= 2.3E-13   CJS= 2.1E-13   XCJC=   0.21
+  PS=  0.80   MS=   0.5   PC=  0.76   MC=   0.53

.MODEL q4  NPN BF=   100   IS= 9.9E-16   VA=    20
+  BR=  2.5   ME=   0.6   NF=  1.03   PTF=    25
+  TF=1.2E-11   CJE= 1.4E-12   XTF=    4   IK= 8.0E-02
+  PE=  1.01   ISE= 3.0E-12   NE=   2.5   VTF=    6
+ XTB=  1.818   ITF= 1.8E-01   RB=   4.86   RE=   0.17
+  RC=  13.15   CJC= 5.5E-13   CJS= 4.0E-13   XCJC=   0.22
+  PS=  0.80   MS=   0.5   PC=  0.76   MC=   0.53
```

Table 3. INA Series RFIC SPICE Parameters.

.MODEL Q NPN				
BF=100	IS=1.7E-18	VA=20		BR=2.5
ME=0.6	NF=1.03	PTF=25		TF=1.2E-11
CJE=2.4E-15	XTF=4	IKF=1.3E-04		PE=1.01
ISE=5.0E-15	NE=2.5	VTF=6		XTB=1.818
ITF=3.0E-04				
.MODEL D1 D				
CJO=2.4E-16	VJ=0.76	M=0.53	BV=45	IS=1E-25
.MODEL D2 D				
CJO=1.2E-16	VJ=0.80	M=0.50	BV=45	IS=1E-25
RS=1.0E+06				
.MODEL R1 R	TC=-0.8E-3			
.MODEL R2 R	TC=6.0E-04			
.MODEL R3 R	TC=8.0E-04			
.MODEL R4 R	TC=1.2E-03			
.MODEL R5 R	TC=1.8E-03			

Table 4. INA RFIC Equivalent Circuit Values.

element	model	INA-01	INA-02	INA-03	INA-10
RBIAS1	R1	155	155	330	1150
RBIAS2	R1	67	67	520	600
RBIAS3	R1				200
RE1	R1				6
RE2	R1	25	25	50	40
RF1	R1	1500	1250	750	1200
RF2	R1	380	475	700	500
LIN		.35	.35	.35	0.35
LOUT		.35	.35	.35	0.35
LP1		.20	.20	.20	0.15
LP2		.20	.20	.20	0.15
CCOMP				1.25	
RES				25	
CP1		.35	.35	.35	0.35
CP2		.50	.50	.50	0.35
C3		.25	.25	.25	
C4		.036	.036	.036	
C5		.086	.086	.086	
C13		.023	.023	.023	
C14		.036	.036	0.36	
C15		.029	.029		
Cin					0.15
Cout					0.15
LGND		.10	.10	.05	0.10

Table 5. Circuit Element Values for INA RFIC Package Models.

element	units	**70**	**84/85**	**86**
Lin	nH	0.35	0.35	0.35
Lout	nH	0.35	0.35	0.35
LE	nH	0.10	0.1	0.10
L1	nH	.05	0.05	0.55
L2	nH	.01	0.01	0.06
L3	nH	.01	0.05	0.25
T1: Z	Ω	40	65	65
T1: l	mils	25	25	25
T1: k	-	7	9	9
T2: Z	Ω	20	30	30
T2: l	mils	5	7	7
T2: k	-	7	9	9
T3: Z	Ω	40	65	65
T3: l	mils	25	25	25
T3: k	-	7	9	9
CEB	pF	.02	0.02	0.02
CEC	pF	.01	0.03	0.03
CBC	pF	.02	0.03	0.03

Table 6. INA-12 Model.

INA-12063 Model

SPICE model

```
*INA-12063 Macromodel
*Version 1.0, March 1997
*Connections:  IBias
*              | Gnd2
*              | | In
*              | | | Vd
*              | | | | Gnd1
*              | | | | | Out & Vd
*              | | | | | |
.subckt INA12  1 2 3 4 5 6
LB1 3 10 1.5n
LB2 6 8 1.5n
LE 11 12 1.2n
C1 10 8 75f
C2 6 5 0.4p
C3 13 5 1n
R1 4 9 4.7k
R2 9 10 2k
RE 12 13 2.5
D1 9 2 bias_diode 1

D2 1 14 bias_diode 200
Vsense 14 2 DC 0
F1 13 2 VSENSE 10.0
Q1 8 10 11 A2_31020

.model A2_31020 npn(is=4.04E-16 ise=1.43E-12 isc=2.74E-12
+iss=4.6E-13 ne=2.0 nc=2.0 nf=1.03 nr=1.0 ns=1.0 vaf=2.2E1
+ikf=3.43E-2 ikr=1.05E-1 bf=1.29E2 br=5.14 rb=1.615E1
+rbm=5 re=9.5E-1 rc=3.1 cje=3.65E-13 mje=4E-1 vje=8.5E-1
+fc=8E-1 cjc=1.42E-13 mjc=5E-1 vjc=7.5E-1 xcjc=4.04E-1
+cjs=1.53E-13 mjs=5E-1 vjs=7E-1 tf=9.5E-12 tr=1.6E-9
+itf=6.87E-2 xtf=3.15 ptf=1.8E1 xti=8 xtb=2.2)

.model bias_diode d(is=1E-14)
.ends
```

example use

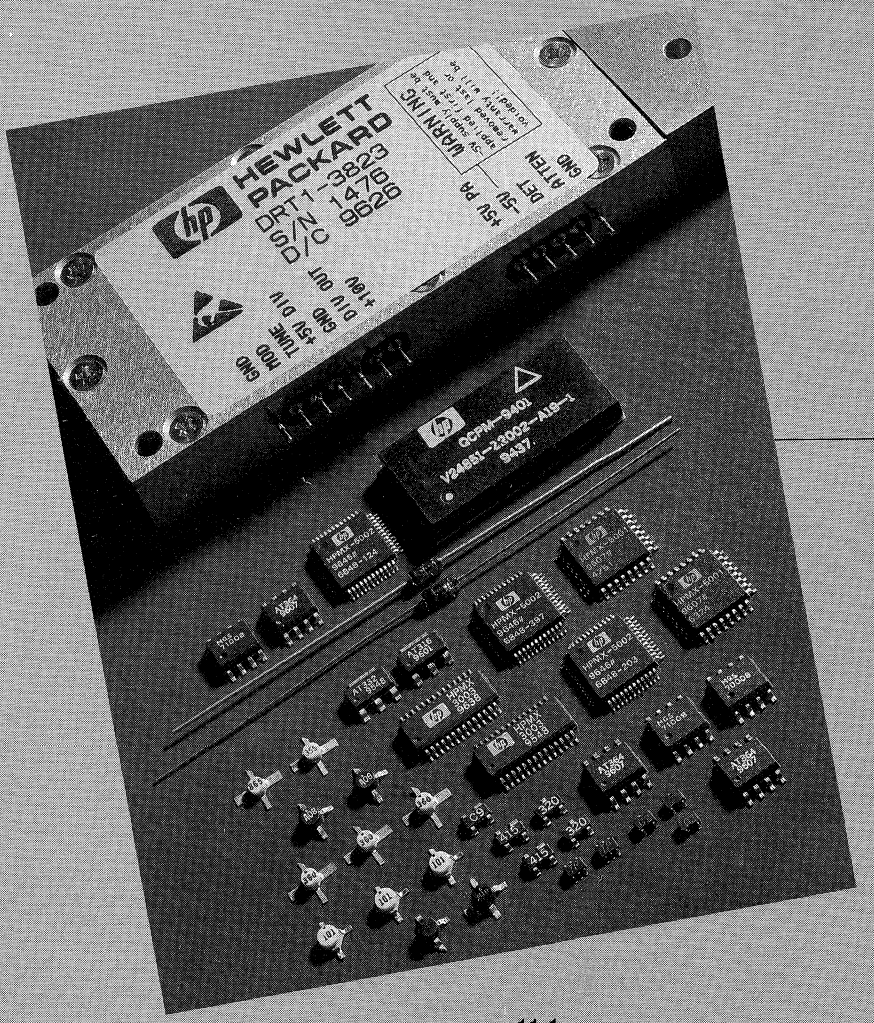
Table 6, continued. **INA-12 Model.**

```
* This PSPICE deck provides an example of how to use the INA-12 macro model
* The application is a 900MHz LNA as shown in Figure 32 of the datasheet
* Hewlett Packard, March 1997
*
Vsupply Vcc 0 3.0
Vin 2 0 DC 0 AC 2 SIN(0 14.1E-3 900E6)
X1 1 0 5 Vcc 0 6 INA12
Rbias Vcc 1 5.6k
RS 2 3 50
RL 7 0 50
R1 Vcc 6 470
L1 4 5 8.2n
L2 Vcc 6 8.2n
C1 3 4 100p
C2 6 7 2.2p

.OP
.AC LIN 501 0.1G 5.1G
*.TRAN 1n 20n 0n 10p
.include d:\pspice\ckt\hp_rfic.lib
.END
```

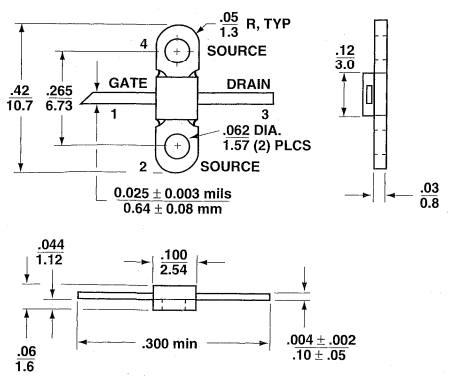
HEWLETT® PACKARD

Packaging



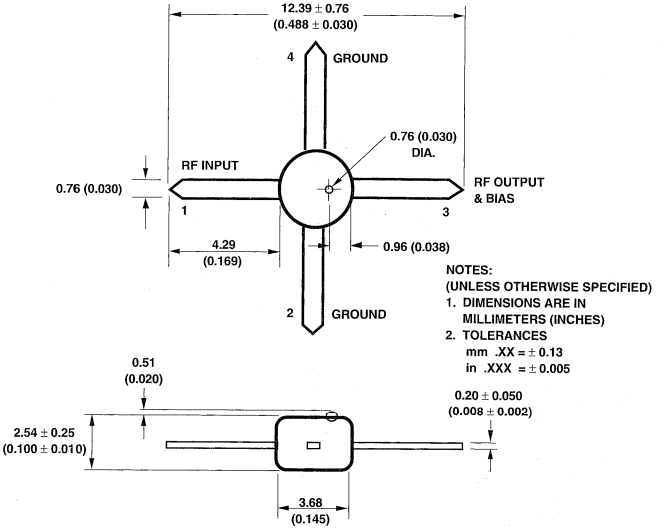
PACKAGE OUTLINES

All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



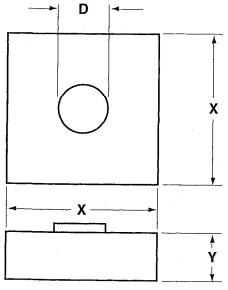
Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ± 0.005
   mm .xx = ± 0.13

01A: 100 mil Flange

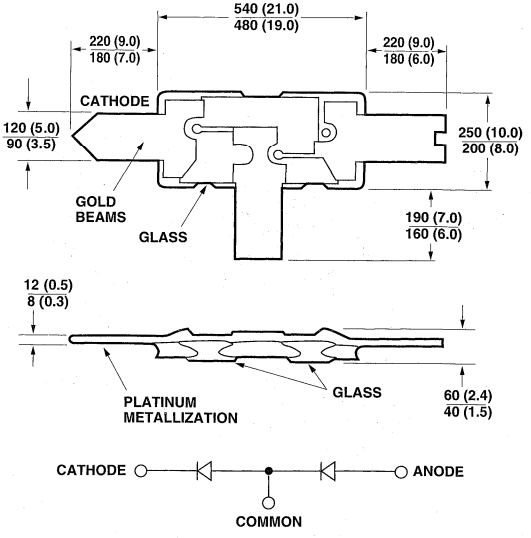


NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. DIMENSIONS ARE IN MILLIMETERS (INCHES)
2. TOLERANCES
   mm .XX = ± 0.13
   in .XXX = ± 0.005

04A: 145 mil Plastic



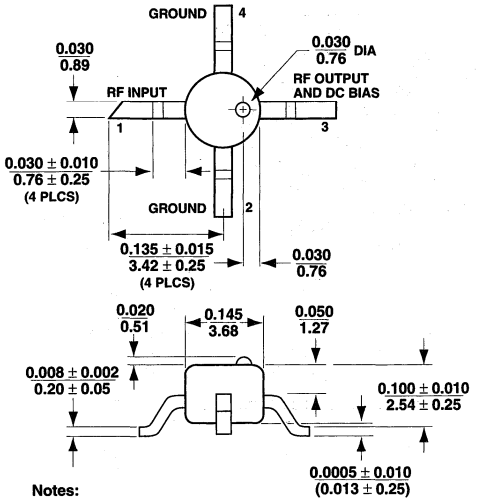
01B



DIMENSIONS IN μm (1/1000 inch)

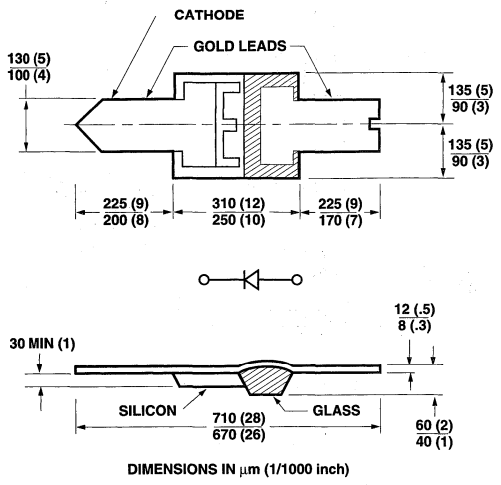
04B

All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



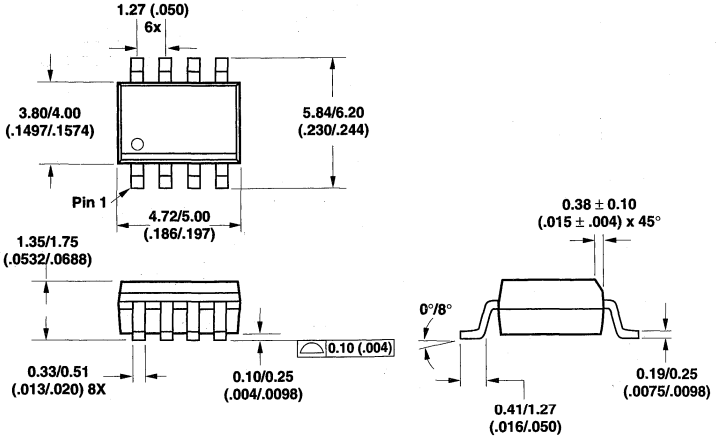
Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ± 0.005
   mm .xx = ± 0.13

05: 145 mil Surface Mount Plastic



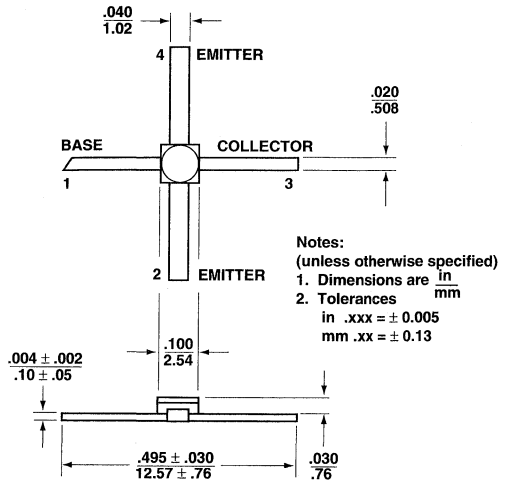
DIMENSIONS IN μm (1/1000 inch)

07

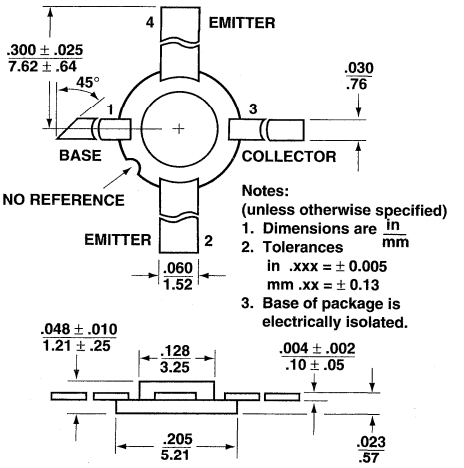


08A: Plastic SO-8

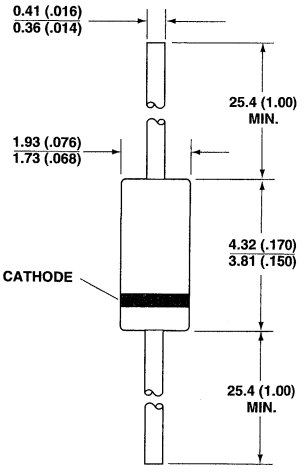
All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



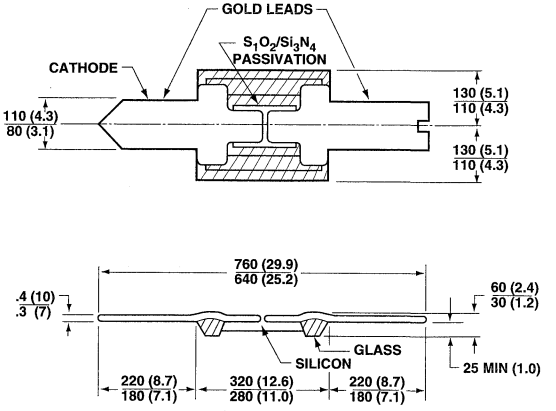
10A: 100 mil Stripline



20: 200 mil BeO



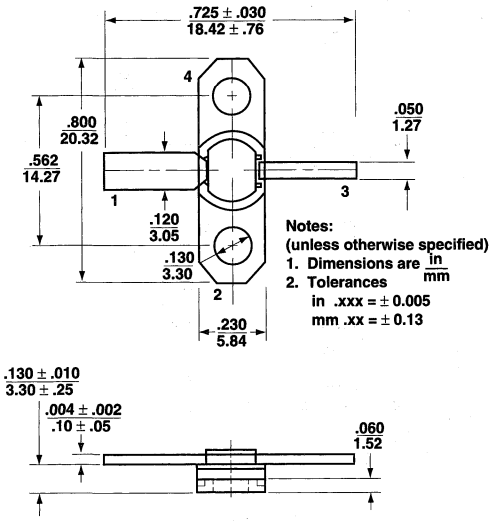
15



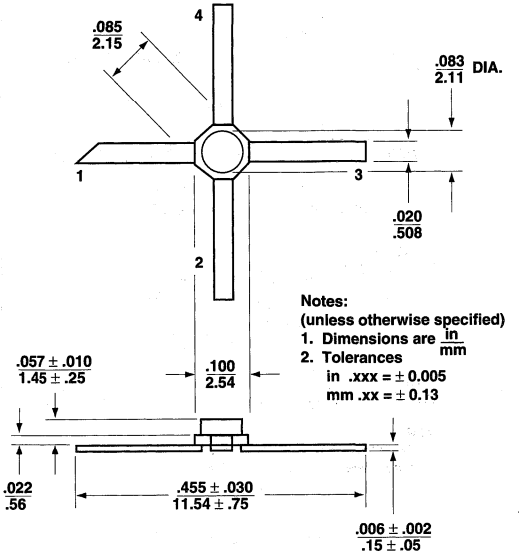
DIMENSIONS IN μm (1/1000 inch)

21

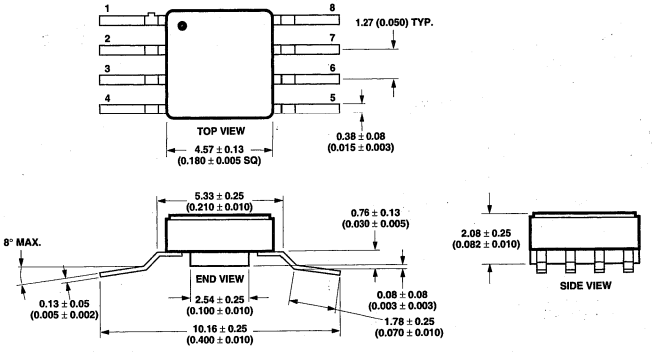
All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



23A: 230 mil BeO Flange

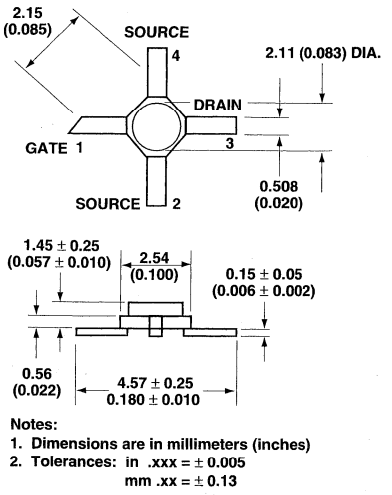


35: micro-X



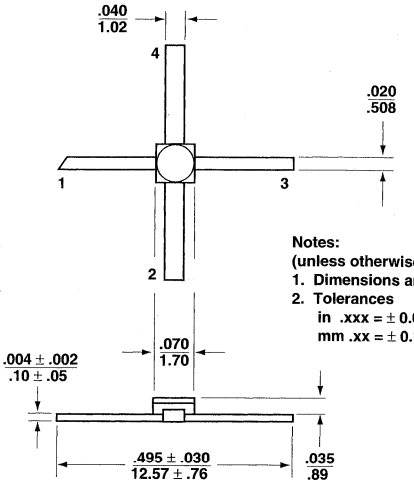
28: 180 mil Ceramic Surface Mount

All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



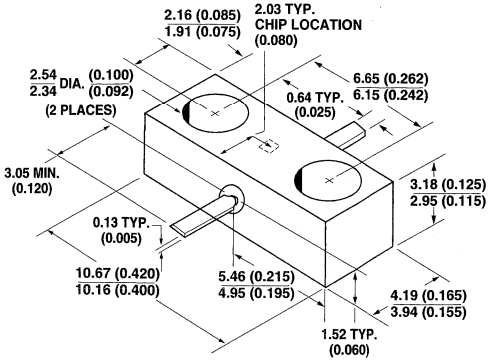
Notes:
1. Dimensions are in millimeters (inches)
2. Tolerances: in .xxx = ± 0.005
mm .xx = ± 0.13

36: Short Lead micro-X

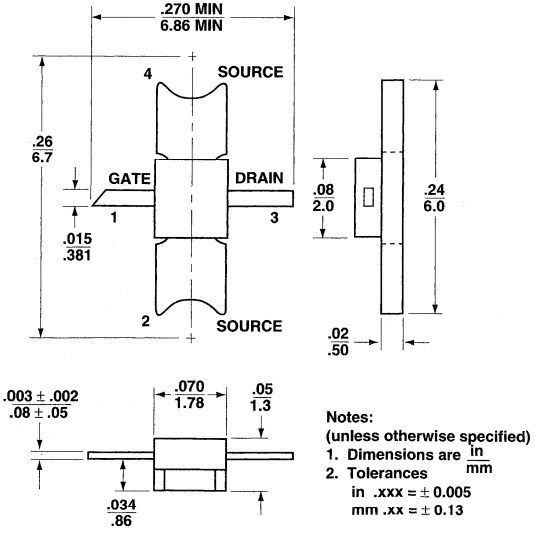


Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
in .xxx = ± 0.005
mm .xx = ± 0.13

70: 70 mil Stripline



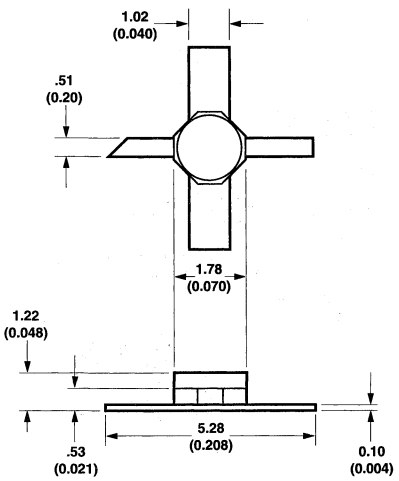
60



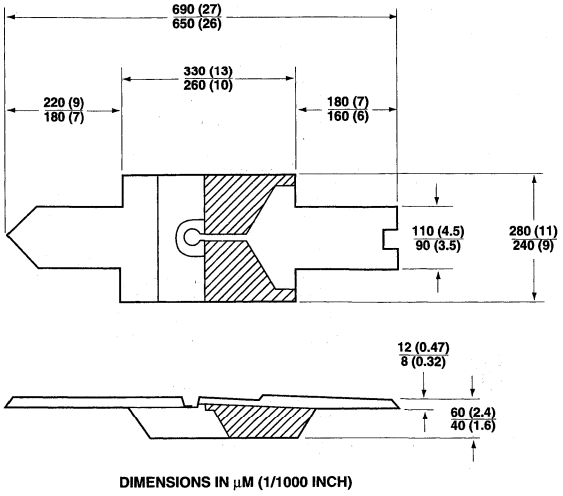
Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
in .xxx = ± 0.005
mm .xx = ± 0.13

71: 70 mil Flange

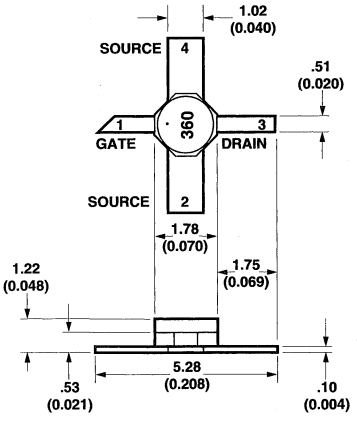
All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



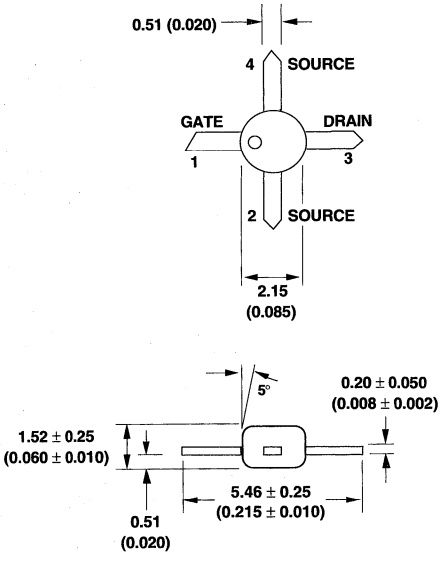
76: 70 mil Ceramic



83

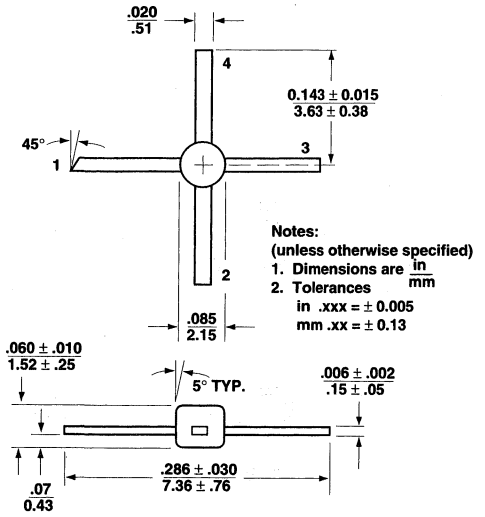


77

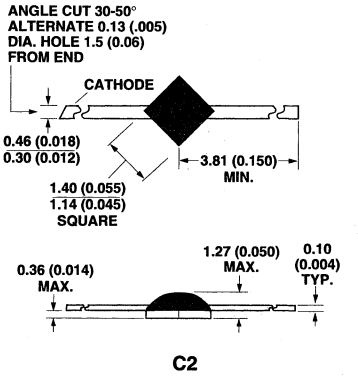


84: Short Lead 85 mil Plastic

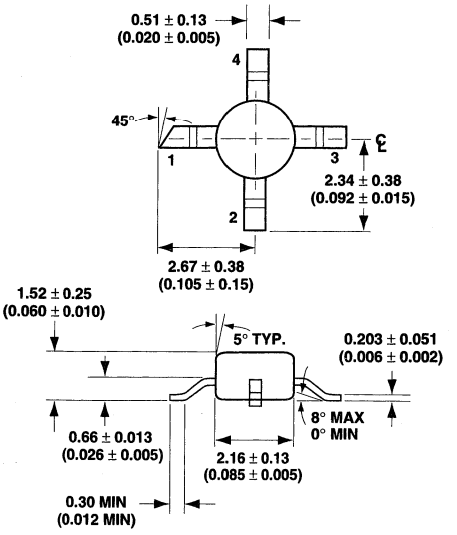
All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



85: 85 mil Plastic

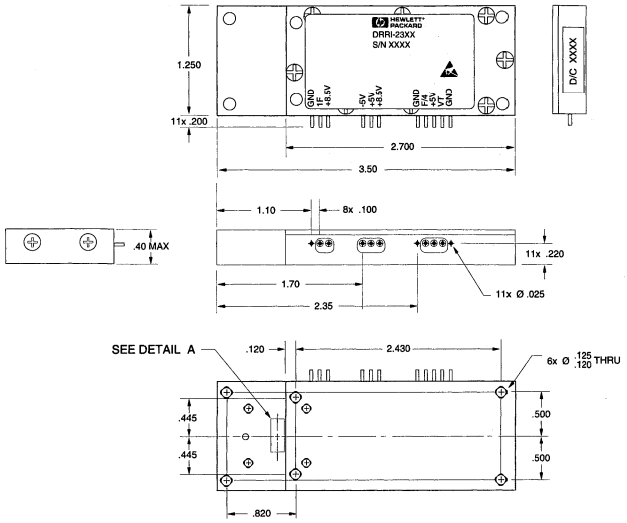


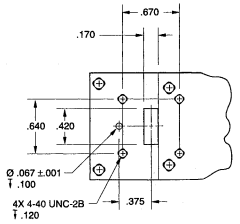
C2



86: 85 mil Surface Mount Plastic

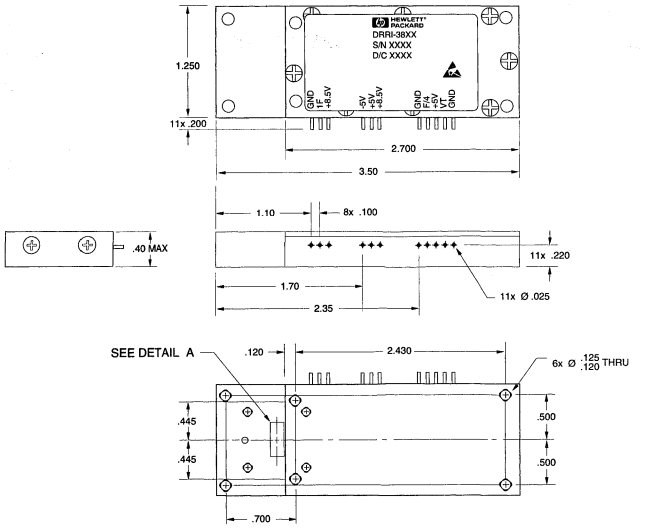
All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.

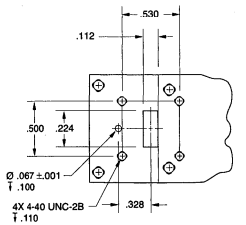




DETAIL A

DRR1-23XX

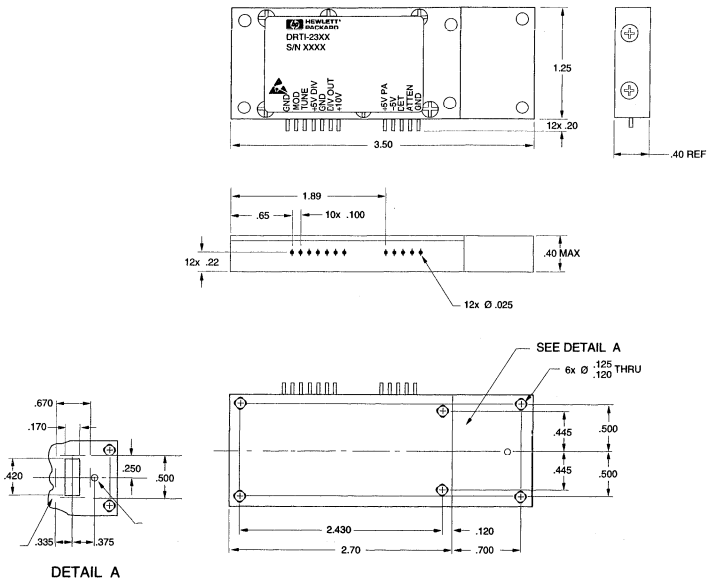




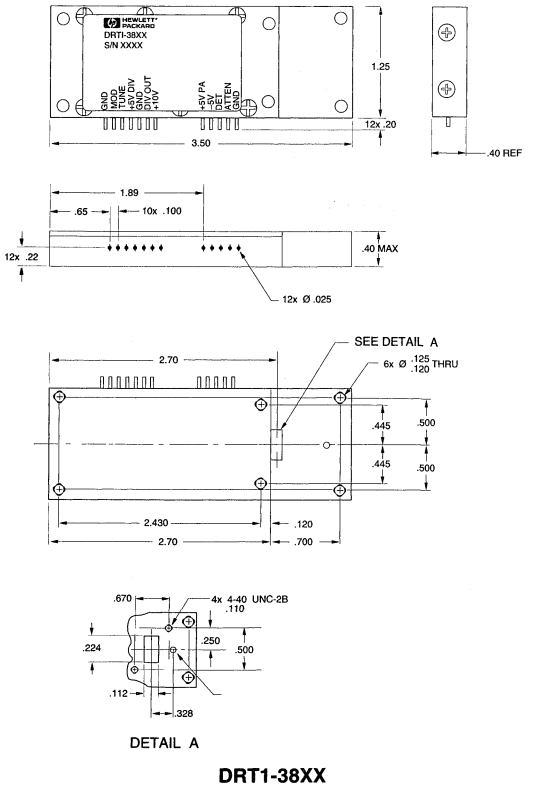
DETAIL A

DRR1-38XX

All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.

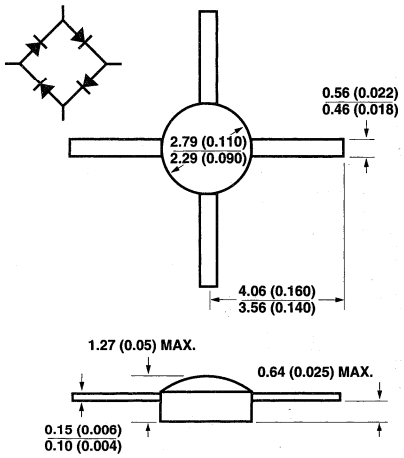


DRT1-23XX

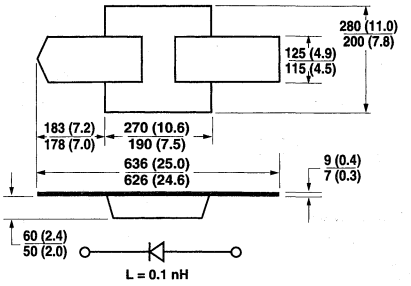


DRT1-38XX

All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



E4



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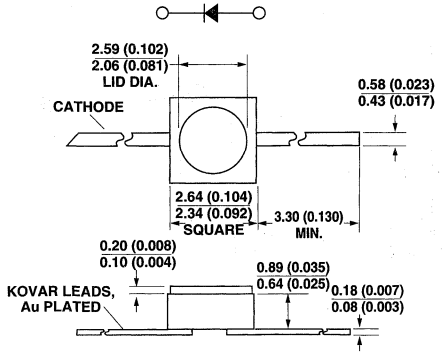
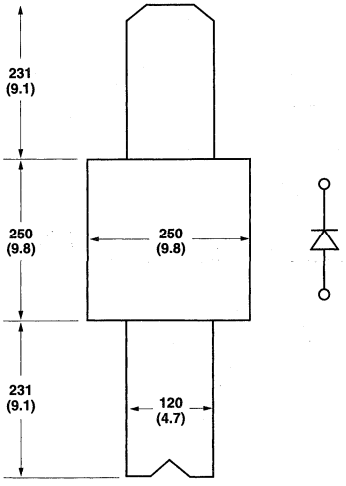


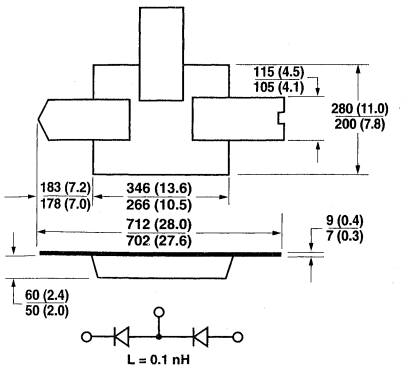
H2



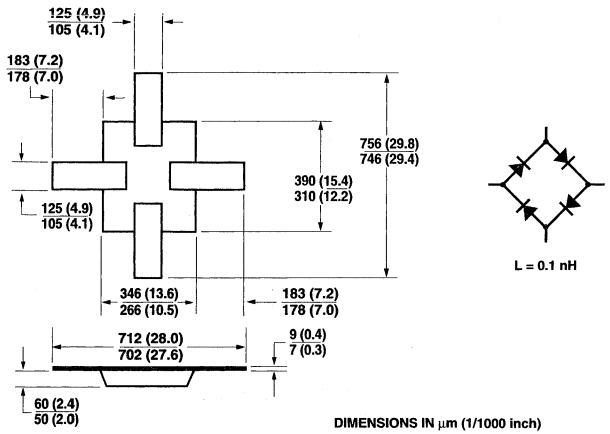
ALL DIMENSIONS IN MICRONS.

HSCH-9161

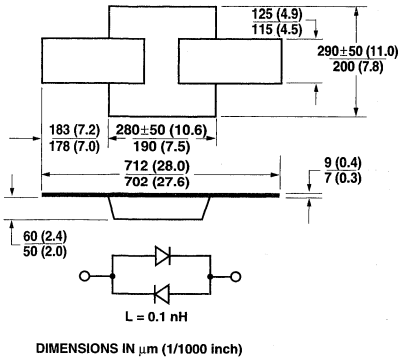
All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



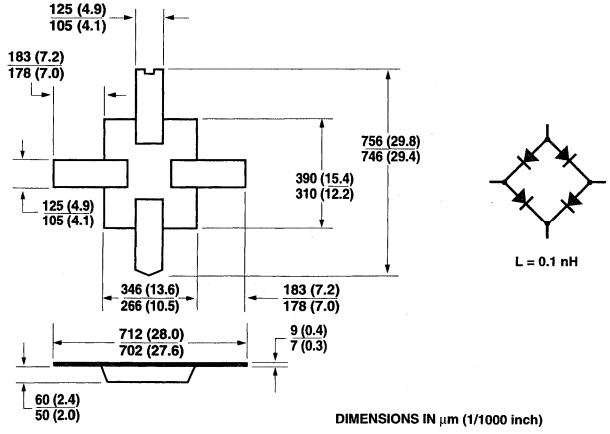
HSCH-9201



HSCH-9301

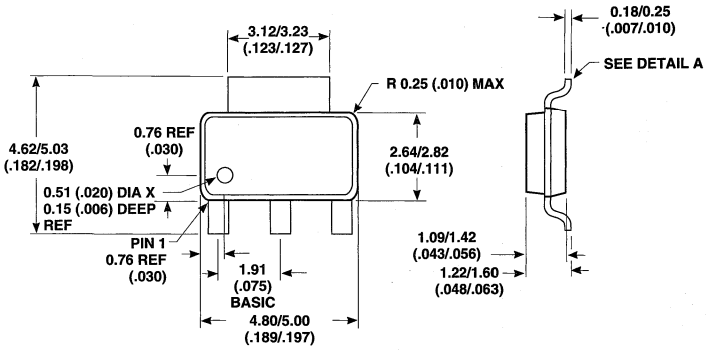


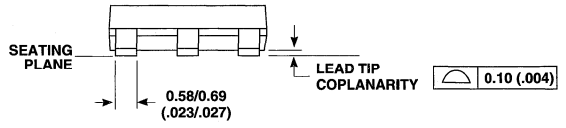
HSCH-9251

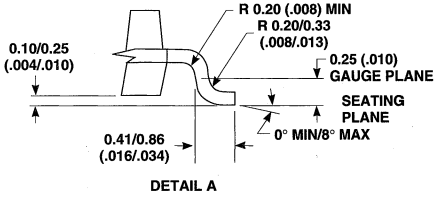


HSCH-9351

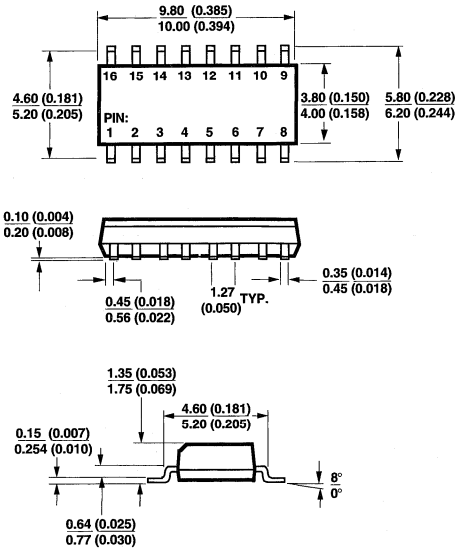
All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.





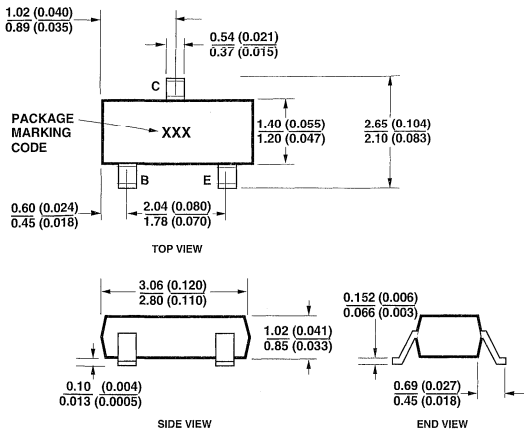


MSOP-3

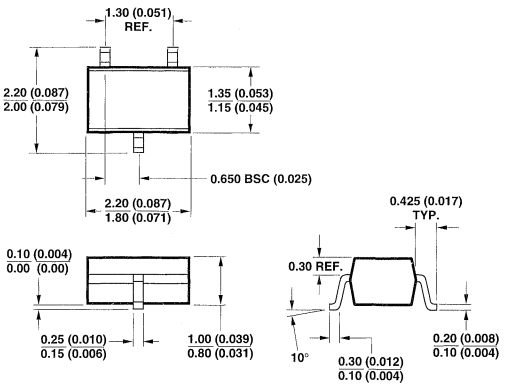


SO-16

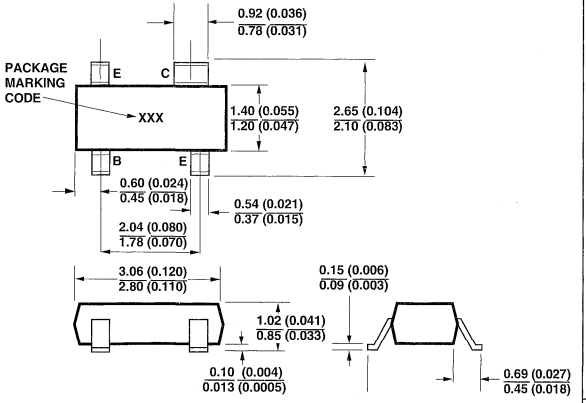
All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



SOT-23

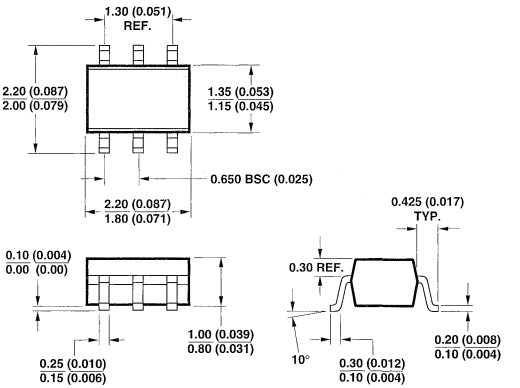


SOT-323

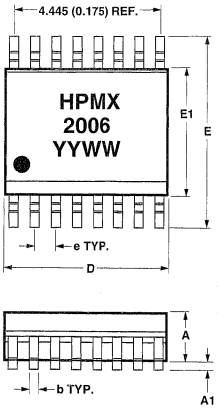


DIMENSIONS ARE IN MILLIMETERS (INCHES)

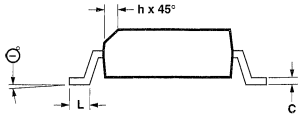
SOT-143



SOT-363

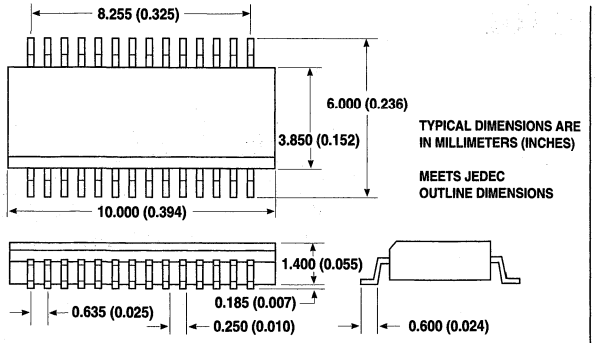


SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	1.372 (0.054)	1.575 (0.062)
A1	0.127 (0.005)	0.254 (0.010)
b	0.203 (0.008)	0.305 (0.012)
C	0.178 (0.007)	0.254 (0.010)
D	4.801 (0.189)	5.004 (0.197)
E	5.867 (0.231)	6.121 (0.241)
e	0.635 BSC (0.025)	
E1	3.835 (0.151)	3.988 (0.157)
h	0.305 (0.012)	0.457 (0.018)
L	0.533 (0.021)	0.787 (0.031)
θ	0	8

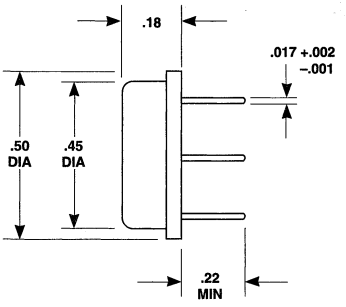


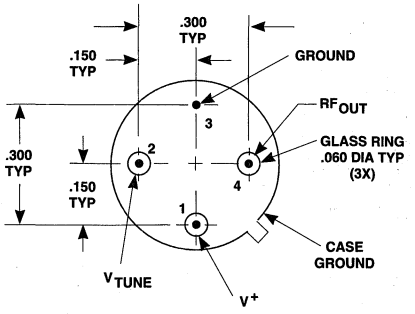
SSOP-16

All dimensions in millimeters (inches), except where noted.
For complete package specifications, as well as chip dimensions,
refer to individual product specification sheets.
Drawings are not to scale.



SSOP-28

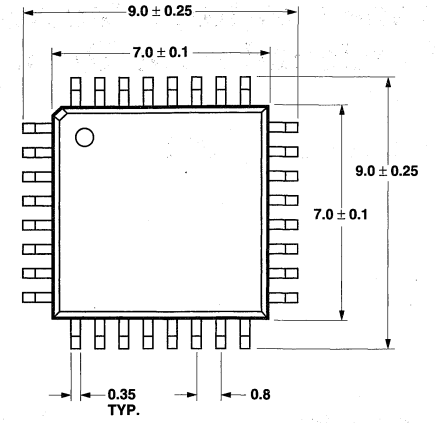


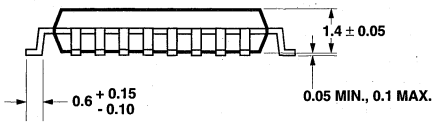


APPROXIMATE WEIGHT 1.7 GRAMS

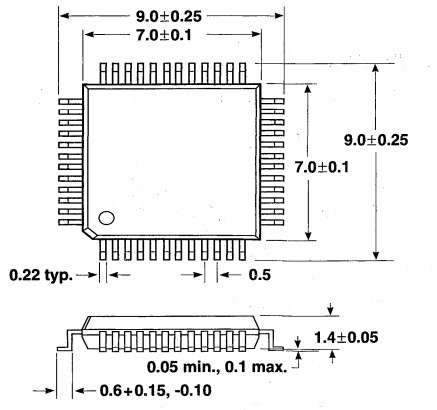
NOTES (UNLESS OTHERWISE SPECIFIED):
1. DIMENSIONS ARE SPECIFIED IN INCHES
2. TOLERANCES: xx ± .02
xxx ± .010

TO-8V





TQFP-32



ALL DIMENSIONS SHOWN IN mm

TQFP-48

HEWLETT® PACKARD

Tape and Reel Packaging for Semiconductor Devices

Technical Data

Package Outlines
05, 08A, 36, 76, 84, 86, MSOP-3, SOIC-8, SOT-23, SOT-143, SOT-323, SOT-363, SSOP-16, TQFP-32, and TQFP-48

Description

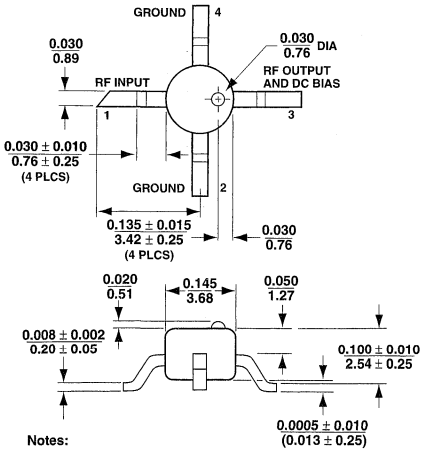
This data sheet is intended to cover standards on tape and reel packaging for Hewlett-Packard Communications Components Division (CMCD) semiconductor devices.This type of tape and reel packaging is designed to be compatible with available automated pick and place machines.

Related Standard

EIA RS481, "Taping of Leadless Components for Automatic Placement." In case of conflict regarding MSD product, this data sheet will govern.

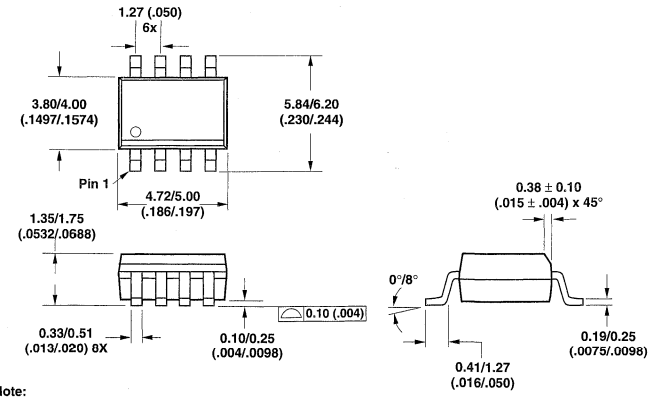
1. Package Outlines

05: 145 mil Surface Mount Plastic (B)



Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
in .xxx = ± 0.005
mm .xx = ± 0.13

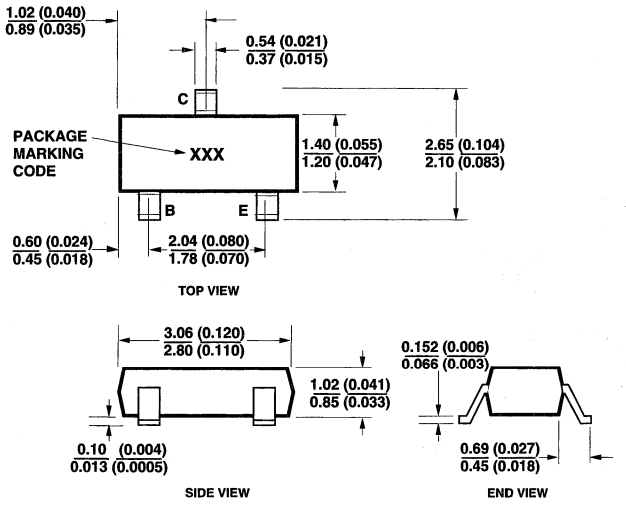
08A: Plastic SO-8



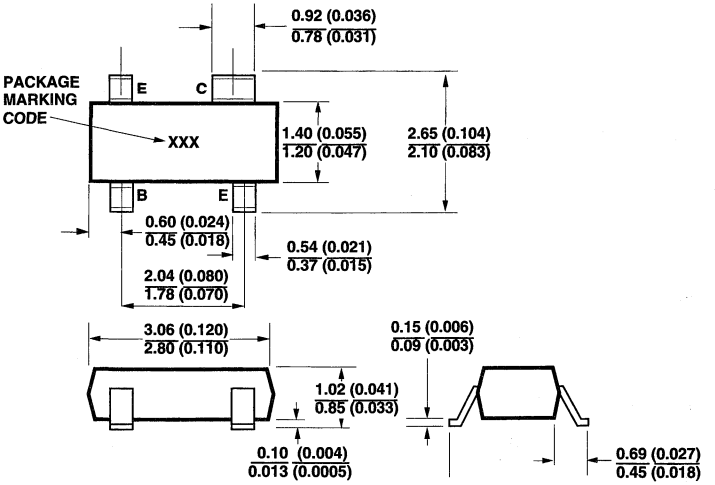
Note:
1. Dimensions are shown in millimeters (inches).

1. Package Outlines, continued

Outline SOT-23



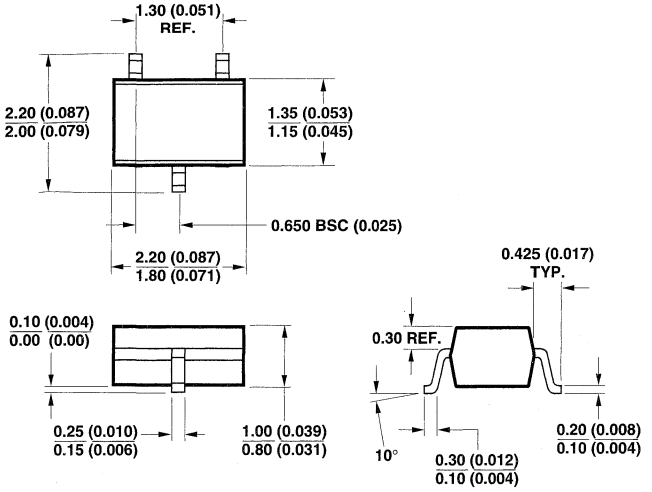
Outline SOT-143



DIMENSIONS ARE IN MILLIMETERS (INCHES)

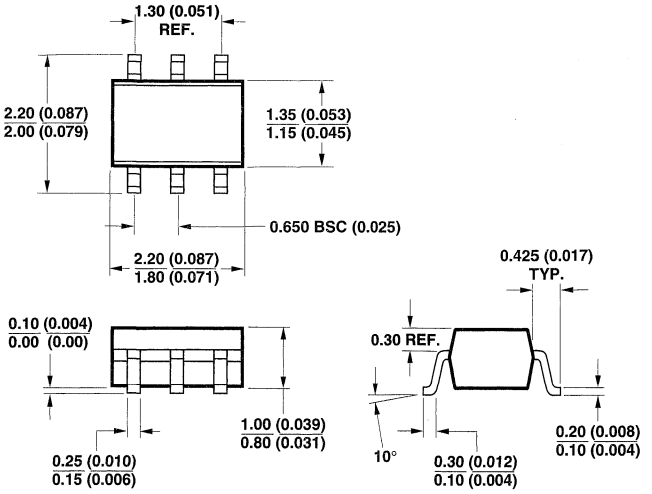
1. Package Outlines, continued

Outline SOT-323 (SC-70 3 Lead)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

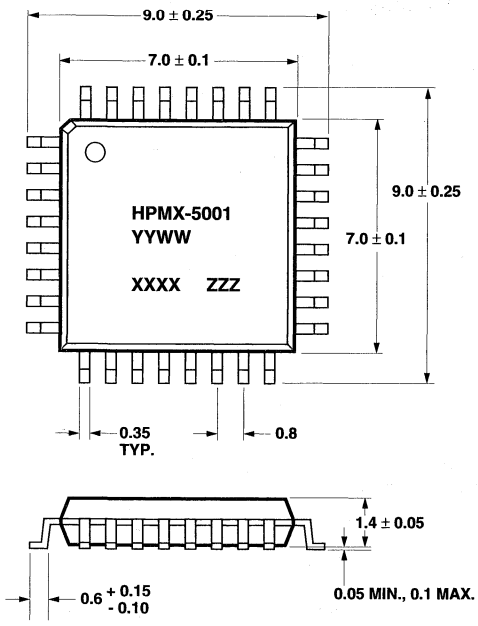
Outline 63 (SOT-363/SC-70)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

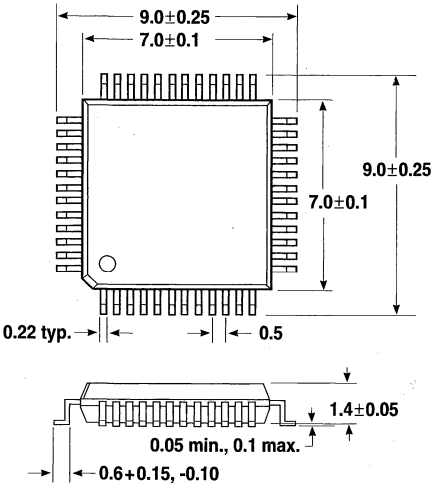
1. Package Outlines, continued

Outline TQFP-32 (32 Pin Thin Quad Flat Package)



ALL DIMENSIONS SHOWN IN mm

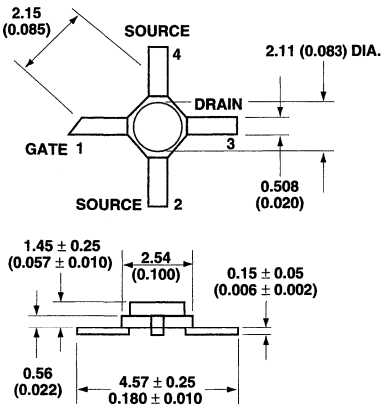
Outline TQFP-48 (48 Pin Thin Quad Flat Package)



ALL DIMENSIONS SHOWN IN mm

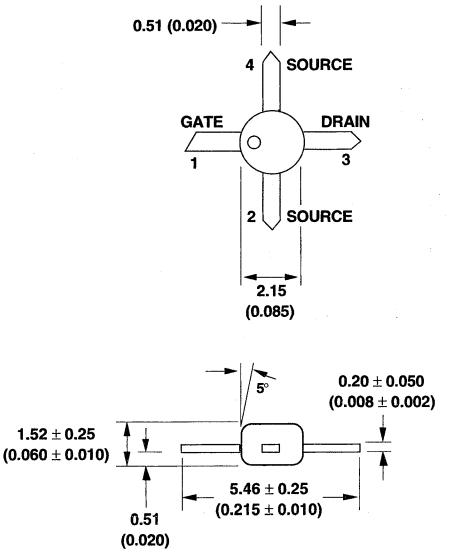
1. Package Outlines, continued

36: Short Lead micro-X (B, D)



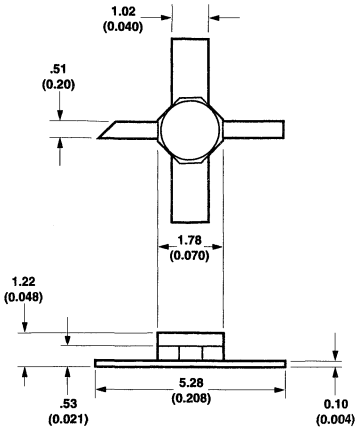
Notes:
1. Dimensions are in millimeters (inches)
2. Tolerances: in .xxx = ± 0.005
   mm .xx = ± 0.13

84: Short Lead 85 mil Plastic (D)



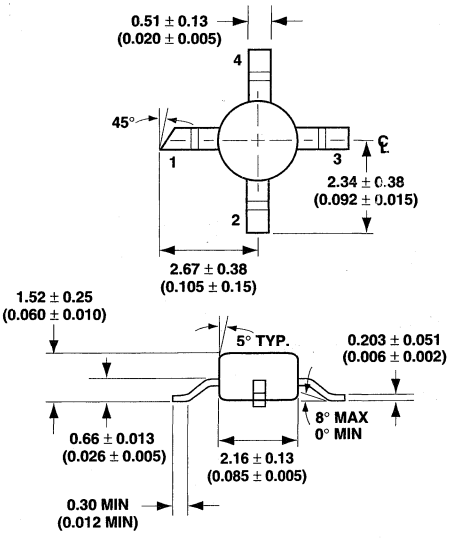
DIMENSIONS ARE IN MILLIMETERS (INCHES)

76: 70 mil Ceramic



TYPICAL DIMENSIONS ARE IN MILLIMETERS (INCHES).

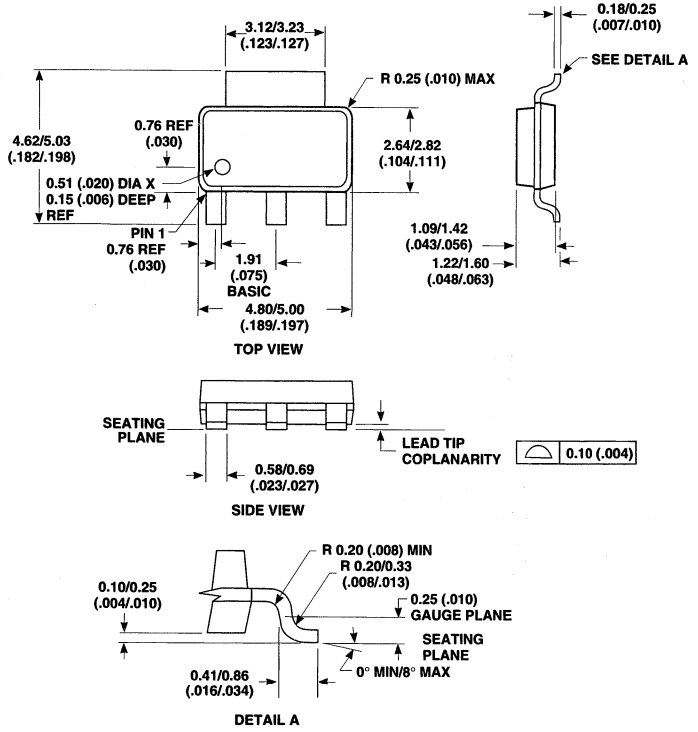
Outline 86



DIMENSIONS ARE IN MILLIMETERS (INCHES)

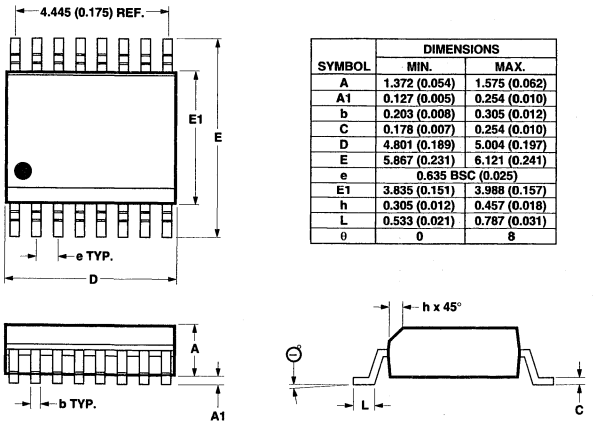
1. Package Outlines, continued

MSOP-3 Surface Mount Plastic Package



NOTE:
DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)

SSOP-16

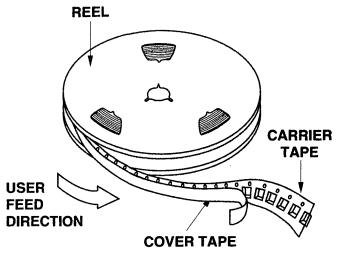


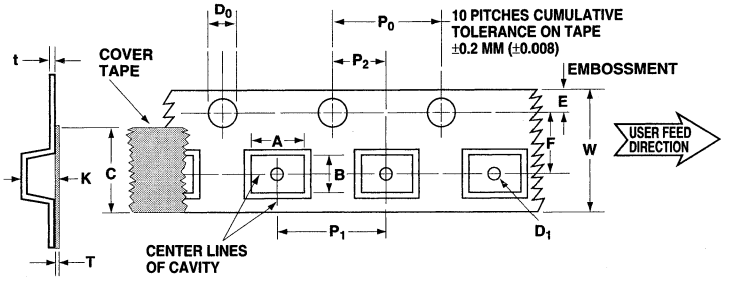
SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	1.372 (0.054)	1.575 (0.062)
A1	0.127 (0.005)	0.254 (0.010)
b	0.203 (0.008)	0.305 (0.012)
C	0.178 (0.007)	0.254 (0.010)
D	4.801 (0.189)	5.004 (0.197)
E	5.867 (0.231)	6.121 (0.241)
e	0.635 BSC (0.025)	
E1	3.835 (0.151)	3.988 (0.157)
h	0.305 (0.012)	0.457 (0.018)
L	0.533 (0.021)	0.787 (0.031)
θ	0	8

DIMENSIONS IN MILLIMETERS AND (INCHES).

2. Tape Dimensions and Product Orientation

For Outlines SOT-23, SOT-143, and 08A (SOIC-8)





SOT-23 and SOT-143 Dimensions

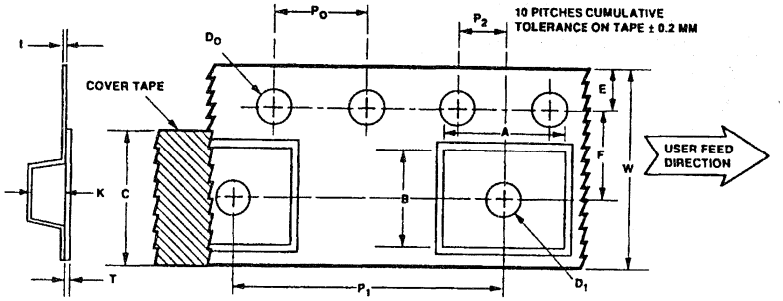
DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A	3.15 ± 0.15	0.124 ± 0.006
	WIDTH	B	2.65 ± 0.25	0.104 ± 0.010
	DEPTH	K	1.30 ± 0.10	0.051 ± 0.004
	PITCH	P_1	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 min.	0.04 min.
PERFORATION	DIAMETER	D_0	1.55 + 0.10/-0	0.061 + 0.004/-0
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.2	0.315 ± 0.008
	THICKNESS	t	0.30 ± 0.05	0.012 ± 0.002
COVER TAPE	WIDTH	C	5.40 ± 0.25	0.205 ± 0.010
	TAPE THICKNESS	T	0.064 ± 0.01	0.003 ± 0.0004
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.10	0.138 ± 0.004
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

2. Tape Dimensions and Product Orientation, continued

For Outline 08A (SOIC-8)

DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A	6.45 ± 0.10	0.254 ± 0.004
	WIDTH	B	5.13 ± 0.10	0.202 ± 0.004
	DEPTH	K	2.11 ± 0.10	0.083 ± 0.004
	PITCH	P_1	8.00 ± 0.10	0.315 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.50 min.	0.059 min.
PERFORATION	DIAMETER	D_0	1.50 + 0.10/-0	0.059 + 0.004/-0
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t	0.255 ± 0.013	0.0100 ± 0.0005
COVER TAPE	WIDTH	C	9.19 ± 0.10	0.362 ± 0.004
	TAPE THICKNESS	T	0.051 ± 0.010	0.0020 ± 0.0004
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	5.51 ± 0.05	0.217 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

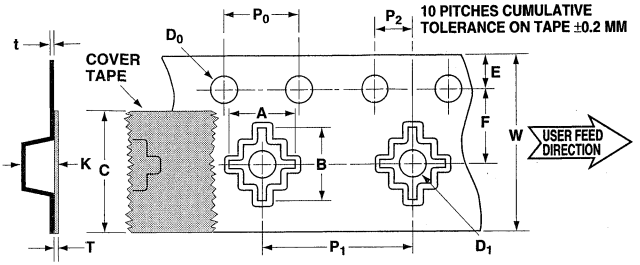
For Outline 05



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A	6.10 ± 0.10	0.240 ± 0.004
	WIDTH	B	6.10 ± 0.10	0.240 ± 0.010
	DEPTH	K	3.18 ± 0.10	0.125 ± 0.004
	PITCH	P_1	12.00 ± 0.10	0.472 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.50 min.	0.059 min.
PERFORATION	DIAMETER	D_0	1.50 + 0.10/-0.05	0.059 + 0.004/-0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	12.00 ± 0.20	0.472 ± 0.008
	THICKNESS	t	0.30 ± 0.05	0.012 ± 0.002
COVER TAPE	WIDTH	C	9.30 ± 0.10	0.366 ± 0.004
	TAPE THICKNESS	T	0.065 ± 0.01	0.003 ± 0.0004
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	5.50 ± 0.05	0.217 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

2. Tape Dimensions and Product Orientation, continued

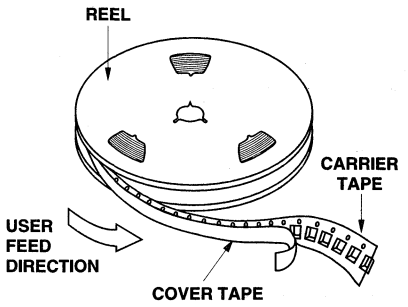
For Outlines 36, 76, 84, and 86

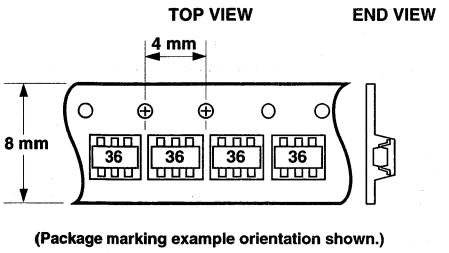


DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A	5.77 ± 0.10	0.227 ± 0.004
	WIDTH	B	6.10 ± 0.10	0.240 ± 0.004
	DEPTH	K	1.70 ± 0.10	0.067 ± 0.004
	PITCH	P_1	8.00 ± 0.10	0.314 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.50 min.	0.059 min.
PERFORATION	DIAMETER	D_0	1.50 + 0.10/-0.05	0.059 + 0.004/-0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	12.00 ± 0.20	0.472 ± 0.008
	THICKNESS	t	0.30 ± 0.05	0.012 ± 0.002
COVER TAPE	WIDTH	C	9.30 ± 0.10	0.366 ± 0.004
	TAPE THICKNESS	T	0.065 ± 0.010	0.0026 ± 0.0004
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	5.50 ± 0.05	0.217 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

2. Tape Dimensions and Product Orientation, continued

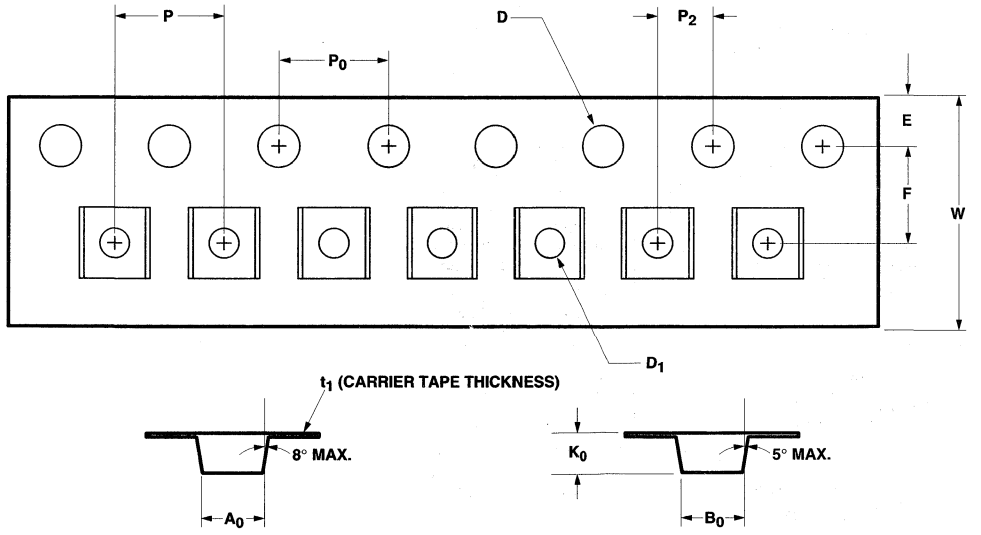
Device Orientation





(Package marking example orientation shown.)

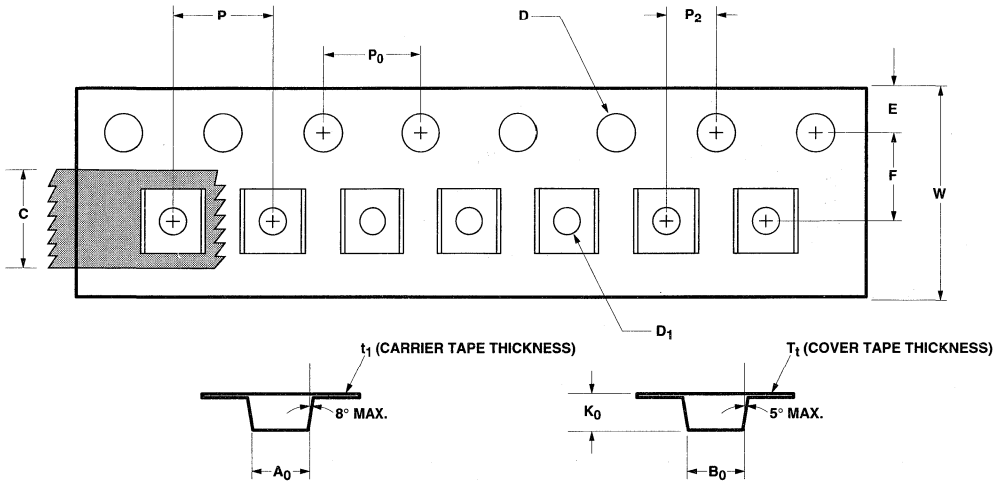
For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

2. Tape Dimensions and Product Orientation, continued

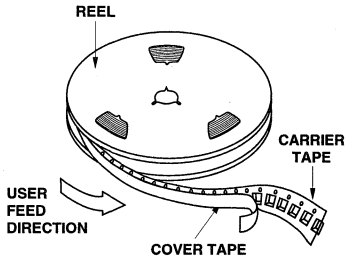
For Outline SOT-323 (SC-70 3 Lead)

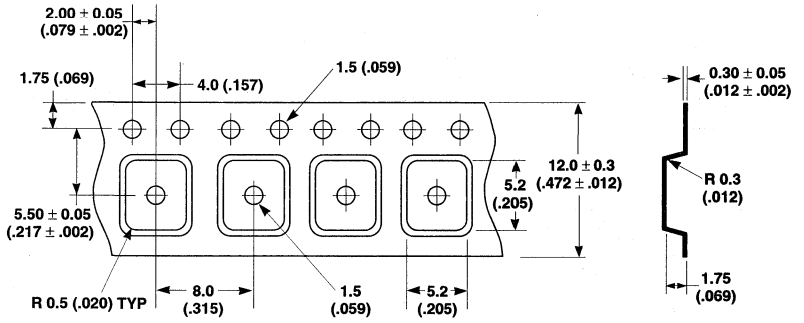


DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

2. Tape Dimensions and Product Orientation, continued

For Package MSOP-3

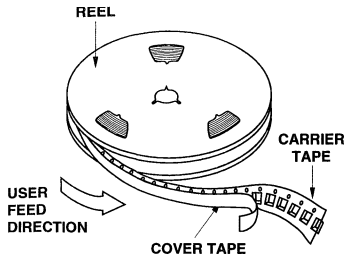


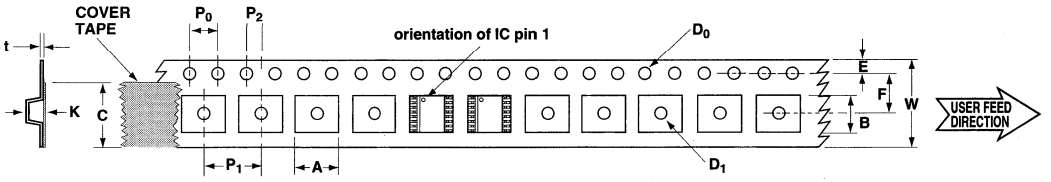


NOTES:
1. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. TOLERANCES: .X ± 0.1 (.XXX ± .004)

2. Tape Dimensions and Product Orientation, continued

For Package SSOP-16

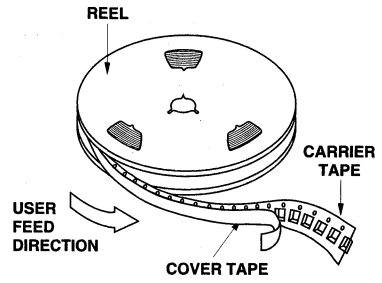


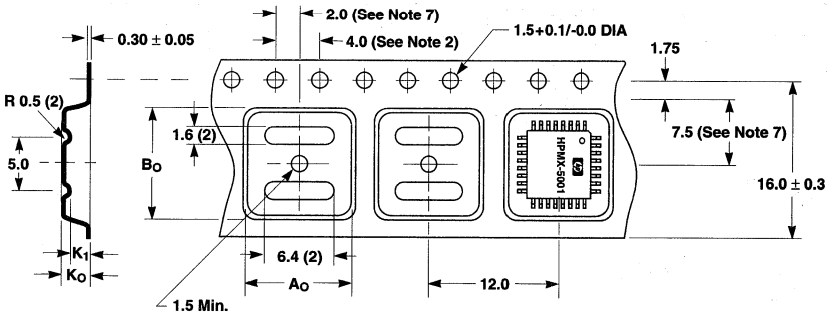


DESCRIPTION		SYMBOL	SIZE (mm)
CAVITY	LENGTH	A	6.4 ± 0.1
	WIDTH	B	5.2 ± 0.1
	DEPTH	K	2.1 ± 0.1
	PITCH	P_1	8.0 ± 0.1
	BOTTOM HOLE DIAMETER	D_1	1.6
PERFORATION	DIAMETER	D_0	1.5
	PITCH	P_0	4.0
	POSITION	E	1.8
CARRIER TAPE	WIDTH	W	12.0
	THICKNESS	t	0.3
COVER TAPE	WIDTH	C	9.2 ± 0.1
	TAPE THICKNESS	T	
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	5.5
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.0

2. Tape Dimensions and Product Orientation, continued

For Outlines TQFP-32 and TQFP-48





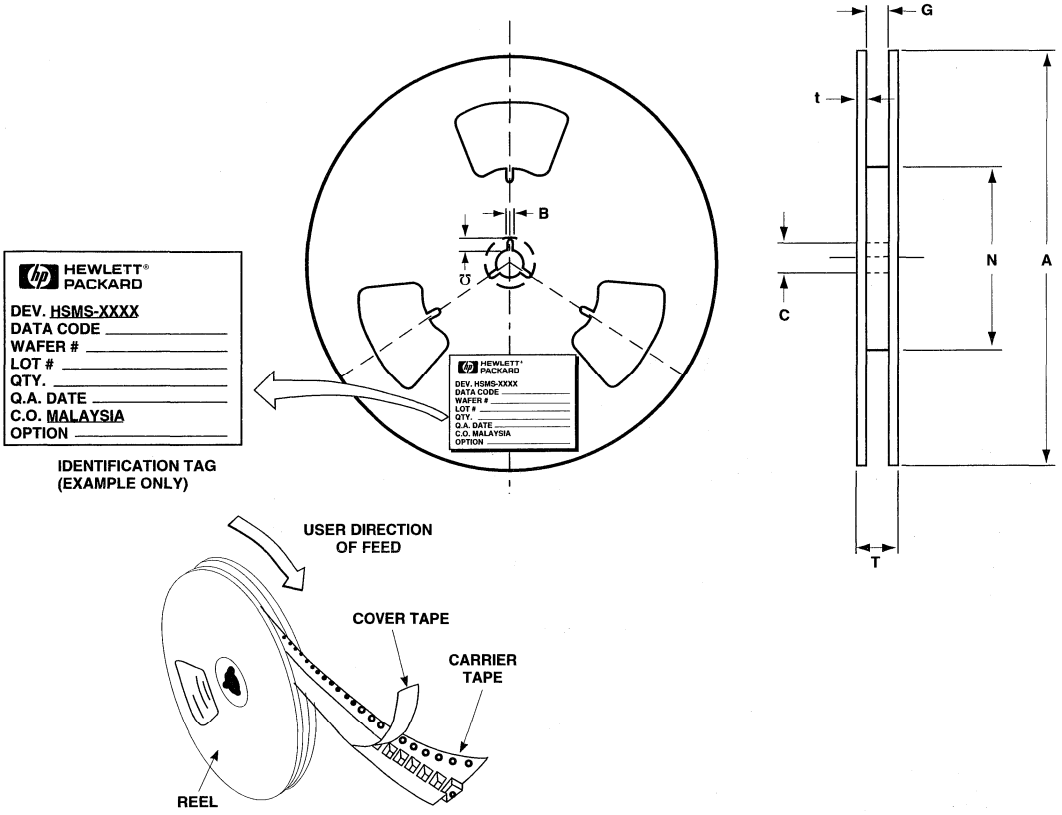
Cover tape width = 13.3 ± 0.1 mm
Cover tape thickness = 0.051 mm (0.002 inch)

A_O = 9.3 mm
B_O = 9.3 mm
K_O = 2.2 mm
K_1 = 1.6 mm

NOTES:
1. Dimensions are in millimeters
2. 10 sprocket hole pitch cumulative tolerance ±0.2
3. Chamber not to exceed 1 mm in 100 mm
4. Material: black conductive Advantek™ polystyrene
5. A_O and B_O measured on a plane 0.3 mm above the bottom of the pocket.
6. K_O measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

3. Reel Dimensions

For Outlines SOT-23 and SOT-143

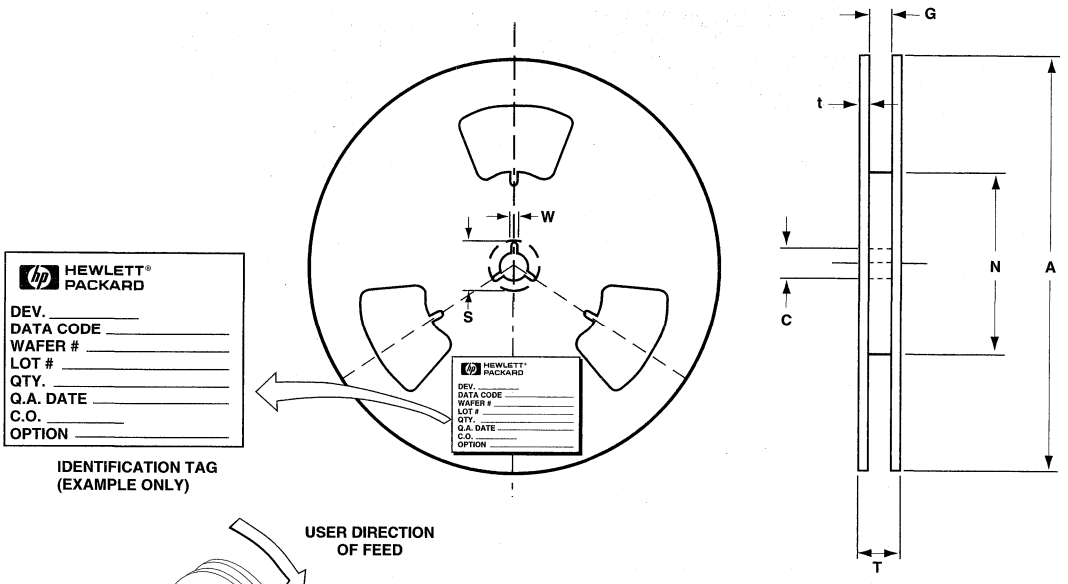


			7" REEL		13" REEL	
	DESCRIPTION	SYMBOL	SIZE (mm)	SIZE (INCHES)	SIZE (mm)	SIZE (INCHES)
FLANGE	DIAMETER	A	178 ± 2.0	7.00 ± 0.079	330 ± 2.0	13.0 ± 0.079
	THICKNESS, MAXIMUM	T	14.4	0.570	14.4	0.570
	SPACE BETWEEN FLANGE	G	9.50 ± 1.0	0.374 ± 0.040	9.15 ± 0.75	0.361 ± 0.03
HUB	OUTER DIAMETER	N	66 ± 1.0	2.598 ± 0.040	55 min	12.16 min
	SPINDLE HOLE DIAMETER	C	13.0 ± 0.5	0.512 ± 0.020	13.0 ± 0.5	0.512 ± 0.02
	KEY SLIT WIDTH	B	2.0 ± 0.5	0.079 + 0.020	1.5 min	0.059 min
	DEPTH	℧	4.0 ± 0.5	0.16 ± 0.020	4.0 ± 0.5	0.16 ± 0.020
	LOCATION	θ	120° ± 5°		120° ± 5°	

Notes:
1. Metric dimensions will govern.
2. Drawing is not to scale.
3. Diodes available on 7" reels only.
4. Monolithic amplifiers and transistors available on 7" (-TR1) and 13" (-TR2) reels.

3. Reel Dimensions, continued

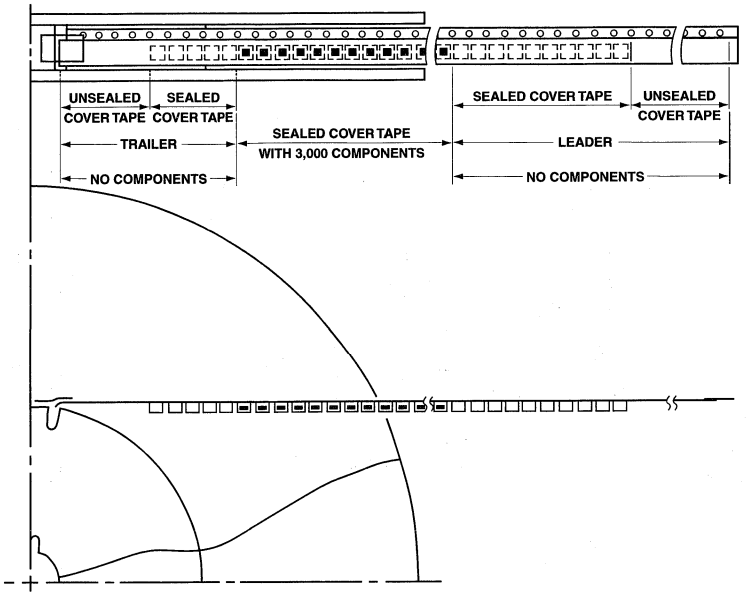
For Outlines 05, 08A, 36, 76, 84, and 86



			7" REEL		13" REEL	
DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)	SIZE (mm)	SIZE (INCHES)
FLANGE	DIAMETER	A	178 ± 2.0	7.0 ± 0.079	330 ± 2.0	13.0 ± 0.079
	THICKNESS, MAX	T	18.4	0.724	18.4	0.724
	SPACE BETWEEN FLANGE	G	12.4 $^{+2.0}_{-0}$	0.488 $^{+0.08}_{-0}$	12.4 $^{+2.0}_{-0}$	0.488 $^{+0.08}_{-0}$
HUB	OUTER DIAMETER, MIN	N	55	2.16	63 min	2.48
	SPINDLE HOLE DIAMETER	C	13.0 ± 0.2	0.512 ± 0.008	13.0 ± 0.2	0.512 ± 0.008
	KEY SLIT WIDTH, MIN	W	1.5	0.059	1.5	0.059 min
	DIAMETER, MIN	S	20.2	0.795	20.2	0.795

4. Packing—Leader and Trailer

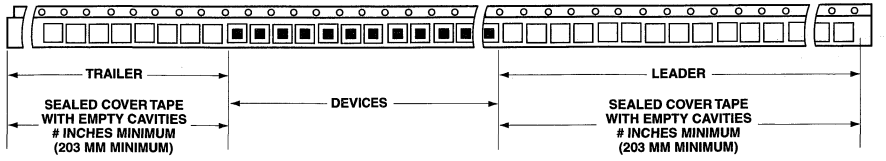
For Outlines SOT-23 and SOT-143



ITEM		SPECIFICATION (inches) (minimum)	SPECIFICATION (inches) (minimum)
LEADER	UNSEALED COVER TAPE	20	0.79
	SEALED COVER TAPE WITH EMPTY CAVITIES	160	6.30
TRAILER	UNSEALED COVER TAPE	20	0.79
	SEALED COVER TAPE WITH EMPTY CAVITIES	120	4.72

Packing

For Outlines 05, 08A, 36, 76, 84, and 86



5. Materials

For Outlines 23 and 143

A. Carrier Tape: Static dissipative polystyrene
Surface resistivity: 10^7 Ω/square maximum

B. Cover Tape: Antistatic semi-transparent polyester

C. Reel: Cardboard (7")

For Outlines 05, 08A, 36, 76, 84, and 86

A. Carrier Tape: Conductive PVC
Surface resistivity: 1.8×10^3 Ω/square

B. Cover Tape: Semi-transparent polyester

C. Reel: Plastic

6. Device Orientation and Ordering Information for Diodes

For Outlines 23 and 143

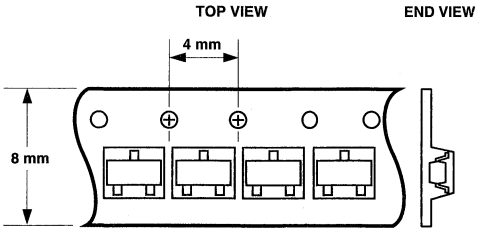
Specify part number followed by option. For example:

HSMS-XXXX L XX

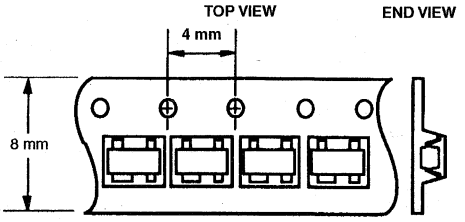
- XX = 30 = Bulk or 31 = Tape and Reel Option
- L = Low Profile
- XXXX = Part Number
- HSMS- = Prefix*

* AT = Transistor
MSA = Monolithic Silicon Amplifier
HSMS = Surface Mount Schottky SOT-23/143
HSMP = Surface Mount PIN SOT-23/143

Conforms to Electronic Industries Standard RS-481 "Taping of Surface Mounted Components for Automated Placement." Standard Quantity is 3,000 Devices/Reel for SOT-23/143.



Option L31 for SOT-23 Packages.

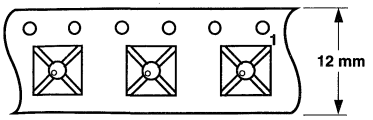


Option L31 for SOT-143 Packages.

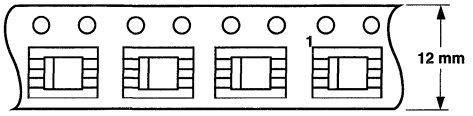
6. Device Orientation and Ordering Information for Diodes

For Outlines 05, 08A, 36, 76, 84, and 86
Tape and Reel Options

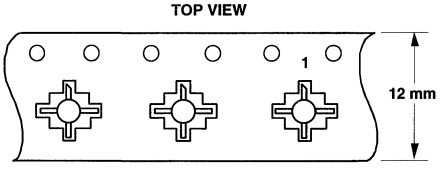
Package 05



Package 08A



Packages
36, 76, 84, and 86



NOTE: 1. INDICATES PIN 1 ORIENTATION.

Part Number Ordering Information

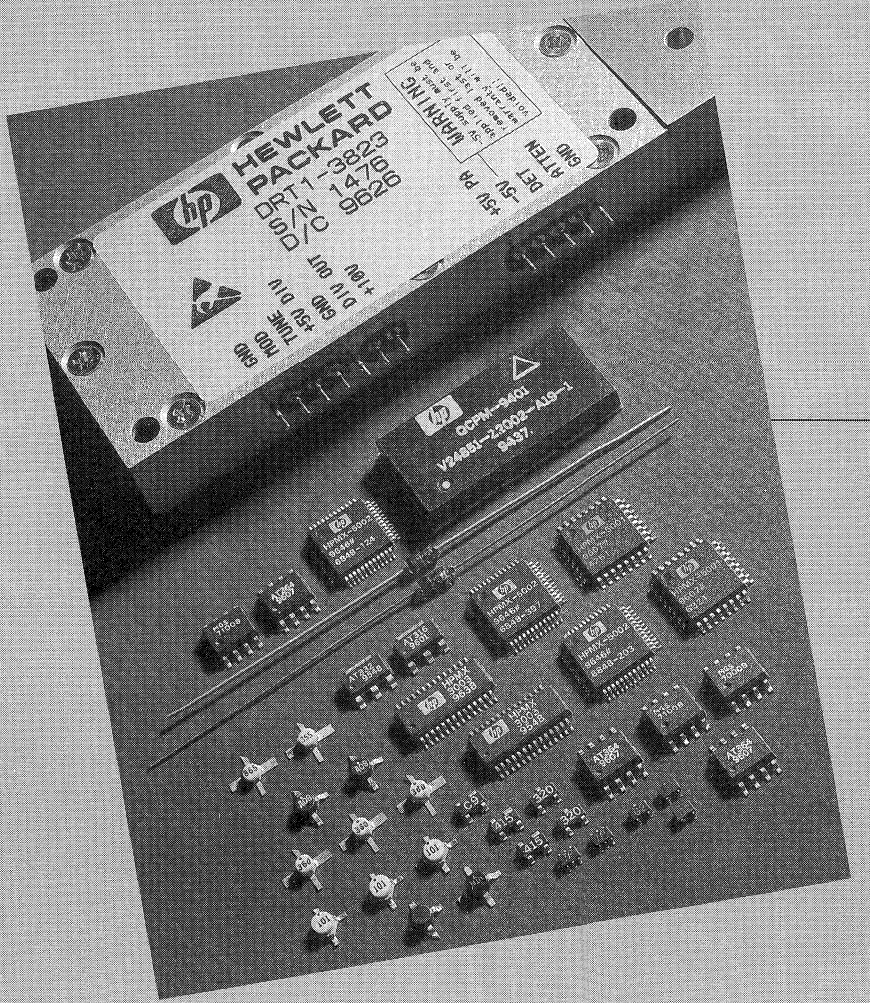
Package Style	Tape Width (mm)	Reel Size	Devices per Reel	Part Number Suffix
05	12	7"	500	-TR1
08A, 36, 74, 84, 86	12	7"	1,000	-TR1
SOT-143	8	7"	3,000	-TR1

Notes:
1. Minimum order quantity is one (1) reel.
2. Orders are required to be in increments of the single reel quantity.
3. To order, specify the device part number followed by the appropriate suffix.

Example:
ATF-13136-TR1
Package 36
7" reel
1,000 devices/reel

HEWLETT® PACKARD

Sales and Service



Ordering and Service Information

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To order any component in this catalog, call your nearest HP authorized distributor or HP sales office.

A complete listing of HP authorized distributors is located on page 12-3. These distributors can offer off-the-shelf delivery for most HP components.

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b) Customer will prepay shipping charges (and will pay all duties and taxes) for Products returned to HP for warranty service. For valid warranty claims, HP will reimburse Customer for prepaid freight charges and return Products to Customer at HP's expense.

c) Unless HP agrees in writing that Customer has configuration control, HP may make process or materials changes affecting the performance or other characteristics of Products. Products supplied after such a change will continue to meet HP's published minimum/maximum specifications, but may not be identical to Products supplied as samples or under prior orders.

d) Some sub-assembly Products may contain remanufactured parts equivalent to new in performance.

e) The above warranties do not apply to defects resulting from improper or inadequate maintenance; Customer or third party supplied software, interfacing or supplies; unauthorized modification; improper use or operation outside of the Specifications for the Product; abuse, negligence, accident, loss or damage in transit; improper site preparation; or unauthorized maintenance or repair.

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